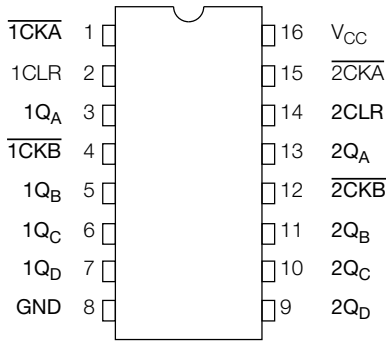
Features:

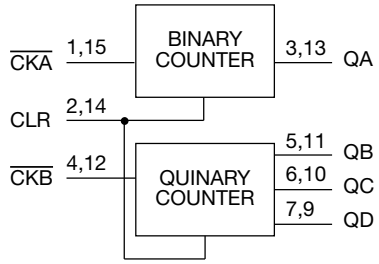
- **High Speed:** f_{MAX} = 160MHz (typ.) at V_{CC} = 5V
- **Low Power Dissipation:** I_{CC} = 8μA (max.) at Ta = 25°C
- **High Noise Immunity:** $V_{NIH} = V_{NIL}$ = 28% V_{CC} (min.)
- **Symmetrical Output Impedance:** $|I_{OH}| = I_{OL}$ = 24mA (min.). Capability of driving 50Ω transmission lines.
- **Balanced Propagation Delays:** $t_{pLH} = t_{pHL}$
- **Wide Operating Voltage Range:** V_{CC} (opr.) = 2V~5.5V
- **Pin and Function Compatible with 74HC390**
- **Available in 16-pin DIP and 150 mil SOIC**

Pin Assignment



(TOP VIEW)

Block Diagram



V_{CC} =16, GND=8

The TC74AC390 is an advanced high speed CMOS DUAL DECADE COUNTER fabricated with silicon gate and double-layer metal wiring C^2MOS technology.

It achieves the high speed operation similar to equivalent Bipolar Schottky TTL, while maintaining the CMOS low power dissipation.

It consists of two independent 4-bit counters, each composed of a divide-by-two and a divide-by-five counter. The divide-by-two counter is incremented on the negative going transition of clock A ($\overline{CKA}$). The divide-by-five counter is incremented on the negative going transition of clock B ($\overline{CKB}$). The counter can be cascaded to form decade, bi-quinary, or various combinations up to a divide-by-100 counter. When the CLEAR input is set high, the Q outputs are set to low independent of the clock inputs.

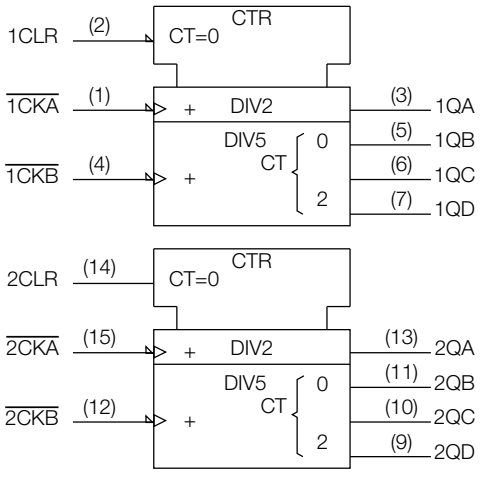
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

Truth Table

INPUTS			OUTPUTS			
$\overline{CKA}$	$\overline{CKB}$	CLR	QA	QB	QC	QD
X	X	H	L	L	L	L
↓	X	L	BINARY COUNT UP			
X	↓	L	QUINARY COUNT UP			

X: Don't Care

IEC Logic Symbol



Absolute Maximum Ratings

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5~7.0	V
DC Input Voltage	V_{IN}	-0.5~V_{CC} + 0.5	V
DC Output Voltage	V_{OUT}	-0.5~V_{CC} + 0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±50	mA
DC Output Current	I_{OUT}	±50	mA
DC V_{CC}/Ground Current	I_{CC}	±200	mA
Power Dissipation	P_D	500 (DIP) */180 (SOP)	mW
Storage Temperature	T_{stg}	-65~150	°C
Lead Temperature 10sec	T_L	300	°C

* 500mW in the range of Ta = -40°C~65°C. From Ta = 65°C to 85°C a derating factor of -10mW/°C should be applied up to 300mW.

Recommended Operating Conditions

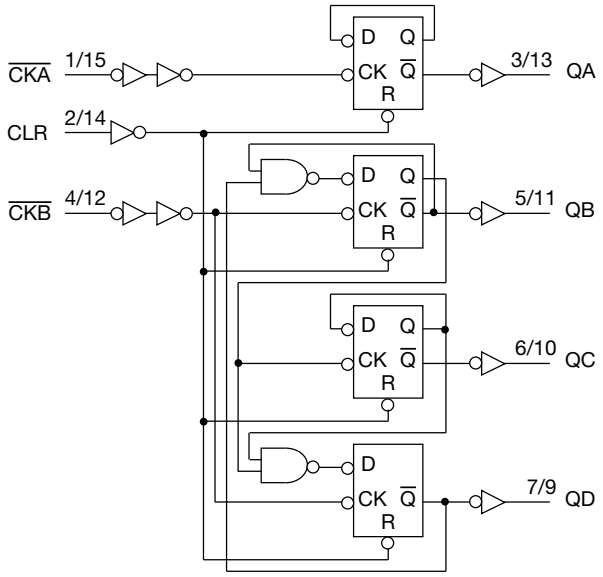
PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2.0~5.5	V
Input Voltage	V_{IN}	0~V_{CC}	V
Output Voltage	V_{OUT}	0~V_{CC}	V
Operating Temperature	T_{opr}	-40~85	°C
Input Rise and Fall Time	dt/dv	0~100 (V_{CC} = 3.3±0.3V) 0~20 (V_{CC} = 5±0.5V)	ns/v

DC Electrical Characteristics

PARAMETER	SYMBOL	TEST CONDITION			Ta = 25°C			Ta = -40~85°C		UNIT
				V_{CC}	Min.	Typ.	Max.	Min.	Max.	
High-Level Input Voltage	V_{IH}	—		2.0	1.50	—	—	1.50	—	V
				3.0	2.10	—	—	2.10	—	
				5.5	3.85	—	—	3.85	—	
Low-Level Input Voltage	V_{IL}	—		2.0	—	—	0.50	—	0.50	V
				3.0	—	—	0.90	—	0.90	
				5.5	—	—	1.65	—	1.65	
High-Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} = -50μA	2.0	1.9	2.0	—	1.9	—	V
				3.0	2.9	3.0	—	2.9	—	
				4.5	4.4	4.5	—	4.4	—	
			I_{OH} = -4mA	3.0	2.58	—	—	2.48	—	
			I_{OH} = -24mA	4.5	3.94	—	—	3.80	—	
			I_{OH} = -75mA*	5.5	—	—	—	3.85	—	
Low-Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 50μA	2.0	—	0.0	0.1	—	0.1	V
				3.0	—	0.0	0.1	—	0.1	
				4.5	—	0.0	0.1	—	0.1	
			I_{OL} =12mA	3.0	—	—	0.36	—	0.44	
			I_{OL} = 24mA	4.5	—	—	0.36	—	0.44	
			I_{OL} = 75mA*	5.5	—	—	—	—	1.65	
Input Leakage Current	I_{IN}	V_{IN} = V_{CC} or GND		5.5	—	—	±0.1	—	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND		5.5	—	—	8.0	—	80.0	

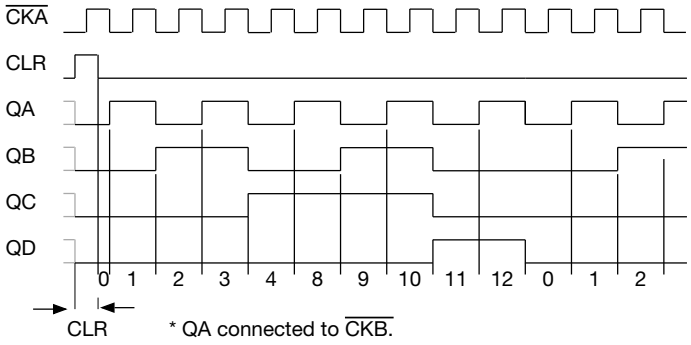
* This spec indicates the capability of driving 50Ω transmission lines.
One output should be tested at a time for a 10ms maximum duration.

System Diagram

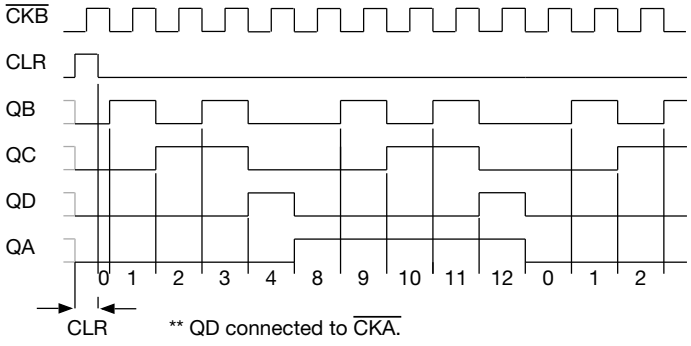


Timing Chart

(1) BCD COUNT SEQUENCE*



(2) BI-QUINARY COUNT SEQUENCE**



Timing Requirements (Input $t_r = t_f = 3n$)

PARAMETER	SYMBOL	TEST CONDITION		Ta=25˚C		Ta= –40~85˚	UNIT
			V_{CC}	Typ.	Max.	Max.	
Minimum Pulse Width ($\overline{CLOCK}$)	$t_{W(H)}$	—	3.0±0.3	—	7.0	7.0	ns
	$t_{W(L)}$		5.0±0.5	—	5.0	5.0	
Minimum Pulse Width (CLR)	$t_{W(H)}$	—	3.0±0.3	—	7.0	7.0	
			5.0±0.5	—	5.0	5.0	
Minimum Removal Time	t_{rem}	—	3.0±0.3	—	7.0	7.0	
			5.0±0.5	—	3.5	3.5	

AC Electrical Characteristics ($C_L = 50pF$, $R_L = 500\Omega$, Input $t_r = t_f = 3ns$)

PARAMETER	SYMBOL	TEST CONDITION		Ta = 25°C			Ta = -40~85°C		UNIT
			V_{CC}	Min.	Typ.	Max.	Min.	Max.	
Propagation Delay Time ($\overline{CKA}$–QA)	t_{pLH}	—	3.0±0.3	—	8.2	14.0	1.0	16.0	ns
	t_{pHL}		5.0±0.5	—	5.5	8.4	1.0	9.6	
Propagation Delay Time ($\overline{CKA}$–QC)	t_{pLH}	QA connected to $\overline{CKB}$	3.0±0.3	—	17.0	30.0	1.0	34.0	
	t_{pHL}		5.0±0.5	—	10.5	17.5	1.0	20.0	
Propagation Delay Time ($\overline{CKB}$–QB, QD)	t_{pLH}	—	3.0±0.3	—	8.8	14.9	1.0	17.0	
	t_{pHL}		5.0±0.5	—	6.0	9.4	1.0	10.7	
Propagation Delay Time ($\overline{CKB}$–QC)	t_{pLH}	—	3.0±0.3	—	11.0	18.8	1.0	21.5	
	t_{pHL}		5.0±0.5	—	7.1	11.3	1.0	12.8	
Propagation Delay Time ($\overline{CKA}$–Qn)	t_{pHL}	—	3.0±0.3	—	7.7	12.5	1.0	14.3	
			5.0±0.5	—	5.7	8.5	1.0	9.7	
Maximum Clock Frequency ($\overline{CKA}$)	f_{MAX}	—	3.0±0.3	60	120	—	60	—	MHz
			5.0±0.5	100	180	—	100	—	
Maximum Clock Frequency ($\overline{CKB}$)	f_{MAX}	—	3.0±0.3	45	90	—	45	—	
			5.0±0.5	90	140	—	90	—	
Input Capacitance	C_{IN}	—	—	—	5	10	—	10	pF
Power Dissipation Capacitance	C_{PD}[1]	—	—	—	40	—	—	—	

Note (1): C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: $I_{CC\ (opr)} = C_{PD} \bullet V_{CC} \bullet f_{IN} + I_{CC} / 2$ (per Counter).