Wireless Components

TV Mixer-Oscillator-PLL

TUA 6010XS Version 1.0

Specification August 1999

preliminary

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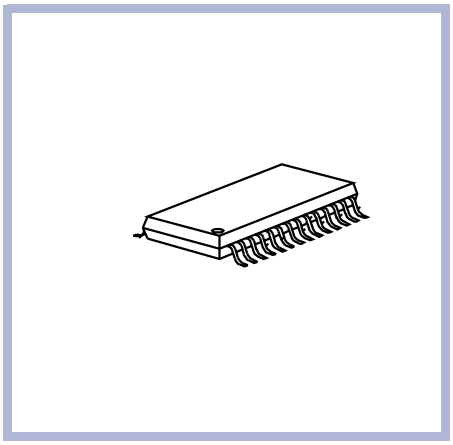
Product Info

General Description

The **TUA 6010XS** device combines a digitally programmable phase locked loop (PLL), with a mixer-oscillator block including two balanced mixers and oscillators for use in TV tuners.

Package



Features

- PLL with short lock-in time; no asynchronous divider stage
- Fast I^2C bus mode possible
- 4 programmable chip addresses
- Short pull-in time for quick channel access and optimized loop stability
- 3 high-current switch outputs
- 2 TTL inputs
- 5-level A/D converter
- Lock-in flag
- Power-down flag
- Few external components
- Frequency and amplitude-stable balanced oscillator for the VHF, HYPER and UHF frequency range
- Optimum decoupling of input frequency from oscillator
- Double balanced mixer with wide dynamic range and low-impedance inputs for the VHF, HYPER and UHF frequency range
- Internal band switch
- Internal low-noise reference voltage source
- Package TSSOP 28
- Full ESD protection

Application

- The IC is suitable for all tuners in TV- and VCR-sets or cable set-top receivers for analog TV an Digital Video Broadcasting.

Ordering Information

Type	Ordering Code	Package
TUA 6010 XS	Q67007-A5211	P-TSSOP-28-1

1 Table of Contents

2 Product Description

Contents of this Chapter

2.1 Overview

The **TUA 6010XS** device combines a digitally programmable phase locked loop (PLL), with a mixer-oscillator block including two balanced mixers and oscillators for use in TV tuners.

The PLL block with four hard-switched chip addresses forms a digitally programmable phase locked loop. With a 4 MHz quartz crystal, the PLL permits precise setting of the frequency of the tuner oscillator up to 900 MHz in increments of 62.5 kHz. The tuning process is controlled by a microprocessor via an I^2C bus. The device has three output ports, which all can also be used as input ports (two TTL inputs and one A/D converter input). A flag is set when the loop is locked. The input ports and lock flag can be read by the processor via the I^2C bus. The mixer-oscillator block includes two balanced mixers (double balanced mixer with low-impedance input), two frequency and amplitude-stable balanced oscillators for VHF, HYPER and UHF, a low-noise reference voltage source and a band switch.

2.2 Features

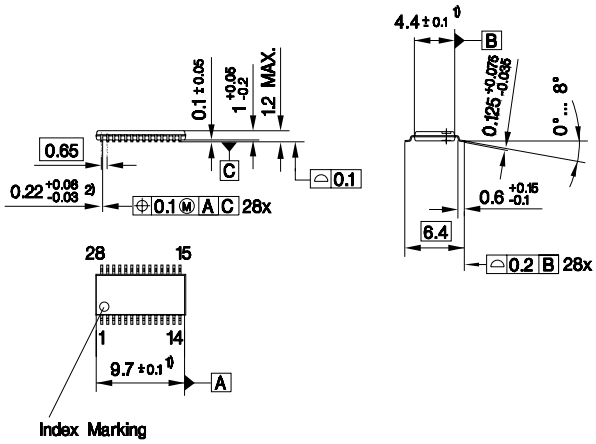
- PLL with short lock-in time; no asynchronous divider stage
- Fast I^2C bus mode possible
- 4 programmable chip addresses
- Short pull-in time for quick channel access and optimized loop stability
- 3 high-current switch outputs
- 2 TTL inputs
- 5-level A/D converter
- Lock-in flag
- Power-down flag
- Few external components
- Frequency and amplitude-stable balanced oscillator for the VHF, HYPER and UHF frequency range
- Optimum decoupling of input frequency from oscillator
- Double balanced mixer with wide dynamic range and low-impedance inputs for the VHF, HYPER and UHF frequency range
- Internal band switch
- Internal low-noise reference voltage source
- Package TSSOP 28
- Full ESD protection

2.3 Application

- The IC is suitable for all tuners in TV- and VCR-sets or cable set-top receivers for analog TV an Digital Video Broadcasting.

2.4 Package Outlines

P-TSSOP-28-1

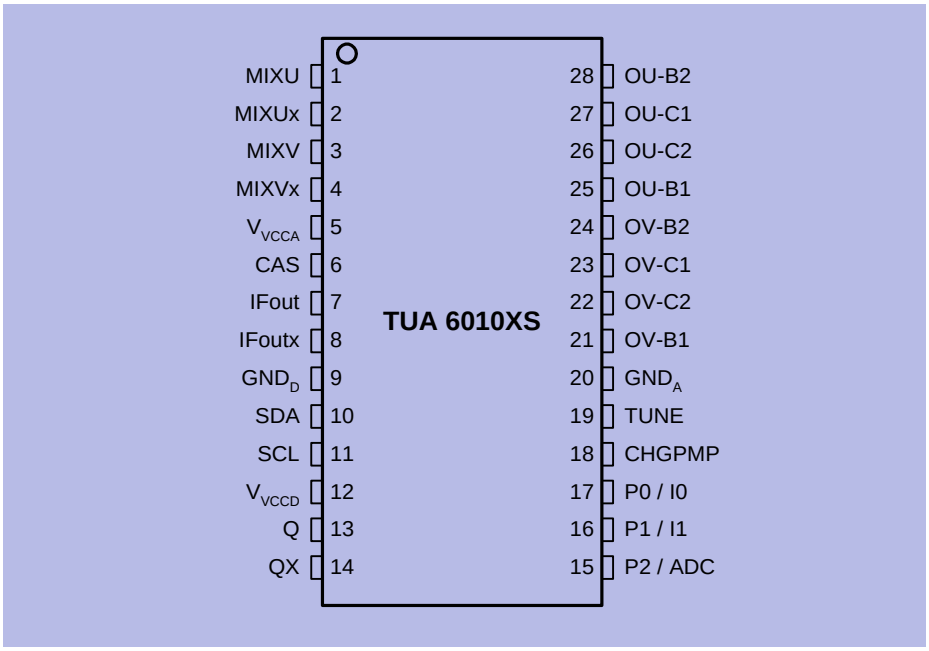


1) Does not include plastic or metal protrusion of 0.15 max. per side
2) Does not include dambar protrusion

3 Functional Description

Contents of this Chapter

3.1 Pin Configuration

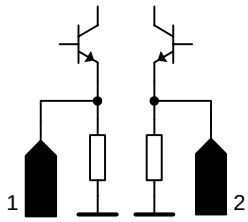
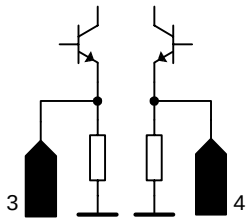
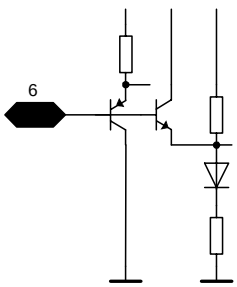
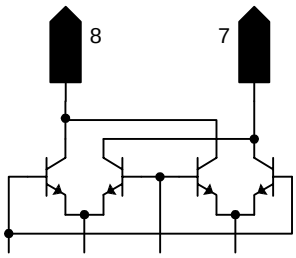


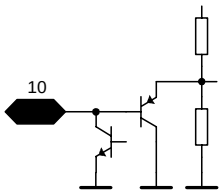
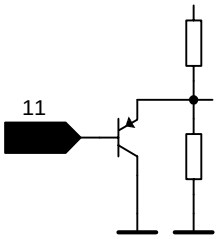
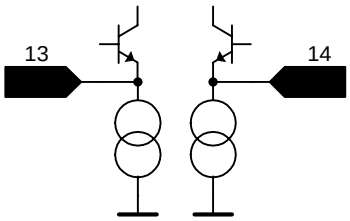
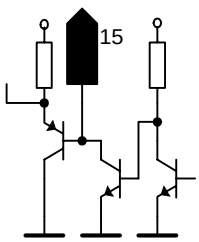
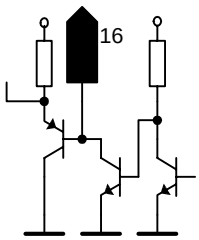
Pin_config.wmf

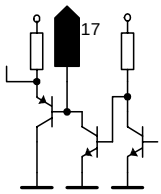
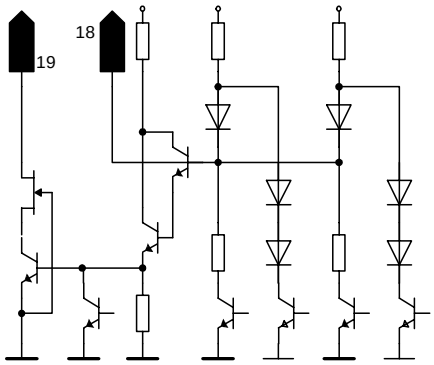
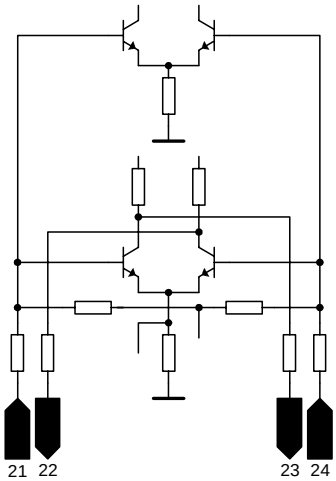
Figure 3-1 Pin Configuration

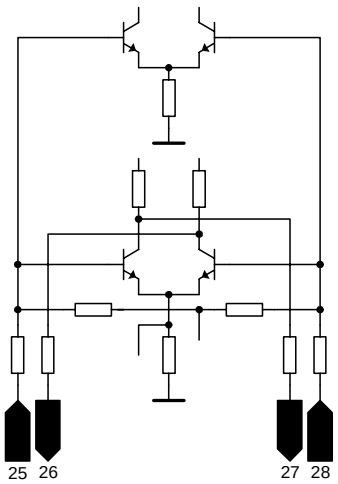
3.2 Pin Definition and Function

Table 3-1 Pin Definition and Function

Pin No.	Symbol		Function
1	MIXU		UHF mixer input, low-impedance, symmetrical to MIXUx
2	MIXUx		UHF mixer input, low-impedance, symmetrical to MIXU
3	MIXV		VHF or HYPER mixer input, low-impedance, symmetrical to MIXVx
4	MIXVx		VHF or HYPER mixer input, low-impedance, symmetrical to MIXV
5	V_{VCCA}		Positive supply voltage for analog block
6	CAS		Chip address select
7	IFout		Open collector mixer output, high-impedance, symmetrical to IFoutx
8	IFoutx		Inverse open collector mixer output, high-impedance, symmetrical to IFout
9	GND_D		Digital Ground

10	SDA		Data input/output for the I^2C bus
11	SCL		Clock input for the I^2C bus
12	V_{VCCD}		Positive supply voltage for digital block (PLL)
13	Q		4 MHz low-impedance crystal oscillator input
14	Qx		Inverse 4 MHz low-impedance crystal oscillator input
15	P2/ADC		Port output / ADC input
16	P1/I1		Port output / TTL input

17	P0/I0		Port output / TTL input
18	CHGPMP		Charge pump output / loop filter
19	TUNE		VCO tuning voltage output
20	GND_A		Analog Ground
21	OV-B1		VHF oscillator amplifier, high-impedance base input, symmetrical to OV-B2
22	OV-C2		VHF oscillator amplifier, high-impedance collector output, symmetrical to OV-C1
23	OV-C1		VHF oscillator amplifier, high-impedance collector output, symmetrical to OV-C2
24	OV-B2		VHF oscillator amplifier, high-impedance base input, symmetrical to OV-B1

25	OU-B1		UHF oscillator amplifier, high-impedance base input, symmetrical to OU-B2
26	OU-C2		UHF oscillator amplifier, high-impedance collector output, symmetrical to OU-C1
27	OU-C1		UHF oscillator amplifier, high-impedance collector output, symmetrical to OU-C2
28	OU-B2		UHF oscillator amplifier, high-impedance base input, symmetrical to OU-B1

3.3 Block Diagram

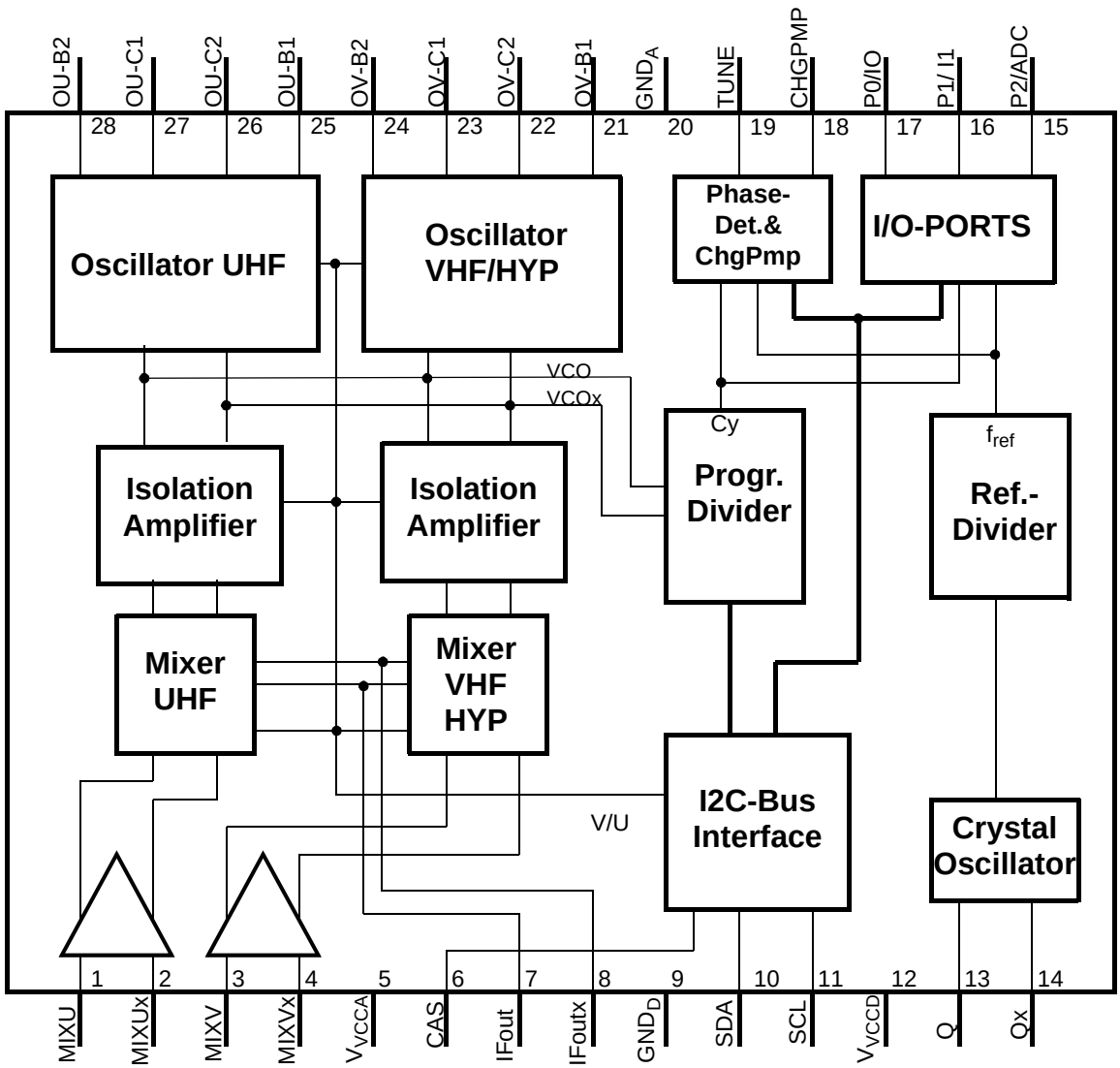


Figure 3-2 Block Diagram

3.4 Circuit Description

3.4.1 Mixer-Oscillator block

The mixer oscillator section includes two balanced mixers (double balanced mixer), two balanced oscillators for VHF and/or HYPER and UHF, a reference voltage source and a band switch.

Filters between tuner input and IC separate the TV frequency signals into two bands. The band switch ensures that only one mixer-oscillator block at a time is activated. In the activated band the signal passes a frontend stage with MOS-FET amplifier, a double-tuned bandpass filter and is then fed to the balanced mixer input of the IC which has a low-impedance input.
The input signal is mixed there with the on chip oscillator signal from the activated oscillator section.

3.4.2 PLL block

The mixer-oscillator signal VCO/VCOx is internally DC-coupled as a differential signal at the programmable divider inputs. The signal subsequently passes through a programmable divider with ratio N = 256 through 32767 and is then compared in a digital frequency / phase detector to a reference frequency f_{ref} = 62.5 kHz.
This frequency is derived from a balanced, low-impedance 4 MHz crystal oscillator (pin Q, Qx) divided by Q = 64.

The phase detector has two outputs UP and DOWN that drive two current sources I+ and I- of a charge pump. If the negative edge of the divided VCO signal appears prior to the negative edge of the reference signal, the I+ current source pulses for the duration of the phase difference. In the reverse case the I- current source pulses. If the two signals are in phase, the charge pump output (CHGPMP) goes into the high-impedance state (PLL is locked). An active low-pass filter integrates the current pulses to generate the tuning voltage for the VCO (internal amplifier, external pullup resistor at TUNE and external RC circuitry). The charge pump output is also switched into the high-impedance state when the control bit T0 = 1. Here it should be noted, however, that the tuning voltage can alter over a long period in the high-impedance state as a result of self-discharge in the peripheral circuity. TUNE may be switched off by the control bit OS to allow external adjustments.

When the VCO is not working the PLL locks to a tuning voltage of 33V.

By means of control bit 5I the pump current can be switched between two values by software. This programmability permits alteration of the control response of the PLL in the locked-in state. In this way different VCO gains can be compensated, for example.

The software-switched ports P0, P1, P2 are general-purpose open-collector outputs. The test bit T1 = 1, switches the test signals f_{ref} (4 MHz / 64) and C_y (divided input signal) to P0 and P1 respectively. P0, P1, P2 are bidirectional.

The lock detector resets the lock flag FL when the width of the charge pump current pulses is greater than the period of the crystal oscillator (i.e. 250 ns). Hence, when FL = 1, the maximum deviation of the input frequency from the programmed frequency is given by

$$\Delta f = \pm I_P (K_{VCO} / f_Q) (C_1+C_2) / (C_1C_2)$$

where I_P is the charge pump current, K_{VCO} the VCO gain, f_Q the crystal oscillator frequency and C_1, C_2 the capacitances in the loop filter (see application circuit). As the charge pump pulses at 62.5 kHz (= f_{ref}), it takes a maximum of 16 µs for FL to be reset after the loop has lost lock state.

Once FL has been reset, it is set only if the charge pump pulse width is less than 250 ns for eight consecutive f_{ref} periods. Therefore it takes between 128 and 144 µs for FL to be set after the loop regains lock.

3.4.3 I^2C-Bus Interface

Data is exchanged between the processor and the PLL via the I^2C bus. The clock is generated by the processor (input SCL), while pin SDA functions as an input or output depending on the direction of the data (open collector, external pull-up resistor). Both inputs have hysteresis and a low-pass characteristic, which enhance the noise immunity of the I^2C bus.

The data from the processor pass through an I^2C bus controller. Depending on their function the data are subsequently stored in registers. If the bus is free, both lines will be in the marking state (SDA, SCL are HIGH). Each telegram begins with the start condition and ends with the stop condition. Start condition: SDA goes LOW, while SCL remains HIGH. Stop condition: SDA goes HIGH while SCL remains HIGH. All further information transfer takes place during SCL = LOW, and the data is forwarded to the control logic on the positive clock edge.

The table 1 ”bit allocation” should be referred to the following description. All telegrams are transmitted byte-by-byte, followed by a ninth clock pulse, during which the control logic returns the SDA line to LOW (acknowledge condition). The first byte is comprised of seven address bits. These are used by the processor to select the PLL from several peripheral components (chip select). The LSB bit (R/W) determines whether data are written into (R/W = 0) or read from (R/W = 1) the PLL.

In the data portion of the telegram during a WRITE operation, the MSB bit of the first or third data byte determines whether a divider ratio or control information is to follow. In each case the second byte of the same data type has to follow the first byte.

If the address byte indicates a READ operation, the PLL generates an acknowledge and then shifts out the status byte onto the SDA line. If the processor generates an acknowledge, a further status byte is output; otherwise the data line

is released to allow the processor to generate a stop condition. The status word consists of two bits from the TTL input ports, three bits from the A/D converter, the lock flag and the power-on flag.

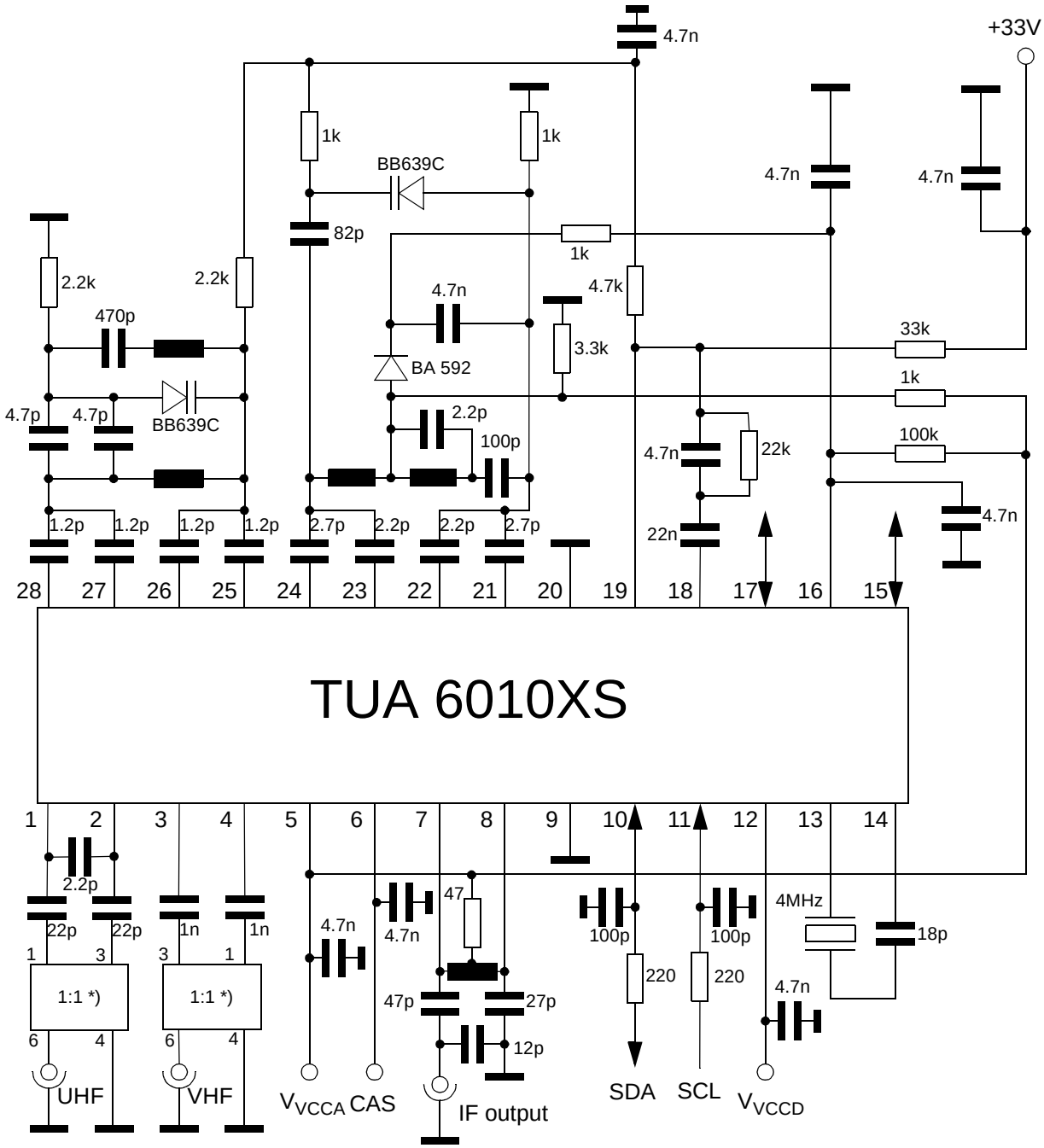
Four different chip addresses can be set by appropriate connection of pin CAS (see table 2 ”address selection”).

When the supply voltage is applied, a power-on reset circuit prevents the PLL from setting the SDA line to LOW, which would block the bus. The power-on reset flag POR is set at power-on and when V_{VCCD} goes below 3.2 V. It will be reset at the end of a READ operation.

4 Applications

Contents of this Chapter

4.1 Application Circuit



*) TOKO B4F Type
617DB-1023

Figure 4-1 Evaluation Board

4.2 Hints

See separate available **Application Note TUA 6010XS**.

5 Reference

Contents of this Chapter

5.1 Electrical Data

5.1.1 Absolute Maximum Ratings

WARNING

The maximum ratings may not be exceeded under any circumstances, not even momentarily and individually, as permanent damage to the IC will result.

Table 5-1 Absolute Maximum Ratings, Ambient temperature T_{AMB}=-20°C ... + 80°C

Parameter	Symbol	Limit Values min	Limit Values max	Unit	Remarks
PLL					
Supply voltage	V_{VCCD}	-0.3	+6	V	
CHGPMP	V_{CHGPMP} I_{CHGPMP}	-0.3	 1	V mA	
Crystal oscillator pins Q, Qx	V_Q I_Q	 -5	V_{VCCD}	V mA	
Bus input/output SDA Bus output current SDA	V_{SDA} $I_{SDA(L)}$	-0.3	+6 5	V mA	
Bus input SCL	V_{SCL}	-0.3	+6	V	
Port outputs P0, P1, P2	V_P	-0.3	+13	V	
Chip address switch CAS	V_{CAS}	-0.3	V_{VCCD}	V	
VCO tuning output (loop filter)	V_{TUNE}	-0.3	+35	V	
Bus output SDA	I_{SDAL}	-1	5	mA	open collector
Port outputs P0, P1, P2	$I_{P(L)}$	-1	15	mA	open collector
Total port output current	$\Sigma I_{P(L)}$		20	mA	t_{max} = 0,1 sec. at 6 V
Junction temperature	T_J		+125	°C	
Storage temperature	T_{Stg}	-40	+125	°C	
Thermal resistance (junction to ambient)	R_{thSA}		130	K/W	

Table 5-1 Absolute Maximum Ratings, Ambient temperature T_{AMB}=-20°C ... + 80°C (continued)					
Parameter	**Symbol**	**Limit Values**		**Unit**	**Remarks**
		min	max		
Mixer-Oscillator					
Supply voltage	V_{VCCA}	-0.3	+6	V	
Mix inputs VHF/UHF	$V_{MIX\ V/U}$ $I_{MIX\ V/U}$	-5	2 6	V mA	
VCO base voltage	$V_{OU\text{-}B/OV\text{-}B}$	-0.3	3	V	
VCO collector voltage	$V_{OU\text{-}C/OV\text{-}C}$		V_{VCCA}	V	
IF output	V_{IFout} V_{IFoutx}		6	V	
All values are referred to ground (pin), unless stated otherwise. Currents with a positive sign flows into the pin and currents with a negative sign flows out of pin.					
ESD-Protection*					
all pins unless otherwise specified	V_{ESD}	-1	1	kV	
Mixer inputs MIXU / MIXV	$V_{ESD\ MIX}$	-500	500	V	Pin 1, 2, 3, 4
Mixer outputs IFout / IFoutx	$V_{ESD\ IF}$	-500	500	V	Pin 7, 8
Ports	$V_{ESD\ P}$	-500	500	V	Pin 15, 16, 17
Charge pump	$V_{ESD\ CP}$	-500	500	V	Pin 18

*according to MIL STD 883D, method 3015.7 and EOS/ESD assn. standard S5.1 - 1993

5.1.2 Operating Range

Within the operational range the IC operates as described in the circuit description. The AC / DC characteristic limits are not guaranteed.

Table 5-2 Operating Range							
Parameter	**Symbol**	**Limit Values**		**Unit**	**Test Conditions**	**L**	**Item**
		min	max				
Supply voltage	V_{VCCD}	+4.5	+5.5	V			
Supply voltage	V_{VCCA}	+4.5	+5.5	V			
Mixer output voltage	V_{IFout} V_{IFoutx}	+4.5	+5.5	V	open collector		
Programmable divider factor	N	256	32767				
VHF Mixer input frequency range	f_{MIXV}	30	500	MHz			
UHF Mixer input frequency range	f_{MIXU}	400	900	MHz			
VHF Oscillator frequency range	f_{OV}	30	500	MHz			
UHF Oscillator frequency range	f_{OU}	400	900	MHz			
Ambient temperature	T_{amb}	-20	+80	°C			

5.1.3 AC/DC Characteristics

Table 5-3 AC/DC Characteristics with T_{amb} 25 °C, V_{VCCA} = 5 V, V_{VCCD} = 5 V

	Symbol	Limit Values			Unit	Test Conditions	L	Item
		min	typ	max				
Digital Unit								
PLL								1.1
Supply current	I_{VCCD}	19	24	29	mA	V_{VCCD} = 5 V		
Crystal oscillator connections Q, Qx								
Crystal frequency	f_Q	3.2	4.0	4.8	MHz	series resonance		
Crystal resistance	R_Q	10		100	Ω	series resonance		
Oscillation frequency	f_Q	3,99975	4,000	4,00025	MHz	f_Q = 4 MHz		
Input impedance	Z_Q	-600	-750	-900	Ω	f_Q = 4 MHz		
Margin from 1st (fundamental) to 2nd and 3rd harmonics	a_H	20			dB	f_Q = 4 MHz		
Charge pump output CHGPMP								
HIGH output current	I_{CPH}	±90	±220	±300	µA	5I = 1, V_{CP} = 2 V		
LOW output current	I_{CPL}	±22	±50	±75	µA	5I = 0, V_{CP} = 2 V		
Tristate current	I_{CPZ}		+1		nA	T0 = 1, V_{CP} = 2 V		
Output voltage	V_{CP}	1.0		2.5	V	locked		
Drive output TUNE (open collector)								
HIGH output current	I_{TH}			10	µA	V_{TH} = 33 V, T0 = 1		
LOW output voltage	V_{TL}			0.5	V	I_{TL} = 1.0 mA		
I^2C-Bus								1.2
Bus inputs SCL, SDA								
HIGH input voltage	V_{IH}	3		5.5	V			
LOW input voltage	V_{IL}	0		1.5	V			
HIGH input current	I_{IH}			10	µA	V_{IH} = V_S		
LOW input current	I_{IL}	-10			µA	V_{IL} = 0 V		
Bus output SDA (open collector)								
HIGH output current	I_{OH}			10	µA	V_{OH} = 5.5 V		
LOW output voltage	V_{OL}			0.4	V	I_{OL} = 3 mA		
Edge speed SCL,SDA								
Rise time	t_r			300	ns			
Fall time	t_f			300	ns			

Table 5-3 AC/DC Characteristics with T_{amb} 25 °C, V_{VCCA} = 5 V, V_{VCCD} = 5 V (Continued)

	Symbol	Limit Values			Unit	Test Conditions	L	Item
		min	typ	max				
Clock timing SCL								
Frequency	f_{SCL}	0		400	kHz			
HIGH pulse width	t_H	0.6			µs			
LOW pulse width	t_L	1.3			µs			
Start condition								
Set-up time	t_{susta}	0.6			µs			
Hold time	t_{hsta}	0.6			µs			
Stop condition								
Set up time	t_{susto}	0.6			µs			
Bus free	t_{buf}	1.3			µs			
Data transfer								
Set-up time	t_{sudat}	0.1			µs			
Hold time	t_{hdat}	0			µs			
Input hysteresis SCL, SDA (1)	V_{hys}		200		mV			
Pulse width of spikes which are suppressed	t_{sp}	0		50	ns			
Capacitive load for each bus line	C_L			400	pF			
Port outputs P0, P1, P2 (open collector)								
HIGH output current	I_{POH}			1	µA	V_{POH} = 5 V		
LOW output voltage	V_{POL}			0.5	V	I_{POL} = 15 mA		
TTL port inputs P0, P1								
HIGH input voltage	V_{PIH}	2.7			V			
LOW input voltage	V_{PIL}			0.8	V			
HIGH input current	I_{PIH}			10	µA	V_{PIH} = 13.5 V		
LOW input current	I_{PIL}	-10			µA	V_{PIL} = 0 V		
ADC port input P2								
HIGH input current	I_{ADCH}			10	µA			
LOW input current	I_{ADCL}	-10			µA			
Address selection input CAS								
HIGH input current	I_{CASH}			50	µA	V_{CASH} = 5 V		
LOW input current	I_{CASL}	-50			µA	V_{CASL} = 0 V		

Table 5-3 AC/DC Characteristics with T_{amb} 25 °C, V_{VCCA} = 5 V, V_{VCCD} = 5 V (Continued)

	Symbol	Limit Values			Unit	Test Conditions	L	Item
		min	typ	max				
Analog Unit								
Mixer-Oscillator								**2.1**
Current consumption	I_{VCCA}	11	15	19	mA	Bit V/U = Low		
	I_{VCCA}	14	18	22	mA	Bit V/U = High		
Mixer current	$I_{IF-V/IF-U}$	4	6	8	mA			
Mixer output impedance	$R_{IFout,IFoutx}$		20		kΩ	Parallel equivalent circuit, f_{IF} = 38,9 MHz		
	$C_{IFout,IFoutx}$		0.5		pF	Parallel equivalent circuit, f_{IF} = 38,9 MHz		
VHF and Hyper Band Section								**2.2**
Oscillator frequency range	f_{OscV}	80		170	MHz	V_d = 0,5..28 V; VHF		
	f_{OscH}	140		450	MHz	V_d = 0,5..28 V; HYP		
Oscillator drift	Δf_{OscV}			400	kHz	V_S = 5 V±10%		
	Δf_{OscV}			500	kHz	ΔT = 25 °C		
	Δf_{OscV}			100	kHz	t = 5 s up to 15 min after switching on		
Oscillator pulling	V_{MIXV}	100	108		dBµV	Δf = 10 kHz in channel E2		
	V_{MIXV}	100	108		dBµV	Δf = 10 kHz in channel S10		
	V_{MIXV}	80	88		dBµV	Δf_{int} = E2 + N + 5 - 1 MHz		
	V_{MIXV}	80	88		dBµV	Δf_{int} = S10 + N + 5 - 1 MHz		
Oscillator phase noise	$L(fm)_{VHF}$	-80	-86		dBc/Hz	fm = 10 kHz, application circuit		
Mixer gain	G_{MixV}	11	14	17	dB			
Mixer noise figure	F_{MixV}		5	8	dB	Channel E2 (DSB)		
	F_{MixV}		5	8	dB	Channel 10 (DSB)		
Crosstalk $f_{in/LO}$	V_{MixV}	150	1000		mV_{rms}	max. input level for 10 dB distance $f_{in/LO}$		

Table 5-3 AC/DC Characteristics with T_{amb} 25 °C, V_{VCCA} = 5 V, V_{VCCD} = 5 V (Continued)

	Symbol	Limit Values			Unit	Test Conditions	L	Item
		min	typ	max				
Mixer input impedance	R_{MixV}		20		W	serial equivalent circuit, f_{MixV} = 300 MHz		
	L_{MixV}		10		nH	serial equivalent circuit, f_{MixV} = 300 MHz		
IF suppression	a_{IF}		20		dB	V_{MixB} = 80 dBµV		
UHF Section								**2.3**
Oscillator frequency range	f_{OscU}	440		900	MHz	V_t = 0,5...28 V		
Oscillator drift	Δf_{OscU}			400	kHz	V_S = 5 V±10%		
	Δf_{OscU}			800	kHz	ΔT = 25 °C		
	Δf_{OscU}			100	kHz	t = 5 s up to 15 min after switching on		
Oscillator pulling	V_{MIXU}	100	108		dBµV	Δf = 10 kHz in channel E21		
	V_{MIXU}	100	108		dBµV	Δf = 10 kHz in channel E68		
	V_{MIXU}	80	88		dBµV	Δf_{int} = E21 + N + 5 - 1 MHz		
	V_{MIXU}	80	88		dBµV	Δf_{int} = E68 + N + 5 - 1 MHz		
Oscillator phase noise	$L(fm)_{UHF}$	-80	-86		dBc/Hz	fm = 10 kHz, application circuit		
Mixer gain	G_{MixU}	11	14	17	dB			
Mixer noise figure	F_{MixU}		6	9	dB	Channel E21 (DSB)		
			7	10	dB	Channel E68 (DSB)		
Crosstalk $f_{in/LO}$	V_{MixU}	150	1000		mV_{rms}	max. input level for 10 dB distance $f_{in/LO}$		
Mixer input impedance	R_{MixU}		20		W	serial equivalent circuit, f_{MixU} = 600 MHz		
	L_{MixU}		10		nH	serial equivalent circuit, f_{MixU} = 600 MHz		
IF suppression	a_{IF}		20		dB	V_{MixB} = 80 dBµV		

■ This value is only guaranteed in lab.

5.2 Bit Allocation Read / Write

Table 5-4

Byte	MSB*)	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	LSB	Ack	Remarks
Write Data										
Address Byte	1	1	0	0	0	MA1	MA0	0	A	
Progr. Divider Byte 1	0	n14	n13	n12	n11	n10	n9	n8	A	
Progr. Divider Byte 2	n7	n6	n5	n4	n3	n2	n1	n0	A	
Control Byte 1	1	5I	T1	T0	1	1	1	OS	A	
Control Byte 2	V/U	x	x	x	x	P2	P1	P0	A	
Read Data										
Address Byte	1	1	0	0	0	MA1	MA0	1	A	
Status Byte	POR	FL	x	I1	I0	A2	A1	A0	A	

*) MSB shifted first.

Divider ratio:

N = 16384 x n14 + 8192 x n13 + 4096 x n12 + 2048 x n11 + 1024 x n10 + 512 x n9 + 256 x n8 +128 x n7 + 64 x n6 + 32 x n5 + 16 x n4 + 8 x n3 + 4 x n2 + 2 x n1 + n0

Control Bytes:

- Ports P0, P1, P2:

P0...P2=1 open-collector output is active
P0...P2=0 open-collector output is inactive, TTL-inputs I1, I0 and ADC available

- Bandswitch V/U:

V/U=1 switch to OSC/MIX UHF
V/U=0 switch to OSC/MIX VHF

- Pump current 5I:

5I=1 high PD output current
5I=0 low PD output current

- Disabling tuning voltage OS:

OS=1 disables TUNE
OS=0 enables TUNE

Status Byte:

- Power On Reset flag POR:

flag is set at power-on and reset at the end of READ operation

- PLL lock flag FL:

flag is set to 1 when loop is locked

- TTL-inputs I1, I0:

input data from pins P1/I1, P0/I0

- ADC bits A2,A1,A0:

digital outputs of the 5-level ADC

Table 5-5 Address Selection

Voltage at CAS	MA1	MA0
(0...0.1) * V_{VCC}	0	0
open circuit	0	1
(0.4...0.6) * V_{VCC}	1	0
(0.9...1) * V_{VCC}	1	1

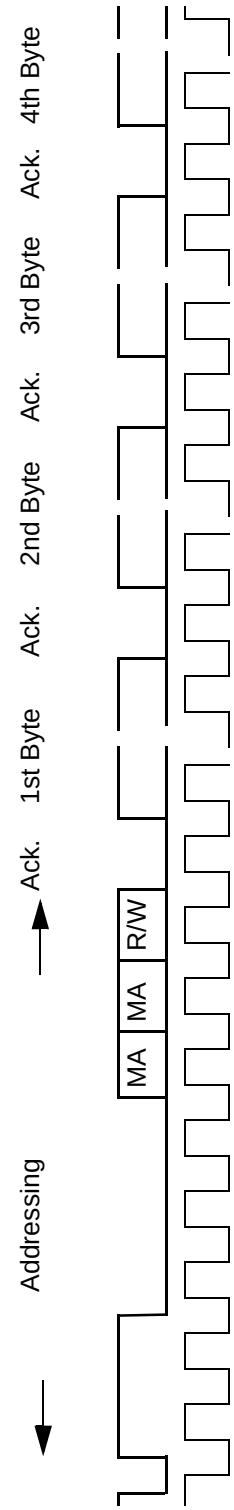
Table 5-6 Test Modes

Test mode	T1	T0
Normal operation	0	0
P1 = Cy output, P0 = f_{ref} output	1	0
Charge pump output, CHGPMP is in high-impedance state	0	1
TTL-inputs I1/I0 are Cy/f_{ref} inputs of phase detector	1	1

Table 5-7 A/D Converter Levels

Voltage at P2 / ADC	A2	A1	A0
(0...0.15) * V_{VCC}	0	0	0
(0.15...0.3) * V_{VCC}	0	0	1
(0.3...0.45) * V_{VCC}	0	1	0
(0.45...0.6) * V_{VCC}	0	1	1
(0.6...1) * V_{VCC}	1	0	0

5.3 I²C Bus Timing Diagram



Telegram examples:

Start-Addr-DR1-DR2-CW1-CW2-Stop
Start-Addr-CW1-CW2-DR1-DR2-Stop
Start-Addr-DR1-DR2-Stop
Start-Addr-CW1-CW2-Stop

Start = start condition
Addr = address byte
DR1 = prog. divider byte 1
DR2 = prog. divider byte 2
CW1 = control byte 1
CW2 = control byte 2
Stop = stop condition

5.4 Test Circuits

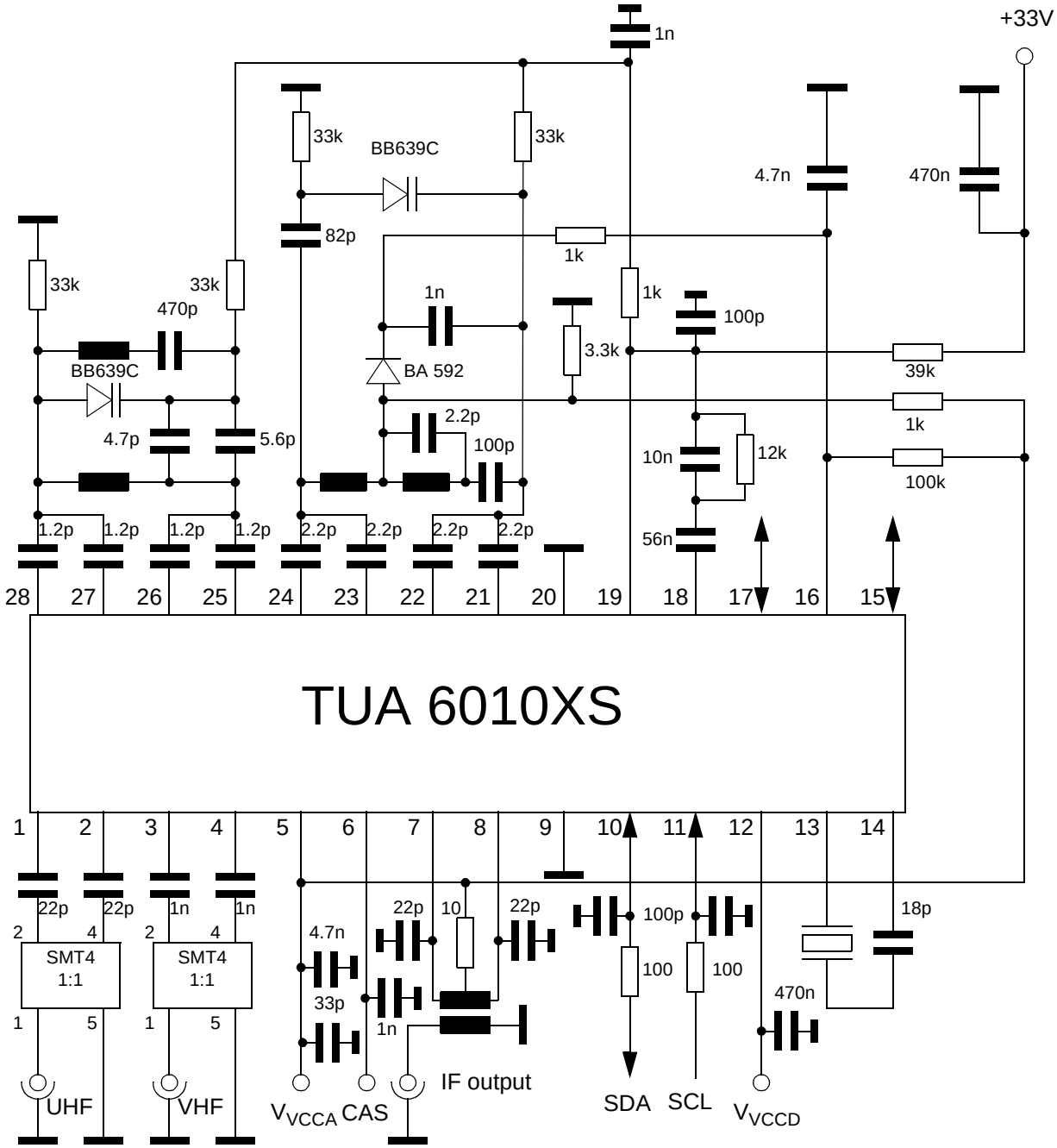


Figure 5-1 DC and RF Parameter Measurement

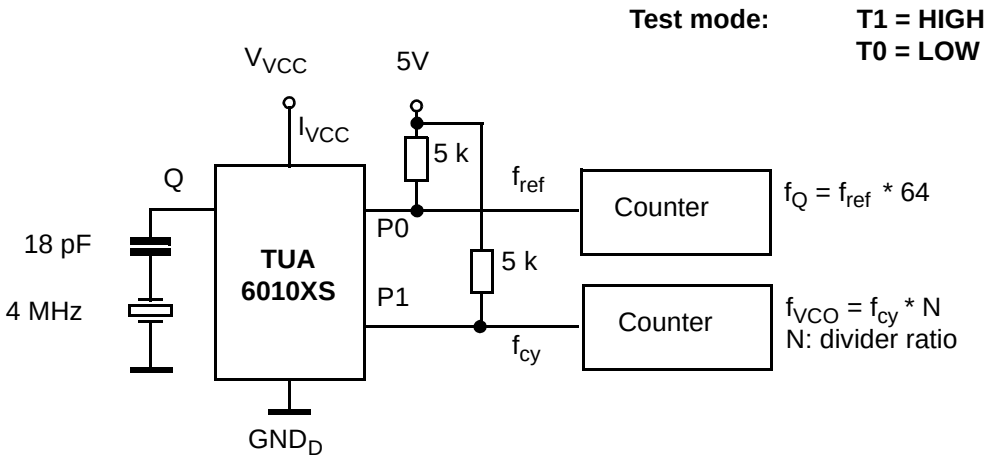


Figure 5-2 Measurement of Crystal Oscillator Frequency