

# BUK961R5-30E

## N-channel TrenchMOS logic level FET

5 October 2012

Product data sheet

## 1. Product profile

### 1.1 General description

Logic level N-channel MOSFET in a SOT404 package using TrenchMOS technology. This product has been designed and qualified to AEC Q101 standard for use in high performance automotive applications.

### 1.2 Features and benefits

- AEC Q101 compliant
- Repetitive avalanche rated
- Suitable for thermally demanding environments due to 175 °C rating
- True Logic level gate with V<sub>GS(th)</sub> rating of greater than 0.5V at 175 °C

### 1.3 Applications

- 12 V Automotive systems
- Motors, lamps and solenoid control
- Start-Stop micro-hybrid applications
- Transmission control
- Ultra high performance power switching

### 1.4 Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V <sub>DS</sub>	drain-source voltage	T <sub>j</sub> ≥ 25 °C; T <sub>j</sub> ≤ 175 °C		-	-	30	V
I <sub>D</sub>	drain current	V <sub>GS</sub> = 5 V; T <sub>mb</sub> = 25 °C; <a href="#">Fig. 1</a>	[1]	-	-	120	A
P <sub>tot</sub>	total power dissipation	T <sub>mb</sub> = 25 °C; <a href="#">Fig. 2</a>		-	-	324	W
<b>Static characteristics</b>							
R <sub>DS(on)</sub>	drain-source on-state resistance	V <sub>GS</sub> = 5 V; I <sub>D</sub> = 25 A; T <sub>j</sub> = 25 °C; <a href="#">Fig. 11</a>		-	1.3	1.5	mΩ
<b>Dynamic characteristics</b>							
Q <sub>GD</sub>	gate-drain charge	V <sub>GS</sub> = 5 V; I <sub>D</sub> = 25 A; V <sub>DS</sub> = 24 V; <a href="#">Fig. 13</a> ; <a href="#">Fig. 14</a>		-	30.8	-	nC

[1] Continuous current is limited by package.

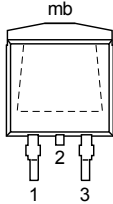
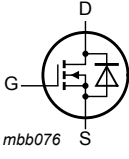


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## 2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate	 <p><b>D2PAK (SOT404)</b></p>	
2	D	drain		
3	S	source		
mb	D	mounting base; connected to drain		

## 3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BUK961R5-30E	D2PAK	plastic single-ended surface-mounted package (D2PAK); 3 leads (one lead cropped)	SOT404

## 4. Marking

Table 4. Marking codes

Type number	Marking code
BUK961R5-30E	BUK961R5-30E

## 5. Limiting values

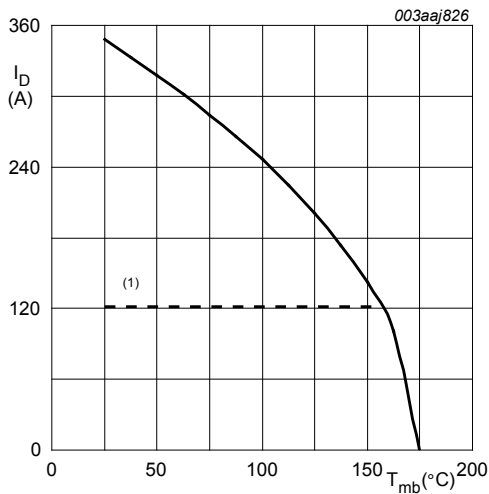
Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
$V_{DS}$	drain-source voltage	$T_j \geq 25\text{ }^{\circ}\text{C}$ ; $T_j \leq 175\text{ }^{\circ}\text{C}$		-	30	V
$V_{DGR}$	drain-gate voltage	$R_{GS} = 20\text{ k}\Omega$		-	30	V
$V_{GS}$	gate-source voltage	$T_j \leq 175\text{ }^{\circ}\text{C}$ ; DC		-10	10	V
		$T_j \leq 175\text{ }^{\circ}\text{C}$ ; Pulsed	[1][2]	-15	15	V
$I_D$	drain current	$T_{mb} = 25\text{ }^{\circ}\text{C}$ ; $V_{GS} = 5\text{ V}$ ; Fig. 1	[3]	-	120	A
		$T_{mb} = 100\text{ }^{\circ}\text{C}$ ; $V_{GS} = 5\text{ V}$ ; Fig. 1	[3]	-	120	A
$I_{DM}$	peak drain current	$T_{mb} = 25\text{ }^{\circ}\text{C}$ ; pulsed; $t_p \leq 10\text{ }\mu\text{s}$ ; Fig. 4		-	1393	A
$P_{tot}$	total power dissipation	$T_{mb} = 25\text{ }^{\circ}\text{C}$ ; Fig. 2		-	324	W
$T_{stg}$	storage temperature			-55	175	$^{\circ}\text{C}$

Symbol	Parameter	Conditions		Min	Max	Unit
T <sub>j</sub>	junction temperature			-55	175	°C
Source-drain diode						
I <sub>S</sub>	source current	T <sub>mb</sub> = 25 °C	[3]	-	120	A
I <sub>SM</sub>	peak source current	pulsed; t <sub>p</sub> ≤ 10 μs; T <sub>mb</sub> = 25 °C		-	1393	A
Avalanche ruggedness						
E <sub>DS(AL)S</sub>	non-repetitive drain-source avalanche energy	I <sub>D</sub> = 120 A; V <sub>sup</sub> ≤ 30 V; R <sub>GS</sub> = 50 Ω; V <sub>GS</sub> = 5 V; T <sub>j(init)</sub> = 25 °C; unclamped; Fig. 3	[4][5]	-	1096	mJ

- [1] Accumulated pulse duration up to 50 hours delivers zero defect ppm
- [2] Significantly longer life times are achieved by lowering T<sub>j</sub> and or V<sub>GS</sub>
- [3] Continuous current is limited by package
- [4] Single-pulse avalanche rating limited by maximum junction temperature of 175 °C.
- [5] Refer to application note AN10273 for further information.



(1) Capped at 120A due to package

Fig. 1. Continuous drain current as a function of mounting base temperature

$V_{GS} \geq 5V$

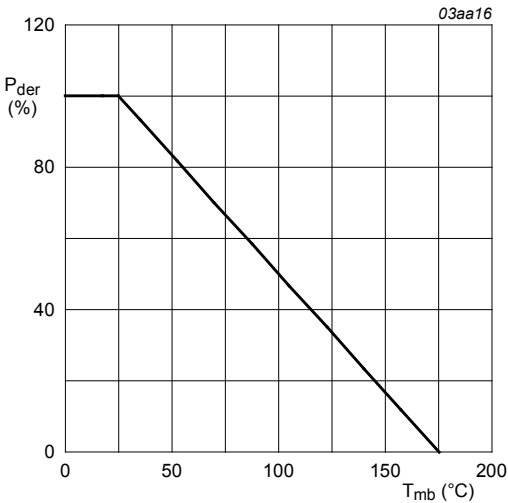


Fig. 2. Normalized total power dissipation as a function of mounting base temperature

$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}C)}} \times 100\%$$

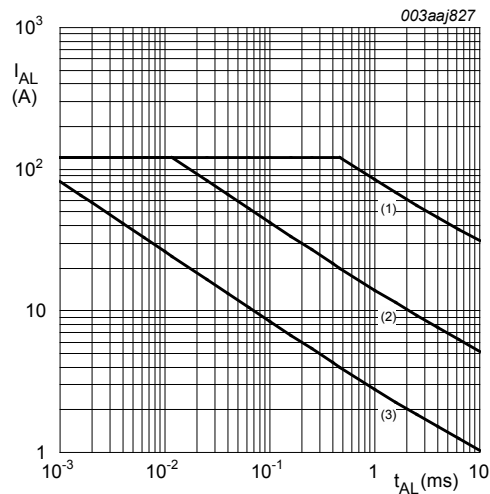


Fig. 3. Avalanche rating; avalanche current as a function of avalanche time.

(1)  $T_{j(int)} = 25^{\circ}\text{C}$ ; (2)  $T_{j(int)} = 150^{\circ}\text{C}$ ; (3) Repetitive Avalanche

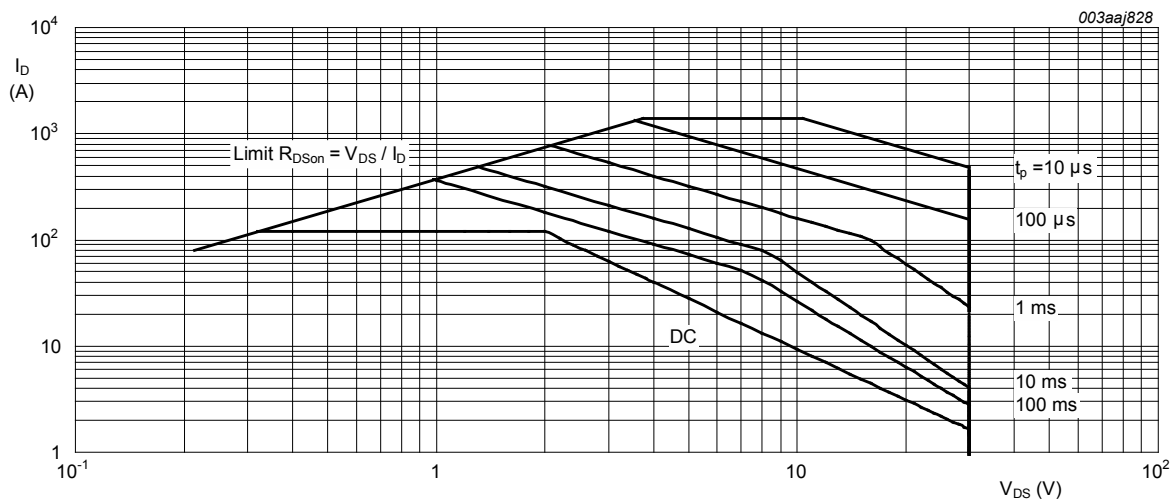


Fig. 4. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

$T_{mb} = 25^{\circ}\text{C}$ ;  $I_{DM}$  is a single pulse

## 6. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	<a href="#">Fig. 5</a>	-	-	0.46	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	minimum footprint ; mounted on a printed-circuit board	-	50	-	K/W

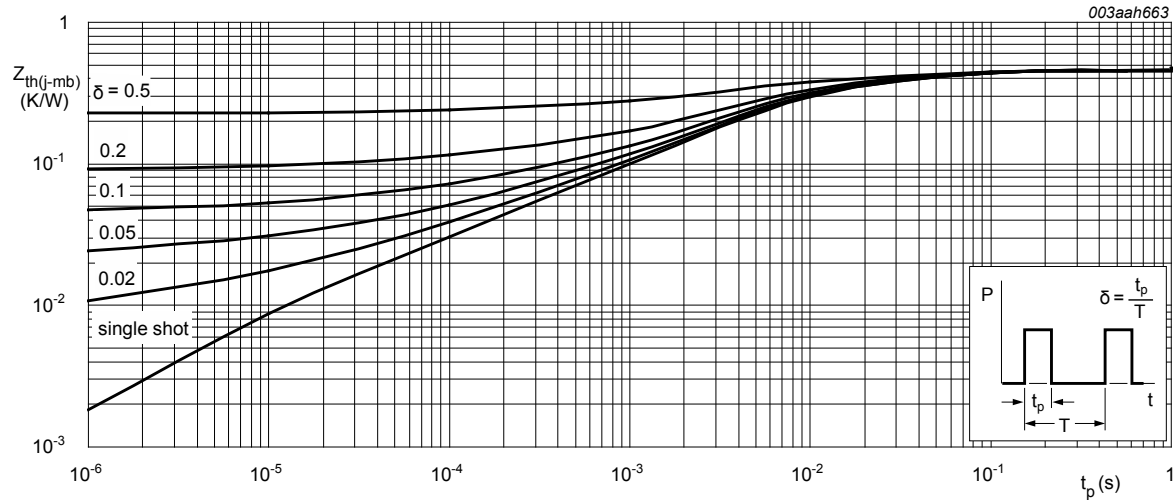


Fig. 5. Transient thermal impedance from junction to mounting base as a function of pulse duration

## 7. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Static characteristics							
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250\text{ }\mu\text{A}$ ; $V_{GS} = 0\text{ V}$ ; $T_j = 25\text{ }^\circ\text{C}$		30	-	-	V
		$I_D = 250\text{ }\mu\text{A}$ ; $V_{GS} = 0\text{ V}$ ; $T_j = -55\text{ }^\circ\text{C}$		27	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1\text{ mA}$ ; $V_{DS} = V_{GS}$ ; $T_j = 25\text{ }^\circ\text{C}$ ; <a href="#">Fig. 9</a> ; <a href="#">Fig. 10</a>		1.4	1.7	2.1	V
		$I_D = 1\text{ mA}$ ; $V_{DS} = V_{GS}$ ; $T_j = -55\text{ }^\circ\text{C}$ ; <a href="#">Fig. 9</a>		-	-	2.45	V
		$I_D = 1\text{ mA}$ ; $V_{DS} = V_{GS}$ ; $T_j = 175\text{ }^\circ\text{C}$ ; <a href="#">Fig. 9</a>		0.5	-	-	V
$I_{DSS}$	drain leakage current	$V_{DS} = 30\text{ V}$ ; $V_{GS} = 0\text{ V}$ ; $T_j = 25\text{ }^\circ\text{C}$		-	0.03	1	$\mu\text{A}$
		$V_{DS} = 30\text{ V}$ ; $V_{GS} = 0\text{ V}$ ; $T_j = 175\text{ }^\circ\text{C}$		-	-	500	$\mu\text{A}$
$I_{GSS}$	gate leakage current	$V_{GS} = 10\text{ V}$ ; $V_{DS} = 0\text{ V}$ ; $T_j = 25\text{ }^\circ\text{C}$		-	2	100	nA
		$V_{GS} = -10\text{ V}$ ; $V_{DS} = 0\text{ V}$ ; $T_j = 25\text{ }^\circ\text{C}$		-	2	100	nA
$R_{DSon}$	drain-source on-state resistance	$V_{GS} = 5\text{ V}$ ; $I_D = 25\text{ A}$ ; $T_j = 25\text{ }^\circ\text{C}$ ; <a href="#">Fig. 11</a>		-	1.3	1.5	m $\Omega$
		$V_{GS} = 10\text{ V}$ ; $I_D = 25\text{ A}$ ; $T_j = 25\text{ }^\circ\text{C}$ ; <a href="#">Fig. 11</a>		-	1.12	1.3	m $\Omega$
		$V_{GS} = 5\text{ V}$ ; $I_D = 25\text{ A}$ ; $T_j = 175\text{ }^\circ\text{C}$ ; <a href="#">Fig. 11</a> ; <a href="#">Fig. 12</a>		-	-	2.7	m $\Omega$
Dynamic characteristics							
$Q_{G(tot)}$	total gate charge	$I_D = 25\text{ A}$ ; $V_{DS} = 24\text{ V}$ ; $V_{GS} = 5\text{ V}$ ; <a href="#">Fig. 13</a> ; <a href="#">Fig. 14</a>		-	93.4	-	nC
$Q_{GS}$	gate-source charge			-	26.1	-	nC

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$Q_{GD}$	gate-drain charge			-	30.8	-	nC
$C_{iss}$	input capacitance	$V_{GS} = 0\text{ V}; V_{DS} = 25\text{ V}; f = 1\text{ MHz};$ $T_j = 25\text{ }^{\circ}\text{C};$ <a href="#">Fig. 15</a>		-	10870	14500	pF
$C_{oss}$	output capacitance			-	1597	1916	pF
$C_{rss}$	reverse transfer capacitance			-	702	961	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = 25\text{ V}; R_L = 1\text{ }\Omega; V_{GS} = 5\text{ V};$ $R_{G(ext)} = 5\text{ }\Omega$		-	55.5	-	ns
$t_r$	rise time			-	101	-	ns
$t_{d(off)}$	turn-off delay time			-	112	-	ns
$t_f$	fall time			-	85	-	ns
$L_D$	internal drain inductance	from upper edge of drain mounting base to center of die		-	2.5	-	nH
$L_S$	internal source inductance	from source lead to source bonding pad		-	7.5	-	nH
Source-drain diode							
$V_{SD}$	source-drain voltage	$I_S = 25\text{ A}; V_{GS} = 0\text{ V}; T_j = 25\text{ }^{\circ}\text{C};$ <a href="#">Fig. 16</a>		-	0.77	1.2	V
$t_{rr}$	reverse recovery time	$I_S = 20\text{ A}; dI_S/dt = -100\text{ A}/\mu\text{s}; V_{GS} = 0\text{ V};$ $V_{DS} = 25\text{ V}$		-	50.6	-	ns
$Q_r$	recovered charge			-	72.2	-	nC

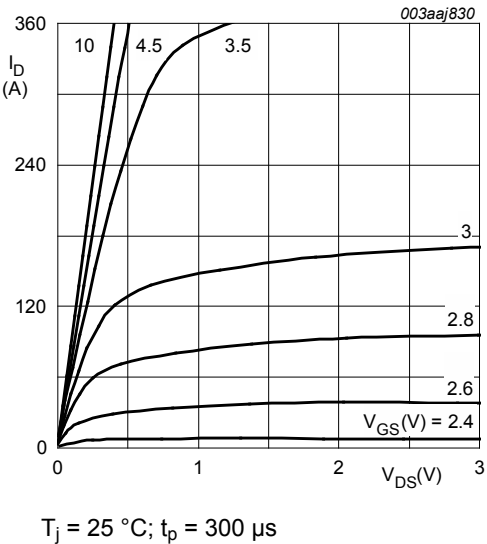


Fig. 6. Output characteristics; drain current as a function of drain-source voltage; typical values

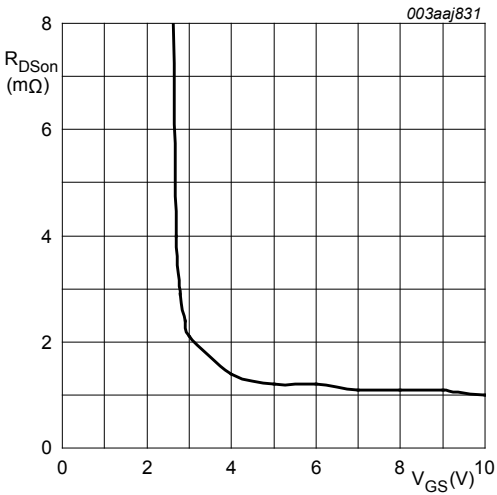


Fig. 7. Drain-source on-state resistance as a function of gate-source voltage; typical values

$T_j = 25\text{ }^{\circ}\text{C}; I_D = 25\text{ A}$

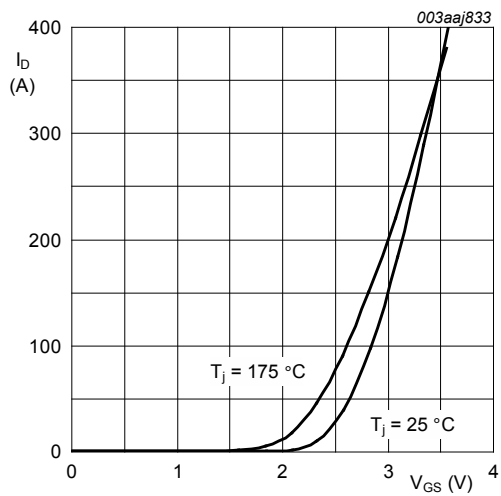


Fig. 8. Transfer characteristics; drain current as a function of gate-source voltage; typical values

$V_{DS} = 10\text{ V}$

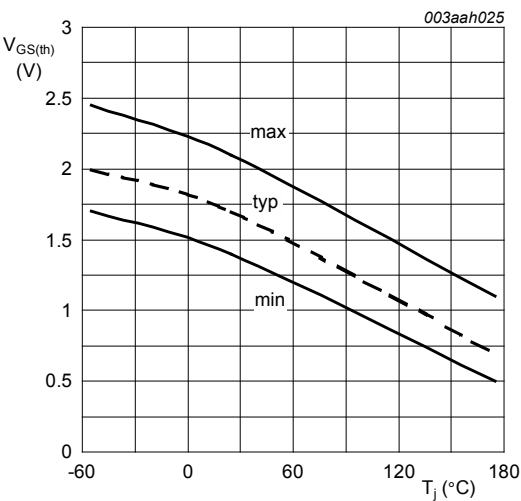


Fig. 9. Gate-source threshold voltage as a function of junction temperature

$I_D = 1\text{ mA}; V_{DS} = V_{GS}$

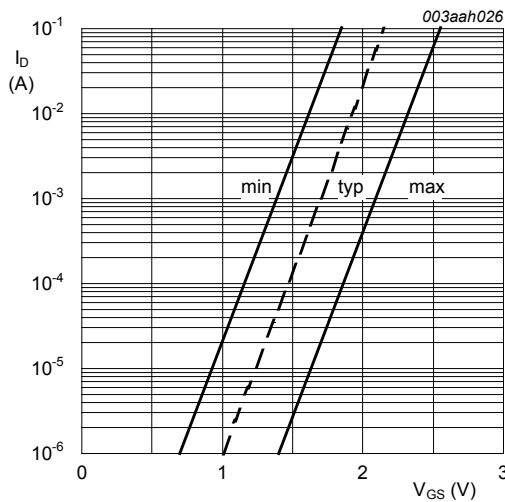


Fig. 10. Sub-threshold drain current as a function of gate-source voltage

$T_j = 25\text{ °C}; V_{DS} = 5\text{ V}$

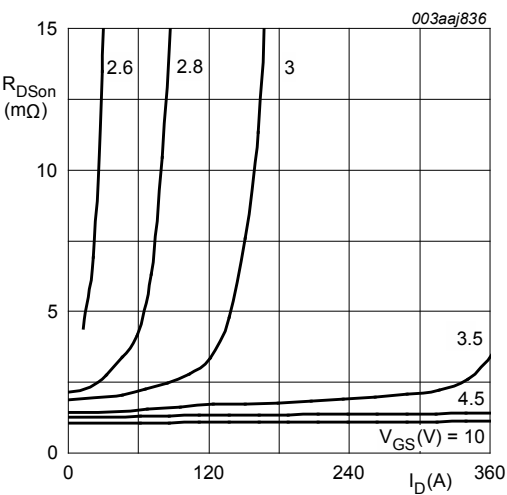


Fig. 11. Drain-source on-state resistance as a function of drain current; typical values

$T_j = 25\text{ °C}; t_p = 300\text{ }\mu\text{s}$

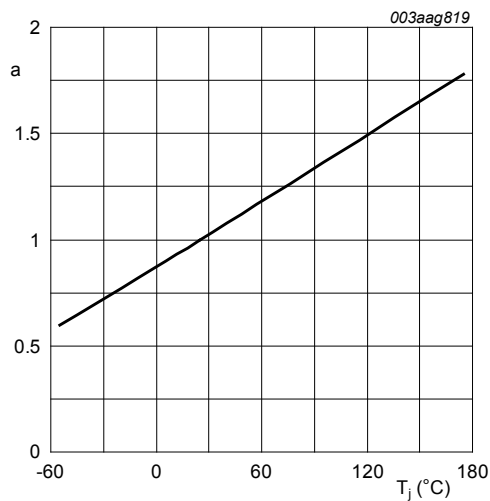


Fig. 12. Normalized drain-source on-state resistance factor as a function of junction temperature

$$a = \frac{R_{DSon}}{R_{DSon(25\text{ }^{\circ}\text{C})}}$$

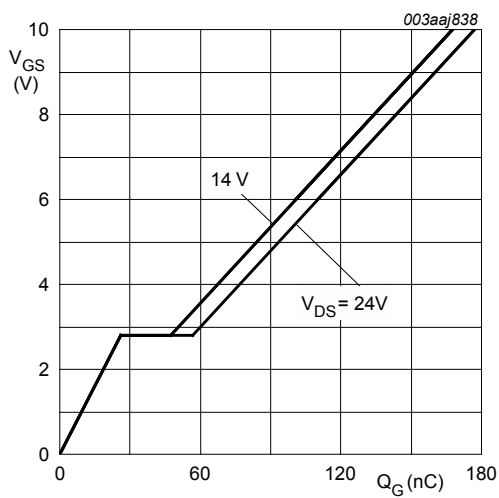


Fig. 14. Gate-source voltage as a function of gate charge; typical values

$$T_j = 25^{\circ}\text{C}; I_D = 25\text{ A}$$

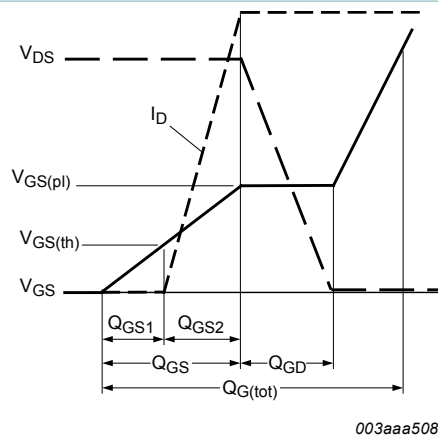


Fig. 13. Gate charge waveform definitions

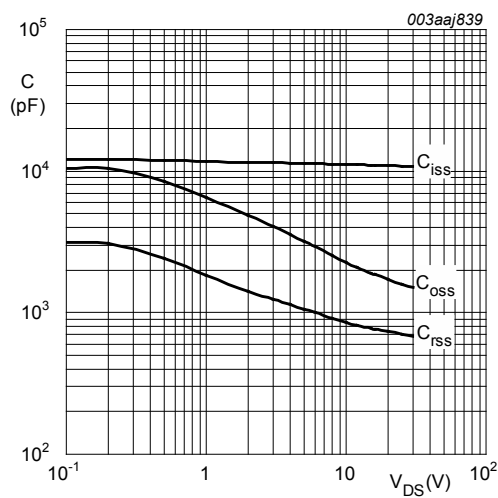


Fig. 15. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

$$V_{GS} = 0\text{ V}; f = 1\text{ MHz}$$

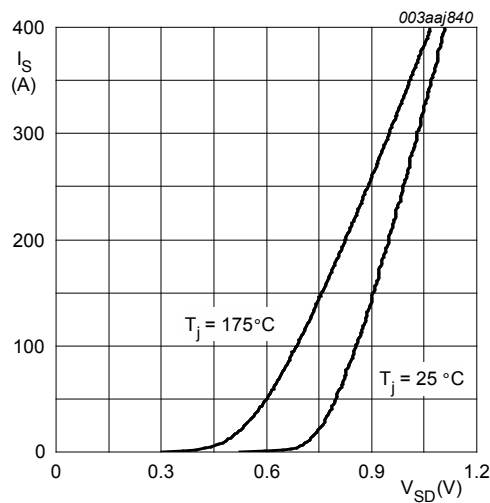


Fig. 16. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values

$V_{GS} = 0\text{V}$

8. Package outline

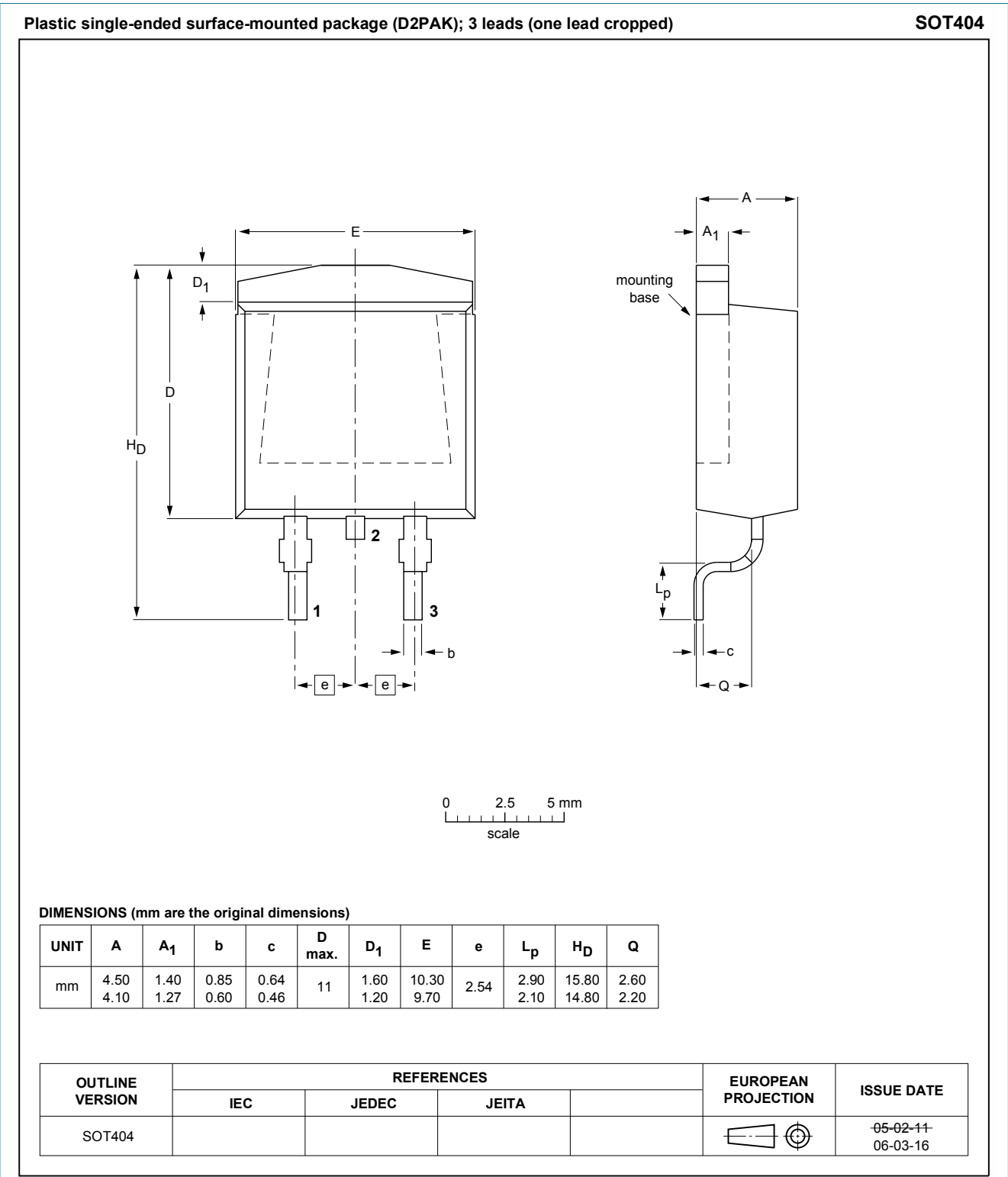


Fig. 17. Package outline D2PAK (SOT404)

## 9. Legal information

### 9.1 Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
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