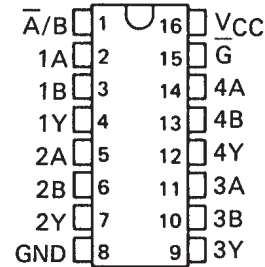


SN54LS257B, SN54LS258B, SN54S257, SN54S258 SN74LS257B, SN74LS258B, SN74S257, SN74S258 QUADRUPLE 2-LINE TO 1-LINE DATA SELECTORS/MULTIPLEXERS

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- Three-State Outputs Interface Directly with System Bus
- 'LS257B and 'LS258B Offer Three Times the Sink-Current Capability of the Original 'LS257 and 'LS258
- Same Pin Assignments as SN54LS157, SN74LS157, SN54S157, SN74S157, and SN54LS158, SN74LS158, SN54S158, SN74S158
- Provides Bus Interface from Multiple Sources in High-Performance Systems

SN54LS257B, SN54S257,
SN54LS258B, SN54S258 . . . J OR W PACKAGE
SN74LS257B, SN74S257,
SN74LS258B, SN74S258 . . . D OR N PACKAGE
(TOP VIEW)



	AVERAGE PROPAGATION DELAY FROM DATA INPUT	TYPICAL POWER DISSIPATION†
'LS257B	9 ns	55 mW
'LS258B	9 ns	55 mW
'S257	4.8 ns	320 mW
'S258	4 ns	280 mW

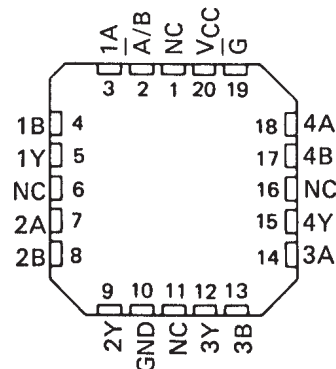
† Off state (worst case)

description

These devices are designed to multiplex signals from four-bit data sources to four-output data lines in bus-organized systems. The 3-state outputs will not load the data lines when the output control pin ($\bar{G}$) is at a high-logic level.

Series 54LS and 54S are characterized for operation over the full military temperature range of -55°C to 125°C ; Series 74LS and 74S are characterized for operation from 0°C to 70°C .

SN54LS257B, SN54S257,
SN54LS258B, SN54S258 . . . FK PACKAGE
(TOP VIEW)



NC-No internal connection.

FUNCTION TABLE

INPUTS				OUTPUT Y	
OUTPUT CONTROL	SELECT	A	B	'LS257B 'S257	'LS258B 'S258
H	X	X	X	Z	Z
L	L	L	X	L	H
L	L	H	X	H	L
L	H	X	L	L	H
L	H	X	H	H	L

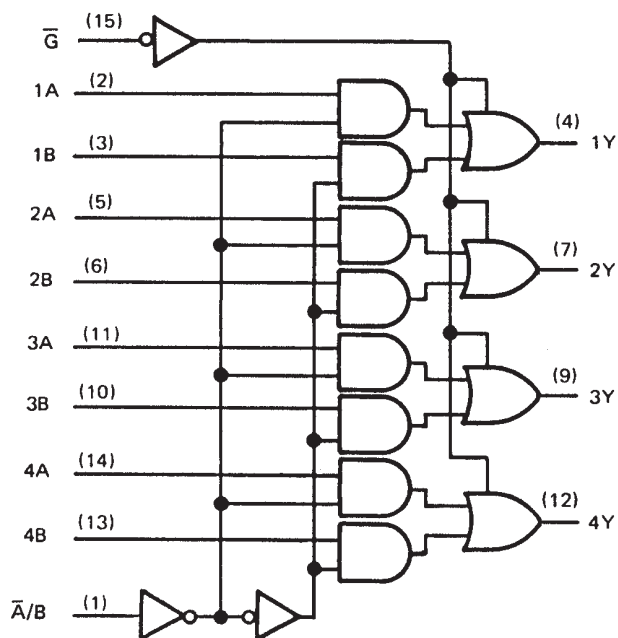
H = high level, L = low level, X = irrelevant,
Z = high impedance (off)

SN54LS257B, SN54LS258B, SN54S257, SN54S258
 SN74LS257B, SN74LS258B, SN74S257, SN74S258
 QUADRUPLE 2-LINE TO 1-LINE DATA SELECTORS/MULTIPLEXERS

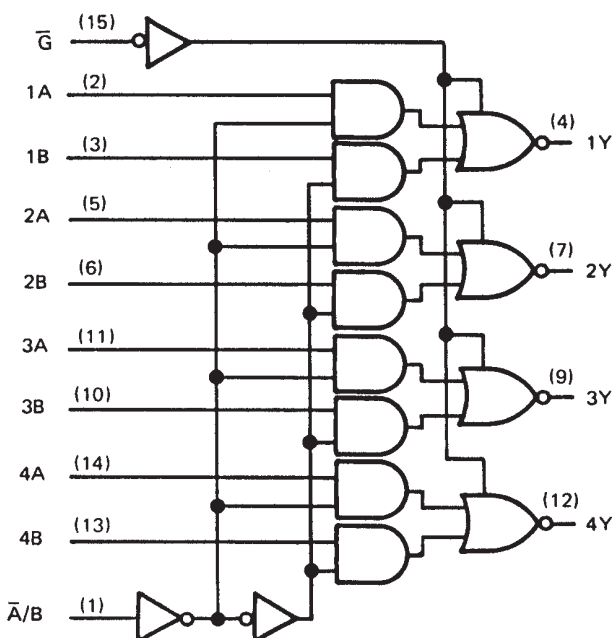
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logic diagrams (positive logic)

'LS257B, 'S257

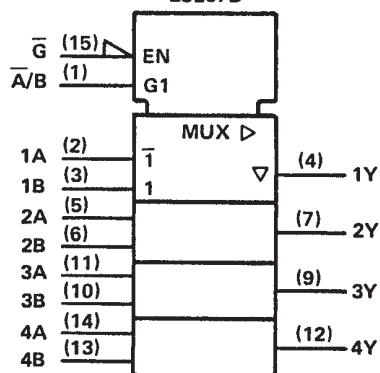


'LS258B, 'S258

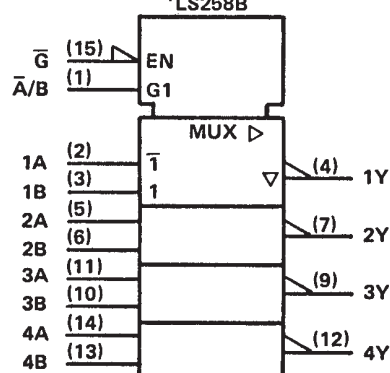


logic symbols†

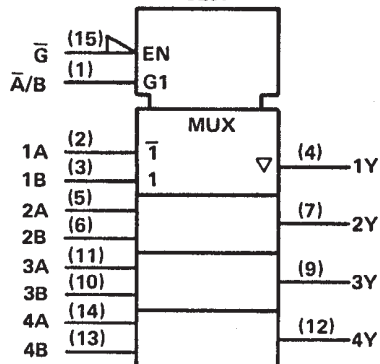
'LS257B



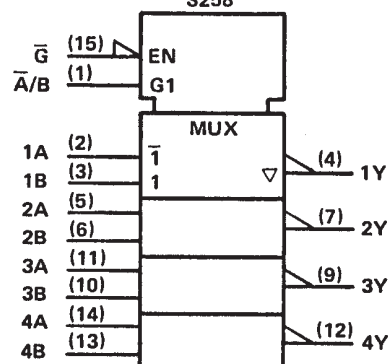
'LS258B



'S257



'S258

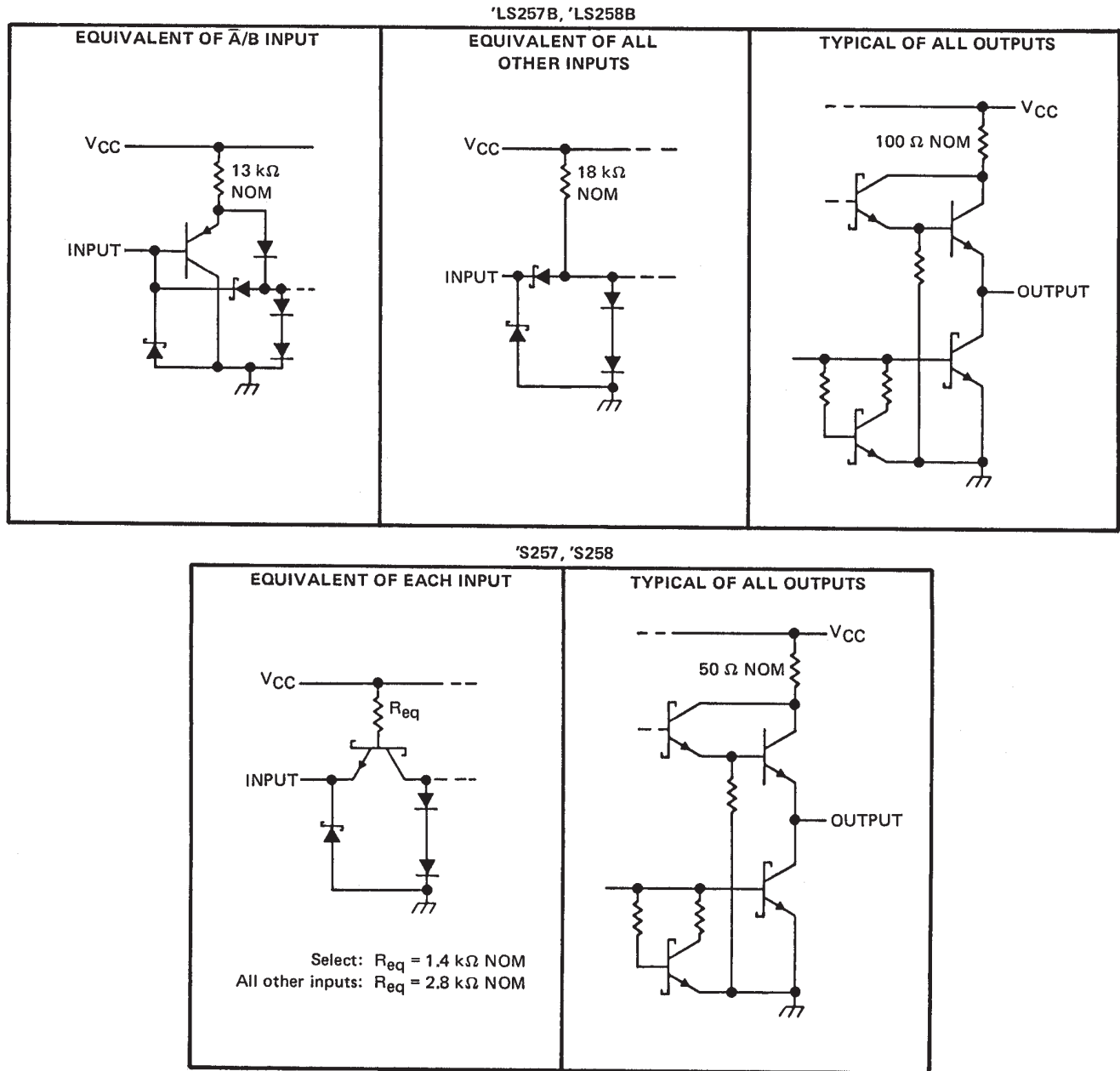


†These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
 Pin numbers shown are for D, J, N, and W packages.

SN54LS257B, SN54LS258B, SN54S257, SN54S258
SN74LS257B, SN74LS258B, SN74S257, SN74S258
QUADRUPLE 2-LINE TO 1-LINE DATA SELECTORS/MULTIPLEXERS

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schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage: 'LS257B, 'LS258B Circuits	7 V
'S257, 'S258 Circuits	5.5 V
Off-state output voltage	5.5 V
Operating free-air temperature range: SN54LS', SN54S' Circuits	-55°C to 125°C
SN74LS', SN74S' Circuits	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

SN54LS257B, SN54LS258B, SN54S257, SN54S258
SN74LS257B, SN74LS258B, SN74S257, SN74S258
QUADRUPLE 2-LINE TO 1-LINE DATA SELECTORS/MULTIPLEXERS

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recommended operating conditions

	SN54LS'			SN74LS'			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC} Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH} High-level input voltage	2			2			V
V_{IL} Low-level input voltage			0.7			0.8	V
I_{OH} High-level output current			– 1			– 2.6	mA
I_{OL} Low-level output current			12			24	mA
T_A Operating free-air temperature	– 55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	SN54LS'			SN74LS'			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}		$V_{CC} = \text{MIN}, I_I = -18 \text{ mA}$			– 1.5			– 1.5	V
V_{OH}		$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = \text{MAX}, I_{OH} = \text{MAX}$	2.4	3.4		2.4	3.1		V
V_{OL}		$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = \text{MAX}, I_{OL} = 12 \text{ mA}$	0.25	0.4		0.25	0.4		V
		$I_{OL} = 24 \text{ mA}$				0.35	0.5		
I_{OZH}		$V_{CC} = \text{MAX}, V_{IH} = 2 \text{ V}, V_O = 2.7 \text{ V}$		20			20		µA
I_{OZL}		$V_{CC} = \text{MAX}, V_{IH} = 2 \text{ V}, V_O = 0.4 \text{ V}$		– 20			– 20		µA
I_I		$V_{CC} = \text{MAX}, V_I = 7 \text{ V}$		0.1			0.1		mA
I_{IH}		$V_{CC} = \text{MAX}, V_I = 2.7 \text{ V}$		20			20		µA
I_{IL}		$V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$		– 0.4			– 0.4		mA
$I_{OS}§$		$V_{CC} = \text{MAX},$	– 30		– 130	– 30		– 130	mA
I_{CC}	All outputs high	$V_{CC} = \text{MAX},$ See Note 2	'LS257B	8	12	'LS258B	8	12	mA
	All outputs low			12	18		12	18	
	All outputs off			13	19		13	19	
	All outputs high		'LS258B	6	9		6	9	
	All outputs low			10	15		10	15	
	All outputs off			11	16		11	16	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$.

§ Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

NOTE 2: I_{CC} is measured with all outputs open and all possible inputs grounded while achieving the stated output conditions.

switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}, R_L = 667 \Omega$

PARAMETER ¹	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'LS257B			'LS258B			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
t _{PLH}	Data	Any	C _L = 45 pF, See Note 3	8	13		7	12	ns	
t _{PHL}				10	15		11	17		
t _{PLH}	Select	Any		16	21		14	21	ns	
t _{PHL}				17	24		19	24		
t _{pZH}	Output Control	Any		15	30		15	30	ns	
t _{pZL}				19	30		20	30		
t _{PHZ}	Output Control	Any	C _L = 5 pF, See Note 3	18	30		18	30	ns	
t _{PLZ}			16	25		16	25			

¶ t_{PLH} = propagation delay time, low-to-high-level output

t_{PHL} = propagation delay time, high-to-low-level output

t_{pZH} = output enable time to high level

t_{pZL} = output enable time to low level

t_{PHZ} = output disable time from high level

t_{PLZ} = output disable time from low level

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.



SN54LS257B, SN54LS258B, SN54S257, SN54S258
SN74LS257B, SN74LS258B, SN74S257, SN74S258
QUADRUPLE 2-LINE TO 1-LINE DATA SELECTORS/MULTIPLEXERS

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recommended operating conditions

	SN54S'			SN74S'			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			-2			-6.5	mA
Low-level output current, I_{OL}			20			20	mA
Operating free-air temperature, T_A	-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†	'S257			'S258			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V _{IH} High-level input voltage						2		2		V
V _{IL} Low-level input voltage							0.8		0.8	V
V _{IK} Input clamp voltage			V _{CC} = MIN, I _I = −18 mA				−1.2		−1.2	V
V _{OH} High-level output voltage			V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = 0.8 V, I _{OH} = −1 mA	SN74S'	2.7		2.7		V	
			V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = 0.8 V, I _{OH} = MAX	SN54S'	2.4	3.4	2.4	3.4		
				SN74S'	2.4	3.2	2.4	3.2		
V _{OL} Low-level output voltage			V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = 0.8 V, I _{OL} = 20 mA				0.5		0.5	V
I _{OZH} Off-state output current, high-level voltage applied			V _{CC} = MAX, V _{IH} = 2 V, V _O = 2.4 V				50		50	μA
I _{OZL} Off-state output current, low-level voltage applied			V _{CC} = MAX, V _{IH} = 2 V, V _O = 0.5 V				−50		−50	μA
I _I Input current at maximum input voltage			V _{CC} = MAX, V _I = 5.5 V				1		1	mA
I _{IH} High-level input current		S input	V _{CC} = MAX, V _I = 2.7 V			100		100		μA
		Any other				50		50		
I _{IL} Low-level input current		S input	V _{CC} = MAX V _I = 0.5 V			−4		−4		mA
		Any other				−2		−2		
I _{OS} Short-circuit output current§			V _{CC} = MAX			−40	−100	−40	−100	mA
I _{CC} Supply current		All outputs high	V _{CC} = MAX, See Note 2			44	68	36	56	mA
		All outputs low				60	93	52	81	
		All outputs off				64	99	56	87	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$.

§ Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

NOTE 2: I_{CC} is measured with all outputs open and all possible inputs grounded while achieving the stated output conditions.

switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}, R_L = 280 \Omega$

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'S257			'S258			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
tPLH	Data	Any	C _L = 15 pF, See Note 3	5	7.5		4	6	ns	
tPHL				4.5	6.5		4	6		
tPLH	Select	Any		8.5	15		8	12	ns	
tPHL				8.5	15		7.5	12		
tPZH	Output	Any		13	19.5		13	19.5	ns	
tPZL	Control			14	21		14	21		
tPHZ	Output	Any	C _L = 5 pF, See Note 3	5.5	8.5		5.5	8.5	ns	
tPLZ	Control		9	14		9	14			

¶ f_{max} = Maximum clock frequency

t_{PLH} = propagation delay time, low-to-high-level output

t_{PHL} = propagation delay time, high-to-low-level output

t_{PZH} = output enable time to high level

t_{PZL} = output enable time to low level

t_{PHZ} = output disable time from high level

t_{PLZ} = output disable time from low level

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.



PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-7603701VEA	ACTIVE	CDIP	J	16	25	TBD	A42	N / A for Pkg Type	-55 to 125	5962-7603701VE A SNV54LS257BJ	Samples
5962-7603701VFA	ACTIVE	CFP	W	16	25	TBD	A42	N / A for Pkg Type	-55 to 125	5962-7603701VF A SNV54LS257BW	Samples
5962-7603701VFA	ACTIVE	CFP	W	16	25	TBD	A42	N / A for Pkg Type	-55 to 125	5962-7603701VF A SNV54LS257BW	Samples
7603701EA	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	7603701EA SNJ54LS257BJ	Samples
7603701EA	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	7603701EA SNJ54LS257BJ	Samples
7603701FA	ACTIVE	CFP	W	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	7603701FA SNJ54LS257BW	Samples
7603701FA	ACTIVE	CFP	W	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	7603701FA SNJ54LS257BW	Samples
76038012A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	76038012A SNJ54LS 258BFBK	Samples
76038012A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	76038012A SNJ54LS 258BFBK	Samples
7603801EA	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	7603801EA SNJ54LS258BJ	Samples
7603801EA	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	7603801EA SNJ54LS258BJ	Samples
7603801FA	ACTIVE	CFP	W	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	7603801FA SNJ54LS258BW	Samples
7603801FA	ACTIVE	CFP	W	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	7603801FA SNJ54LS258BW	Samples
8002301EA	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	8002301EA SNJ54S258J	Samples
8002301EA	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	8002301EA SNJ54S258J	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
8002301FA	ACTIVE	CFP	W	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	8002301FA SNJ54S258W	Samples
8002301FA	ACTIVE	CFP	W	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	8002301FA SNJ54S258W	Samples
JM38510/07906BEA	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/ 07906BEA	Samples
JM38510/07906BEA	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/ 07906BEA	Samples
JM38510/07906BFA	ACTIVE	CFP	W	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/ 07906BFA	Samples
JM38510/07906BFA	ACTIVE	CFP	W	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/ 07906BFA	Samples
JM38510/30906B2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	JM38510/ 30906B2A	Samples
JM38510/30906B2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	JM38510/ 30906B2A	Samples
JM38510/30906BEA	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/ 30906BEA	Samples
JM38510/30906BEA	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/ 30906BEA	Samples
JM38510/30906BFA	ACTIVE	CFP	W	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/ 30906BFA	Samples
JM38510/30906BFA	ACTIVE	CFP	W	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/ 30906BFA	Samples
M38510/07906BEA	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/ 07906BEA	Samples
M38510/07906BEA	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/ 07906BEA	Samples
M38510/07906BFA	ACTIVE	CFP	W	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/ 07906BFA	Samples
M38510/07906BFA	ACTIVE	CFP	W	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/ 07906BFA	Samples
M38510/30906B2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	JM38510/ 30906B2A	Samples
M38510/30906B2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	JM38510/ 30906B2A	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
M38510/30906BEA	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/ 30906BEA	Samples
M38510/30906BEA	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/ 30906BEA	Samples
M38510/30906BFA	ACTIVE	CFP	W	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/ 30906BFA	Samples
M38510/30906BFA	ACTIVE	CFP	W	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/ 30906BFA	Samples
SN54LS257BJ	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	SN54LS257BJ	Samples
SN54LS257BJ	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	SN54LS257BJ	Samples
SN54LS258BJ	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	SN54LS258BJ	Samples
SN54LS258BJ	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	SN54LS258BJ	Samples
SN54S257J	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	SN54S257J	Samples
SN54S257J	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	SN54S257J	Samples
SN54S258J	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	SN54S258J	Samples
SN54S258J	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	SN54S258J	Samples
SN74LS257BD	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	LS257B	Samples
SN74LS257BD	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	LS257B	Samples
SN74LS257BDE4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	LS257B	Samples
SN74LS257BDE4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	LS257B	Samples
SN74LS257BDG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	LS257B	Samples
SN74LS257BDG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	LS257B	Samples
SN74LS257BDR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	LS257B	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74LS257BDR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	LS257B	Samples
SN74LS257BN	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN74LS257BN	Samples
SN74LS257BN	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN74LS257BN	Samples
SN74LS257BN3	OBSOLETE	PDIP	N	16		TBD	Call TI	Call TI	0 to 70		
SN74LS257BN3	OBSOLETE	PDIP	N	16		TBD	Call TI	Call TI	0 to 70		
SN74LS257BNE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN74LS257BN	Samples
SN74LS257BNE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN74LS257BN	Samples
SN74LS257BNSR	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	74LS257B	Samples
SN74LS257BNSR	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	74LS257B	Samples
SN74LS258BD	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	LS258B	Samples
SN74LS258BD	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	LS258B	Samples
SN74LS258BDR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	LS258B	Samples
SN74LS258BDR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	LS258B	Samples
SN74LS258BN	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN74LS258BN	Samples
SN74LS258BN	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN74LS258BN	Samples
SN74LS258BN3	OBSOLETE	PDIP	N	16		TBD	Call TI	Call TI	0 to 70		
SN74LS258BN3	OBSOLETE	PDIP	N	16		TBD	Call TI	Call TI	0 to 70		
SN74S257N	NRND	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN74S257N	
SN74S257N	NRND	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN74S257N	
SN74S257N3	OBSOLETE	PDIP	N	16		TBD	Call TI	Call TI	0 to 70		

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74S257N3	OBSOLETE	PDIP	N	16		TBD	Call TI	Call TI	0 to 70		
SN74S258DR	OBSOLETE	SOIC	D	16		TBD	Call TI	Call TI	0 to 70		
SN74S258DR	OBSOLETE	SOIC	D	16		TBD	Call TI	Call TI	0 to 70		
SN74S258N	OBSOLETE	PDIP	N	16		TBD	Call TI	Call TI	0 to 70		
SN74S258N	OBSOLETE	PDIP	N	16		TBD	Call TI	Call TI	0 to 70		
SN74S258N3	OBSOLETE	PDIP	N	16		TBD	Call TI	Call TI	0 to 70		
SN74S258N3	OBSOLETE	PDIP	N	16		TBD	Call TI	Call TI	0 to 70		
SNJ54LS257BFK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	SNJ54LS 257BFK	Samples
SNJ54LS257BFK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	SNJ54LS 257BFK	Samples
SNJ54LS257BJ	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	7603701EA SNJ54LS257BJ	Samples
SNJ54LS257BJ	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	7603701EA SNJ54LS257BJ	Samples
SNJ54LS257BW	ACTIVE	CFP	W	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	7603701FA SNJ54LS257BW	Samples
SNJ54LS257BW	ACTIVE	CFP	W	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	7603701FA SNJ54LS257BW	Samples
SNJ54LS258BFK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	76038012A SNJ54LS 258BFK	Samples
SNJ54LS258BFK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	76038012A SNJ54LS 258BFK	Samples
SNJ54LS258BJ	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	7603801EA SNJ54LS258BJ	Samples
SNJ54LS258BJ	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	7603801EA SNJ54LS258BJ	Samples
SNJ54LS258BW	ACTIVE	CFP	W	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	7603801FA SNJ54LS258BW	Samples
SNJ54LS258BW	ACTIVE	CFP	W	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	7603801FA SNJ54LS258BW	Samples
SNJ54S257FK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	SNJ54S 257FK	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SNJ54S257FK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	SNJ54S 257FK	Samples
SNJ54S257J	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	SNJ54S257J	Samples
SNJ54S257J	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	SNJ54S257J	Samples
SNJ54S257W	ACTIVE	CFP	W	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	SNJ54S257W	Samples
SNJ54S257W	ACTIVE	CFP	W	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	SNJ54S257W	Samples
SNJ54S258FK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	SNJ54S 258FK	Samples
SNJ54S258FK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	SNJ54S 258FK	Samples
SNJ54S258J	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	8002301EA SNJ54S258J	Samples
SNJ54S258J	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	8002301EA SNJ54S258J	Samples
SNJ54S258W	ACTIVE	CFP	W	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	8002301FA SNJ54S258W	Samples
SNJ54S258W	ACTIVE	CFP	W	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	8002301FA SNJ54S258W	Samples

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

- ⁽³⁾ MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.
- ⁽⁴⁾ There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.
- ⁽⁵⁾ Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.
- ⁽⁶⁾ Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF SN54LS257B, SN54LS257B-SP, SN54LS258B, SN54S257, SN54S258, SN74LS257B, SN74LS258B, SN74S257, SN74S258 :

- Catalog: [SN74LS257B](#), [SN54LS257B](#), [SN74LS258B](#), [SN74S257](#), [SN74S258](#)
- Military: [SN54LS257B](#), [SN54LS258B](#), [SN54S257](#), [SN54S258](#)
- Space: [SN54LS257B-SP](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications
- Space - Radiation tolerant, ceramic packaging and qualified for use in Space-based application

TAPE AND REEL INFORMATION
REEL DIMENSIONS

TAPE DIMENSIONS


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LS257BDR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN74LS257BNSR	SO	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
SN74LS258BDR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LS257BDR	SOIC	D	16	2500	333.2	345.9	28.6
SN74LS257BNSR	SO	NS	16	2000	367.0	367.0	38.0
SN74LS258BDR	SOIC	D	16	2500	333.2	345.9	28.6

J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



PINS ** DIM	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package is hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

W (R-GDFP-F16)

CERAMIC DUAL FLATPACK



- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package can be hermetically sealed with a ceramic lid using glass frit.
 - Index point is provided on cap for terminal identification only.
 - Falls within MIL STD 1835 GDFP2-F16

FK (S-CQCC-N**)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.740 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)



4040140/D 01/11

- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package can be hermetically sealed with a metal lid.
 - Falls within JEDEC MS-004

N (R-PDIP-T**)

16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



PINS ** DIM	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS-001 VARIATION	AA	BB	AC	AD



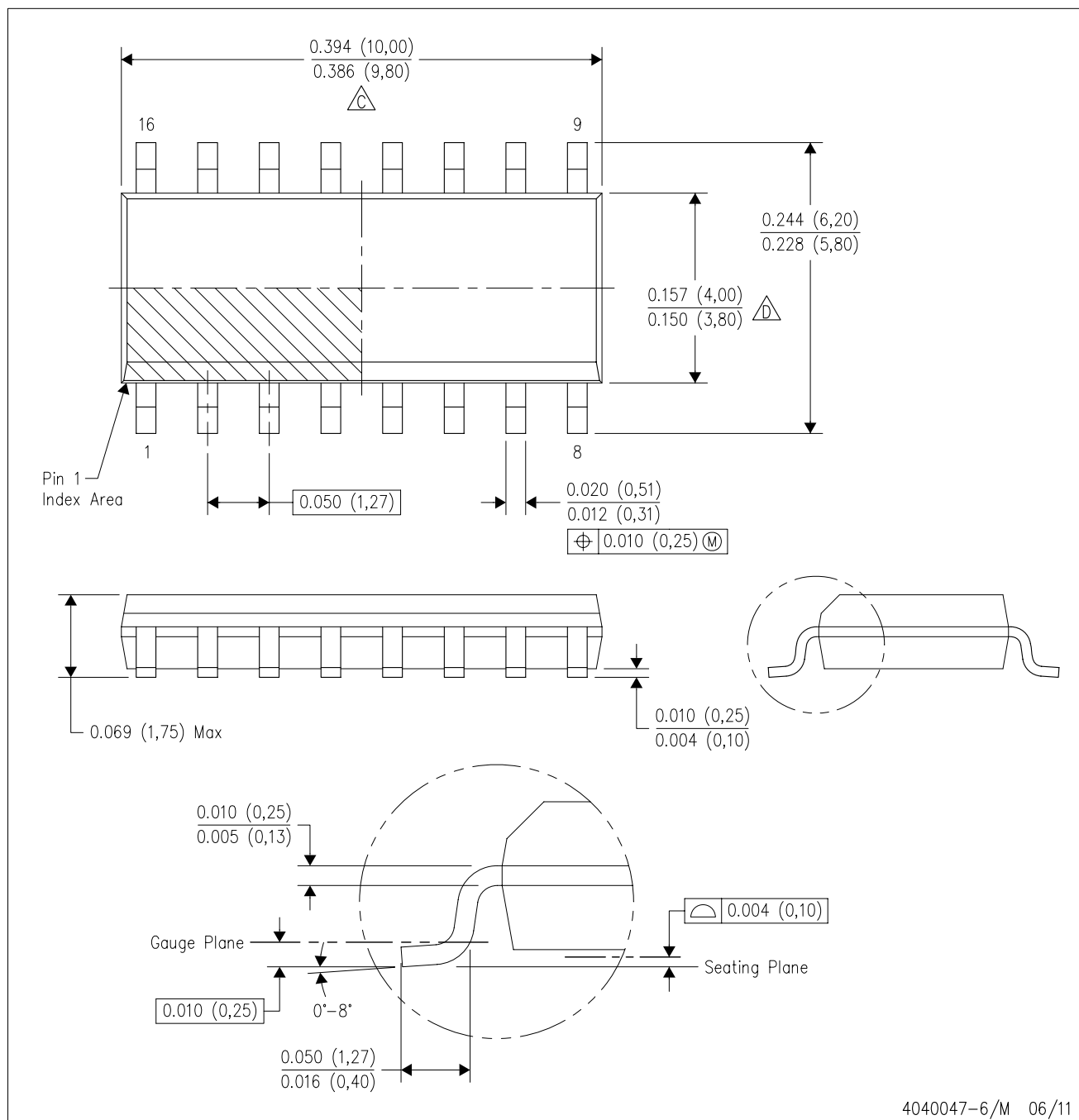
4040049/E 12/2002

NOTES:

- A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
-  Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 The 20 pin end lead shoulder width is a vendor option, either half or full width.

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 -  C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 -  D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AC.

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

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