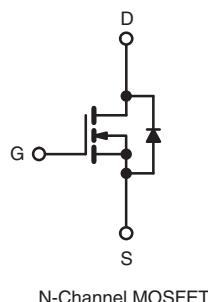
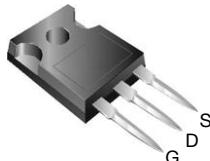


## Power MOSFET

PRODUCT SUMMARY	
V <sub>DS</sub> (V)	500
R <sub>DS(on)</sub> (Ω)	V <sub>GS</sub> = 10 V 0.135
Q <sub>g</sub> (Max.) (nC)	190
Q <sub>gs</sub> (nC)	59
Q <sub>gd</sub> (nC)	84
Configuration	Single

TO-247AC



N-Channel MOSFET

### FEATURES

- Low Gate Charge Q<sub>g</sub> Results in Simple Drive Requirement
- Improved Gate, Avalanche and Dynamic dV/dt Ruggedness
- Fully Characterized Capacitance and Avalanche Voltage and Current
- Low R<sub>DS(on)</sub>
- Compliant to RoHS Directive 2002/95/EC


**RoHS\***  
COMPLIANT

### APPLICATIONS

- Switch Mode Power Supply (SMPS)
- Uninterruptible Power Supply
- High Speed Power Switching
- Hard Switching and High Frequency Circuits

### ORDERING INFORMATION

Package	TO-247AC
Lead (Pb)-free	IRFP32N50KPbF SiHFP32N50K-E3
SnPb	IRFP32N50K SiHFP32N50K

### ABSOLUTE MAXIMUM RATINGS (T<sub>C</sub> = 25 °C, unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-Source Voltage	V <sub>DS</sub>	500	
Gate-Source Voltage	V <sub>GS</sub>	± 30	V
Continuous Drain Current	V <sub>GS</sub> at 10 V	T <sub>C</sub> = 25 °C	I <sub>D</sub>
		T <sub>C</sub> = 100 °C	
Pulsed Drain Current <sup>a</sup>	I <sub>DM</sub>	130	A
Linear Derating Factor		3.7	W/°C
Single Pulse Avalanche Energy <sup>b</sup>	E <sub>AS</sub>	450	mJ
Repetitive Avalanche Current <sup>a</sup>	I <sub>AR</sub>	32	A
Repetitive Avalanche Energy <sup>a</sup>	E <sub>AR</sub>	46	mJ
Maximum Power Dissipation	P <sub>D</sub>	460	W
Peak Diode Recovery dV/dt <sup>c</sup>	dV/dt	13	V/ns
Operating Junction and Storage Temperature Range	T <sub>J</sub> , T <sub>stg</sub>	- 55 to + 150	°C
Soldering Recommendations (Peak Temperature)	for 10 s	300 <sup>d</sup>	
Mounting Torque	6-32 or M3 screw	10	lbf · in
		1.1	N · m

#### Notes

- Repetitive rating; pulse width limited by maximum junction temperature.
- Starting T<sub>J</sub> = 25 °C, L = 0.87 mH, R<sub>g</sub> = 25 Ω, I<sub>AS</sub> = 32 A.
- I<sub>SD</sub> ≤ 32 A, dI/dt ≤ 197 A/μs, V<sub>DD</sub> ≤ V<sub>DS</sub>, T<sub>J</sub> ≤ 150 °C.
- 1.6 mm from case.

\* Pb containing terminations are not RoHS compliant, exemptions may apply

## THERMAL RESISTANCE RATINGS

PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient	$R_{thJA}$	-	40	°C/W
Case-to-Sink, Flat, Greased Surface	$R_{thCS}$	0.24	-	
Maximum Junction-to-Case (Drain)	$R_{thJC}$	-	0.26	

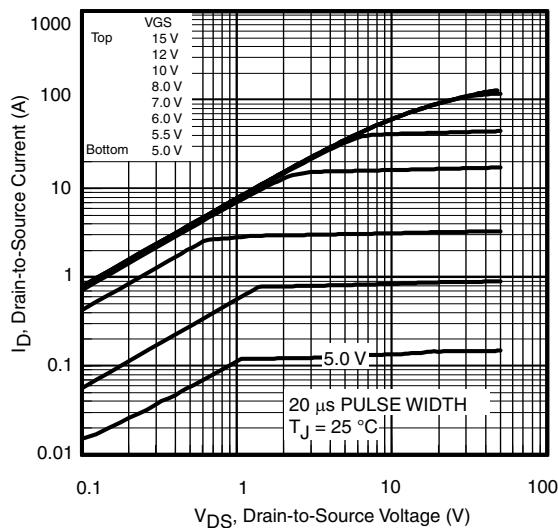
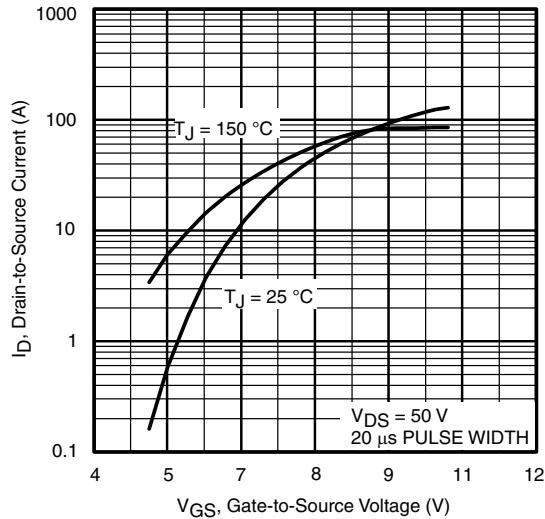
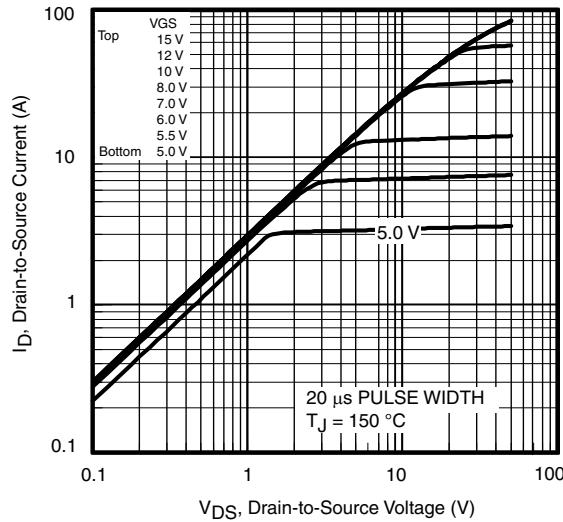
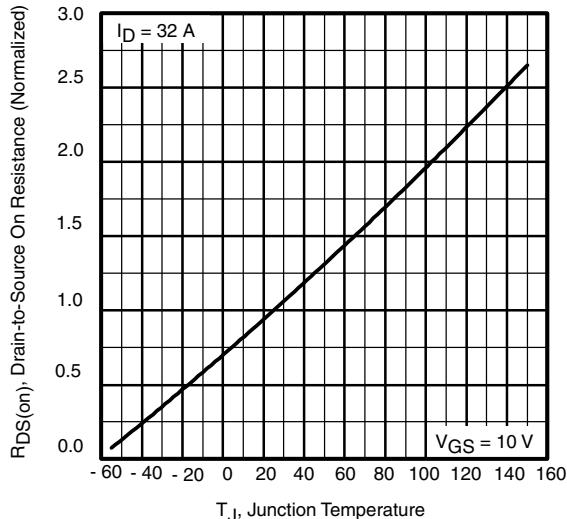
SPECIFICATIONS ( $T_J = 25$  °C, unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
<b>Static</b>							
Drain-Source Breakdown Voltage	$V_{DS}$	$V_{GS} = 0$ V, $I_D = 250$ μA		500	-	-	V
$V_{DS}$ Temperature Coefficient	$\Delta V_{DS}/T_J$	Reference to 25 °C, $I_D = 1$ mA		-	0.54	-	V/°C
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$ , $I_D = 250$ μA		3.0	-	5.0	V
Gate-Source Leakage	$I_{GSS}$	$V_{GS} = \pm 30$ V		-	-	$\pm 100$	nA
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 500$ V, $V_{GS} = 0$ V		-	-	50	μA
		$V_{DS} = 400$ V, $V_{GS} = 0$ V, $T_J = 150$ °C		-	-	250	
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS} = 10$ V	$I_D = 32$ A <sup>b</sup>	-	0.135	0.16	Ω
Forward Transconductance	$g_{fs}$	$V_{DS} = 50$ V, $I_D = 32$ A		14	-	-	S
<b>Dynamic</b>							
Input Capacitance	$C_{iss}$	$V_{GS} = 0$ V, $V_{DS} = 25$ V, $f = 1.0$ MHz, see fig. 5		-	5280	-	pF
Output Capacitance	$C_{oss}$			-	550	-	
Reverse Transfer Capacitance	$C_{rss}$			-	45	-	
Output Capacitance	$C_{oss}$	$V_{GS} = 0$ V	$V_{DS} = 1.0$ V, $f = 1.0$ MHz	-	5630	-	
			$V_{DS} = 400$ V, $f = 1.0$ MHz	-	155	-	
			$V_{DS} = 0$ V to 400 V <sup>c</sup>	-	265	-	
Total Gate Charge	$Q_g$	$V_{GS} = 10$ V	$I_D = 32$ A, $V_{DS} = 400$ V <sup>b</sup>	-	-	190	nC
Gate-Source Charge	$Q_{gs}$			-	-	59	
Gate-Drain Charge	$Q_{gd}$			-	-	84	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 250$ V, $I_D = 32$ A, $R_g = 4.3$ Ω, $V_{GS} = 10$ V <sup>b</sup>		-	28	-	ns
Rise Time	$t_r$		-	120	-		
Turn-Off Delay Time	$t_{d(off)}$		-	48	-		
Fall Time	$t_f$		-	54	-		
<b>Drain-Source Body Diode Characteristics</b>							
Continuous Source-Drain Diode Current	$I_S$	MOSFET symbol showing the integral reverse p - n junction diode		-	-	32	A
Pulsed Diode Forward Current <sup>a</sup>	$I_{SM}$			-	-	130	
Body Diode Voltage	$V_{SD}$	$T_J = 25$ °C, $I_S = 32$ A, $V_{GS} = 0$ V <sup>b</sup>		-	-	1.5	V
Body Diode Reverse Recovery Time	$t_{rr}$	$T_J = 25$ °C, $I_F = 32$ A, $dl/dt = 100$ A/μs <sup>b</sup>		-	530	800	ns
Body Diode Reverse Recovery Charge	$Q_{rr}$		-	9.0	13.5	μC	
Body Diode Reverse Recovery Current	$I_{RRM}$		-	30	-	A	
Forward Turn-On Time	$t_{on}$	Intrinsic turn-on time is negligible (turn-on is dominated by $L_S$ and $L_D$ )					

## Notes

a. Repetitive rating; pulse width limited by maximum junction temperature.

b. Pulse width  $\leq 400$  μs; duty cycle  $\leq 2$  %.c.  $C_{oss}$  eff. is a fixed capacitance that gives the same charging time as  $C_{oss}$  while  $V_{DS}$  is rising from 0 % to 80 %  $V_{DS}$ .

**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)

**Fig. 1 - Typical Output Characteristics**

**Fig. 3 - Typical Transfer Characteristics**

**Fig. 2 - Typical Output Characteristics**

**Fig. 4 - Normalized On-Resistance vs. Temperature**

# IRFP32N50K, SiHFP32N50K

Vishay Siliconix

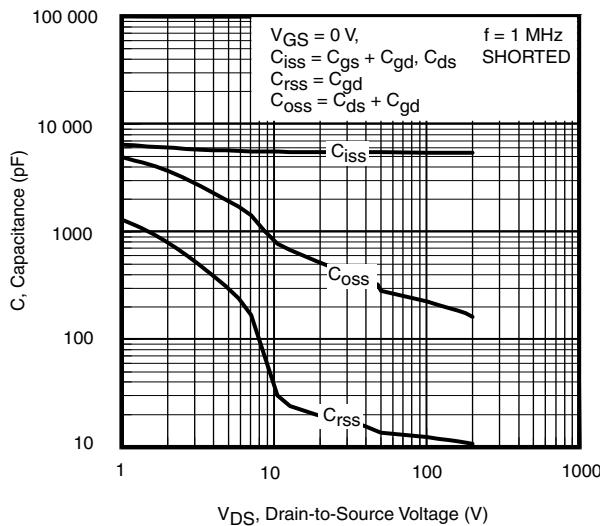


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

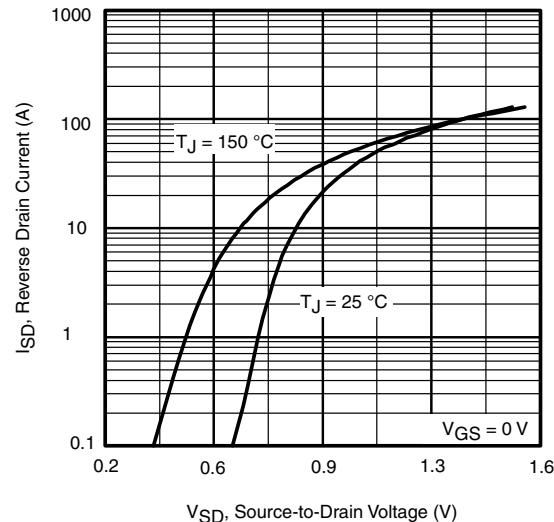


Fig. 7 - Typical Source-Drain Diode Forward Voltage

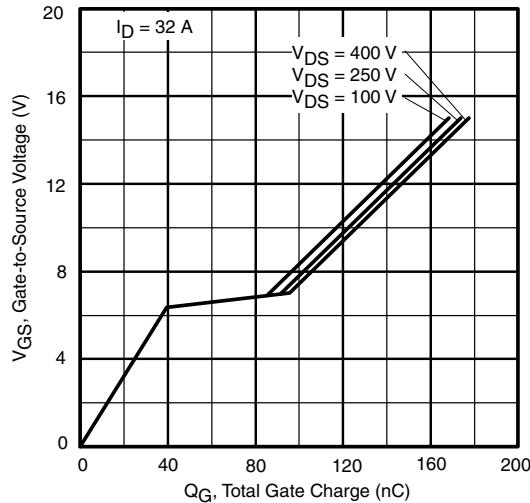


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

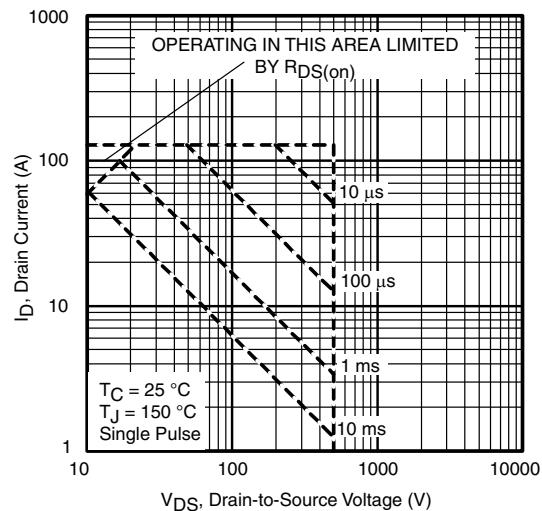
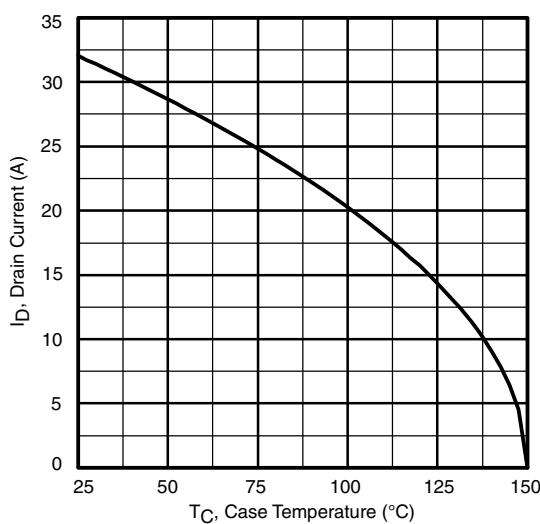
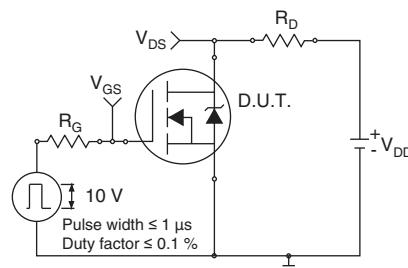


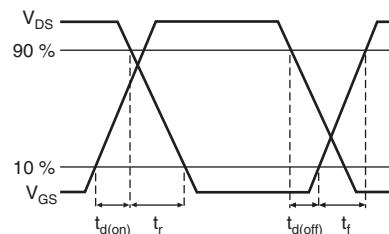
Fig. 8 - Maximum Safe Operating Area



**Fig. 9 - Maximum Drain Current vs. Case Temperature**



**Fig. 10a - Switching Time Test Circuit**



**Fig. 10b - Switching Time Waveforms**

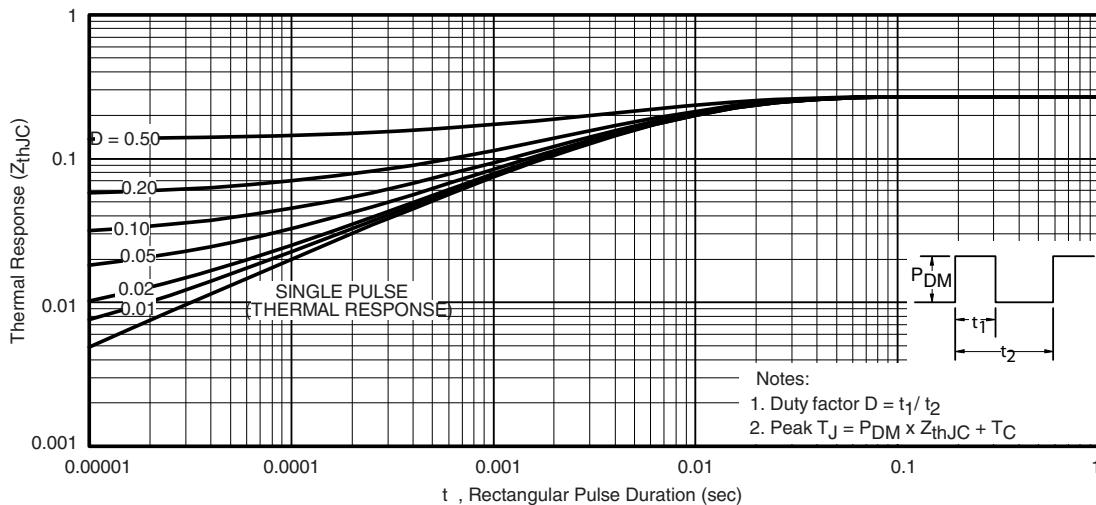


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

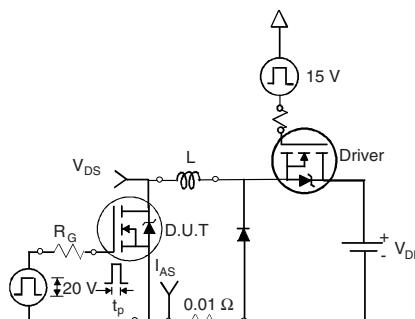


Fig. 12a - Unclamped Inductive Test Circuit

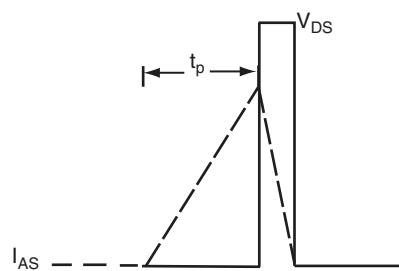


Fig. 12b - Unclamped Inductive Waveforms

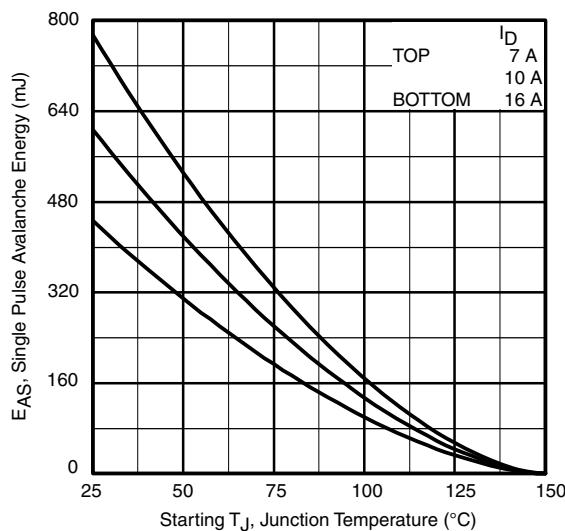


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

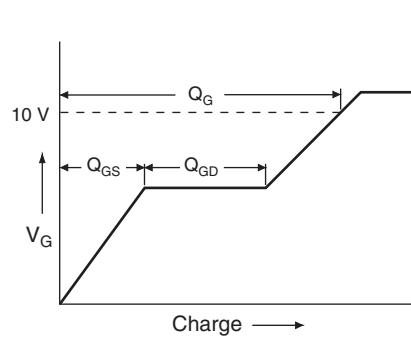


Fig. 13a - Basic Gate Charge Waveform

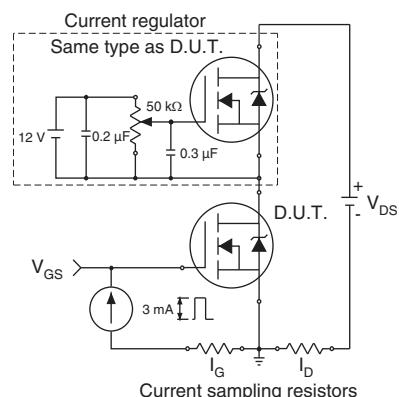
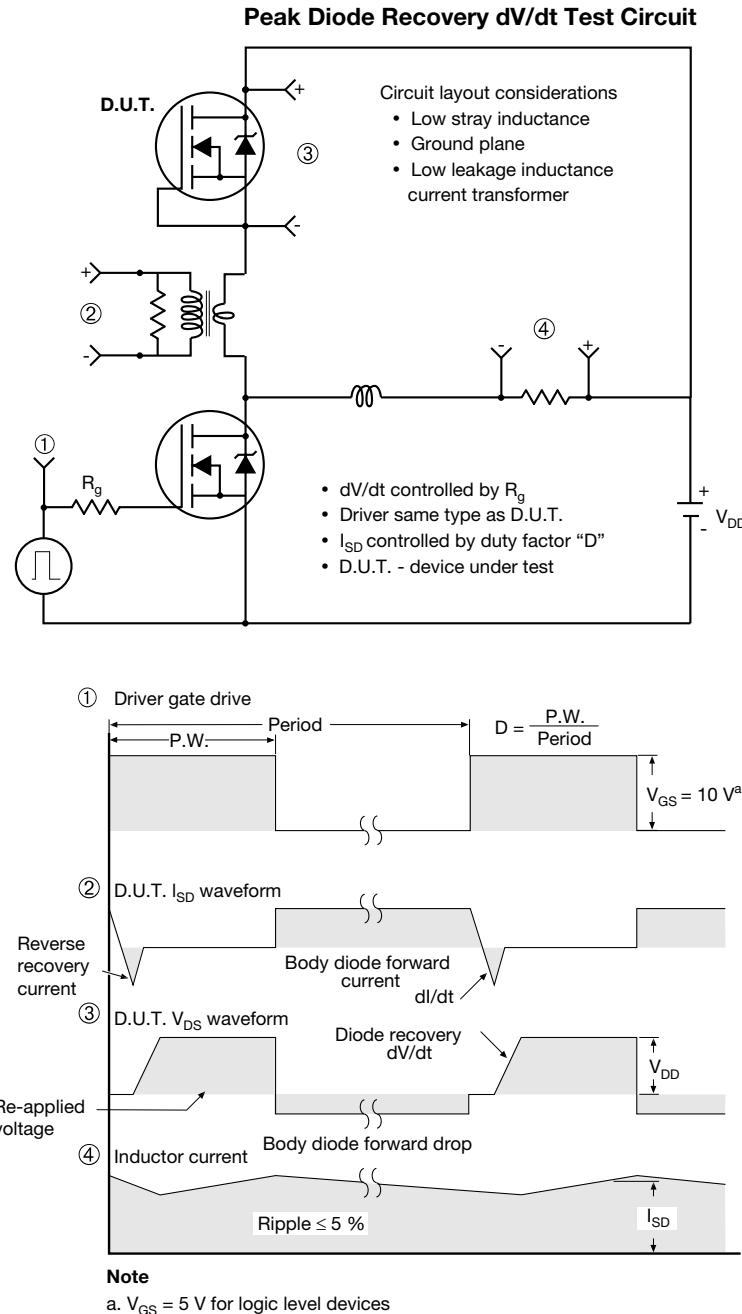


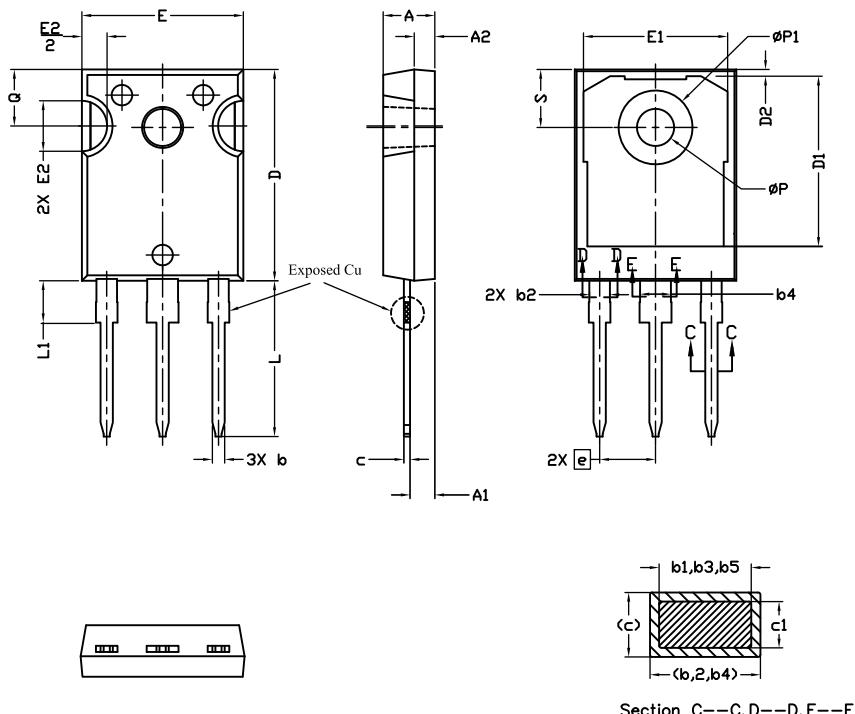
Fig. 13b - Gate Charge Test Circuit


**Fig. 14 - For N-Channel**

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## TO-247AC (High Voltage)

### VERSION 1: FACILITY CODE = 9



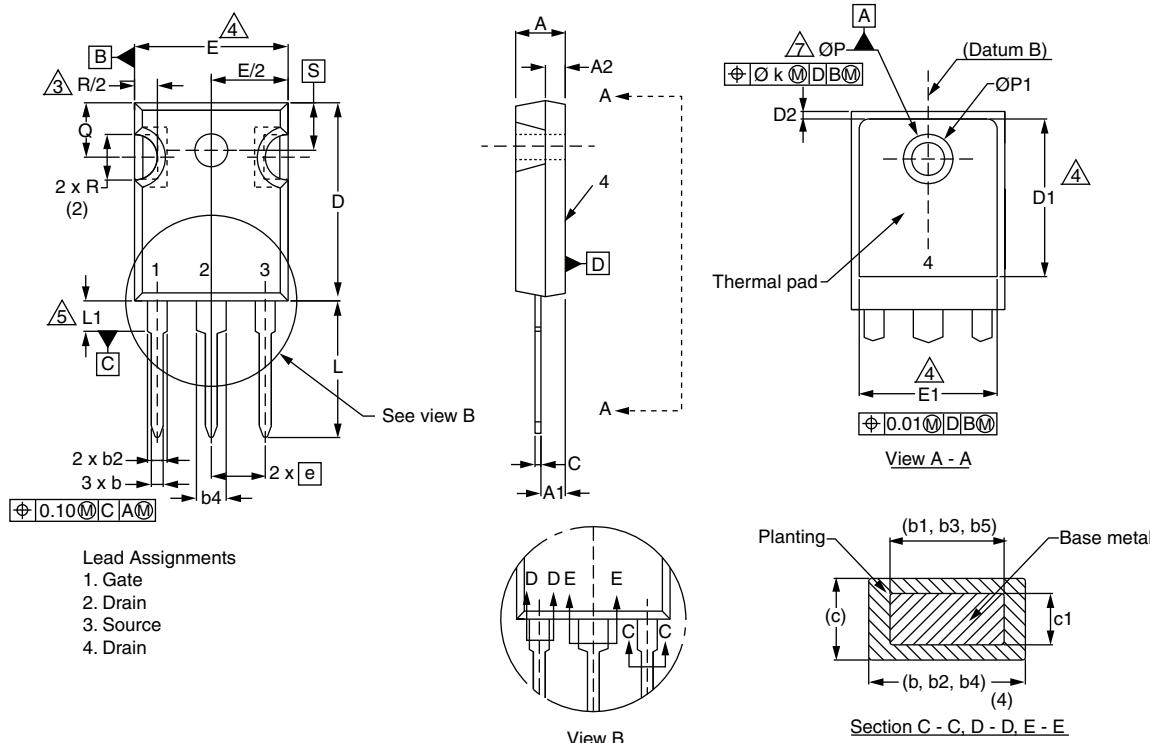
MILLIMETERS			
DIM.	MIN.	MAX.	NOTES
A	4.83	5.21	
A1	2.29	2.55	
A2	1.50	2.49	
b	1.12	1.33	
b1	1.12	1.28	
b2	1.91	2.39	6
b3	1.91	2.34	
b4	2.87	3.22	6, 8
b5	2.87	3.18	
c	0.55	0.69	6
c1	0.55	0.65	
D	20.40	20.70	4

#### Notes

- (1) Package reference: JEDEC® TO247, variation AC
- (2) All dimensions are in mm
- (3) Slot required, notch may be rounded
- (4) Dimension D and E do not include mold flash. Mold flash shall not exceed 0.127 mm per side. These dimensions are measured at the outermost extremes of the plastic body
- (5) Thermal pad contour optional with dimensions D1 and E1
- (6) Lead finish uncontrolled in L1
- (7) Ø P to have a maximum draft angle of 1.5° to the top of the part with a maximum hole diameter of 3.91 mm
- (8) Dimension b2 and b4 does not include dambar protrusion. Allowable dambar protrusion shall be 0.1 mm total in excess of b2 and b4 dimension at maximum material condition

MILLIMETERS			
DIM.	MIN.	MAX.	NOTES
D1	16.25	16.85	5
D2	0.56	0.76	
E	15.50	15.87	4
E1	13.46	14.16	5
E2	4.52	5.49	3
e	5.44 BSC		
L	14.90	15.40	
L1	3.96	4.16	6
Ø P	3.56	3.65	7
Ø P1	7.19 ref.		
Q	5.31	5.69	
S	5.54	5.74	

### VERSION 2: FACILITY CODE = Y



MILLIMETERS			
DIM.	MIN.	MAX.	NOTES
A	4.58	5.31	
A1	2.21	2.59	
A2	1.17	2.49	
b	0.99	1.40	
b1	0.99	1.35	
b2	1.53	2.39	
b3	1.65	2.37	
b4	2.42	3.43	
b5	2.59	3.38	
c	0.38	0.86	
c1	0.38	0.76	
D	19.71	20.82	
D1	13.08	-	

ECN: E19-0614-Rev. E, 08-Jan-2020

DWG: 5971

DIM.	MIN.	MAX.	NOTES
D2	0.51	1.30	
E	15.29	15.87	
E1	13.72	-	
e	5.46 BSC		
Ø k	0.254		
L	14.20	16.25	
L1	3.71	4.29	
Ø P	3.51	3.66	
Ø P1	-	7.39	
Q	5.31	5.69	
R	4.52	5.49	
S	5.51 BSC		

#### Notes

- (1) Dimensioning and tolerancing per ASME Y14.5M-1994
- (2) Contour of slot optional
- (3) Dimension D and E do not include mold flash. Mold flash shall not exceed 0.127 mm (0.005") per side. These dimensions are measured at the outermost extremes of the plastic body
- (4) Thermal pad contour optional with dimensions D1 and E1
- (5) Lead finish uncontrolled in L1
- (6) Ø P to have a maximum draft angle of 1.5 to the top of the part with a maximum hole diameter of 3.91 mm (0.154")
- (7) Outline conforms to JEDEC outline TO-247 with exception of dimension c

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