

## Quad Low-side Driver

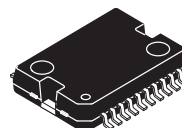
The MC33385 is a Quad Low-side Driver fully protected switch. This device is a general purpose Low-side Driver but has been especially designed to operate in engine management applications as injector driver or automotive gear box. It is interfaced directly with a microcontroller for parallel control of the load and the individual output diagnostic is done through a SPI. The diagnostic logic recognizes 4 failure types at each output stage: overcurrent, short to GND, open load, and over-temperature.

### Features

- RDSON of 250mΩ per Output at 25°C
- Supplied from the main 5V V<sub>CC</sub>
- Input CMOS Compatible
- Diagnostic through SPI
- Nominal Current of 2A per Output
- Current Limitation at 3A with Automatic Turn Off
- Output Internally Clamped at 50V typ for Inductive Load Drive
- Junction to Case Thermal Resistance of 4.4°C/W
- Individual Output over Temperature Shutdown
- Pb-Free Packaging Designated by Suffix Code VW

**33385**

**LOW-SIDE DRIVER**



**DH SUFFIX  
VW SUFFIX (PB-FREE)  
98ASH70702A  
20-PIN HSOP**

### ORDERING INFORMATION

Device	Temperature Range (T <sub>A</sub> )	Package
MC33385DH/R2	-40°C to 125°C	20 HSOP
MC33385VW/R2		

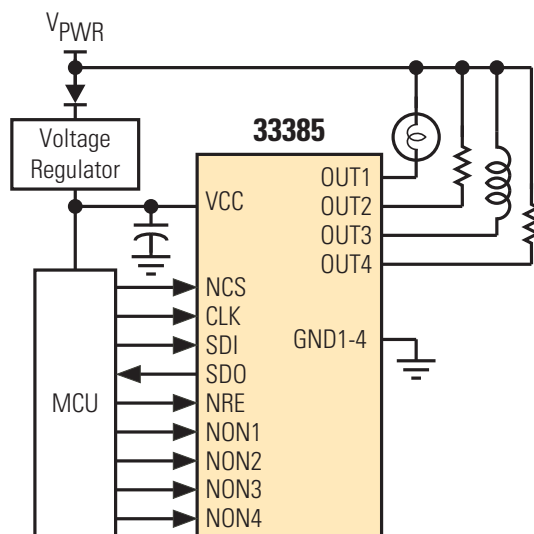


Figure 1. MC33385 Simplified Application Diagram

## BLOCK DIAGRAM

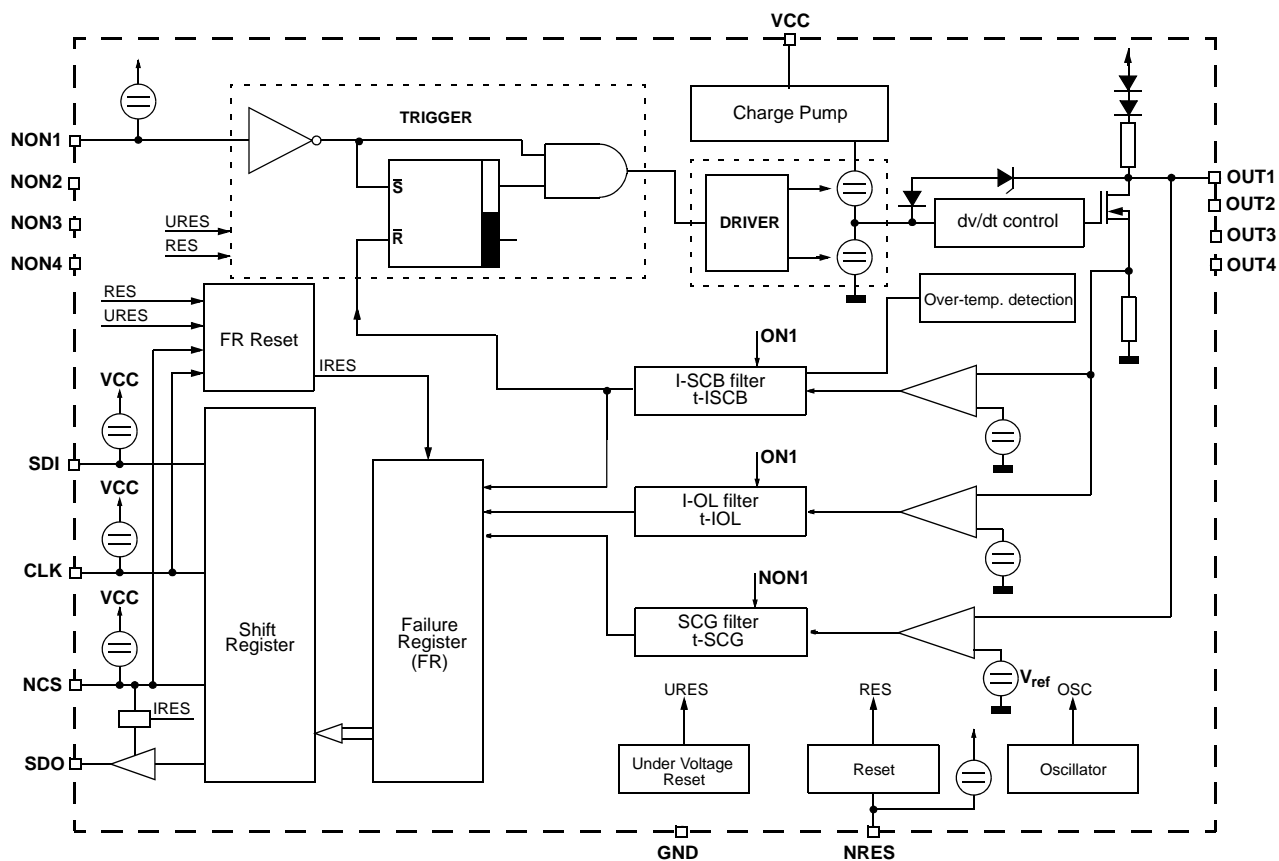


Figure 2. 33385 Simplified Internal Block Diagram

## PIN CONNECTIONS

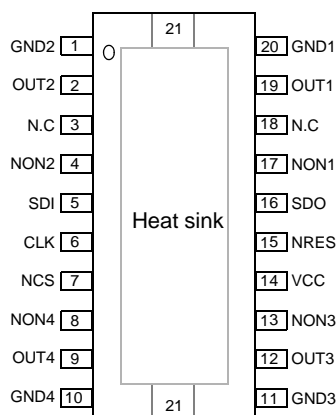


Figure 3. 33385 Pin Connections

Table 1. 33385 Pin Definitions

Pin Number	Pin Name	Definition
1	GND2	Ground 2
2	OUT2	Output Channel 2
3		NC
4	NON2	Input Control Signal for Channel 2
5	SDI	Serial Data Input
6	CLK	Clock Line for Serial Interface
7	NCS	Chip Select for Serial Interface
8	NON4	Input Control Signal for Channel 4
9	OUT4	Output Channel 4
10	GND4	Ground 4
11	GND3	Ground 3
12	OUT3	Output Channel 3
13	NON3	Input Control Signal for Channel 3
14	Vcc	5V Power Supply
15	NRES	Reset Input
16	SDO	Data Output of Serial Interface
17	NON1	Input Control Signal Channel 1
18		NC
19	OUT1	Output Channel 1
20	GND1	Ground 1
	Case	Connected to the PCB Ground for Thermal Purposes

## ELECTRICAL CHARACTERISTICS

## MAXIMUM RATINGS

Table 2. Maximum Ratings

All voltages are with respect to ground unless otherwise noted. Exceeding these ratings may cause a malfunction or permanent damage to the device.

Ratings	Symbol	Value	Unit
<b>ELECTRICAL RATINGS</b>			
Voltage Range	$V_{CC}$	7.0	V
Continuous Output Voltage (With no reverse current)	$V_{OUT}$	45	V
Continuous Current	$I_{OUTC}$	2.5	A
Peak Output Current	$I_{OUTP}$	$I_{SCBMAX}$	A
Clamped Energy at the Switching OFF (See <a href="#">Figure 9</a> )	$W_{OFF}$	70	mJ for 1ms
Input Voltage (Inputs)	$V_{IN}$	$V_{CC} + 0.3$	V
Input Protection Diode Current	$I_{IN}$	1.0	mA
Input Voltage (Outputs)	$V_O$	$V_{CC} + 0.3$	V
Input Protection Diode Current	$I_O$	1.0	mA
<b>THERMAL RATINGS</b>			
Operating Junction Temperature	$T_J$	150	°C
Thermal Resistance : Junction-case (One power stage in use)	$R_{THJC}$	4.5	kΩ
Thermal Resistance : Junction-ambient (Device soldered on printed circuit board)	$R_{THJA}$	50	kΩ
Peak Package Reflow Temperature During Reflow <sup>(1), (2)</sup>	$T_{PPRT}$	<a href="#">Note 2</a>	°C

## Notes

1. Pin soldering temperature limit is for 10 seconds maximum duration. Not designed for immersion soldering. Exceeding these limits may cause malfunction or permanent damage to the device.
2. Freescale's Package Reflow capability meets Pb-free requirements for JEDEC standard J-STD-020C. For Peak Package Reflow Temperature and Moisture Sensitivity Levels (MSL), Go to [www.freescale.com](http://www.freescale.com), search by part number [e.g. remove prefixes/suffixes and enter the core ID to view all orderable parts. (i.e. MC33xxxD enter 33xxx), and review parametrics.

## STATIC CHARACTERISTICS

Table 3. Static Electrical Characteristics

Characteristics noted under conditions  $7.0\text{ V} \leq V_{\text{SUP}} \leq 18\text{ V}$ ,  $-40^{\circ}\text{C} \leq T_{\text{A}} \leq 125^{\circ}\text{C}$ ,  $\text{GND} = 0\text{ V}$  unless otherwise noted. Typical values noted reflect the approximate parameter means at  $T_{\text{A}} = 25^{\circ}\text{C}$  under nominal conditions unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
<b>SUPPLY VOLTAGE</b>					
Supply Voltage Range	$V_{\text{CC}}$	4.5		5.5	V
<b>JUNCTION TEMPERATURE</b>					
Junction Temperature Continuous (Continuous)	$T_{\text{J1}}$	- 40		150	$^{\circ}\text{C}$
Junction Temperature Dynamical (Time limited)	$T_{\text{J2}}$			185	$^{\circ}\text{C}$
<b>OUTPUT CURRENT</b>					
Output Current Range	$I_{\text{OUT}}$			$I_{\text{SCBMAX}}$	A
<b>RESET BEHAVIOUR</b>					
Reset Changeable (at NRES-Pin)	$V_{\text{CC}}$	$V_{\text{CCRES}}$		5.5	V
Undervoltage Reset (Independent of NRES) Active for $V_{\text{CC}} = 0\text{V}$ to $V_{\text{CCPRO}}$	$V_{\text{CCRES}}$	3.35		3.95	V
<b>UNDERVOLTAGE PROTECTION</b>					
Protection active for $V_{\text{CC}} = 0\text{V}$ to $V_{\text{CCPRO}}$	$V_{\text{CCPRO}}$	1.5		4.0	V
<b>OVER TEMPERATURE</b>					
Temperature Detection Threshold	$T_{\text{OFF}}$	155		185	$^{\circ}\text{C}$
<b>SUPPLY CURRENT</b>					
Standby Current (without load) (NON1...NON4 = High Level) $5.15\text{V} \geq V_{\text{CC}}$ $5.5\text{V} \geq V_{\text{CC}}$	$I_{\text{CCSTB1}}$ $I_{\text{CCSTB2}}$			6.0 7.0	mA mA
Operating Mode (For $5.15\text{V} \geq V_{\text{CC}}$ ) ( $I_{\text{OUT}} 1...4$ ) = 2A	$I_{\text{CCOPM}}$			17	mA
$\Delta I_{\text{CC}}$ During Reverse Output Current ( $I_{\text{OUT}} = - 5\text{A}$ on one output)	$\Delta I_{\text{CC}}$			100 50	mA mA
<b>INPUTS (NONx, NCS, CLK, NRES, SDI)</b>					
Low Threshold	$V_{\text{INL}}$	-0.3		$0.2 \cdot V_{\text{CC}}$	V
High Threshold	$V_{\text{INH}}$	$0.7 \cdot V_{\text{CC}}$		$V_{\text{CC}} + 0.3$	V
Hysteresis	$V_{\text{HYST}}$	0.85			V
Input Current ( $V_{\text{IN}} = V_{\text{CC}}$ )	$I_{\text{IN}}$			10	$\mu\text{A}$
Input Current ( $V_{\text{CC}} > V_{\text{RES}}$ & $0\text{V} < V_{\text{IN}} < 0.9 \cdot V_{\text{CC}}$ )	$I_{\text{IN}}$	- 100		- 20	$\mu\text{A}$
<b>SERIAL DATA OUTPUT</b>					
High Output Level ( $I_{\text{SDO}} = -2\text{mA}$ )	$V_{\text{SDOH}}$	$V_{\text{CC}} - 0.4$			V
Low Output Level ( $I_{\text{SDO}} = 3.2\text{mA}$ )	$V_{\text{SDOL}}$			0.4	V
Tristate Leakage Current (NCS = HIGH, $V_{\text{SDO}} = 0\text{V}$ to $V_{\text{CC}}$ )	$I_{\text{SDOL}}$	- 10		10	$\mu\text{A}$
<b>OUTPUTS (OUT 1...4)</b>					
Average Output Current	$I_{\text{OUTA}}$	2.5			A
Output Peak Current	$I_{\text{OUTP}}$	$I_{\text{SCBMAX}}$			A

**Table 3. Static Electrical Characteristics (continued)**

Characteristics noted under conditions  $7.0\text{ V} \leq V_{\text{SUP}} \leq 18\text{ V}$ ,  $-40^{\circ}\text{C} \leq T_{\text{A}} \leq 125^{\circ}\text{C}$ ,  $\text{GND} = 0\text{ V}$  unless otherwise noted. Typical values noted reflect the approximate parameter means at  $T_{\text{A}} = 25^{\circ}\text{C}$  under nominal conditions unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
Leakage Current 1 (NON = High, $V_{\text{OUT}} = 25\text{V}$ , $V_{\text{CC}} = 5\text{V}$ )	$I_{\text{OUTL}}$			10	$\mu\text{A}$
Leakage Current 2 (NON = High, $V_{\text{OUT}} = 16\text{V}$ , $V_{\text{CC}} = 1\text{V}$ )	$I_{\text{OUTL2}}$			10	$\mu\text{A}$
Output Clamp Voltage ( $I_{\text{OUT}} = 1\text{A}$ )	$V_{\text{CLP}}$	45	50	58	V
Matching Clamp Voltage (Between two outputs)	$V_{\text{CLPM}}$	$V_{\text{CLP-1}}$		$V_{\text{CLP+1}}$	V
Clamped Energy at the Switching OFF (See <a href="#">Figure 9</a> )	$W_{\text{OFF}}$	50			mJ for 1ms
On Resistance ( $I_{\text{OUT}} = 2\text{A}$ , $T_{\text{J}} = 150^{\circ}\text{C}$ , NON = LOW)	$R_{\text{DS(on)}}$			500	$\text{m}\Omega$
Output Low Voltage Limitation ( $I_{\text{OUT}} = 150\text{mA}$ )	$V_{\text{OUTLIM}}$	65		220	mV
Output Capacitance (Guaranteed by design)	$C_{\text{OUT}}$			350	pF

**OUTPUTS REVERSE DIODE**

Reverse Output Current	$I_{\text{RD}}$	2.5			A
Reverse Peak current <sup>(1)</sup>	$I_{\text{RDP}}$	5.0			A
Reverse Voltage Drop					
- $I_{\text{OUT}} = -5\text{A}$	$V_{\text{RD1}}$	1.0		1.7	V
- $I_{\text{OUT}} = -2.5\text{A}$	$V_{\text{RD2}}$	0.85		1.7	V

**POWERSTAGE PROTECTION**

Short Current Limit	$I_{\text{SCB}}$	3.0		5	A
$V_{\text{CC}}$ Undervoltage	$V_{\text{CCMIN}}$	3.35		3.95	V

**DIAGNOSTIC**

Short to GND Threshold Voltage for $I_{\text{OUT}} \leq 2\text{A}$	$V_{\text{REF}}$	$0.390 \times V_{\text{CC}}$		$0.435 \times V_{\text{CC}}$	V
Open Load Threshold Current	$I_{\text{OL}}$	10		50	mA
Pull-up Resistor	$R_{\text{OL}}$	2.0		8.0	$\text{k}\Omega$
Temperature Detection Threshold	$T_{\text{OFF}}$	155		185	$^{\circ}\text{C}$

## Notes

- For  $t \leq 2\text{ms}$ . Max. reverse current is limited to - 10A (for all outputs together)

## DYNAMIC CHARACTERISTIC

Table 4. Dynamic Electrical Characteristics

Characteristics noted under conditions  $7.0\text{ V} \leq V_{\text{SUP}} \leq 18\text{ V}$ ,  $-40^{\circ}\text{C} \leq T_{\text{A}} \leq 125^{\circ}\text{C}$ ,  $\text{GND} = 0\text{ V}$  unless otherwise noted. Typical values noted reflect the approximate parameter means at  $T_{\text{A}} = 25^{\circ}\text{C}$  under nominal conditions unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
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## INPUTS

Input Frequency (NON1 to NON4)	$f_{\text{IN}}$	0.0		1000	Hz
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## OUTPUTS TIMING

Positive Output Voltage Ramp (with inductive load) $V_{\text{OUT}} = 4\text{V} \dots 16\text{V}$ $V_{\text{OUT}} = 16\text{V} \dots V_{\text{clp}}$	$\text{OVR}_{\text{P1}}$ $\text{OVR}_{\text{P2}}$	2.0 3.5	3.0 6.0	5.0 10	$\text{V}/\mu\text{s}$ $\text{V}/\mu\text{s}$
Negative Output Voltage Ramp (25%... 75%)	$\text{OVR}_{\text{N}}$	1.75	3.0	4.0	$\text{V}/\mu\text{s}$
Internal Switch-on-Time Charge Pump (NON = LOW... $V_{\text{GATE}} = 0.9 * V_{\text{BAT}}$ )	$t_{\text{DCP}}$			40	$\mu\text{s}$
Turn ON Delay (NON = 50%, $V_{\text{OUT}} = 0.9 * V_{\text{BAT}}$ )	$t_{\text{DON}}$	1.0	2.5	5.0	$\mu\text{s}$
Turn OFF Delay (NON = 50%, $V_{\text{OUT}} = 0.1 * V_{\text{BAT}}$ ) (NON = 50%, $V_{\text{OUT}} = 4\text{V}$ )	$t_{\text{DOFFA}}$ $t_{\text{DOFFB}}$		1.0 4.7	3.0 7.5	$\mu\text{s}$ $\mu\text{s}$
Undervoltage Protection Max ON time after a output voltage ramp from 0V to 25V at $V_{\text{CC}} = 0\text{V} \dots V_{\text{CCPRO}}$	$t_{\text{RPON}}$			100	$\mu\text{s}$
Matching Turn ON Delay (NON = 50%, $V_{\text{OUT}} = 0.9 * V_{\text{BAT}}$ )	$t_{\text{MON}}$	- 3.0		3.0	$\mu\text{s}$
Rise time Turn OFF (10% - 90% of $V_{\text{CLP}}$ )	$t_{\text{ROFF}}$		8.5	12	$\mu\text{s}$

## DIAGNOSTIC

Short to GND Filter Time	$T_{\text{SCG}}$	140		250	$\mu\text{s}$
Open Load Filter Time	$t_{\text{OL}}$	140		250	$\mu\text{s}$

## SERIAL DIAGNOSTIC LINK : LOAD CAPACITOR AT SDI AND SDO = 100PF

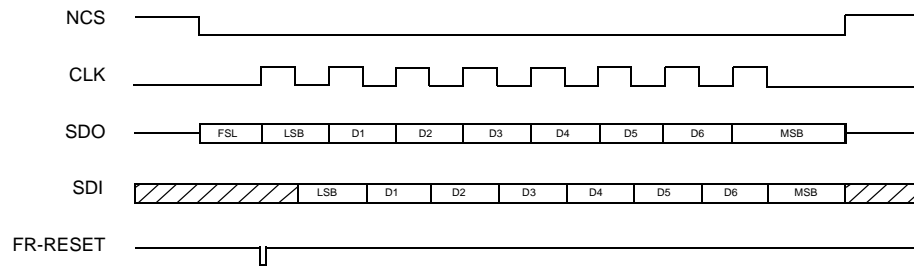
Clock Frequency (50% duty cycle)	$f_{\text{CLK}}$	3.0			MHz
Minimum Time CLK = HIGH	$t_{\text{CLH}}$	100			ns
Minimum Time CLK = LOW	$t_{\text{CLL}}$	100			ns
Propagation Delay (CLF Data at SDO valid)	$t_{\text{PCLD}}$			100	ns
NCS = LOW to Data at SDO Valid	$t_{\text{PCLD}}$			100	ns
CLK Low Before NCS Low (Setup time CLK to NCS change High/Low)	$t_{\text{SCLCH}}$	100			ns
CLK Change Low/High after NCS = Low	$t_{\text{HCLCL}}$	100			ns
SDI Input Set up Time (CLK change High/Low after SDI data valid)	$t_{\text{SCLD}}$	20			ns
SDI Input Hold Time (SDI data hold after CLK change High/Low)	$t_{\text{HCLD}}$			20	ns
CLK Low Before NCS High	$t_{\text{SCLCL}}$	150			ns

**Table 4. Dynamic Electrical Characteristics (continued)**

Characteristics noted under conditions  $7.0\text{ V} \leq V_{\text{SUP}} \leq 18\text{ V}$ ,  $-40^{\circ}\text{C} \leq T_{\text{A}} \leq 125^{\circ}\text{C}$ ,  $\text{GND} = 0\text{ V}$  unless otherwise noted. Typical values noted reflect the approximate parameter means at  $T_{\text{A}} = 25^{\circ}\text{C}$  under nominal conditions unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
CLK High After NCS High	$t_{\text{HCLCH}}$	150			ns
NCSLow/High to Output Data Flout	$t_{\text{PCHDZ}}$			100	ns
Capacitance at SDI, SDO, CLK, CS	$t_{\text{PCLD}}$			10	pF
NCS Filter time (Pulses $\leq t_{\text{FNCS}}$ will be ignored)	$t_{\text{FNCS}}$	10		40	ns

## TIMING DIAGRAMS



NOTE : FR -RESET means Reset failure storage (internal signal)

Figure 4. Timing Diagram to Read the Diagnostic Register

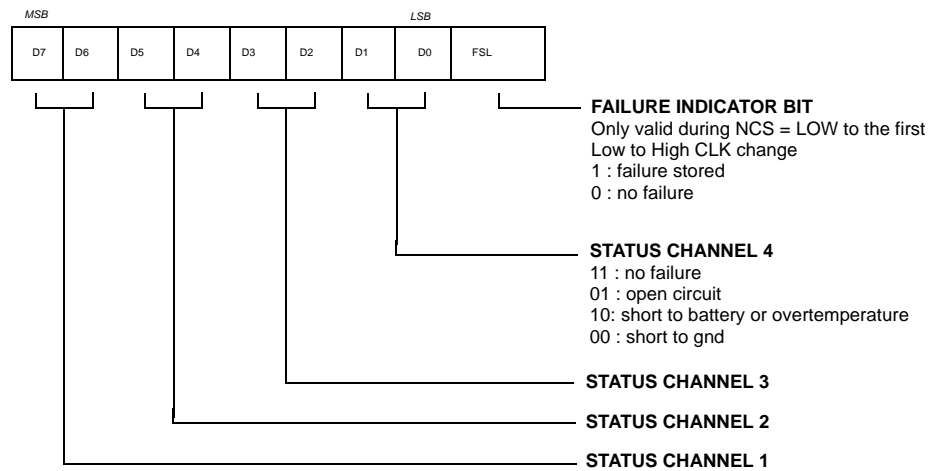


Figure 5. Diagnostic Failure Register Structure

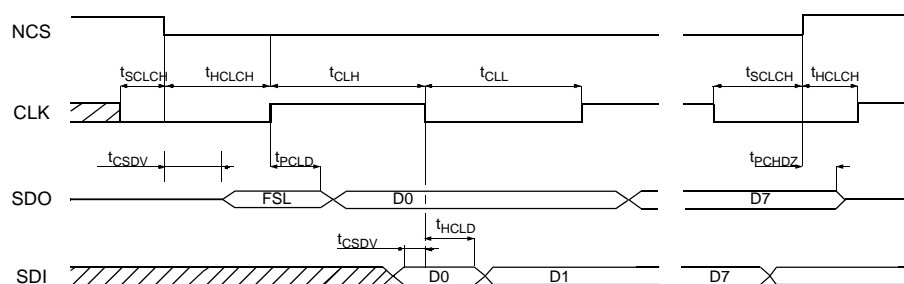
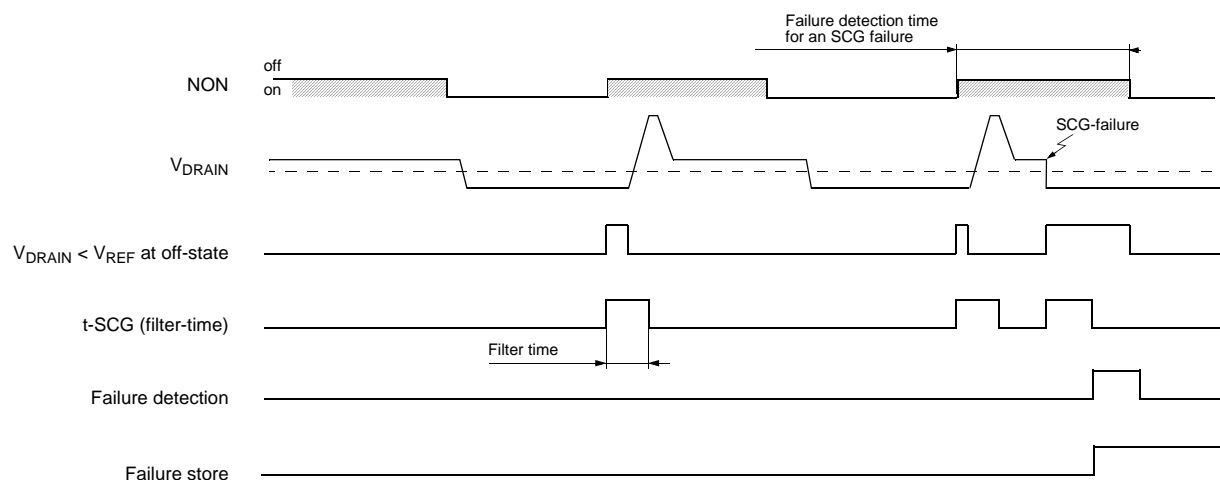
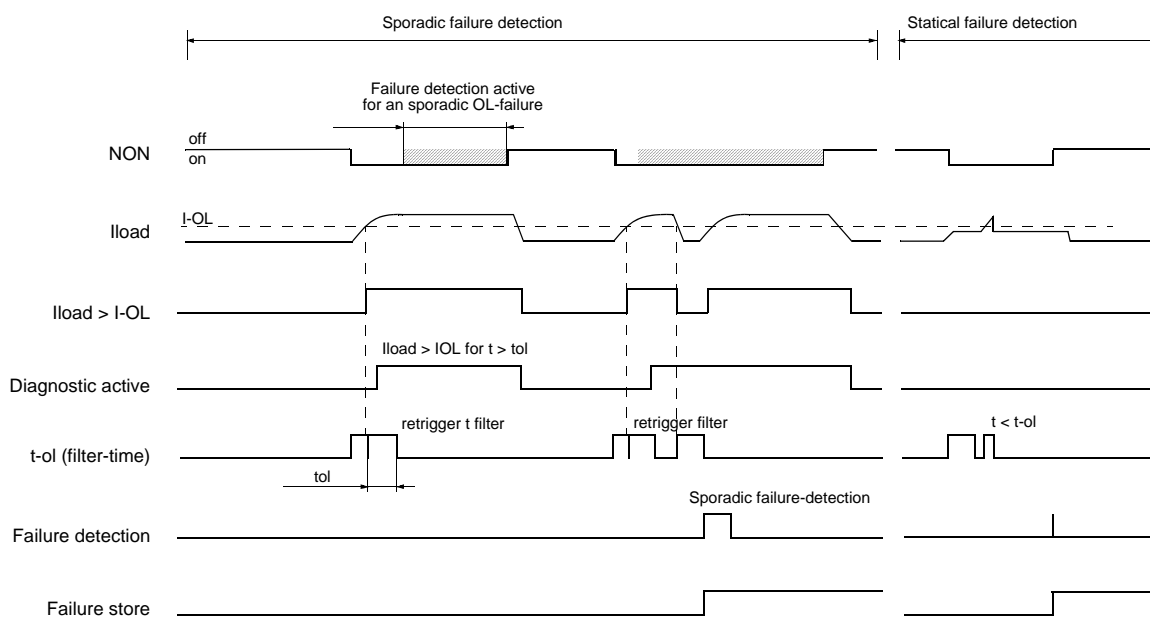


Figure 6. Serial Interface Timing



**Figure 7. Diagram to Short-Circuit to GND Failure (SCG-Failure) Detection**



**Figure 8. Diagram to Open Load Failure (OL-Failure) Detection**

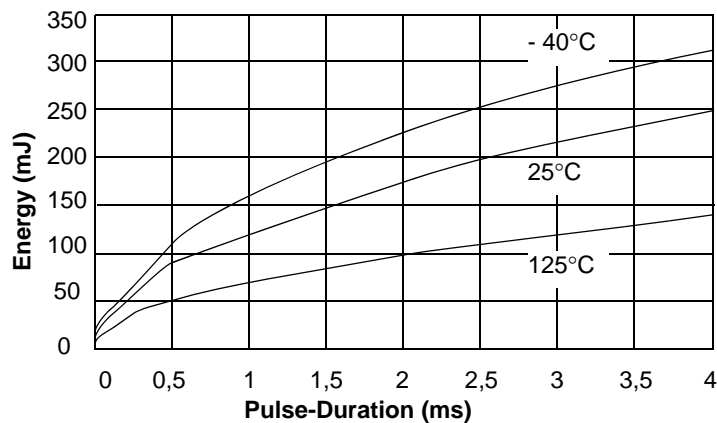


Figure 9. Max Clamp- Energy Specification

ELECTRICAL PERFORMANCE CURVES

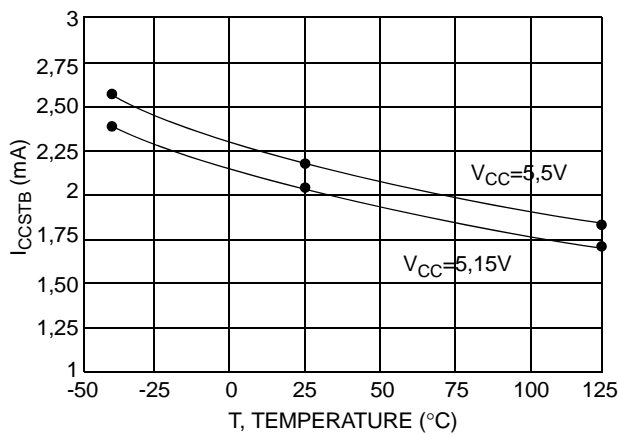


Figure 10. Standby Current versus Temperature

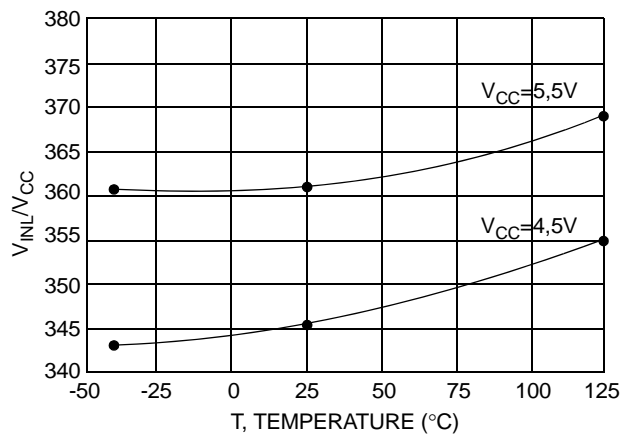


Figure 12. Low Threshold Input Voltage versus Temperature

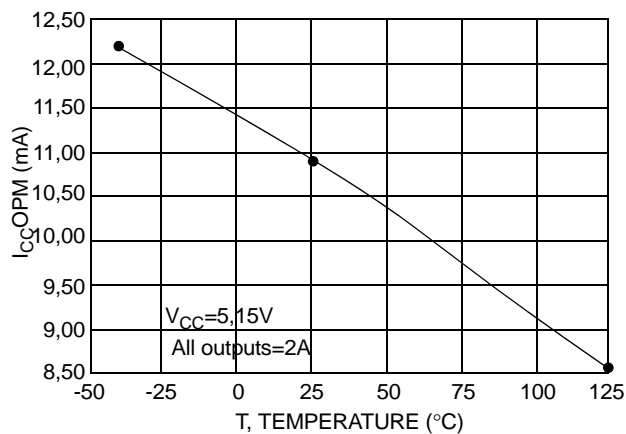


Figure 11. Operating Mode Current versus Temperature

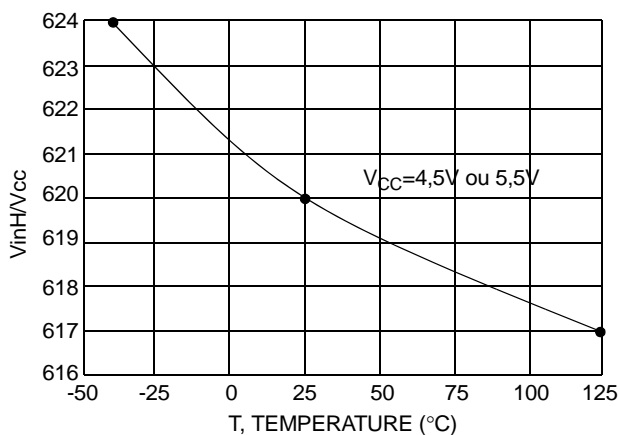


Figure 13. High Threshold Input Voltage versus Temperature

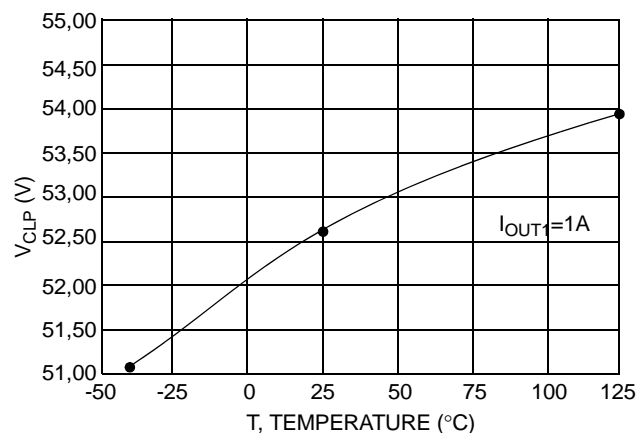


Figure 14. Output Clamp Voltage versus Temperature

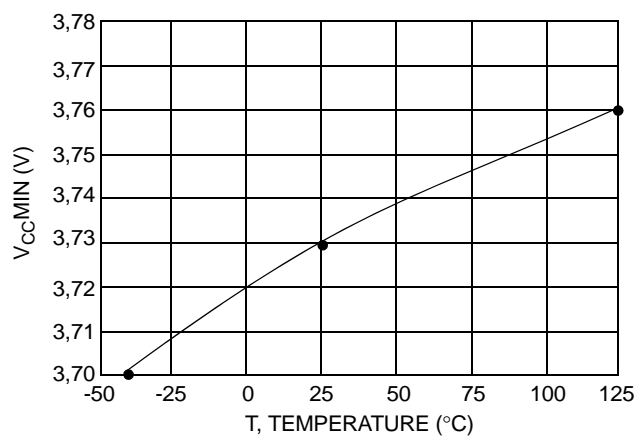


Figure 17. Vcc Undervoltage versus Temperature

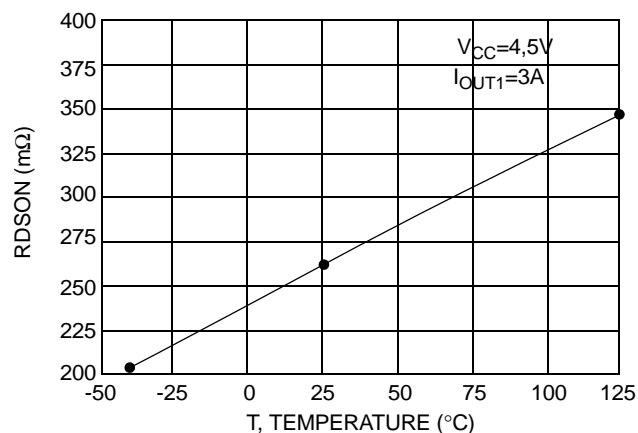


Figure 15. Rds on versus Temperature

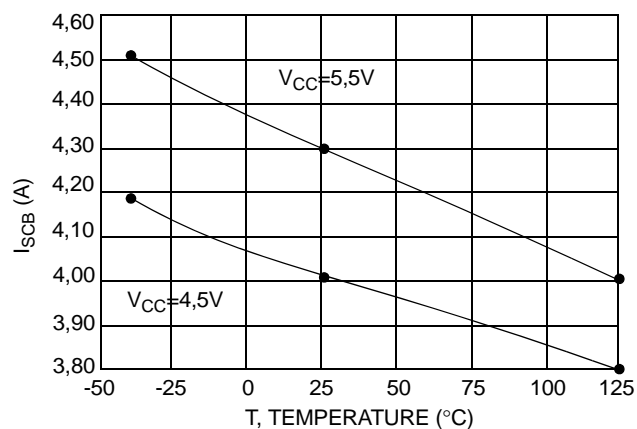


Figure 18. Short Current Limit versus Temperature

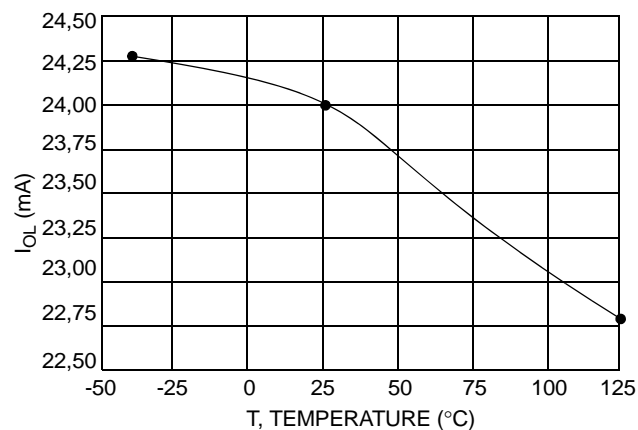


Figure 16. Open Load versus Temperature

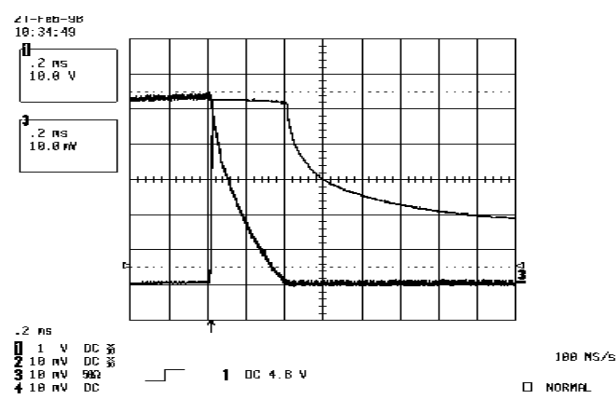


Figure 19. Inductive Switching

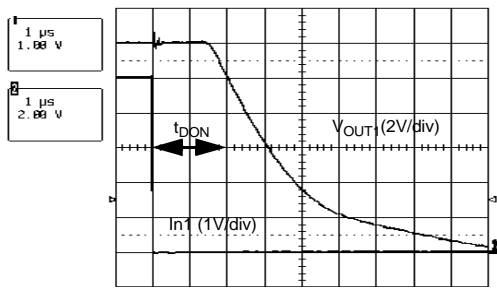


Figure 20. Turn on Delay

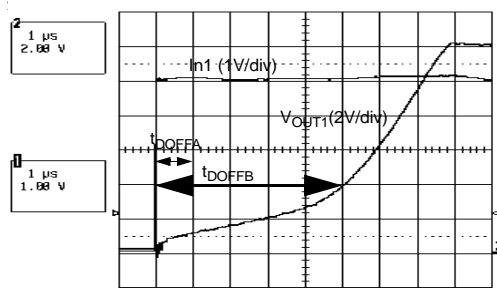


Figure 21. Turn off Delay

## FUNCTIONAL DESCRIPTION

### INTRODUCTION

The device is a Quad Low-side Driver driven by four CMOS input stages. Each output power transistor is protected against short to  $V_{BAT}$  by a zener clamp against overvoltage.

A diagnostic logic recognizes four failure types at the output stage : overcurrent, short to GND, open-load and overtemperature.

The failures are individually stored in a byte which can be read out via the serial interface (SPI).

### OUTPUT STAGE CONTROL

Each of the four output stages is switched ON and OFF by an individual control line (NON-Input). The logic level of the control line is CMOS compatible. The output transistors are switched off when the inputs are not connected.

### POWER TRANSISTORS

Each of the four output stages has its own zener clamp. This causes a voltage limitation at the power transistors when inductive loads are switched off. The drain voltage ramp occurring when output is switched on or off, is within defined limits. Output transistors can be connected in parallel to increase current capability. In this case, the associated inputs should be connected together.

### SHORT-CIRCUIT AND OVERTEMPERATURE PROTECTION

If the output current increases above the short current limit for a time longer than  $t_{SCB}$  or if the temperature increases above  $T_{OFF}$  then the power transistor is immediately switched off. It remains switched off until the control signal on the NON-Input is switched off and on again.

### DIAGNOSTICS

The following failures at the output stage are recognized :

Short -Circuit to  $V_{BAT}$  or overtemp = SCB (Highest priority)

Short -Circuit to GND..... = SCG

Open Load..... = OL (Lowest priority)

The SCB failure is recognized by an overcurrent (current above the short current limit) or an overtemperature.

If the current through the output stage is lower than the IOL-reference, after a filter time an OL failure will be recognized. This measurement is active while the power stage is switched on.

The SCG failure will recognize when the drain voltage is lower than the OL reference limit, while the output stage is switched off. All four outputs have an independent overtemperature detection and shutdown. All failures are stored in individual registers.

They can be read by the microprocessor via the serial interface. There is no failure detected if the power stage control time is shorter than the filter time.

### DIAGNOSTIC INTERFACE

The communication between the microprocessor and the failure register runs via the SPI link. If there is a failure stored in the failure register, the first bit of the shift register is set to a high level. With the High/Low change on the NCS pin, the first bit of the diagnostic shift register will be transmitted to the SDO output. The SDO output is the serial output from the diagnostic shift register and it is put into a tri-state when the NCS pin is high. The CLK pin clocks the diagnostic shift register. New SDO data will appear on every rising edge of this pin and new SDI data will be latched on every CLK's falling edge into the shift register. With the first positive pulse of the CLK, the failure register will be cleared. There is no bus collision at a small spike at the NCS. The CLK is always LOW while the NCS-signal is changing.

### RESET

There are two different reset functions realized :

Under voltage reset : as long as the  $V_{CC}$  voltage is lower than  $V_{CCRES}$ , the power stages are switched off and the failure-registers are reset.

Reset pin : as long as the NRES-pin is low, following circuits are reset :

- Power stages
- Failure register

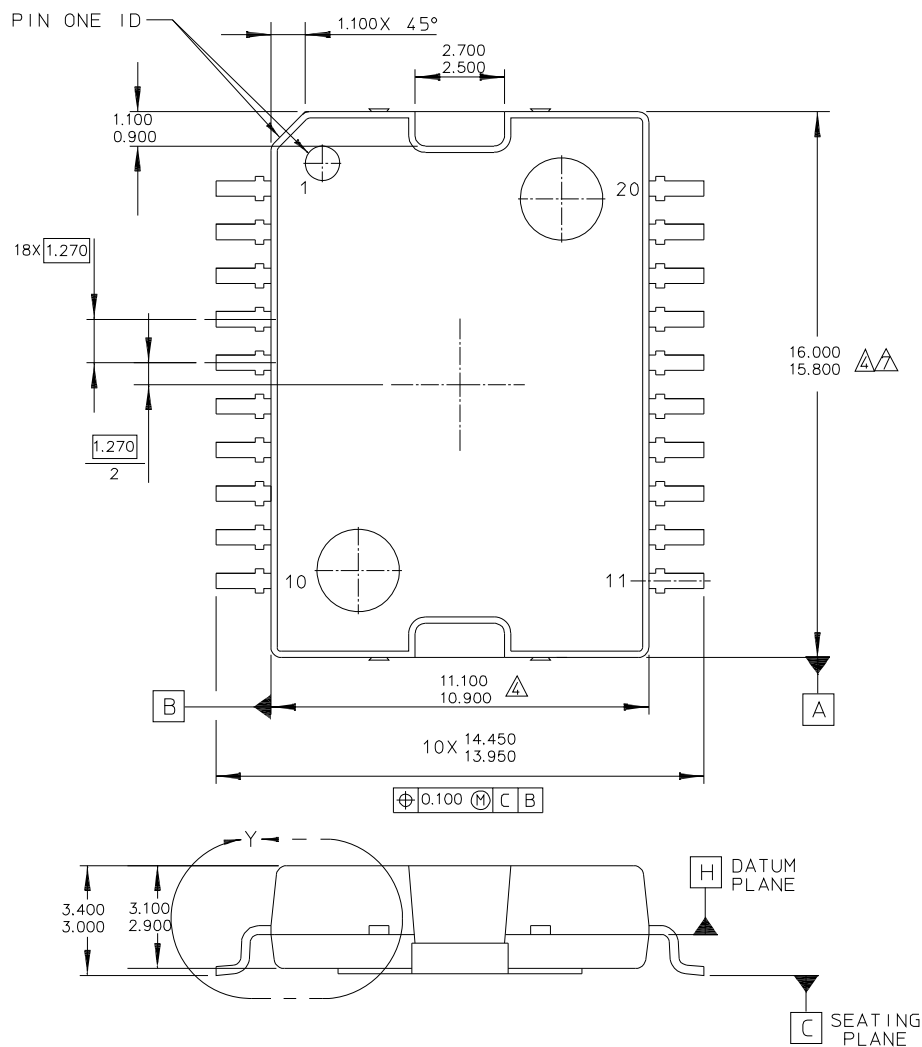
### UNDERVOLTAGE PROTECTION

At low  $V_{CC}$  voltage, the device remains switched off even if there is a voltage ramp at the OUT pin.

## PACKAGING

### PACKAGE DIMENSIONS

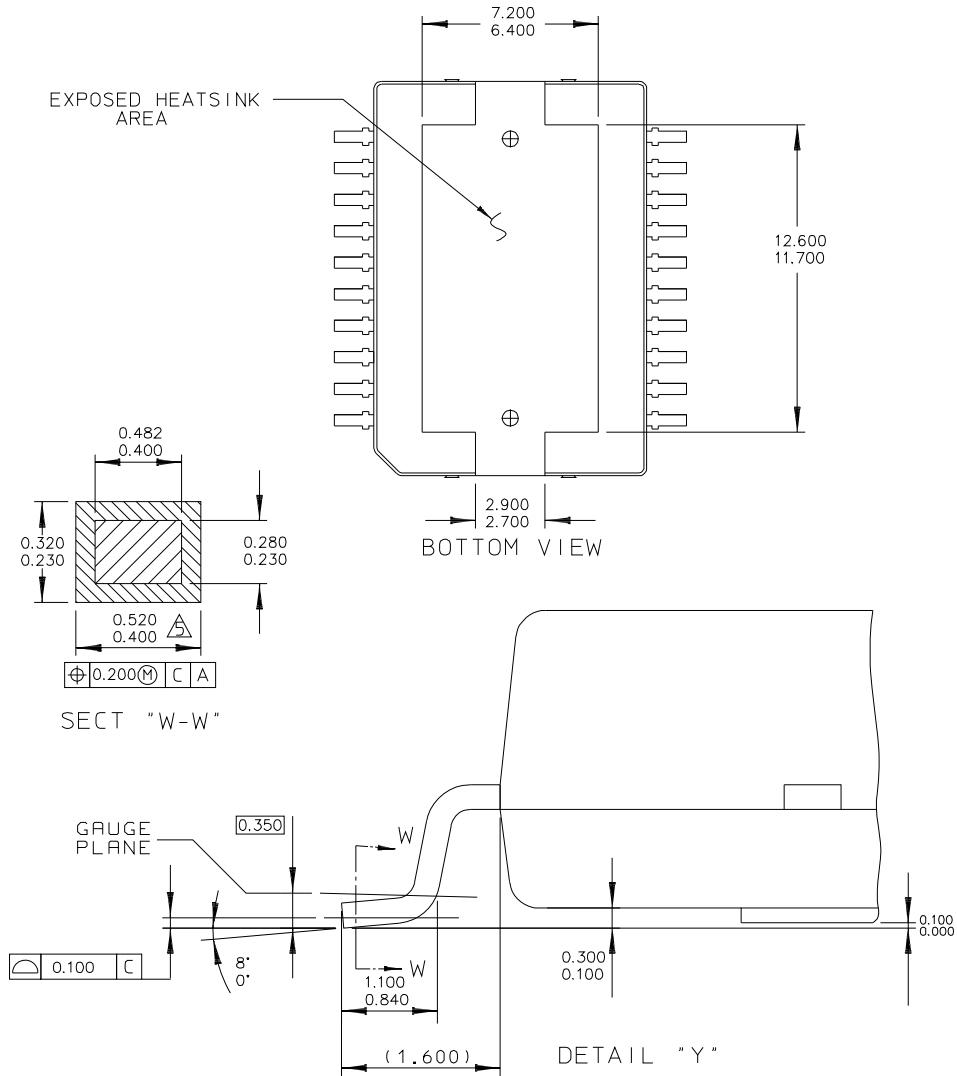
For the most current package revision, visit [www.freescale.com](http://www.freescale.com) and perform a keyword search using the "98A" listed below.



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TITLE: 20 LEAD HSOP W/PROTRUDING HEATSINK	DOCUMENT NO: 98ASH70702A	REV: B
	CASE NUMBER: 979	11 OCT 2005
	STANDARD: NON-JEDEC	

DH SUFFIX  
VW (PB-FREE) SUFFIX  
20-PIN HSOP  
PLASTIC PACKAGE  
98ASH70702A  
ISSUE B

PACKAGE DIMENSIONS (CONTINUED)



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TITLE: 20 LEAD HSOP W/PROTRUDING HEATSINK		DOCUMENT NO: 98ASH70702A		REV: B	
		CASE NUMBER: 979		11 OCT 2005	
		STANDARD: NON-JEDEC			

DH SUFFIX  
VW (PB-FREE) SUFFIX  
20-PIN HSOP  
PLASTIC PACKAGE  
98ASH70702A  
ISSUE B

**REVISION HISTORY**

REVISION	DATE	DESCRIPTION OF CHANGES
6.0	11/2006	<ul style="list-style-type: none"><li>• Implemented Revision History page</li><li>• Added Pb-Free suffix code VW</li><li>• Converted to Freescale format, and adjusted to the prevailing form and style</li></ul>

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