



STP1N120 STU1N120

N-channel 1200 V - 30 Ω - 500 mA - TO-220 - IPAK
Zener - protected SuperMESH™ Power MOSFET

Preliminary Data

Features

Type	V _{DSS}	R _{DS(on)} max	I _D	P _W
STP1N120	1200 V	< 38 Ω	500 mA	45 W
STU1N120	1200 V	< 38 Ω	500 mA	45 W

- 100% avalanche tested
- Extremely high dv/dt capability
- ESD improved capability
- New high voltage benchmark
- Gate charge minimized

Application

- Switching applications

Description

The SuperMESH™ series is obtained through an extreme optimization of ST's well established strip-based PowerMESH™ layout. In addition to pushing on-resistance significantly down, special care is taken to ensure a very good dv/dt capability for the most demanding applications. Such series complements ST full range of high voltage Power MOSFETs including revolutionary MDmesh™ products.

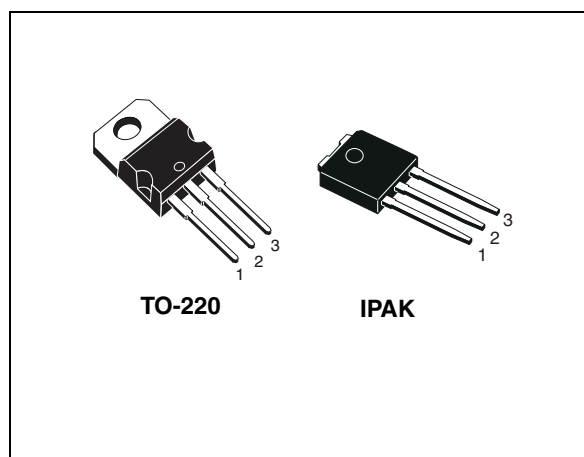


Figure 1. Internal schematic diagram

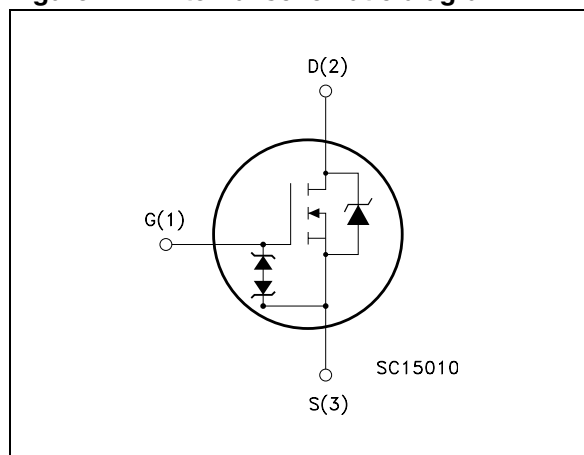


Table 1. Device summary

Order codes	Marking	Package	Packaging
STP1N120	1N120	TO-220	Tube
STU1N120	1N120	IPAK	Tube

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1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage ($V_{GS}=0$)	1200	V
V_{GS}	Gate-source voltage	± 30	V
I_D	Drain current (continuous) at $T_C = 25\text{ }^{\circ}\text{C}$	500	mA
I_D	Drain current (continuous) at $T_C = 100\text{ }^{\circ}\text{C}$	315	mA
$I_{DM}^{(1)}$	Drain current (pulsed)	2	A
	Derating factor	0.36	W/ $^{\circ}\text{C}$
P_{TOT}	Total dissipation at $T_C = 25\text{ }^{\circ}\text{C}$	45	W
T_{stg}	Storage temperature	-55 to 150	$^{\circ}\text{C}$
T_j	Max operating junction temperature	150	$^{\circ}\text{C}$

1. Pulse width limited by safe operating area

Table 3. Thermal data

Symbol	Parameter	Value		Unit
		TO-220	IPAK	
$R_{thj-case}$	Thermal resistance junction-case max	2.78		$^{\circ}\text{C}/\text{W}$
$R_{thj-amb}$	Thermal resistance junction-amb max	62.5	100	$^{\circ}\text{C}/\text{W}$
T_l	Maximum lead temperature for soldering purpose	300		$^{\circ}\text{C}$

Table 4. Avalanche characteristics

Symbol	Parameter	Max value	Unit
I_{AS}	Avalanche current, repetitive or not-repetitive (pulse width limited by T_j max)	0.5	A
E_{AS}	Single pulse avalanche energy (starting $T_j=25\text{ }^{\circ}\text{C}$, $I_D=I_{AS}$, $V_{DD}=50\text{ V}$)	300	mJ

2 Electrical characteristics

(T_{CASE}=25 °C unless otherwise specified)

Table 5. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V _{(BR)DSS}	Drain-source breakdown voltage	I _D = 1 mA, V _{GS} = 0	1200			V
I _{DSS}	Zero gate voltage drain current (V _{GS} = 0)	V _{DS} = Max rating, V _{DS} = Max rating, T _c =125 °C			1 50	μA μA
I _{GSS}	Gate body leakage current (V _{DS} = 0)	V _{GS} = ± 30 V			±10	μA
V _{GS(th)}	Gate threshold voltage	V _{DS} = V _{GS} , I _D = 50 μA	3	4	5	V
R _{DS(on)}	Static drain-source on resistance	V _{GS} = 10 V, I _D = 0.25 A		30	38	Ω

Table 6. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
g _{fs} ⁽¹⁾	Forward transconductance	V _{DS} = 20 V, I _D = 0.25 A		1		S
C _{iss} C _{oss} C _{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V _{DS} = 25 V, f = 1 MHz, V _{GS} = 0		189 24 3	246	pF pF pF
C _{oss eq.} ⁽²⁾	Equivalent output capacitance	V _{GS} = 0, V _{DS} = 0 to 960 V		24		pF
Q _g Q _{gs} Q _{gd}	Total gate charge Gate-source charge Gate-drain charge	V _{DD} = 960 V, I _D = 500 mA V _{GS} = 10 V (see Figure 3)		7.3 1.3 4.4		nC nC nC
R _g	Intrinsic gate resistance	f = 1 MHz open drain		2.3		Ω

1. Pulsed: pulse duration=300μs, duty cycle 1.5%

2. C_{oss eq.} is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}

Table 7. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD}=600\text{ V}$, $I_D=0.25\text{ A}$, $R_G=4.7\ \Omega$, $V_{GS}=10\text{ V}$ (see Figure 5)		10.7		ns
t_r	Rise time			28.5		ns
$t_{d(off)}$	Turn-off delay time			28		ns
t_f	Fall time			88		ns

Table 8. Source drain diode

Symbol	Parameter	Test conditions	Min	Typ.	Max	Unit
I_{SD}	Source-drain current				500	mA
I_{SDM}	Source-drain current (pulsed)				2	A
$V_{SD}^{(1)}$	Forward on voltage	$I_{SD}=500\text{ mA}$, $V_{GS}=0$			1.6	V
t_{rr}	Reverse recovery time	$I_{SD}=500\text{ mA}$, $V_{DD}=100\text{ V}$ $di/dt = 50\text{ A}/\mu\text{s}$ (see Figure 4)		332		ns
Q_{rr}	Reverse recovery charge			0.56		μC
I_{RRM}	Reverse recovery current			3.4		A
t_{rr}	Reverse recovery time	$I_{SD}=500\text{ mA}$, $V_{DD}=100\text{ V}$ $di/dt=50\text{ A}/\mu\text{s}$, $T_j=150\text{ }^\circ\text{C}$ (see Figure 4)		326		ns
Q_{rr}	Reverse recovery charge			0.58		μC
I_{RRM}	Reverse recovery current			6.3		A

1. Pulsed: pulse duration = 300 μs , duty cycle 1.5%

Table 9. Gate-source Zener diode

Symbol	Parameter	Test conditions	Min	Typ.	Max	Unit
$BV_{GSO}^{(1)}$	Gate-source breakdown voltage	$I_{gs} \pm 1\text{ mA}$, (open drain)	30			V

1. The built-in-back Zener diodes have specifically been designed to enhance not only the device's ESD capability, but also to make them safely absorb possible voltage transients that may occasionally be applied from gate to source. In this respect the zener voltage is appropriate to achieve an efficient and cost-effective intervention to protect the device's integrity. These integrated zener diodes thus avoid the usage of external components.

3 Test circuits

Figure 2. Switching times test circuit for resistive load

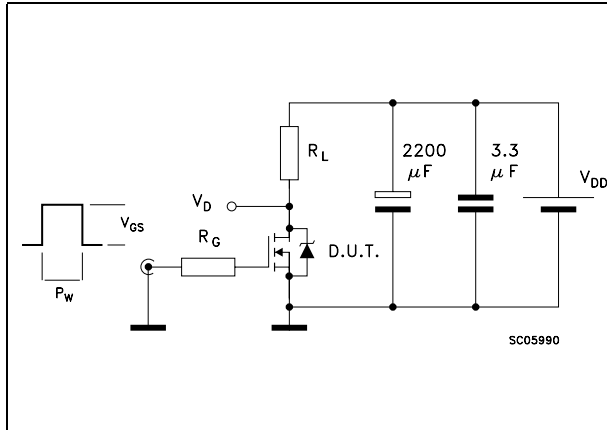


Figure 3. Gate charge test circuit

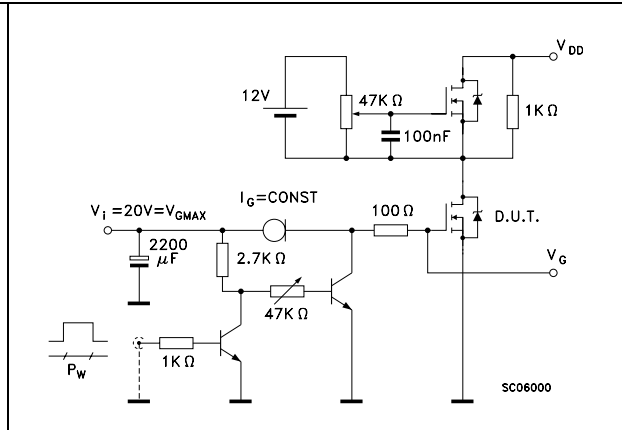


Figure 4. Test circuit for inductive load switching and diode recovery times

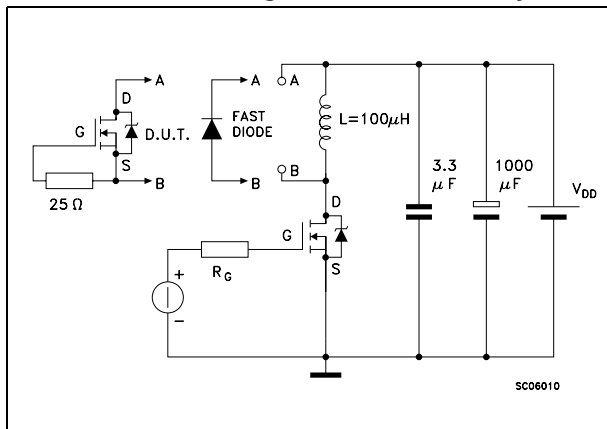


Figure 5. Unclamped inductive load test circuit

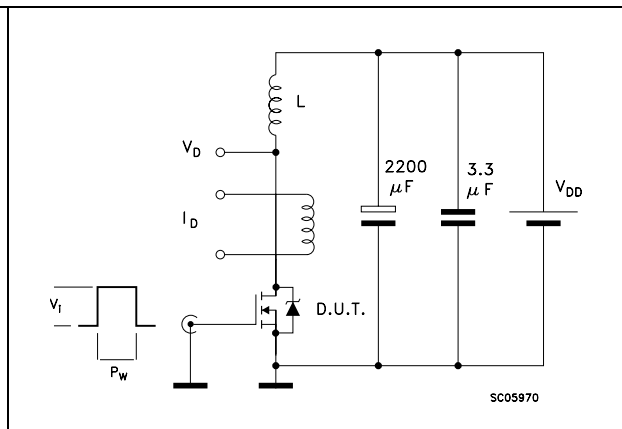


Figure 6. Unclamped inductive waveform

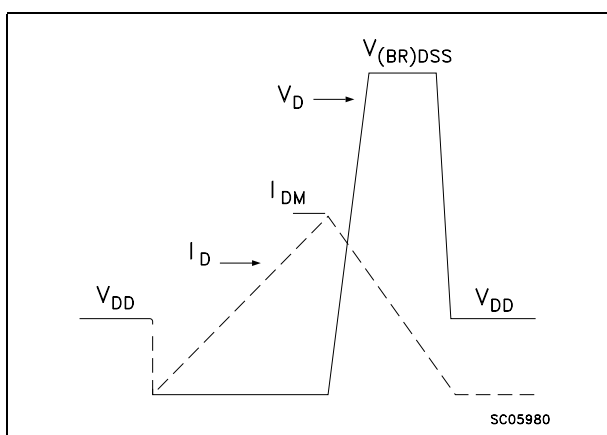
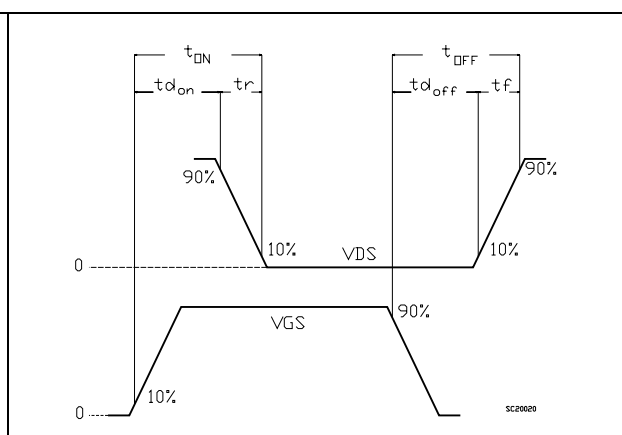


Figure 7. Switching time waveform

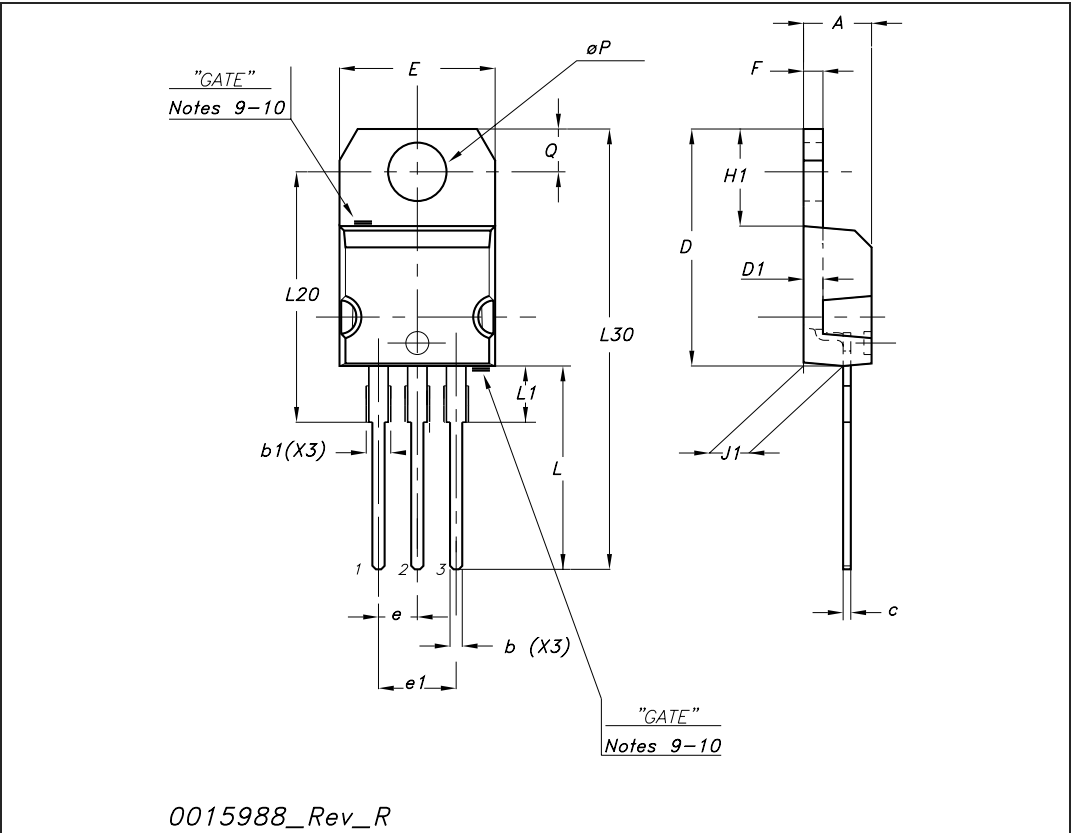


4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect . The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com

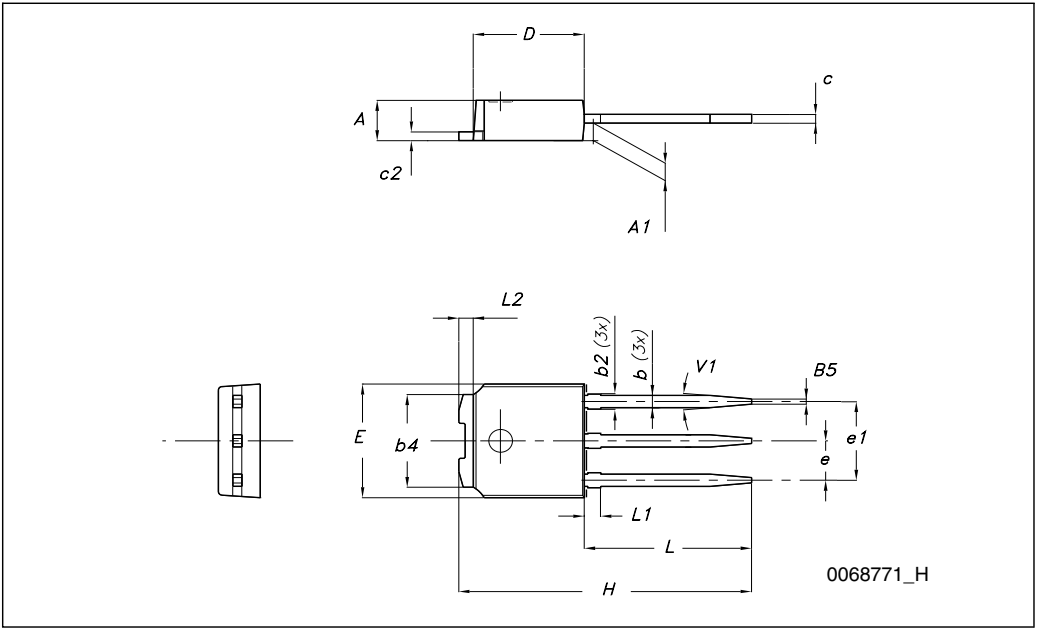
TO-220 mechanical data

Dim	mm			inch		
	Min	Typ	Max	Min	Typ	Max
A	4.40		4.60	0.173		0.181
b	0.61		0.88	0.024		0.034
b1	1.14		1.70	0.044		0.066
c	0.48		0.70	0.019		0.027
D	15.25		15.75	0.6		0.62
D1		1.27			0.050	
E	10		10.40	0.393		0.409
e	2.40		2.70	0.094		0.106
e1	4.95		5.15	0.194		0.202
F	1.23		1.32	0.048		0.051
H1	6.20		6.60	0.244		0.256
J1	2.40		2.72	0.094		0.107
L	13		14	0.511		0.551
L1	3.50		3.93	0.137		0.154
L20		16.40			0.645	
L30		28.90			1.137	
ØP	3.75		3.85	0.147		0.151
Q	2.65		2.95	0.104		0.116



TO-251 (IPAK) mechanical data

DIM.	mm.		
	min.	typ	max.
A	2.20		2.40
A1	0.90		1.10
b	0.64		0.90
b2			0.95
b4	5.20		5.40
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
E	6.40		6.60
e		2.28	
e1	4.40		4.60
H		16.10	
L	9.00		9.40
(L1)	0.80		1.20
L2		0.80	
V1		10 °	



5 Revision history

Table 10. Document revision history

Date	Revision	Changes
11-Oct-2006	1	First release
20-Mar-2008	2	Added IPAK package, preliminary version

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