

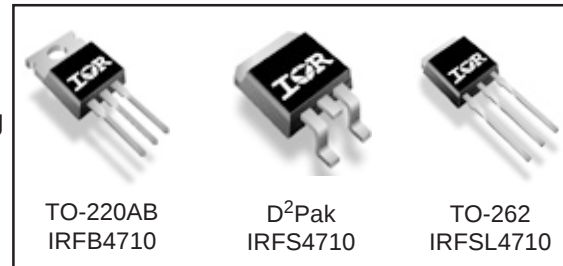
Applications

- High frequency DC-DC converters
- Motor Control
- Uninterruptible Power Supplies

V_{DSS}	$R_{DS(on)}$ max	I_D
100V	0.014 Ω	75A

Benefits

- Low Gate-to-Drain Charge to Reduce Switching Losses
- Fully Characterized Capacitance Including Effective C_{OSS} to Simplify Design, (See App. Note AN1001)
- Fully Characterized Avalanche Voltage and Current



Absolute Maximum Ratings

	Parameter	Max.	Units
I_D @ $T_C = 25^\circ\text{C}$	Continuous Drain Current, V_{GS} @ 10V	75	A
I_D @ $T_C = 100^\circ\text{C}$	Continuous Drain Current, V_{GS} @ 10V	53	
I_{DM}	Pulsed Drain Current ①	300	
P_D @ $T_A = 25^\circ\text{C}$	Power Dissipation ②	3.8	W
P_D @ $T_C = 25^\circ\text{C}$	Power Dissipation	200	
	Linear Derating Factor	1.4	W/ $^\circ\text{C}$
V_{GS}	Gate-to-Source Voltage	± 20	V
dv/dt	Peak Diode Recovery dv/dt ③	8.2	V/ns
T_J	Operating Junction and	-55 to + 175	$^\circ\text{C}$
T_{STG}	Storage Temperature Range		
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	
	Mounting torque, 6-32 or M3 screw⑥	10 lbf•in (1.1N•m)	

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	0.74	$^\circ\text{C}/\text{W}$
$R_{\theta CS}$	Case-to-Sink, Flat, Greased Surface ④	0.50	—	
$R_{\theta JA}$	Junction-to-Ambient⑤	—	62	
$R_{\theta JA}$	Junction-to-Ambient⑦	—	40	

Notes ① through ⑦ are on page 11

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Static @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	100	—	—	V	$V_{GS} = 0V, I_D = 250\mu A$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.11	—	V/ $^\circ\text{C}$	Reference to 25°C , $I_D = 1mA$
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	0.011	0.014	Ω	$V_{GS} = 10V, I_D = 45A$ ④
$V_{GS(th)}$	Gate Threshold Voltage	3.5	—	5.5	V	$V_{DS} = V_{GS}, I_D = 250\mu A$
I_{DSS}	Drain-to-Source Leakage Current	—	—	1.0	μA	$V_{DS} = 95V, V_{GS} = 0V$
		—	—	250		$V_{DS} = 80V, V_{GS} = 0V, T_J = 150^\circ\text{C}$
I_{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	$V_{GS} = 20V$
	Gate-to-Source Reverse Leakage	—	—	-100		$V_{GS} = -20V$

Dynamic @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
g_{fs}	Forward Transconductance	35	—	—	S	$V_{DS} = 50V, I_D = 45A$
Q_g	Total Gate Charge	—	110	170	nC	$I_D = 45A$
Q_{gs}	Gate-to-Source Charge	—	43	—		$V_{DS} = 50V$
Q_{gd}	Gate-to-Drain ("Miller") Charge	—	40	—		$V_{GS} = 10V,$
$t_{d(on)}$	Turn-On Delay Time	—	35	—	ns	$V_{DD} = 50V$
t_r	Rise Time	—	130	—		$I_D = 45A$
$t_{d(off)}$	Turn-Off Delay Time	—	41	—		$R_G = 4.5\Omega$
t_f	Fall Time	—	38	—		$V_{GS} = 10V$ ④
C_{iss}	Input Capacitance	—	6160	—	pF	$V_{GS} = 0V$
C_{oss}	Output Capacitance	—	440	—		$V_{DS} = 25V$
C_{rss}	Reverse Transfer Capacitance	—	250	—		$f = 1.0MHz$
C_{oss}	Output Capacitance	—	1580	—		$V_{GS} = 0V, V_{DS} = 1.0V, f = 1.0MHz$
C_{oss}	Output Capacitance	—	280	—		$V_{GS} = 0V, V_{DS} = 80V, f = 1.0MHz$
$C_{oss \text{ eff.}}$	Effective Output Capacitance	—	430	—		$V_{GS} = 0V, V_{DS} = 0V \text{ to } 80V$ ⑤

Avalanche Characteristics

	Parameter	Typ.	Max.	Units
E_{AS}	Single Pulse Avalanche Energy②	—	190	mJ
I_{AR}	Avalanche Current①	—	45	A
E_{AR}	Repetitive Avalanche Energy①	—	20	mJ

Diode Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	75	A	MOSFET symbol showing the integral reverse p-n junction diode.
I_{SM}	Pulsed Source Current (Body Diode) ①⑥	—	—	300		
V_{SD}	Diode Forward Voltage	—	—	1.3	V	$T_J = 25^\circ\text{C}, I_S = 45A, V_{GS} = 0V$ ④
t_{rr}	Reverse Recovery Time	—	74	110	ns	$T_J = 25^\circ\text{C}, I_F = 45A$
Q_{rr}	Reverse Recovery Charge	—	180	260	nC	$di/dt = 100A/\mu s$ ④
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by $L_S + L_D$)				

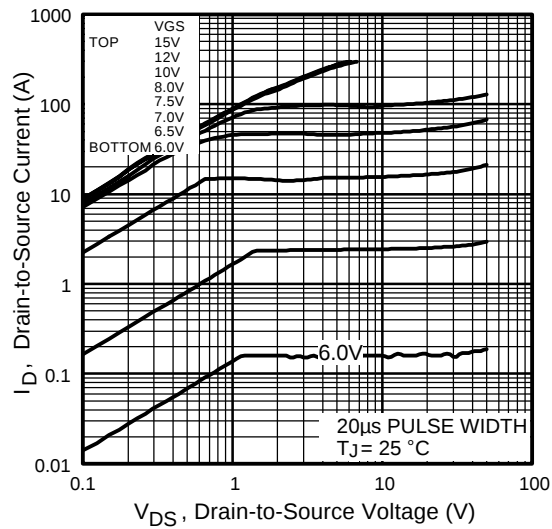


Fig 1. Typical Output Characteristics

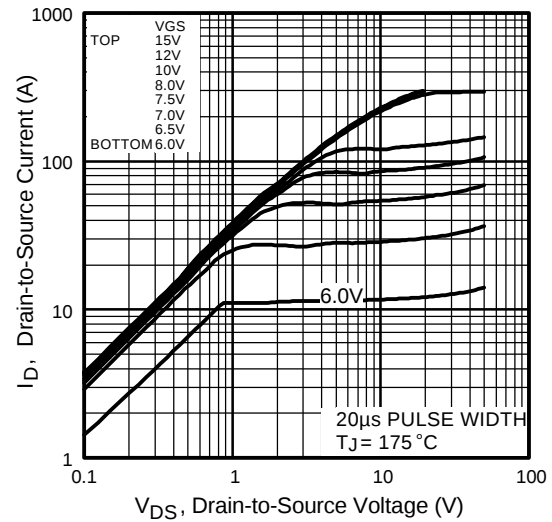


Fig 2. Typical Output Characteristics

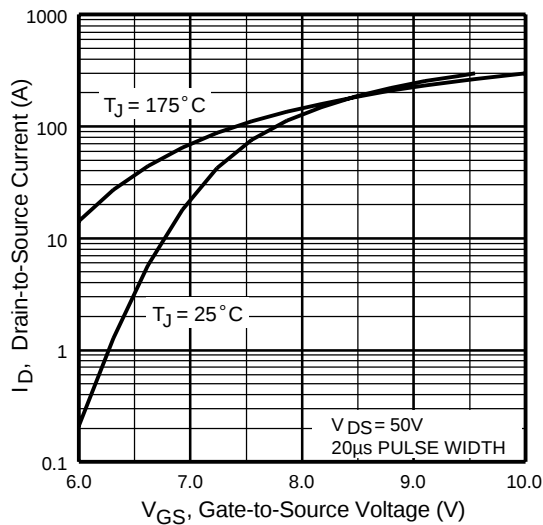


Fig 3. Typical Transfer Characteristics

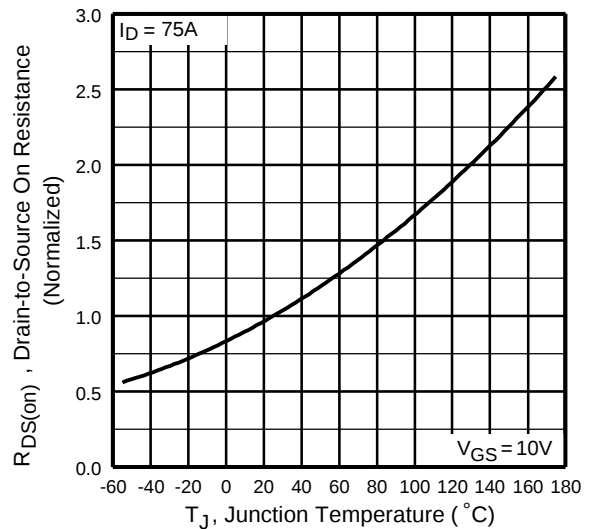


Fig 4. Normalized On-Resistance Vs. Temperature

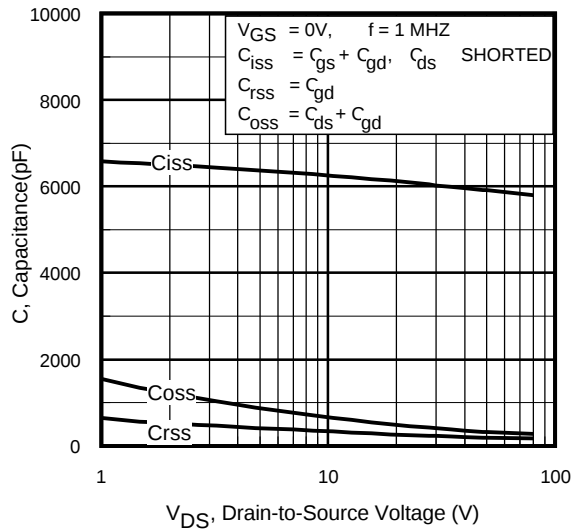


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

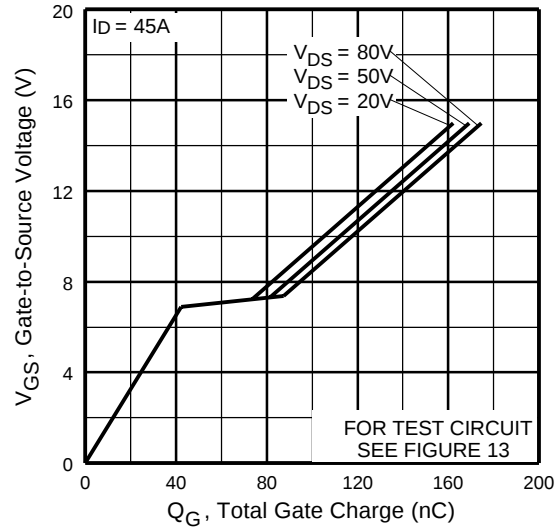


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

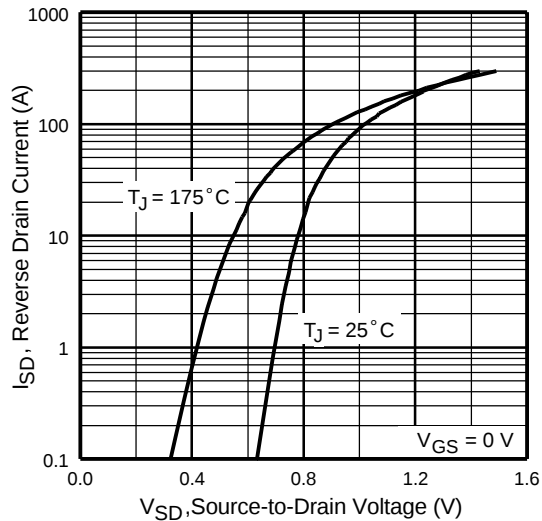


Fig 7. Typical Source-Drain Diode Forward Voltage

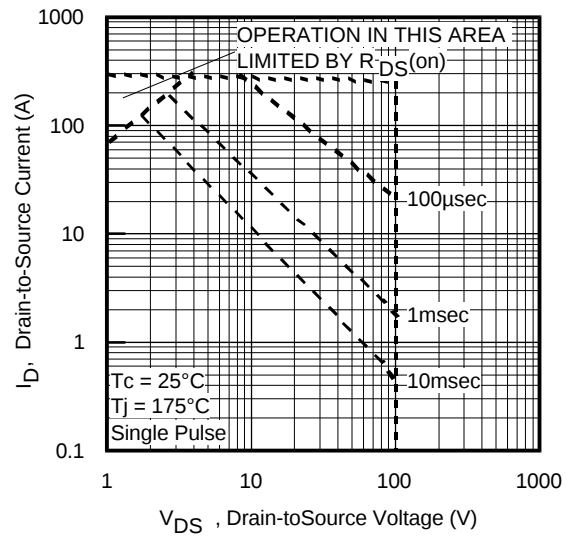


Fig 8. Maximum Safe Operating Area

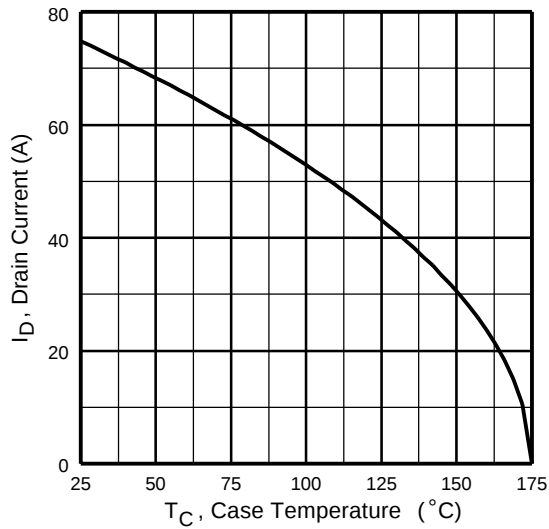


Fig 9. Maximum Drain Current Vs. Case Temperature



Fig 10a. Switching Time Test Circuit



Fig 10b. Switching Time Waveforms

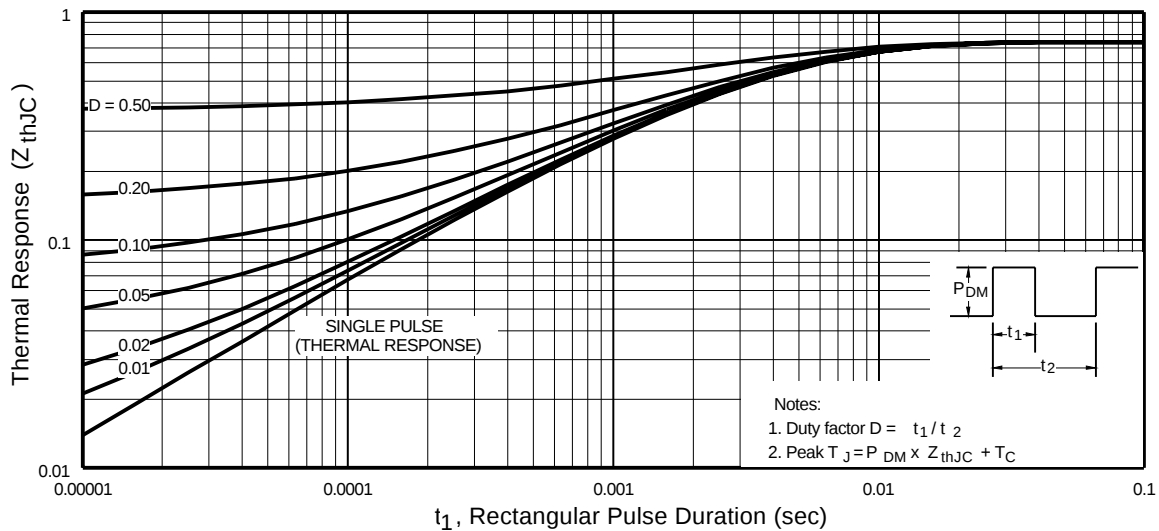


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

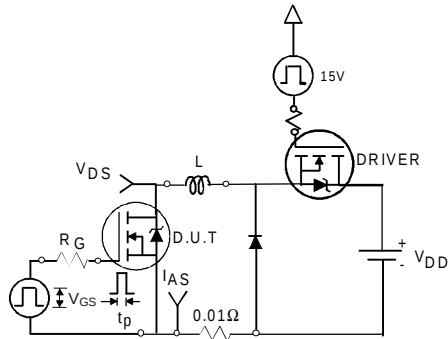


Fig 12a. Unclamped Inductive Test Circuit



Fig 12b. Unclamped Inductive Waveforms

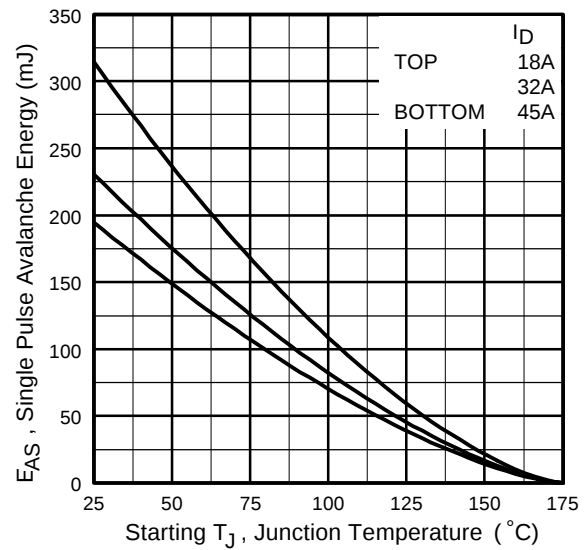


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

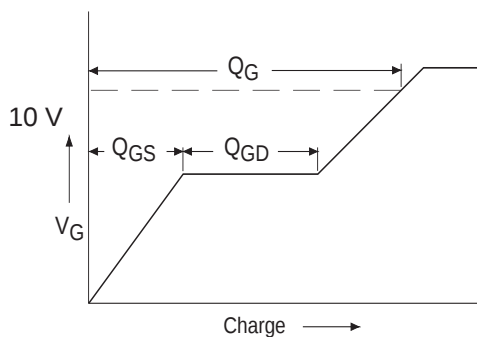


Fig 13a. Basic Gate Charge Waveform



Fig 13b. Gate Charge Test Circuit

Peak Diode Recovery dv/dt Test Circuit



* $V_{GS} = 5V$ for Logic Level Devices

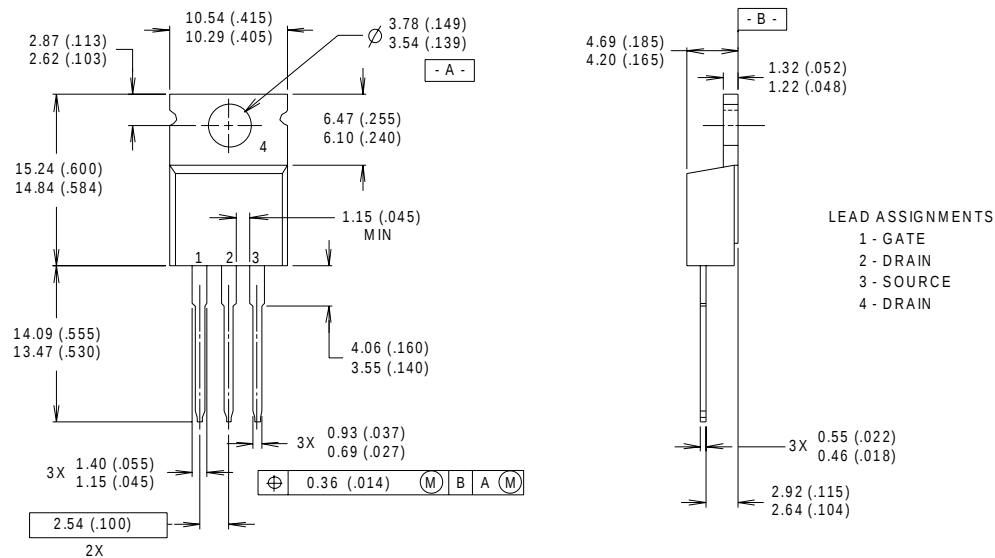
Fig 14. For N-Channel HEXFET® Power MOSFETs

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TO-220AB Package Outline

Dimensions are shown in millimeters (inches)



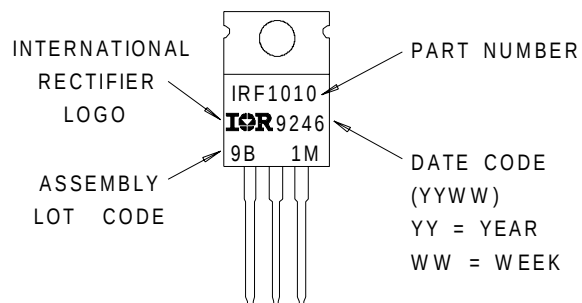
NOTES:

- 1 DIMENSIONING & TOLERANCING PER ANSI Y14.5M, 1982.
- 2 CONTROLLING DIMENSION : INCH

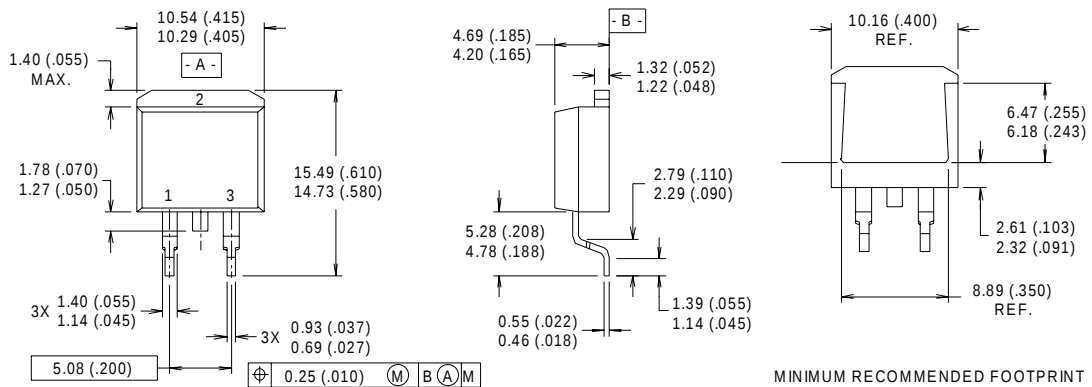
- 3 OUTLINE CONFORMS TO JEDEC OUTLINE TO-220AB.
- 4 HEATSINK & LEAD MEASUREMENTS DO NOT INCLUDE BURRS.

TO-220AB Part Marking Information

EXAMPLE : THIS IS AN IRF1010
WITH ASSEMBLY
LOT CODE 9B1M



D²Pak Package Outline



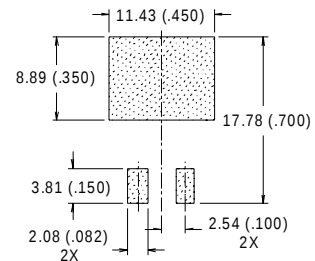
NOTES:

- 1 DIMENSIONS AFTER SOLDER DIP.
- 2 DIMENSIONING & TOLERANCING PER ANSI Y14.5M, 1982.
- 3 CONTROLLING DIMENSION : INCH.
- 4 HEATSINK & LEAD DIMENSIONS DO NOT INCLUDE BURRS.

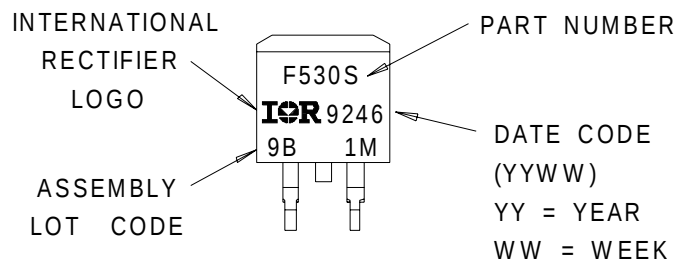
LEAD ASSIGNMENTS

- 1 - GATE
- 2 - DRAIN
- 3 - SOURCE

MINIMUM RECOMMENDED FOOTPRINT



D²Pak Part Marking Information



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[illegible]

Technical drawing of a shaft with the following dimensions:

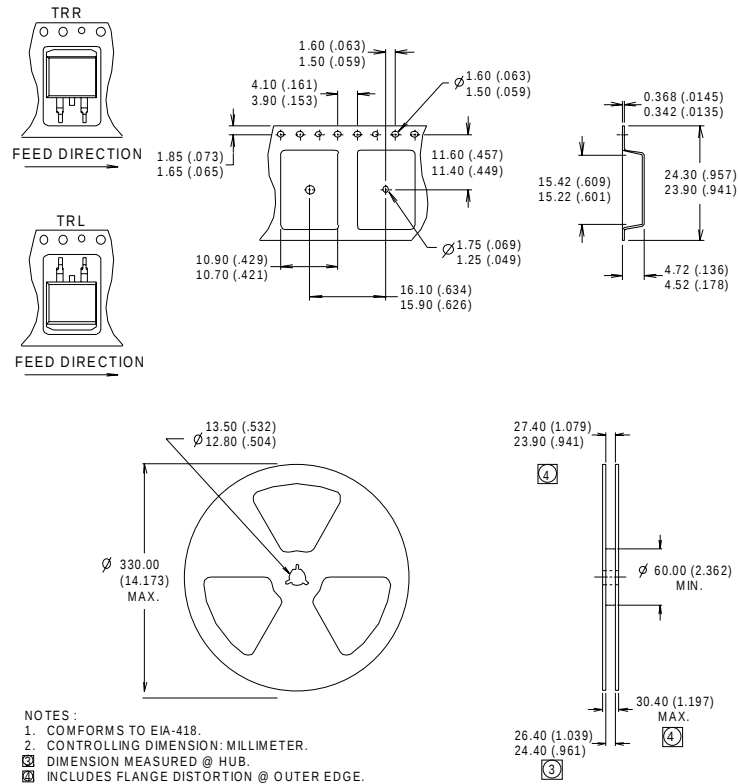
- Top diameter: 4.69 [.185]
- Second diameter from top: 4.20 [.165]
- Third diameter from top: 1.32 [.052]
- Fourth diameter from top: 1.22 [.048]
- Bottom diameter: 2.92 [.115]
- Bottom diameter (alternative): 2.64 [.104]
- Length of the bottom section: 3X
- Length of the section above the bottom section: 0.55 [.022]
- Length of the section above the bottom section (alternative): 0.46 [.018]

1. DIMENSIONING & TOLERANCING PER ANSI Y14.5M-1982
2. CONTROLLING DIMENSION: INCH.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. HEATSINK & LEAD DIMENSIONS DO NOT INCLUDE BURRS.

Diagram illustrating the marking on the IRL3103L MOSFET package:

- INTERNATIONAL RECTIFIER** (Logo)
- PART NUMBER** (IRL3103L)
- DATE CODE** (719C)
- YEAR 7 = 1997**
- WEEK 19**
- LINE C**
- ASSEMBLY LOT CODE** (17 89)

D²Pak Tape & Reel Information



Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature.
- ② Starting $T_J = 25^\circ\text{C}$, $L = 190\mu\text{H}$
 $R_G = 25\Omega$, $I_{AS} = 45\text{A}$, $V_{GS} = 10\text{V}$
- ③ $I_{SD} \leq 45\text{A}$, $di/dt \leq 420\text{A}/\mu\text{s}$, $V_{DD} \leq V_{(BR)DSS}$, $T_J \leq 175^\circ\text{C}$
- ④ Pulse width $\leq 400\mu\text{s}$; duty cycle $\leq 2\%$.
- ⑤ C_{OSS} eff. is a fixed capacitance that gives the same charging time as C_{OSS} while V_{DS} is rising from 0 to 80% V_{DSS}
- ⑥ This is only applied to TO-220AB package
- ⑦ This is applied to D²Pak, when mounted on 1" square PCB (FR-4 or G-10 Material).
For recommended footprint and soldering techniques refer to application note #AN-994.

Data and specifications subject to change without notice.
This product has been designed and qualified for the Industrial market.
Qualification Standards can be found on IR's Web site.

Note: For the most current drawings please refer to the IR website at:
<http://www.irf.com/package/>