CY7C1041DV33

4-Mbit (256K x 16) Static RAM

Features

- Pin- and function-compatible with CY7C1041CV33
- High speed
  — t_{AA} =10 ns
- Low active power
  — I_{CC} = 90 mA @ 10 ns (Industrial)
- Low CMOS standby power
  — I_{SB2} = 10 mA
- 2.0 V data retention
- Automatic power-down when deselected
- TTL-compatible inputs and outputs
- Easy memory expansion with $\overline{CE}$ and $\overline{OE}$ features
- Available in lead-free 48-ball VFBGA, 44-lead (400-mil) Molded SOJ and 44-pin TSOP II packages

Functional Description[1]

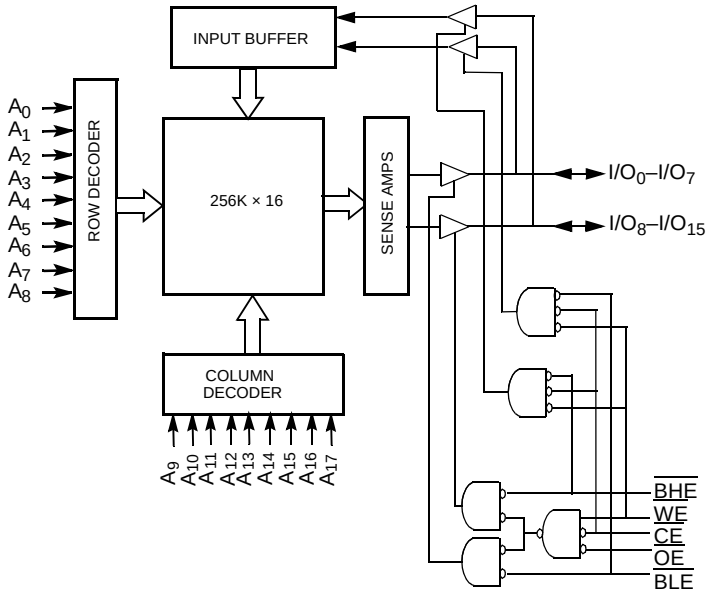
The CY7C1041DV33 is a high-performance CMOS Static RAM organized as 256K words by 16 bits. Writing to the device is accomplished by taking Chip Enable ($\overline{CE}$) and Write Enable ($\overline{WE}$) inputs LOW. If Byte LOW Enable ($\overline{BLE}$) is LOW, then data from I/O pins (I/O_0–I/O_7), is written into the location specified on the address pins (A_0–A_{17}). If Byte HIGH Enable ($\overline{BHE}$) is LOW, then data from I/O pins (I/O_8–I/O_{15}) is written into the location specified on the address pins (A_0–A_{17}).

Reading from the device is accomplished by taking Chip Enable ($\overline{CE}$) and Output Enable ($\overline{OE}$) LOW while forcing the Write Enable ($\overline{WE}$) HIGH. If Byte LOW Enable ($\overline{BLE}$) is LOW, then data from the memory location specified by the address pins will appear on I/O_0 – I/O_7. If Byte HIGH Enable ($\overline{BHE}$) is LOW, then data from memory will appear on I/O_8 to I/O_{15}. See the truth table at the back of this data sheet for a complete description of Read and Write modes.

The input/output pins (I/O_0–I/O_{15}) are placed in a high-impedance state when the device is deselected ($\overline{CE}$ HIGH), the outputs are disabled ($\overline{OE}$ HIGH), the $\overline{BHE}$ and $\overline{BLE}$ are disabled ($\overline{BHE}$, $\overline{BLE}$ HIGH), or during a Write operation ($\overline{CE}$ LOW, and $\overline{WE}$ LOW).

The CY7C1041DV33 is available in a standard 44-pin 400-mil-wide body width SOJ and 44-pin TSOP II package with center power and ground (revolutionary) pinout, as well as a 48-ball fine-pitch ball grid array (FBGA) package.

Logic Block Diagram



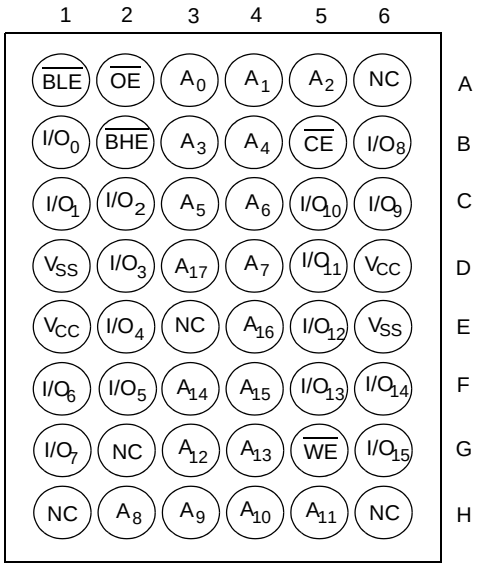
Note
1. For guidelines on SRAM system design, please refer to the “System Design Guidelines” Cypress application note, available on the internet at www.cypress.com.

Selection Guide

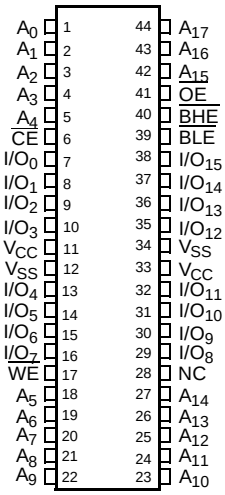
	–10 (Industrial)	–12 (Automotive)[2]	Unit
Maximum Access Time	10	12	ns
Maximum Operating Current	90	95	mA
Maximum CMOS Standby Current	10	15	mA

Pin Configurations

48-ball Mini FBGA
(Top View)



SOJ
TSOP II
Top View



Note
2. Automotive product information is Preliminary.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature .....–65°C to +150°C

Ambient Temperature with Power Applied.....–55°C to +125°C

Supply Voltage on V_{CC} to Relative GND[3] .... –0.3V to +4.6V

DC Voltage Applied to Outputs in High-Z State[3] .....–0.3V to V_{CC} +0.3V

DC Input Voltage[3].....–0.3V to V_{CC} +0.3V

Current into Outputs (LOW)..... 20 mA

Static Discharge Voltage..... .....>2001V (per MIL-STD-883, Method 3015)

Latch-up Current.....>200 mA

Operating Range

Range	Ambient Temperature	V_{CC}	Speed
Industrial	–40°C to +85°C	3.3V ± 0.3V	10 ns
Automotive	–40°C to +125°C	3.3V ± 0.3V	12 ns

DC Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions		–10 (Industrial)		–12 (Automotive)		Unit
				Min.	Max.	Min.	Max.	
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = –4.0 mA		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.4		0.4	V
V_{IH}[3]	Input HIGH Voltage			2.0	V_{CC} + 0.3	2.0	V_{CC} + 0.3	V
V_{IL}[3]	Input LOW Voltage			–0.3	0.8	–0.3	0.8	V
I_{IX}	Input Leakage Current	GND ≤ V_I ≤ V_{CC}		–1	+1	–1	+1	µA
I_{OZ}	Output Leakage Current	GND ≤ V_{OUT} ≤ V_{CC}, Output Disabled		–1	+1	–1	+1	µA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., f = f_{MAX} = $1/t_{RC}$	100MHz		90		-	mA
			83MHz		80		95	mA
			66MHz		70		85	mA
			40MHz		60		75	mA
I_{SB1}	Automatic CE Power-down Current—TTL Inputs	Max. V_{CC}, $\overline{CE}$ ≥ V_{IH} V_{IN} ≥ V_{IH} or V_{IN} ≤ V_{IL}, f = f_{MAX}			20		25	mA
I_{SB2}	Automatic CE Power-down Current—CMOS Inputs	Max. V_{CC}, $\overline{CE}$ ≥ V_{CC} – 0.3V, V_{IN} ≥ V_{CC} – 0.3V, or V_{IN} ≤ 0.3V, f = 0			10		15	mA

Note

3. Minimum voltage is–2.0V and V_{IH}(max) = V_{CC} + 2V for pulse durations of less than 20 ns.

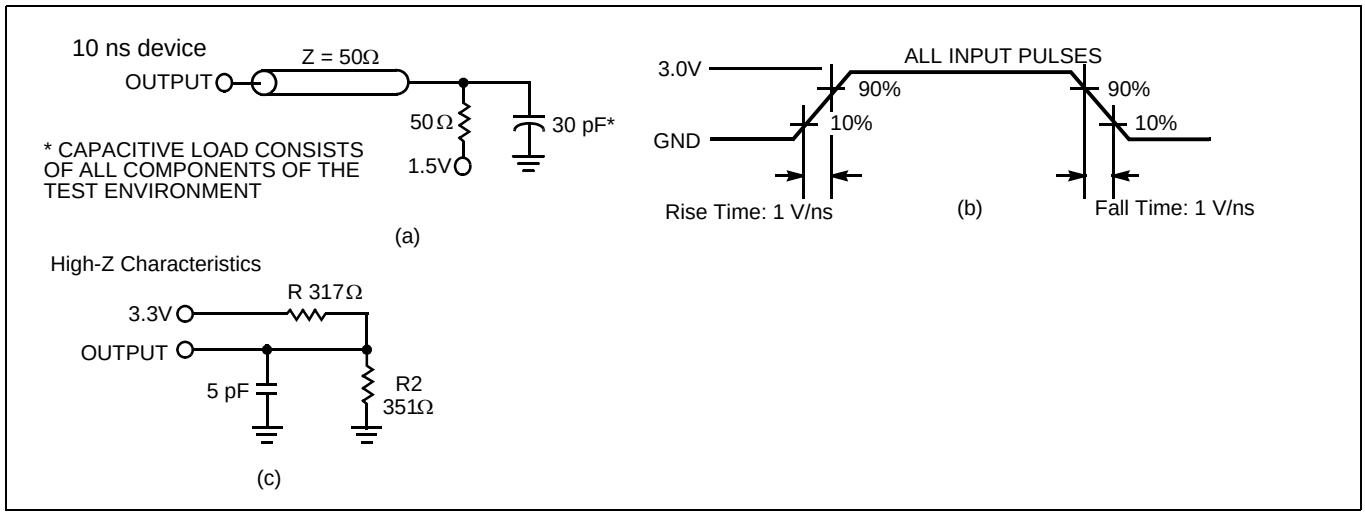
Capacitance[4]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 3.3V	8	pF
C_{OUT}	I/O Capacitance		8	pF

Thermal Resistance[4]

Parameter	Description	Test Conditions	FBGA Package	SOJ Package	TSOP II Package	Unit
Θ_{JA}	Thermal Resistance (Junction to Ambient)	Still Air, soldered on a 3 × 4.5 inch, four-layer printed circuit board	27.89	57.91	50.66	°C/W
Θ_{JC}	Thermal Resistance (Junction to Case)		14.74	36.73	17.17	°C/W

AC Test Loads and Waveforms[5]



Notes
4. Tested initially and after any design or process changes that may affect these parameters.
5. AC characteristics (except High-Z) are tested using the load conditions shown in Figure (a). High-Z characteristics are tested for all speeds using the test load shown in Figure (c).

AC Switching Characteristics Over the Operating Range[6]

Parameter	Description	–10 (Industrial)		–12 (Automotive)		Unit
		Min.	Max.	Min.	Max.	
Read Cycle						
t_{power}[7]	V_{CC}(typical) to the first access	100		100		µs
t_{RC}	Read Cycle Time	10		12		ns
t_{AA}	Address to Data Valid		10		12	ns
t_{OHA}	Data Hold from Address Change	3		3		ns
t_{ACE}	$\overline{CE}$ LOW to Data Valid		10		12	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		5		6	ns
t_{LZOE}	$\overline{OE}$ LOW to Low-Z	0		0		ns
t_{HZOE}	$\overline{OE}$ HIGH to High-Z[8, 9]		5		6	ns
t_{LZCE}	$\overline{CE}$ LOW to Low-Z[9]	3		3		ns
t_{HZCE}	$\overline{CE}$ HIGH to High-Z[8, 9]		5		6	ns
t_{PU}	$\overline{CE}$ LOW to Power-Up	0		0		ns
t_{PD}	$\overline{CE}$ HIGH to Power-Down		10		12	ns
t_{DBE}	Byte Enable to Data Valid		5		6	ns
t_{LZBE}	Byte Enable to Low-Z	0		0		ns
t_{HZBE}	Byte Disable to High-Z		6		6	ns

Notes

6. Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
7. t_{POWER} gives the minimum amount of time that the power supply should be at typical V_{CC} values until the first memory access can be performed.
8. t_{HZOE}, t_{HZCE},t_{HZBE} and t_{HZWE} are specified with a load capacitance of 5 pF as in part (c) of AC Test Loads. Transition is measured when the outputs enter a high impedance state.
9. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZOE} is less than t_{LZOE}, t_{HZBE} is less than t_{LZBE}, and t_{HZWE} is less than t_{LZWE} for any given device.

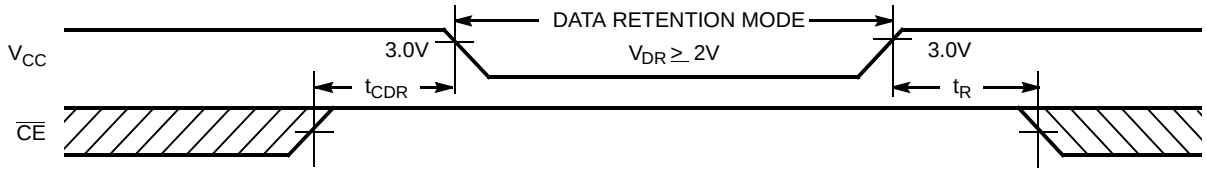
AC Switching Characteristics Over the Operating Range[6](continued)

Parameter	Description	–10 (Industrial)		–12 (Automotive)		Unit
		Min.	Max.	Min.	Max.	
Write Cycle[10, 11]						
t_{WC}	Write Cycle Time	10		12		ns
t_{SCE}	$\overline{CE}$ LOW to Write End	7		8		ns
t_{AW}	Address Set-Up to Write End	7		8		ns
t_{HA}	Address Hold from Write End	0		0		ns
t_{SA}	Address Set-Up to Write Start	0		0		ns
t_{PWE}	$\overline{WE}$ Pulse Width	7		8		ns
t_{SD}	Data Set-Up to Write End	5		6		ns
t_{HD}	Data Hold from Write End	0		0		ns
t_{LZWE}	$\overline{WE}$ HIGH to Low-Z[9]	3		3		ns
t_{HZWE}	$\overline{WE}$ LOW to High-Z[8, 9]		5		6	ns
t_{BW}	Byte Enable to End of Write	7		8		ns

Data Retention Characteristics Over the Operating Range

Parameter	Description	Conditions[12]		Min.	Max.	Unit
V_{DR}	V_{CC} for Data Retention			2.0		V
I_{CCDR}	Data Retention Current	$V_{CC} = V_{DR} = 2.0V$, $\overline{CE} \geq V_{CC} - 0.3V$, $V_{IN} \geq V_{CC} - 0.3V$ or $V_{IN} \leq 0.3V$	Ind'l		10	mA
			Auto		15	mA
t_{CDR}[4]	Chip Deselect to Data Retention Time			0		ns
t_R[13]	Operation Recovery Time			t_{RC}		ns

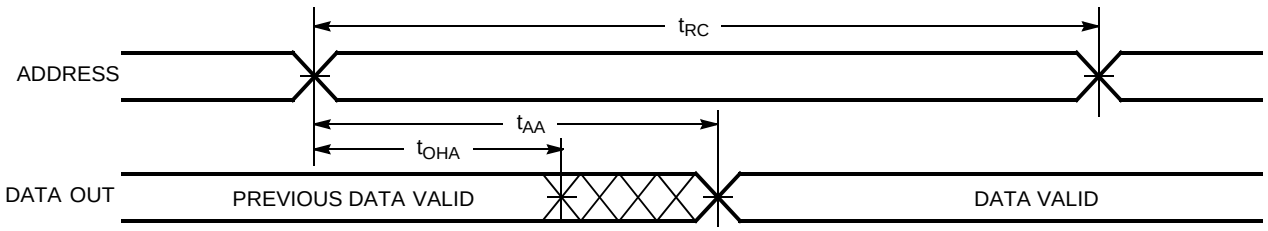
Data Retention Waveform



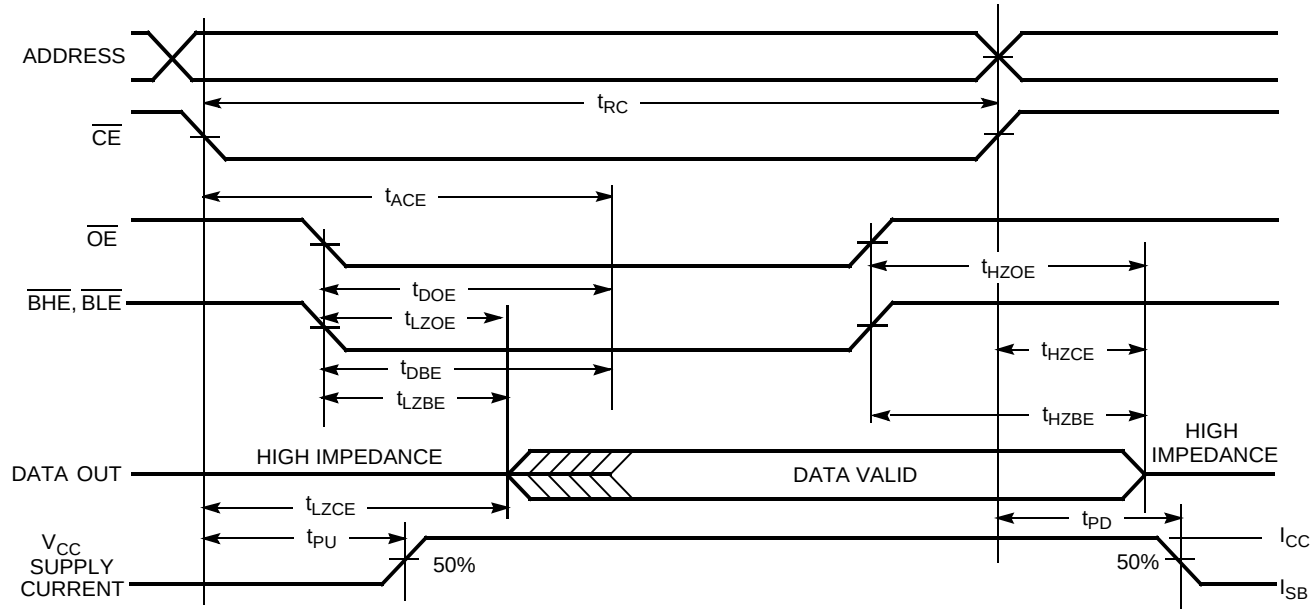
Notes
10. The internal Write time of the memory is defined by the overlap of $\overline{CE}$ LOW, and $\overline{WE}$ LOW. $\overline{CE}$ and $\overline{WE}$ must be LOW to initiate a Write, and the transition of either of these signals can terminate the Write. The input data set-up and hold timing should be referenced to the leading edge of the signal that terminates the Write.
11. The minimum Write cycle time for Write Cycle No. 4 ($\overline{WE}$ controlled, $\overline{OE}$ LOW) is the sum of t_{HZWE} and t_{SD}.
12. No input may exceed V_{CC} + 0.3V.
13. Full device operation requires linear V_{CC} ramp from V_{DR} to $V_{CC(min.)} \geq 50$ µs or stable at $V_{CC(min.)} \geq 50$ µs

Switching Waveforms

Read Cycle No. 1[14, 15]



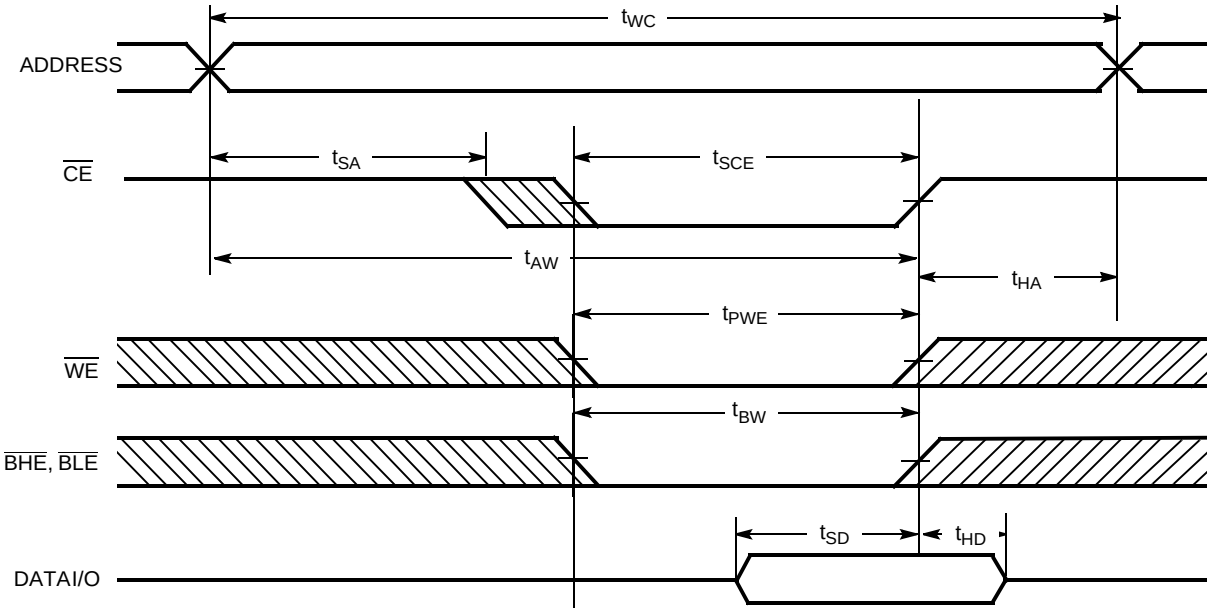
Read Cycle No. 2 ($\overline{OE}$ Controlled)[15, 16]



Notes
14. Device is continuously selected. $\overline{OE}$, $\overline{CE}$, $\overline{BHE}$ and/or $\overline{BHE}$ = V_{IL}.
15. $\overline{WE}$ is HIGH for Read cycle.
16. Address valid prior to or coincident with $\overline{CE}$ transition LOW.

Switching Waveforms (continued)

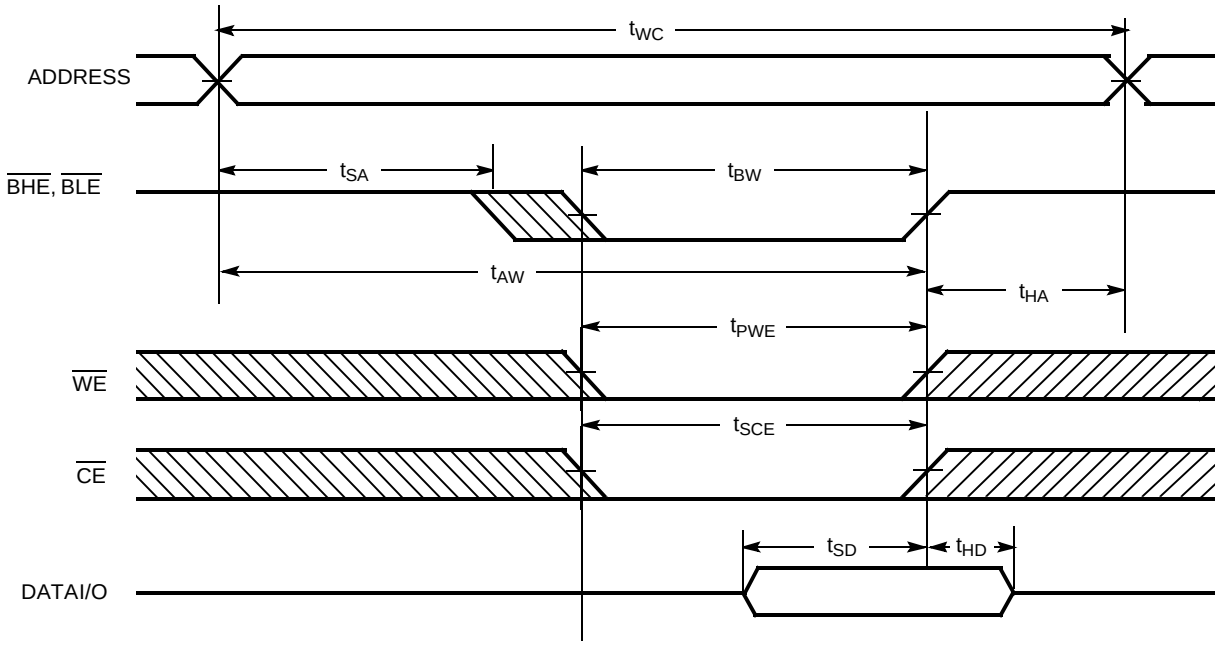
Write Cycle No. 1 ($\overline{CE}$ Controlled)[17, 18]



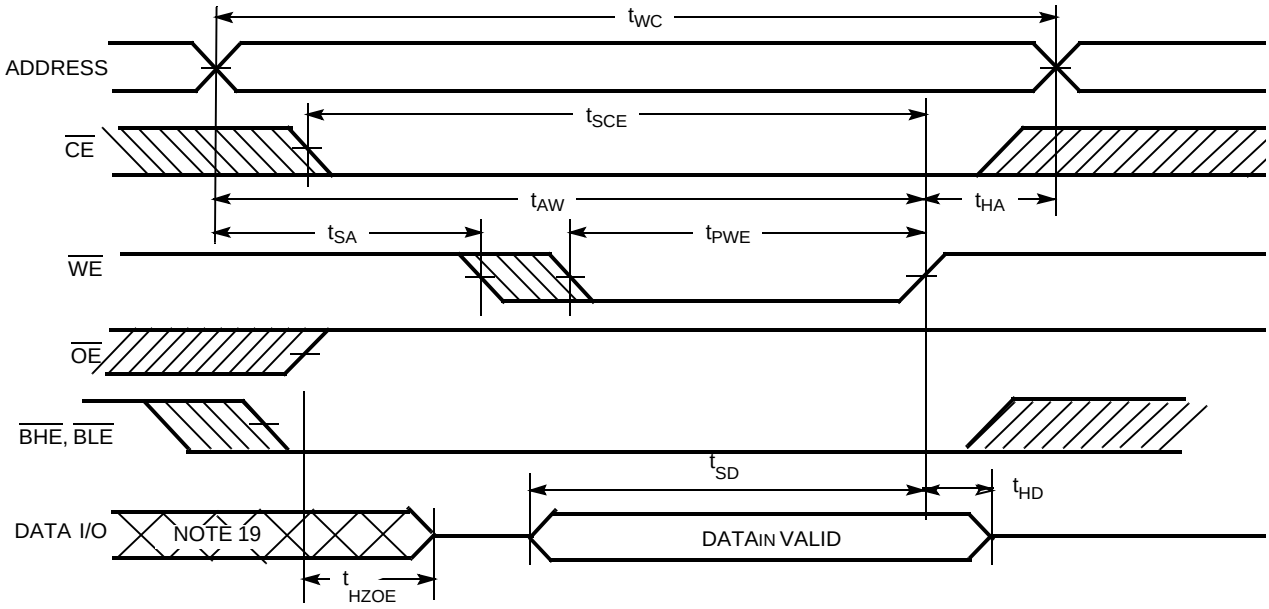
Notes
17. Data I/O is high-impedance if $\overline{OE}$ or $\overline{BHE}$ and/or $\overline{BLE}$ = V_{IH}.
18. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ going HIGH, the output remains in a high-impedance state.

Switching Waveforms (continued)

Write Cycle No. 2 (BLE or BHE Controlled)



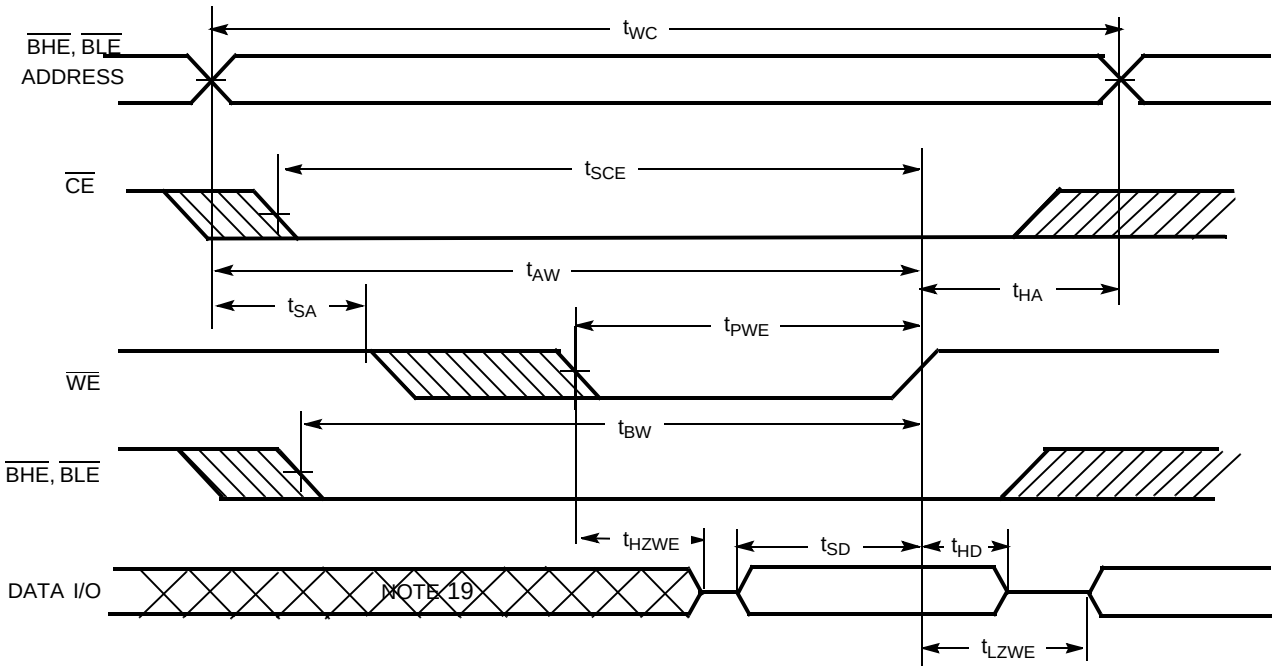
Write Cycle No. 3 (WE Controlled, OE HIGH During Write)[17, 18]



Note
19. During this period the I/Os are in the output state and input signals should not be applied.

Switching Waveforms (continued)

Write Cycle No. 4 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW)



Truth Table

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	$\overline{BLE}$	$\overline{BHE}$	I/O_0–I/O_7	I/O_8–I/O_{15}	Mode	Power
H	X	X	X	X	High-Z	High-Z	Power-down	Standby (I_{SB})
L	L	H	L	L	Data Out	Data Out	Read All Bits	Active (I_{CC})
L	L	H	L	H	Data Out	High-Z	Read Lower Bits Only	Active (I_{CC})
L	L	H	H	L	High-Z	Data Out	Read Upper Bits Only	Active (I_{CC})
L	X	L	L	L	Data In	Data In	Write All Bits	Active (I_{CC})
L	X	L	L	H	Data In	High-Z	Write Lower Bits Only	Active (I_{CC})
L	X	L	H	L	High-Z	Data In	Write Upper Bits Only	Active (I_{CC})
L	H	H	X	X	High-Z	High-Z	Selected, Outputs Disabled	Active (I_{CC})

Ordering Information

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
10	CY7C1041DV33-10BVI	51-85150	48-ball VFBGA	Industrial
	CY7C1041DV33-10BVXI		48-ball VFBGA (Pb-Free)	
	CY7C1041DV33-10VXI	51-85082	44-lead (400-mil) Molded SOJ (Pb-Free)	
	CY7C1041DV33-10ZSXI	51-85087	44-pin TSOP II (Pb-Free)	

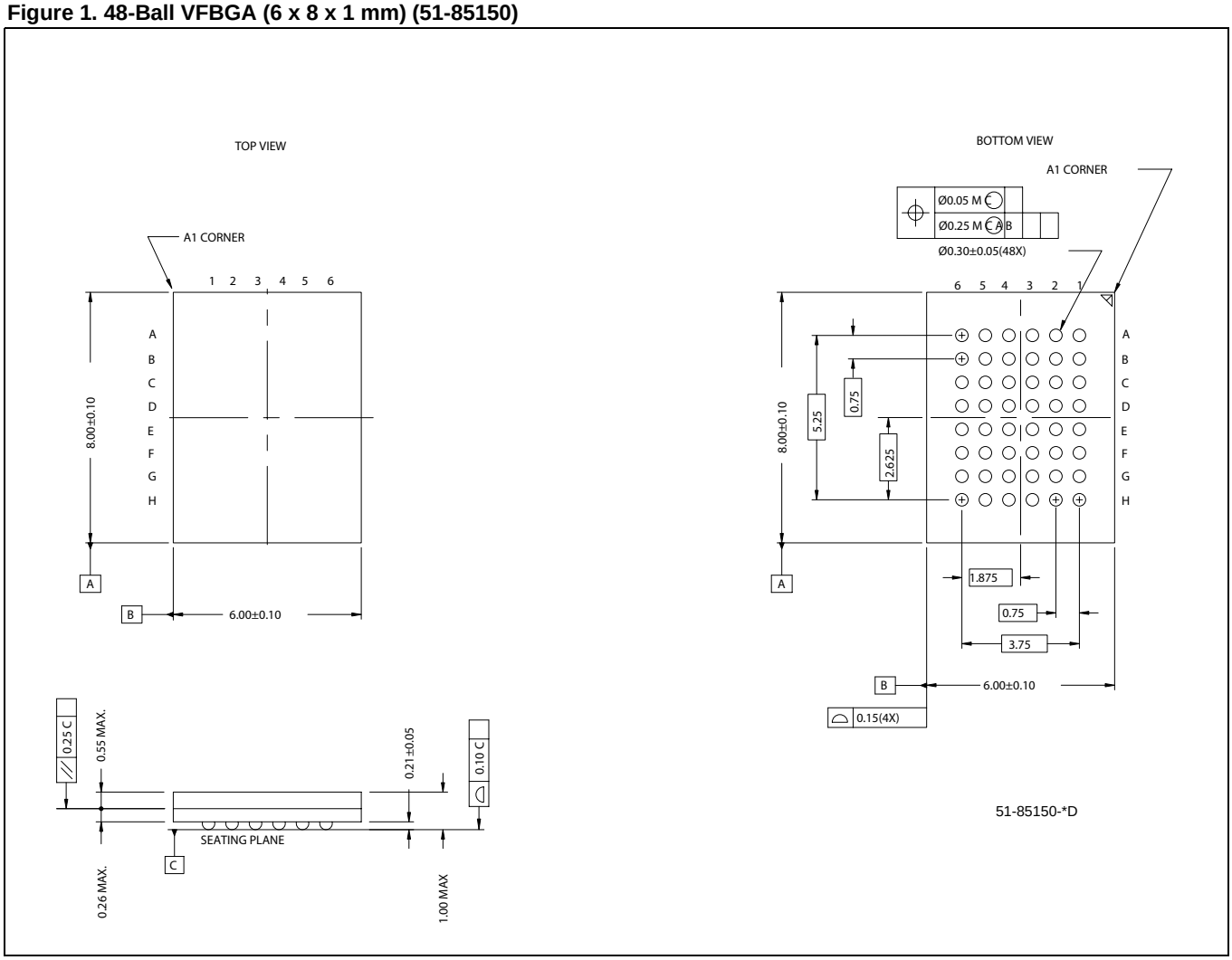
Ordering Information

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
12	CY7C1041DV33-12BVXE	51-85150	48-ball VFBGA (Pb-Free)	Automotive
	CY7C1041DV33-12VXE	51-85082	44-lead (400-mil) Molded SOJ (Pb-Free)	
	CY7C1041DV33-12ZSXE	51-85087	44-pin TSOP II (Pb-Free)	

Please contact your local Cypress sales representative for availability of these parts

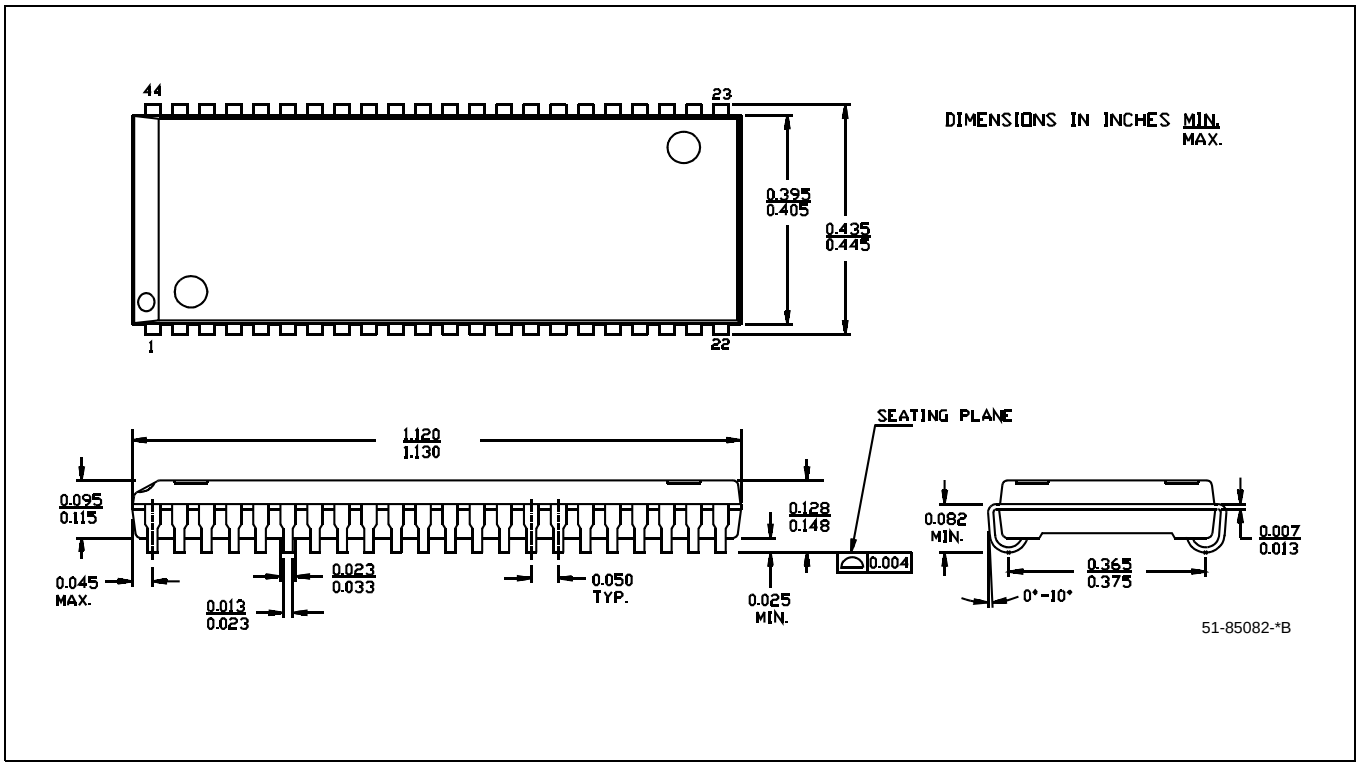
Package Diagrams

Figure 1. 48-Ball VFBGA (6 x 8 x 1 mm) (51-85150)



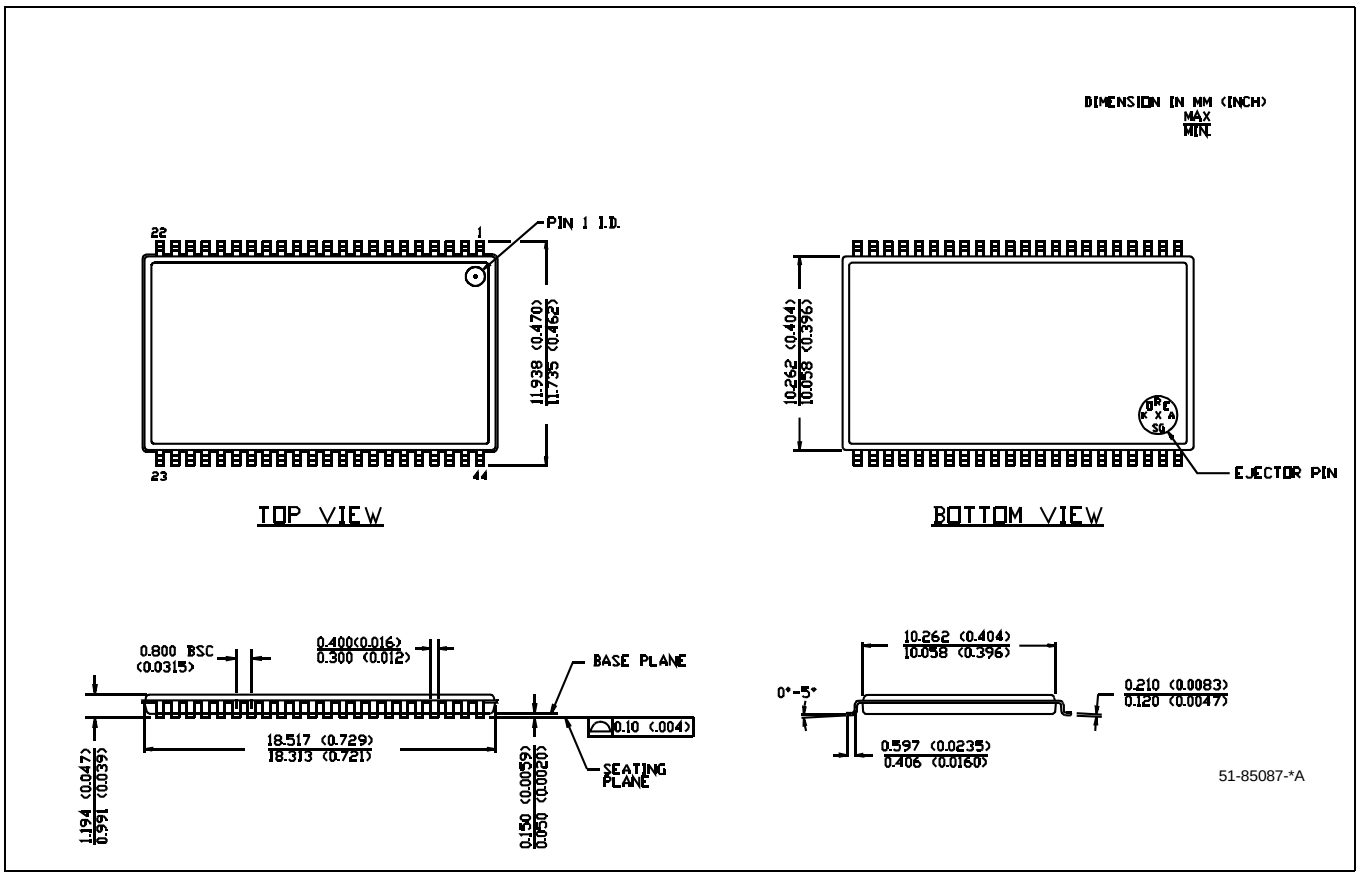
Package Diagrams(continued)

Figure 2. 44-lead (400-mil) Molded SOJ (51-85082)



Package Diagrams(continued)

Figure 3. 44-pin TSOP II (51-85087)



Document History Page

Document Title: CY7C1041DV33 4-Mbit (256K x 16) Static RAM Document Number: 38-05473				
REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	201560	See ECN	SWI	Advance Data sheet for C9 IPP
*A	233729	See ECN	RKF	1.AC, DC parameters are modified as per EROS(Spec # 01-2165) 2.Pb-free offering in the 'Ordering information'
*B	351117	See ECN	PCI	Changed from Advance to Preliminary Removed 15 and 20 ns Speed bin Corrected DC voltage (min) value in maximum ratings section from - 0.5 to - 0.3V Redefined I_{CC} values for Com'l and Ind'l temperature ranges I_{CC} (Com'l): Changed from 100, 80 and 67 mA to 90, 80 and 75 mA for 8, 10 and 12ns speed bins respectively I_{CC} (Ind'l): Changed from 80 and 67 mA to 90 and 85 mA for 10 and 12ns speed bins respectively Added Static Discharge Voltage and latch-up current spec Added $V_{IH(max)}$ spec in Note# 2 Changed Note# 4 on AC Test Loads Changed reference voltage level for measurement of Hi-Z parameters from $\pm$500 mV to $\pm$200 mV Added Data Retention Characteristics/Waveform and footnote # 11, 12 Added Write Cycle (WE Controlled, OE HIGH During Write) Timing Diagram Changed Package Diagram name from 44-pin TSOP II Z44 to 44-pin TSOP II ZS44 and from 44-lead (400-mil) Molded SOJ V34 to 44-lead (400-mil) Molded SOJ V44 Changed part names from Z to ZS in the Ordering Information Table Added 8 ns Product Information Added Lead-Free Ordering Information Shaded Ordering Information Table
*C	446328	See ECN	NXR	Converted from Preliminary to Final Removed -8 speed bin Removed Commercial Operating Range product information Included Automotive Operating Range product information Updated Thermal Resistance table Updated footnote #8 on High-Z parameter measurement Updated the ordering information and replaced Package Name column with Package Diagram in the Ordering Information Table
*D	480177	See ECN	VKN	Added -10BVI product ordering code in the Ordering Information table