



# 76V, APD, Bias Output Stage with Current Monitoring

DS1842

## General Description

The DS1842 integrates the discrete high-voltage components necessary for avalanche photodiode (APD) bias and monitor applications. A switch FET is used in conjunction with an external DC-DC controller to create a boost DC-DC converter. A current clamp limits current through the APD and also features an external shutdown. The device also includes a dual current mirror to monitor the APD current.

## Applications

APD Biasing

GPON Optical Network Unit and Optical Line Transmission

## Features

- ◆ 76V Maximum Boost Voltage
- ◆ Switch FET
- ◆ Current Monitor with a Wide 1 $\mu$ A to 2mA Range, Fast 50ns Time Constant, and 10:1 and 5:1 Ratio
- ◆ 2mA Current Clamp with External Shutdown
- ◆ Multiple External Filtering Options
- ◆ 3mm x 3mm, 14-Pin TDFN Package with Exposed Pad

## Ordering Information

| PART        | TEMP RANGE     | PIN-PACKAGE |
|-------------|----------------|-------------|
| DS1842N+    | -40°C to +85°C | 14 TDFN-EP* |
| DS1842N+T&R | -40°C to +85°C | 14 TDFN-EP* |

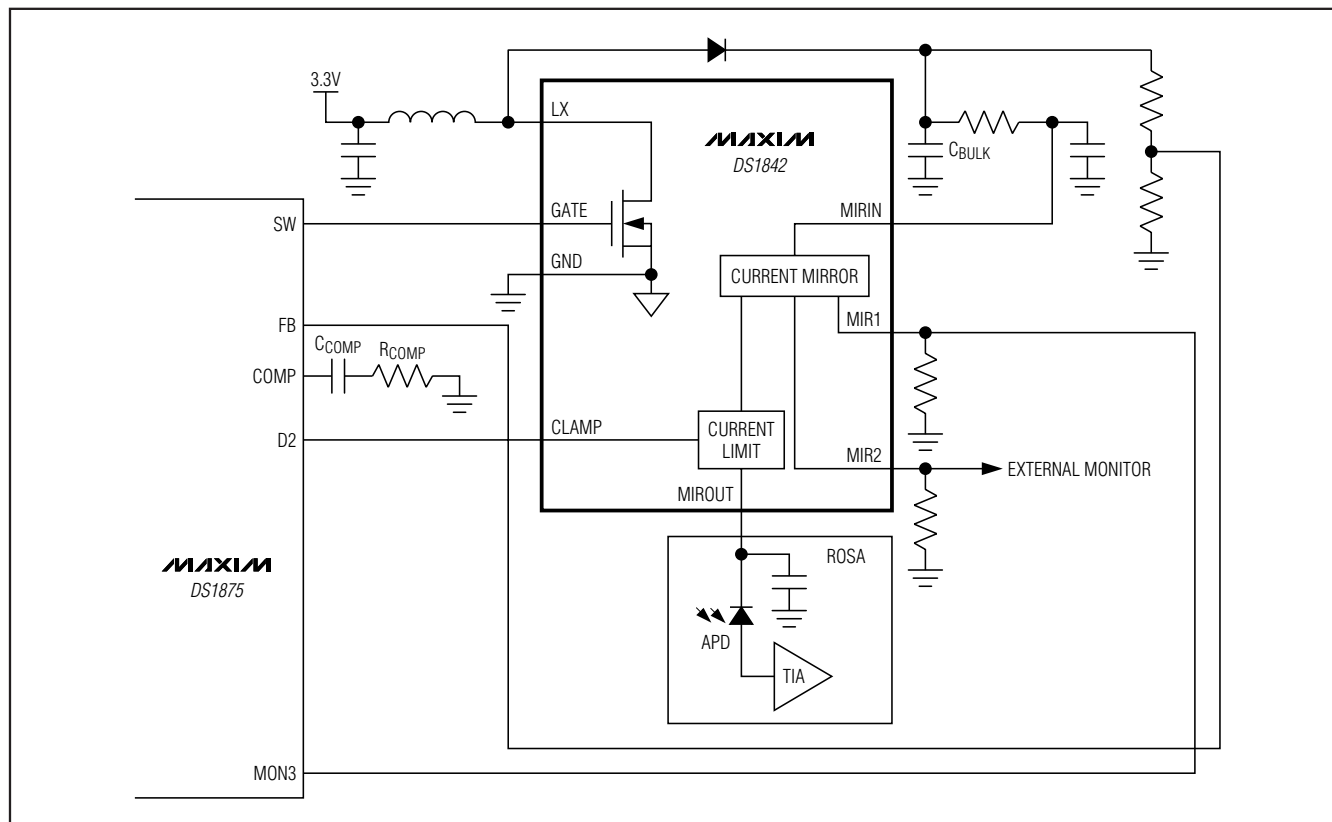
+ Denotes a lead(Pb)-free/RoHS-compliant package.

T&R = Tape and reel.

\*EP = Exposed pad.

Pin Configuration appears at end of data sheet.

## Typical Application Circuit



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## ABSOLUTE MAXIMUM RATINGS

Voltage Range on GATE and CLAMP  
Relative to GND ..... -0.3V to +12V  
Voltage Range on MIRIN, MIROUT,  
MIR1, and MIR2 Relative to GND ..... -0.3V to +80V  
Voltage Range on LX Relative to GND ..... -0.3V to +85V

Continuous Power Dissipation ( $T_A = +70^\circ\text{C}$ )  
TDFN (derate 24.4mW/ $^\circ\text{C}$  above  $+70^\circ\text{C}$ ) ..... 1951.2mW  
Operating Junction Temperature Range .....  $-40^\circ\text{C}$  to  $+150^\circ\text{C}$   
Storage Temperature Range .....  $-55^\circ\text{C}$  to  $+135^\circ\text{C}$   
Lead Temperature (soldering, 10s) .....  $+300^\circ\text{C}$   
Soldering Temperature (reflow) .....  $+260^\circ\text{C}$

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## PACKAGE THERMAL CHARACTERISTICS (Note 1)

TDFN

Junction-to-Ambient Thermal Resistance ( $\theta_{JA}$ ) .....  $41^\circ\text{C}/\text{W}$   
Junction-to-Case Thermal Resistance ( $\theta_{JC}$ ) .....  $8^\circ\text{C}/\text{W}$

**Note 1:** Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to [www.maxim-ic.com/thermal-tutorial](http://www.maxim-ic.com/thermal-tutorial).

## ELECTRICAL CHARACTERISTICS

( $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ , unless otherwise noted.)

| PARAMETER                      | SYMBOL       | CONDITIONS                          | MIN   | TYP   | MAX   | UNITS            |
|--------------------------------|--------------|-------------------------------------|-------|-------|-------|------------------|
| Switching Frequency            | $f_{SW}$     |                                     | 0     |       | 1.2   | MHz              |
| FET Capacitance                | $C_{GATE}$   | $V_{GS} = 0V, V_{DS} = 25V$         |       | 40    |       | pF               |
|                                | $C_{LX}$     | $f_{SW} = 1MHz$                     |       | 90    |       |                  |
| FET Gate Resistance            | $R_G$        |                                     |       | 22    |       | $\Omega$         |
| FET On-Resistance              | $R_{DS(on)}$ | $V_{GS} = 3V, I_D = 170mA$          |       | 4.6   | 10    | $\Omega$         |
|                                |              | $V_{GS} = 10V, I_D = 170mA$         |       | 3.7   | 8     |                  |
| GATE Voltage                   | $V_{GS}$     |                                     | 0     |       | 11    | V                |
| Switching Current              | $I_{LX}$     | Duty cycle = 10%, $f_{SW} = 100kHz$ |       |       | 680   | mA               |
| LX Voltage                     | $V_{LX}$     |                                     |       |       | 80    | V                |
| LX Leakage                     | $I_{L(LX)}$  | $V_{GATE} = 0V, V_{LX} = 76V$       | -1    |       | +1    | $\mu A$          |
| CLAMP Voltage                  | $V_{CLAMP}$  |                                     | 0     |       | 11    | V                |
| CLAMP Threshold                | $V_{CLT}$    |                                     | 2     | 4     | 7     | V                |
| Maximum MIROUT Current         | $I_{MIROUT}$ | CLAMP = low                         | 1.75  | 2.6   | 4     | mA               |
|                                |              | CLAMP = high                        |       |       | 10    | $\mu A$          |
| MIR1 to MIROUT Ratio           | $K_{MIR1}$   | $I_{MIROUT} = 1mA$                  | 0.095 | 0.100 | 0.105 | A/A              |
|                                |              | $I_{MIROUT} = 1\mu A$               | 0.094 | 0.100 | 0.106 |                  |
|                                |              | $15V < V_{MIRIN} < 76V$             |       |       |       |                  |
| MIR2 to MIROUT Ratio           | $K_{MIR2}$   | $I_{MIROUT} = 1mA$                  | 0.190 | 0.200 | 0.210 | A/A              |
|                                |              | $I_{MIROUT} = 1\mu A$               | 0.188 | 0.200 | 0.212 |                  |
|                                |              | $15V < V_{MIRIN} < 76V$             |       |       |       |                  |
| MIR1, MIR2 Rise Time (20%/80%) | $t_{RC}$     | (Note 2)                            |       | 30    |       | ns               |
| Shutdown Temperature           | $T_{SHDN}$   | (Note 3)                            |       | +150  |       | $^\circ\text{C}$ |
| Leakage on GATE and CLAMP      | $I_{IL}$     |                                     | -1    |       | +1    | $\mu A$          |

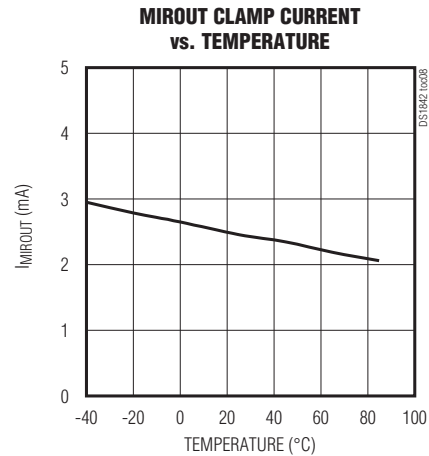
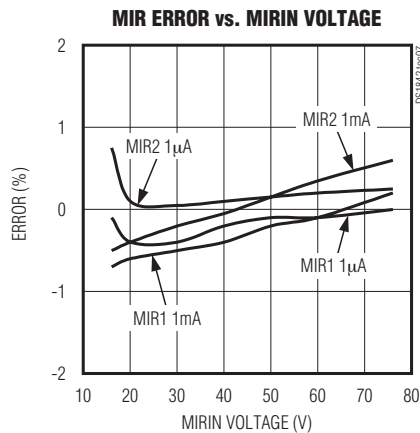
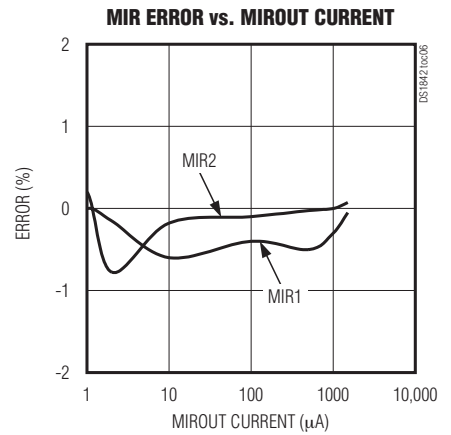
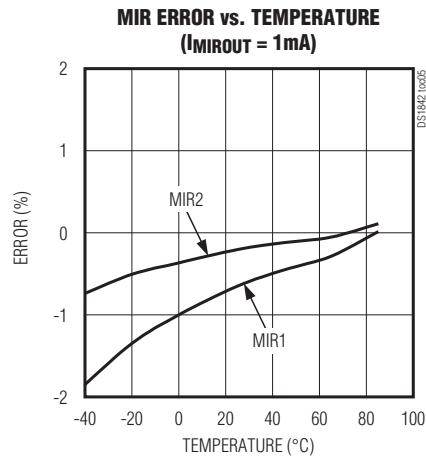
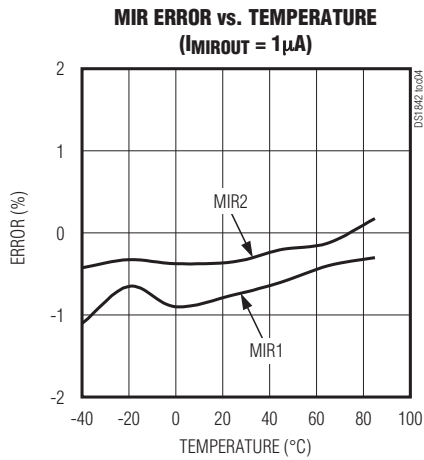
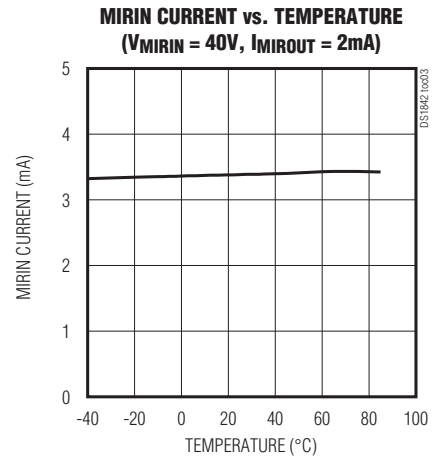
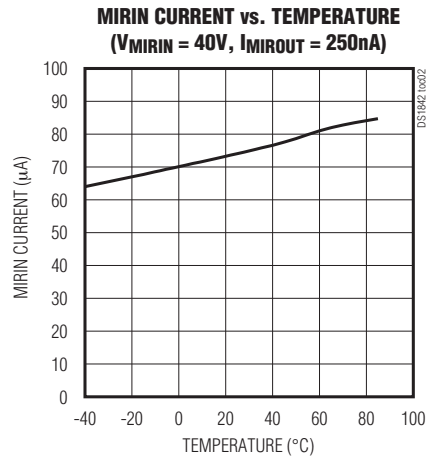
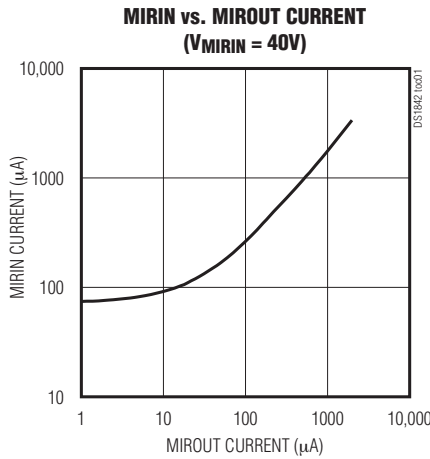
**Note 2:** Rising MIROUT transition from  $10\mu A$  to  $1mA$ ;  $V_{MIRIN} = 40V$ ,  $2.5k\Omega$  load.

**Note 3:** Guaranteed by design; not production tested.

# 76V, APD, Bias Output Stage with Current Monitoring

## Typical Operating Characteristics

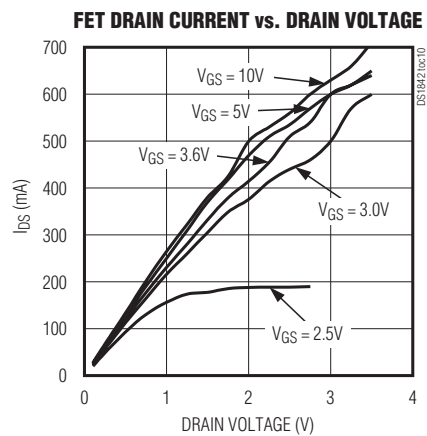
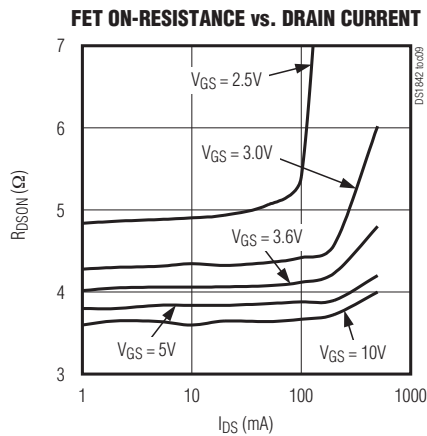
( $T_A = +25^\circ\text{C}$ , unless otherwise noted.)



# 76V, APD, Bias Output Stage with Current Monitoring

## Typical Operating Characteristics (continued)

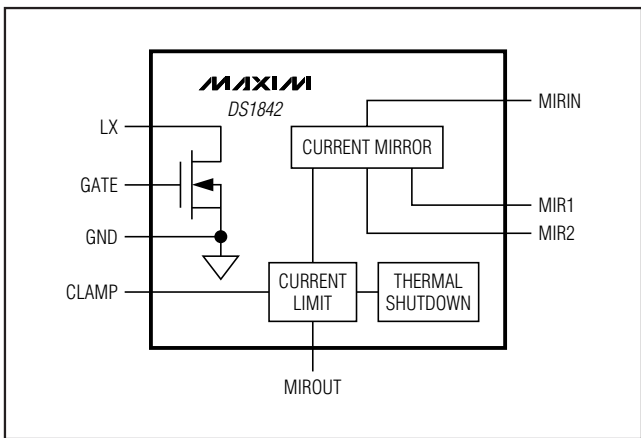
(T<sub>A</sub> = +25°C, unless otherwise noted.)



## Pin Description

| PIN     | NAME   | FUNCTION                                                                   |
|---------|--------|----------------------------------------------------------------------------|
| 1       | MIR1   | Current Mirror Monitor Output, 10:1 Ratio                                  |
| 2       | MIR2   | Current Mirror Monitor Output, 5:1 Ratio                                   |
| 3       | N.C.   | No Connection. Can be connected to GND for compatibility with the DS1842A. |
| 4, 9–12 | N.C.   | No Connection. Not internally connected.                                   |
| 5       | CLAMP  | Clamp Input. Disables the current mirror output (MIROUT).                  |
| 6       | GATE   | FET Gate Connection                                                        |
| 7       | GND    | Ground                                                                     |
| 8       | LX     | FET Drain Connection. Connect to switching inductor.                       |
| 13      | MIRIN  | Current Mirror Input                                                       |
| 14      | MIROUT | Current Mirror Output. Connect to APD bias pin.                            |
| —       | EP     | Exposed Pad. Connect to ground.                                            |

## Block Diagram



## 76V, APD, Bias Output Stage with Current Monitoring

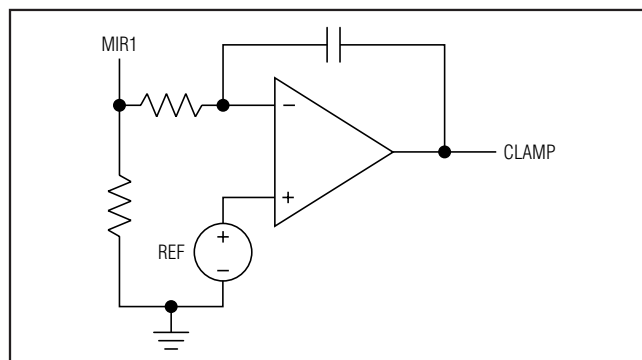


Figure 1. Current Clamp from Current Feedback

### Detailed Description

The DS1842 contains discrete high-voltage components required to create an APD bias voltage and to monitor the APD bias current. The device's mirror outputs are a current that is a precise ratio of the output current across a large dynamic range. The mirror response time is fast enough to comply with GPON Rx burst-mode monitoring requirements. The device has a built-in current-limiting feature to protect APDs. The APD current can also be shut down by CLAMP or thermal shutdown. The internal FET is used in conjunction with a DC-DC boost controller to precisely create the APD bias voltage.

#### Current Mirror

The DS1842 has two current mirror outputs. One is a 10:1 mirror connected at MIR1, and the other is a 5:1 mirror connected to MIR2.

The mirror output is typically connected to an ADC using a resistor to convert the mirrored current into a voltage. The resistor to ground should be selected such that the maximum full-scale voltage of the ADC is reached when the maximum mirrored current is reached. For example, if the maximum monitored current through the APD is 2mA with a 1V ADC full scale,

and the 10:1 mirror is used, then the correct resistor is approximately 5kΩ. If both MIR1 and MIR2 are connected together, the correct resistor is 1.6kΩ.

The mirror response time is dominated by the amount of capacitance placed on the output. For burst-mode Rx systems where the fastest response times are required (approximately a 50ns time constant), a 3.3pF capacitor and external op amp should be used to buffer the signal sent to the ADC. For continuous mode applications, a 10nF capacitor is all that is required on the output.

#### Current Clamp

The DS1842 has a current clamping circuit to protect the APD by limiting the amount of current from MIROUT. There are three methods of current clamping available.

##### 1) Internally Defined Current Limit

The device's current clamp circuit automatically clamps the current when it exceeds ICLAMP.

##### 2) External Shutdown Signal

The CLAMP pin can completely shut down the current from MIROUT. The CLAMP pin is active high.

##### 3) Precise Level Set by External Feedback Circuit

A feedback circuit is used to control the level applied to the CLAMP pin. Figure 1 shows an example feedback circuit.

#### Thermal Shutdown

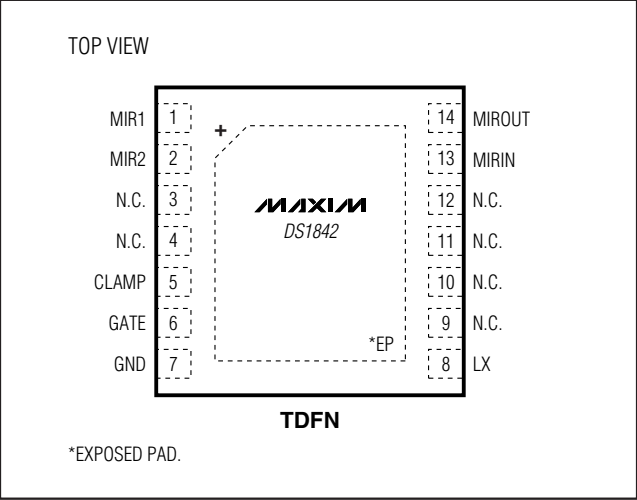
As a safety feature, the DS1842 has a thermal-shutdown circuit that turns off the MIROUT and MIRIN currents when the internal die temperature exceeds TSHDN. These currents resume after the device has cooled.

#### Switch FET and Diode

The DS1842 switching FET is designed to complement the DS1875 controller's built-in DC-DC boost controller. Other DC-DC converters are also compatible, including the MAX1932. APD biasing of 16V to 76V can be achieved using the DS1842.

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## Pin Configuration



## Package Information

For the latest package outline information and land patterns (footprints), go to [www.maxim-ic.com/packages](http://www.maxim-ic.com/packages). Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

| PACKAGE TYPE | PACKAGE CODE | OUTLINE NO.             | LAND PATTERN NO.        |
|--------------|--------------|-------------------------|-------------------------|
| 14 TDFN-EP   | T1433+2      | <a href="#">21-0137</a> | <a href="#">90-0063</a> |

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## Revision History

| REVISION NUMBER | REVISION DATE | DESCRIPTION                                                                                                                                                                                              | PAGES CHANGED |
|-----------------|---------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------|
| 0               | 4/09          | Initial release                                                                                                                                                                                          | —             |
| 1               | 3/11          | Updated the <i>Absolute Maximum Ratings</i> section; added the <i>Package Thermal Characteristics</i> section; changed pin 3 from GND to N.C. in the <i>Pin Description</i> and <i>Pin Configuration</i> | 2, 4, 6       |

DS1842

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