

40A, 100V, 0.040 Ohm, Logic Level N-Channel Power MOSFETs

These N-Channel enhancement mode power MOSFETs are manufactured using the latest manufacturing process technology. This process, which uses feature sizes approaching those of LSI integrated circuits gives optimum utilization of silicon, resulting in outstanding performance. They were designed for use in applications such as switching regulators, switching converters, motor drivers and relay drivers. These transistors can be operated directly from integrated circuits.

Formerly developmental type TA49163.

Ordering Information

PART NUMBER	PACKAGE	BRAND
RFG40N10LE	TO-247	FG40N10L
RFP40N10LE	TO-220AB	FP40N10L
RF1S40N10LESM	TO-263AB	F40N10LE

NOTE: When ordering, use the entire part number. Add the suffix, 9A, to obtain the TO-263AB variant in tape and reel, i.e. RF1S40N10LESM9A.

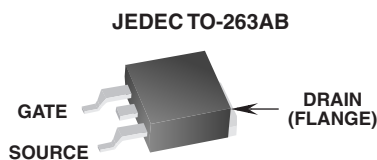
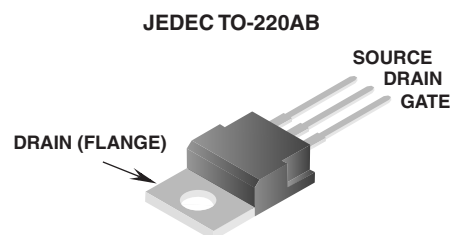
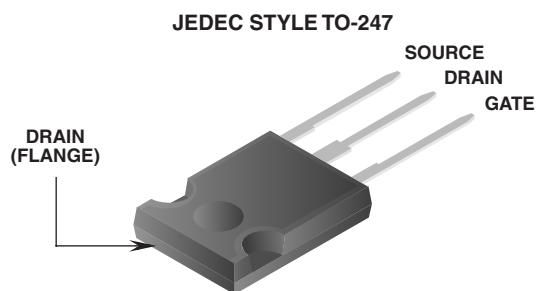
Features

- 40A, 100V
- $r_{DS(ON)} = 0.040\Omega$
- Temperature Compensating PSPICE® Model
- Peak Current vs Pulse Width Curve
- UIS Rating Curve
- 175°C Operating Temperature
- Related Literature
 - TB334 "Guidelines for Soldering Surface Mount Components to PC Boards"

Symbol



Packaging



RFG40N10LE, RFP40N10LE, RF1S40N10LESM

Absolute Maximum Ratings $T_C = 25^{\circ}\text{C}$, Unless Otherwise Specified

	RFG40N10LE, RFP40N10LE, RF1S40N10LESM	UNITS
Drain to Source Breakdown Voltage (Note 1)	V_{DSS}	100
Drain to Gate Voltage ($R_{GS} = 20k\Omega$) (Note 1)	V_{DGR}	100
Gate to Source Voltage (Note 4)	V_{GS}	± 10
Continuous Drain Current	I_D	40
Pulsed Drain Current (Note 3)	I_{DM}	Refer to Peak Current Curve
Single Pulse Avalanche Energy Rating	E_{AS}	Refer to UIS Curve
Power Dissipation (Figure 1)	P_D	150
Derate Above 25°C		1.00
Operating and Storage Temperature	T_J, T_{STG}	-55 to 175
Maximum Temperature for Soldering		
Leads at 0.063in (1.6mm) from Case for 10s.	T_L	300
Package Body for 10s, See Techbrief 334	T_{pkg}	260

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. $T_J = 25^{\circ}\text{C}$ to 150°C .

Electrical Specifications $T_C = 25^{\circ}\text{C}$, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNITS
Drain to Source Breakdown Voltage	BV_{DSS}	$I_D = 250\mu A$, $V_{GS} = 0V$ (Figure 13)		100	-	-	V
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}$, $I_D = 250\mu A$ (Figure 12)		1	-	3	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 95V$, $V_{GS} = 0V$		-	-	1	μA
		$V_{DS} = 90V$, $V_{GS} = 0V$, $T_C = 150^{\circ}C$		-	-	250	μA
Gate to Source Leakage Current	I_{GSS}	$V_{GS} = \pm 10V$		-	-	10	μA
Drain to Source On Resistance (Note 2)	$r_{DS(ON)}$	$I_D = 40A$, $V_{GS} = 5V$		-	-	0.040	Ω
Turn-On Time	t_{ON}	$V_{DD} = 50V$, $I_D = 40A$, $R_L = 1.25\Omega$, $V_{GS} = 5V$, $R_{GS} = 2.5\Omega$ (Figures 10, 18, 19)		-	-	200	ns
Turn-On Delay Time	$t_{d(ON)}$			-	22	-	ns
Rise Time	t_r			-	140	-	ns
Turn-Off Delay Time	$t_{d(OFF)}$			-	70	-	ns
Fall Time	t_f			-	65	-	ns
Turn-Off Time	t_{OFF}			-	-	165	ns
Total Gate Charge	$Q_{g(TOT)}$	$V_{GS} = 0V$ to $10V$	$V_{DD} = 80V$, $I_D = 40A$, $R_L = 2.0\Omega$ (Figures 20, 21)	-	145	180	nC
Gate Charge at 5V	$Q_{g(5)}$	$V_{GS} = 0V$ to $5V$		-	85	105	nC
Threshold Gate Charge	$Q_{g(TH)}$	$V_{GS} = 0V$ to $1V$		-	3	4	nC
Input Capacitance	C_{ISS}	$V_{DS} = 25V$, $V_{GS} = 0V$, $f = 1MHz$ (Figure 14)		-	3000	-	pF
Output Capacitance	C_{OSS}			-	500	-	pF
Reverse Transfer Capacitance	C_{RSS}			-	200	-	pF
Thermal Resistance Junction-to-Case	$R_{\theta JC}$	All Packages		-	-	1.0	$^{\circ}C/W$
Thermal Resistance Junction-to-Ambient	$R_{\theta JA}$	TO-247		-	-	30	$^{\circ}C/W$
		TO-220AB and TO-263AB		-	-	80	$^{\circ}C/W$

Source to Drain Diode Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Source to Drain Diode Voltage	V_{SD}	$I_{SD} = 40\text{A}$	-	-	1.5	V
Diode Reverse Recovery Time	t_{rr}	$I_{SD} = 40\text{A}$, $dI_{SD}/dt = 100\text{A}/\mu\text{s}$	-	-	205	ns

NOTES:

2. Pulse test: pulse width $\leq 80\mu\text{s}$, duty cycle $\leq 2\%$.
3. Repetitive rating: pulse width limited by Max junction temperature. See Transient Thermal Impedance curve (Figure 3).

Typical Performance Curves Unless Otherwise Specified

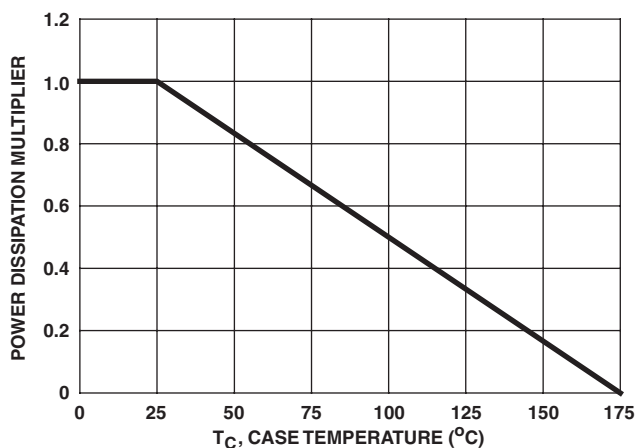


FIGURE 1. NORMALIZED POWER DISSIPATION vs CASE TEMPERATURE

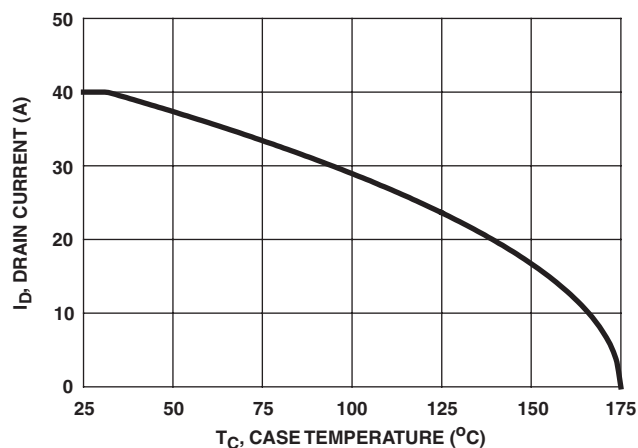


FIGURE 2. MAXIMUM CONTINUOUS DRAIN CURRENT vs CASE TEMPERATURE

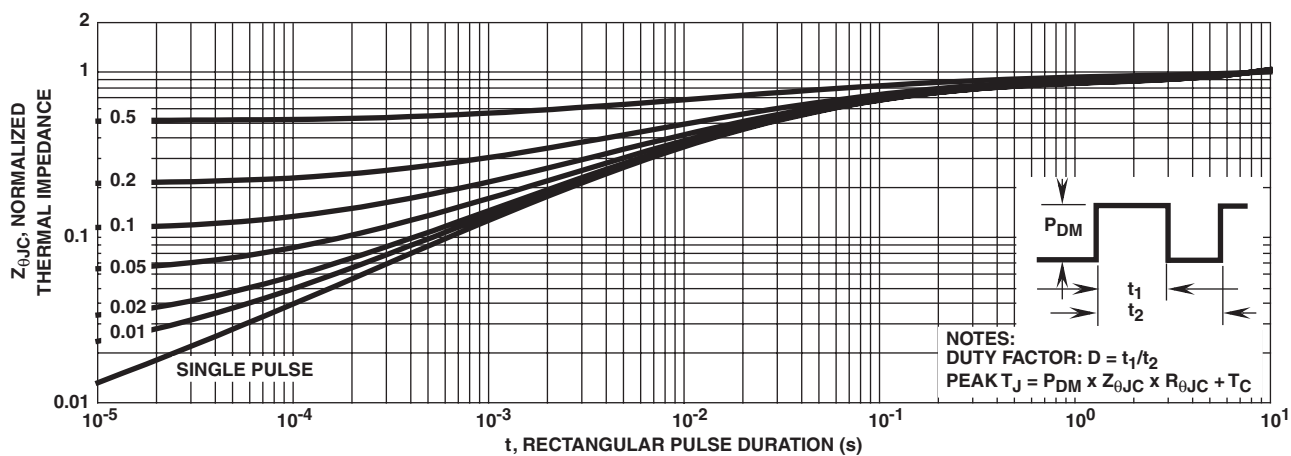


FIGURE 3. NORMALIZED MAXIMUM TRANSIENT THERMAL IMPEDANCE

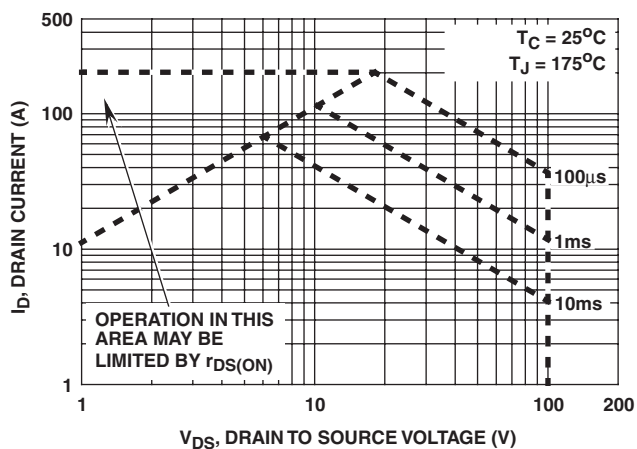


FIGURE 4. FORWARD BIAS SAFE OPERATING AREA

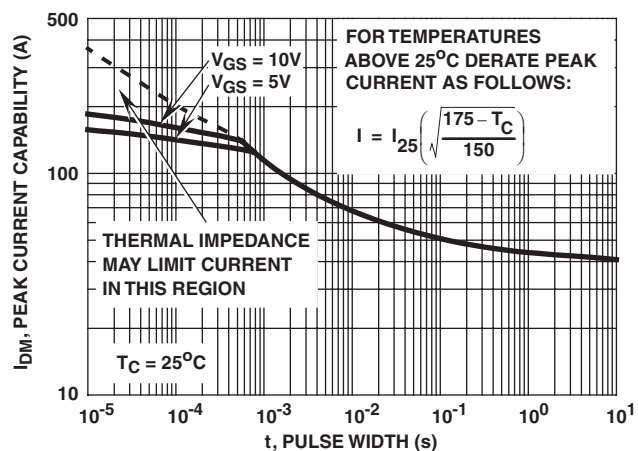
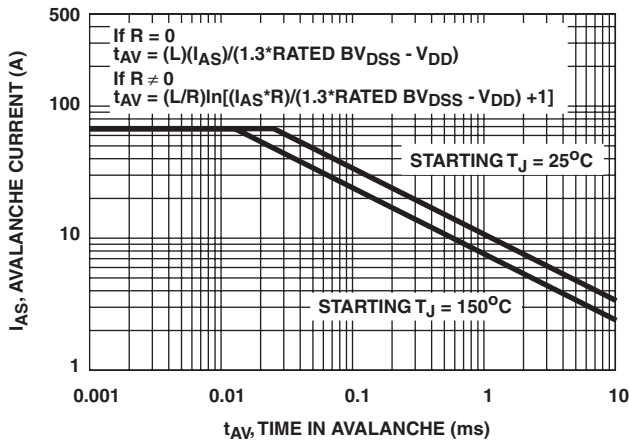


FIGURE 5. PEAK CURRENT CAPABILITY

Typical Performance Curves Unless Otherwise Specified (Continued)



NOTE: Refer to Fairchild Application Notes AN9321 and AN9322.

FIGURE 6. UNCLAMPED INDUCTIVE SWITCHING

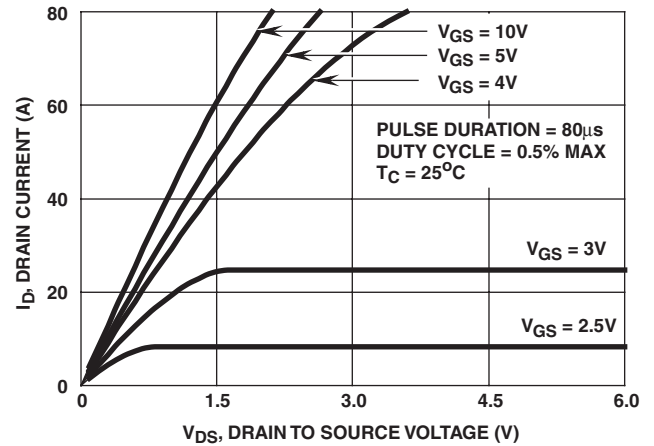


FIGURE 7. SATURATION CHARACTERISTICS

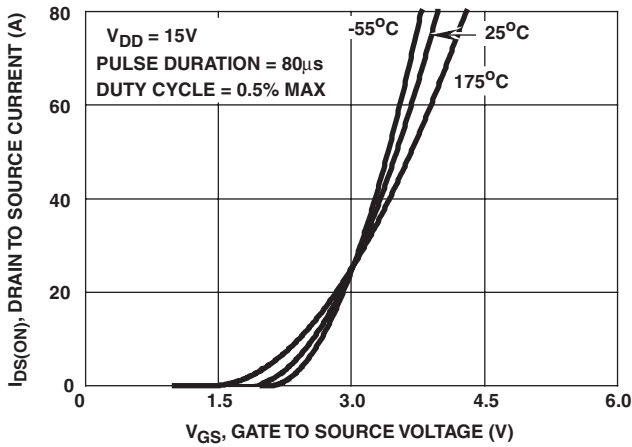


FIGURE 8. TRANSFER CHARACTERISTICS

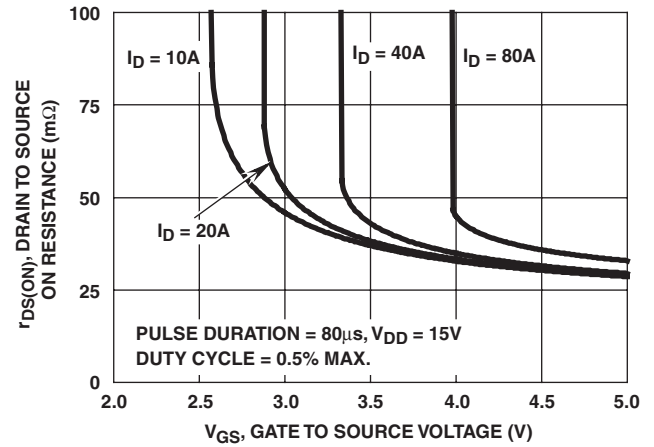


FIGURE 9. DRAIN TO SOURCE ON RESISTANCE vs GATE VOLTAGE AND DRAIN CURRENT

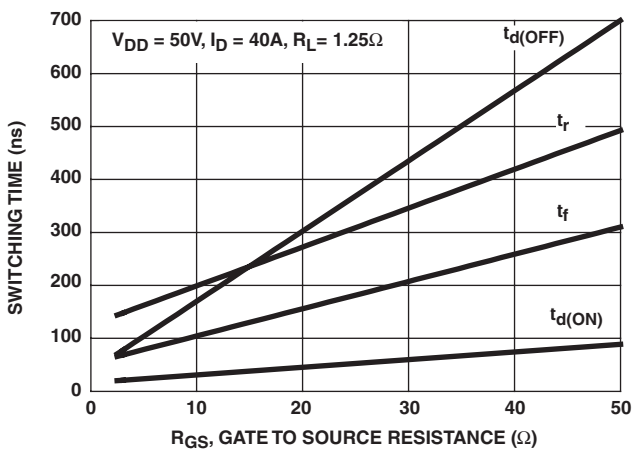


FIGURE 10. SWITCHING TIME vs GATE RESISTANCE

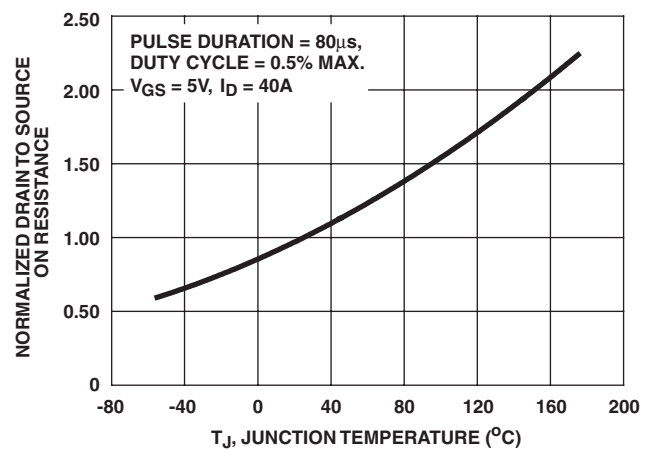


FIGURE 11. NORMALIZED DRAIN TO SOURCE ON RESISTANCE vs JUNCTION TEMPERATURE

Typical Performance Curves Unless Otherwise Specified (Continued)

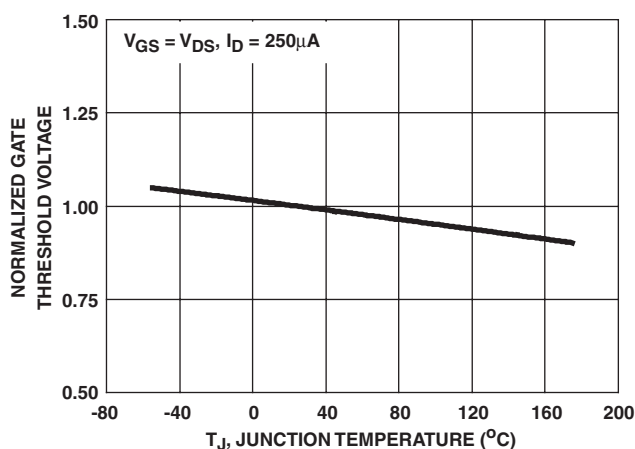


FIGURE 12. NORMALIZED GATE THRESHOLD VOLTAGE vs JUNCTION TEMPERATURE

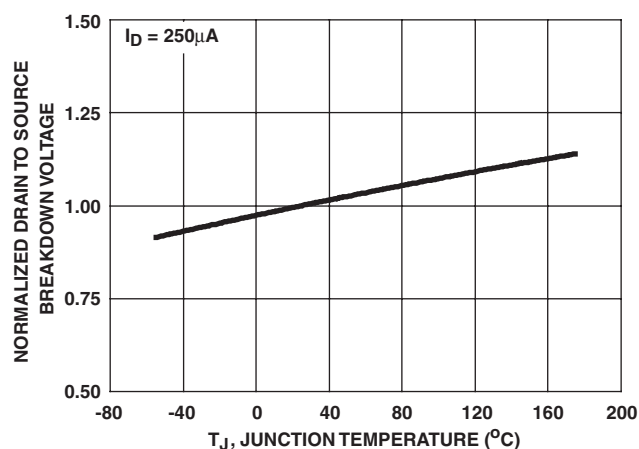


FIGURE 13. NORMALIZED DRAIN TO SOURCE BREAKDOWN VOLTAGE vs JUNCTION TEMPERATURE

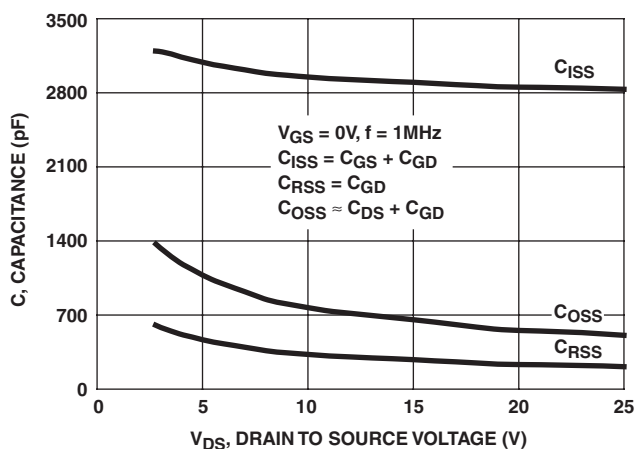
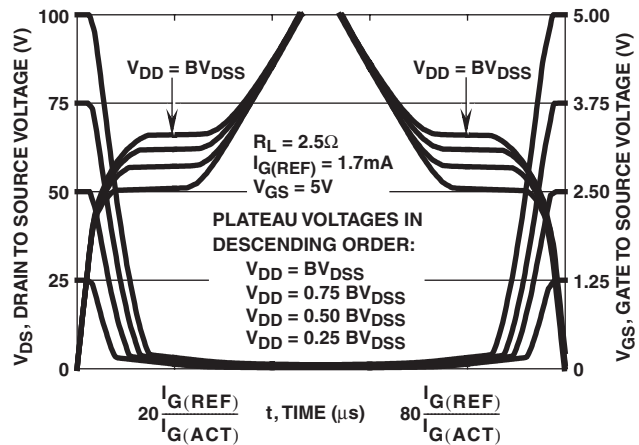


FIGURE 14. CAPACITANCE vs DRAIN TO SOURCE VOLTAGE



NOTE: Refer to Fairchild Application Notes AN7254 and AN7260.

FIGURE 15. SWITCHING WAVEFORMS FOR CONSTANT GATE CURRENT

Test Circuits and Waveforms

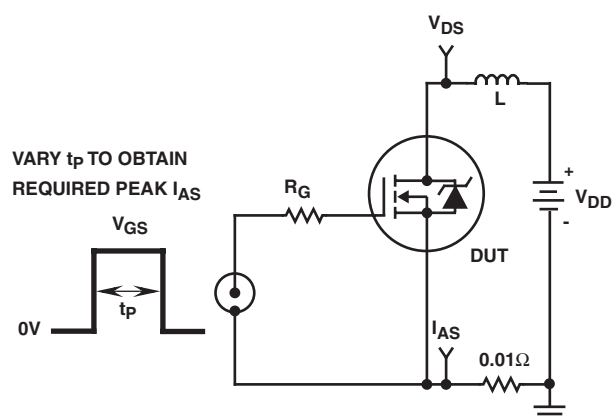


FIGURE 16. UNCLAMPED ENERGY TEST CIRCUIT

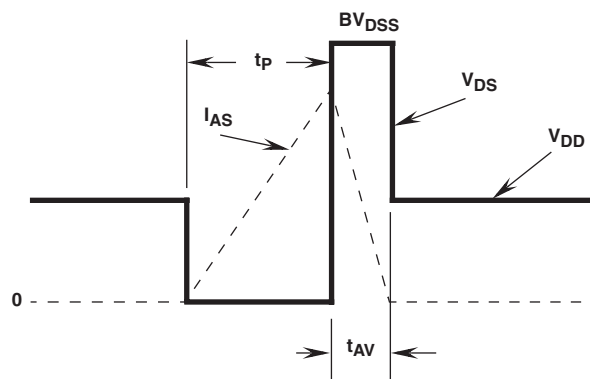


FIGURE 17. UNCLAMPED ENERGY WAVEFORMS

Test Circuits and Waveforms (Continued)

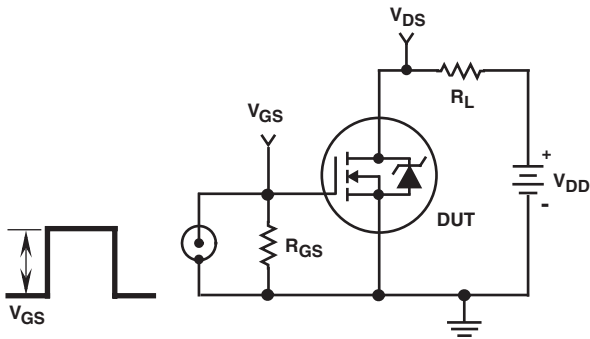


FIGURE 18. SWITCHING TIME TEST CIRCUIT

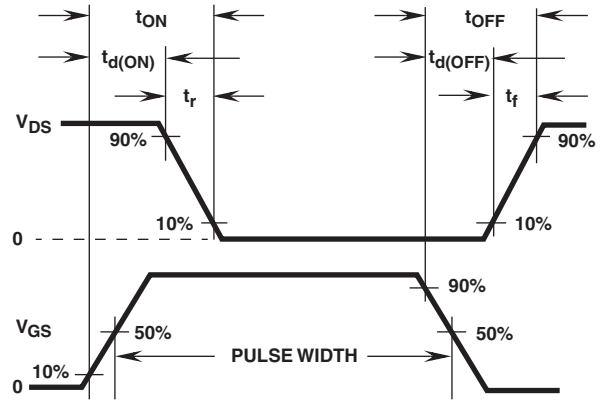


FIGURE 19. RESISTIVE SWITCHING WAVEFORMS

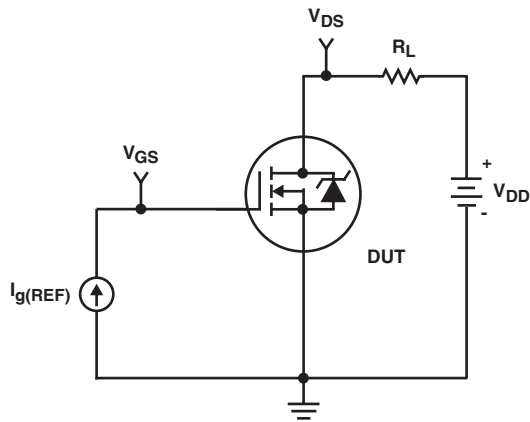


FIGURE 20. GATE CHARGE TEST CIRCUIT

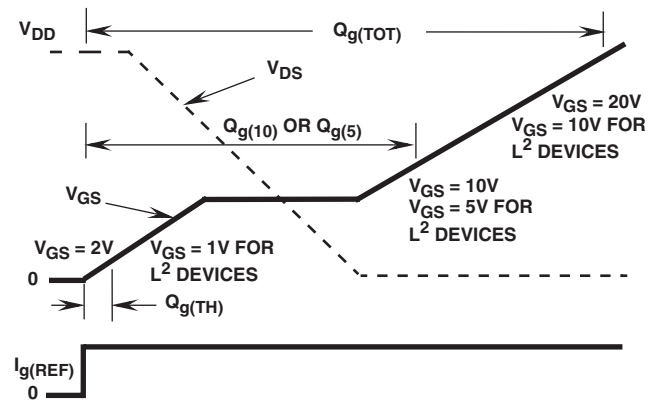


FIGURE 21. GATE CHARGE WAVEFORMS

PSpice Electrical Model

SUBCKT 40N10LE 2 1 3 ; rev 8/15/95

CA 12 8 3.50e-9
CB 15 14 3.50e-9
CIN 6 8 1.70e-9

DBODY 7 5 DBODYMOD
DBREAK 5 11 DBREAKMOD
DPLCAP 10 5 DPLCAPMOD

EBREAK 11 7 17 18 120.7
EDS 14 8 5 8 1
EGS 13 8 6 8 1
ESG 6 10 6 8 1
EVTHRES 6 21 19 8 1
EVTEMP 20 6 18 22 1

IT 8 17 1

LDRAIN 2 5 1.00e-9
LGATE 1 9 5.17e-9
LSOURCE 3 7 2.13e-9

MMED 16 6 8 8 MMEDMOD
MSTRO 16 6 8 8 MSTROMOD
MWEAK 16 21 8 8 MWEAKMOD

RBREAK 17 18 RBREAKMOD 1
RDRAIN 50 16 RDRAINMOD 2.04e-2
RGATE 9 20 2.15
RLDRAIN 2 5 10
RLGATE 1 9 51.7
RLSOURCE 3 7 21.3
RSLC1 5 51 RSLCMOD 1e-6
RSLC2 5 50 1e3
RSOURCE 8 7 RSOURCEMOD 4.85e-3
RVTHRES 22 8 RVTHRESMOD 1
RVTEMP 18 19 RVTEMPMOD 1

S1A 6 12 13 8 S1AMOD
S1B 13 12 13 8 S1BMOD
S2A 6 15 14 13 S2AMOD
S2B 13 15 14 13 S2BMOD

VBAT 22 19 DC 1

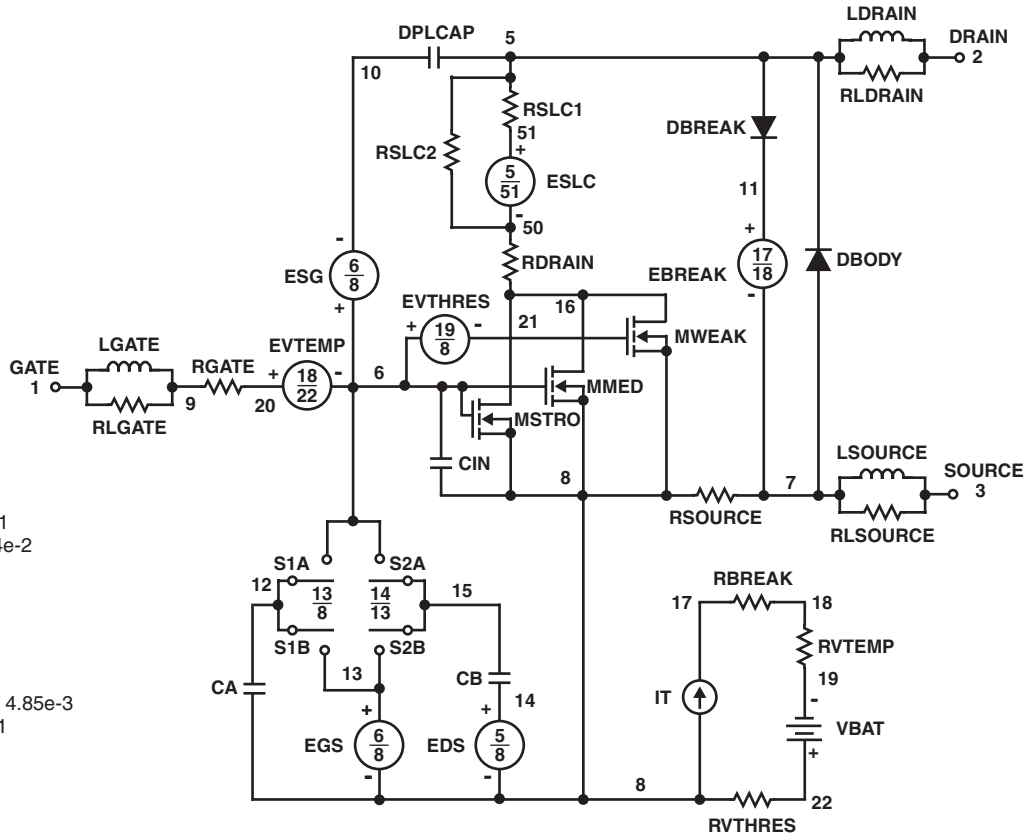
ESLC 51 50 VALUE=({(V(5,51)/ABS(V(5,51)))})*(PWR(V(5,51)/(1e-6*79),3.5)))

.MODEL DBODYMOD D (IS = 1.96e-12 RS = 3.87e-3 TRS1 = 9.93e-4 TRS2 = 4.97e-6 CJO = 1.53e-9 TT = 7.41e-8 M = 0.50)
.MODEL DBREAKMOD D (RS = 3.12e-1 TRS1 = 1.07e-3 TRS2 = 0)
.MODEL DPLCAPMOD D (CJO = 1.97e-9 IS = 1e-30 M = 0.87)
.MODEL MMEDMOD NMOS (VTO = 1.73 KP = 2.80 IS = 1e-30 N = 10 TOX = 1 L = 1u W = 1u RG = 2.15)
.MODEL MSTROMOD NMOS (VTO = 2.04 KP = 80 IS = 1e-30 N = 10 TOX = 1 L = 1u W = 1u)
.MODEL MWEAKMOD NMOS (VTO = 1.50 KP = 0.10 IS = 1e-30 N = 10 TOX = 1 L = 1u W = 1u RG = 21.5 RS = 0.1)
.MODEL RBREAKMOD RES (TC1 = 9.74e-4 TC2 = -3.71e-7)
.MODEL RDRAINMOD RES (TC1 = 9.71e-3 TC2 = 2.90e-5)
.MODEL RSLCMOD RES (TC1 = 2.17e-3 TC2 = 1.27e-6)
.MODEL RSOURCEMOD RES (TC1 = 1e-3 TC2 = 0)
.MODEL RVTHRESMOD RES (TC1 = -2.08e-3 TC2 = -6.82e-6)
.MODEL RVTEMPMOD RES (TC1 = -1.52e-3 TC2 = -1.21e-7)

.MODEL S1AMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -6.00 VOFF = -1.50)
.MODEL S1BMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -1.50 VOFF = -6.00)
.MODEL S2AMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -0.50 VOFF = 0.0)
.MODEL S2BMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = 0.0 VOFF = -0.50)

.ENDS

NOTE: For further discussion of the PSpice model, consult **A New PSpice Sub-Circuit for the Power MOSFET Featuring Global Temperature Options**; IEEE Power Electronics Specialist Conference Records, 1991, written by William J. Hepp and C. Frank Wheatley.



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DenseTrench TM	GTO TM	Power247 TM	SuperSOT TM -6	
DOME TM	HiSeC TM	PowerTrench [®]	SuperSOT TM -8	
EcoSPARK TM	ISOPLANAR TM	QFET TM	SyncFET TM	
E ² CMOS TM	LittleFET TM	QS TM	TinyLogic TM	
EnSigna TM	MicroFET TM	QT Optoelectronics TM	TruTranslation TM	
FACT TM	MicroPak TM	Quiet Series TM	UHC TM	
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