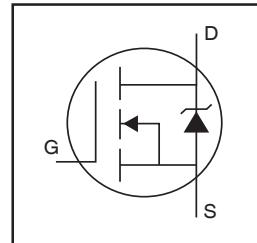


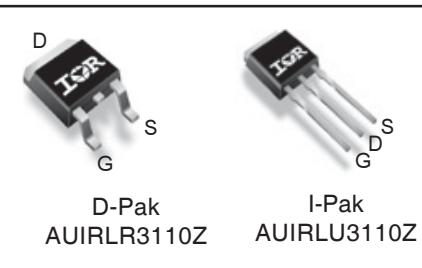
Features

- Advanced Process Technology
- Ultra Low On-Resistance
- Logic Level Gate Drive
- 175°C Operating Temperature
- Fast Switching
- Repetitive Avalanche Allowed up to T_{jmax}
- Lead-Free, RoHS Compliant
- Automotive Qualified *



HEXFET® Power MOSFET

V_{DSS}	100V
$R_{DS(on)}$ typ.	11mΩ
	max. 14mΩ
I_D (Silicon Limited)	63A⑨
I_D (Package Limited)	42A



G	D	S
Gate	Drain	Source

Description

Specifically designed for Automotive applications, this HEXFET® Power MOSFET utilizes the latest processing techniques to achieve extremely low on-resistance per silicon area. Additional features of this design are a 175°C junction operating temperature, fast switching speed and improved repetitive avalanche rating. These features combine to make this design an extremely efficient and reliable device for use in Automotive applications and a wide variety of other applications.

Base part number	Package Type	Standard Pack		Orderable Part Number
		Form	Quantity	
AUIRLR3110Z	D-Pak	Tube	75	AUIRLR3110Z
		Tape and Reel	2000	AUIRLR3110ZTR
		Tape and Reel Left	3000	AUIRLR3110ZTRL
		Tape and Reel Right	3000	AUIRLR3110ZTRR
AUIRLU3110Z	I-Pak	Tube	75	AUIRLU3110Z

Absolute Maximum Ratings

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only; and functional operation of the device at these or any other condition beyond those indicated in the specifications is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions. Ambient temperature (T_A) is 25°C, unless otherwise specified.

	Parameter	Max.	Units
I_D @ $T_C = 25^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10\text{V}$ (Silicon Limited)	63 ⑨	A
I_D @ $T_C = 100^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10\text{V}$ (Silicon Limited)	45 ⑨	
I_D @ $T_C = 25^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10\text{V}$ (Package Limited)	42	
I_{DM}	Pulsed Drain Current ①	250	
P_D @ $T_C = 25^\circ\text{C}$	Power Dissipation	140	W
	Linear Derating Factor	0.95	W/°C
V_{GS}	Gate-to-Source Voltage	±16	V
E_{AS} (Thermally limited)	Single Pulse Avalanche Energy ②	110	mJ
E_{AS} (Tested)	Single Pulse Avalanche Energy Tested Value ⑥	140	
I_{AR}	Avalanche Current ①	See Fig.12a, 12b, 15, 16	
E_{AR}	Repetitive Avalanche Energy ③	mJ	
T_J	Operating Junction and	-55 to + 175	°C
T_{STG}	Storage Temperature Range		
	Reflow Soldering Temperature, for 10 seconds		
	Mounting Torque, 6-32 or M3 screw	300	
		10 lbf·in (1.1N·m)	

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{θJC}$	Junction-to-Case ⑧	—	1.05	°C/W
$R_{θJA}$	Junction-to-Ambient (PCB mount) ⑦	—	40	
$R_{θJA}$	Junction-to-Ambient	—	110	

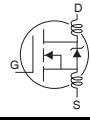
HEXFET® is a registered trademark of International Rectifier.

*Qualification standards can be found at <http://www.irf.com/>

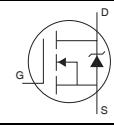
Static Electrical Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(\text{BR})\text{DSS}}$	Drain-to-Source Breakdown Voltage	100	—	—	V	$V_{\text{GS}} = 0\text{V}$, $I_D = 250\mu\text{A}$
$\Delta V_{(\text{BR})\text{DSS}/\Delta T_J}$	Breakdown Voltage Temp. Coefficient	—	0.077	—	V/ $^\circ\text{C}$	Reference to 25°C , $I_D = 1\text{mA}$
$R_{\text{DS}(\text{on})}$	Static Drain-to-Source On-Resistance	—	11	14	$\text{m}\Omega$	$V_{\text{GS}} = 10\text{V}$, $I_D = 38\text{A}$ ③
		—	12	16		$V_{\text{GS}} = 4.5\text{V}$, $I_D = 32\text{A}$ ③
$V_{\text{GS}(\text{th})}$	Gate Threshold Voltage	1.0	—	2.5	V	$V_{\text{DS}} = V_{\text{GS}}$, $I_D = 100\mu\text{A}$
g_{fs}	Forward Transconductance	52	—	—	S	$V_{\text{DS}} = 25\text{V}$, $I_D = 38\text{A}$
I_{DSS}	Drain-to-Source Leakage Current	—	—	20	μA	$V_{\text{DS}} = 100\text{V}$, $V_{\text{GS}} = 0\text{V}$
		—	—	250		$V_{\text{DS}} = 100\text{V}$, $V_{\text{GS}} = 0\text{V}$, $T_J = 125^\circ\text{C}$
I_{GSS}	Gate-to-Source Forward Leakage	—	—	200	nA	$V_{\text{GS}} = 16\text{V}$
	Gate-to-Source Reverse Leakage	—	—	-200		$V_{\text{GS}} = -16\text{V}$

Dynamic Electrical Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

Q_g	Total Gate Charge	—	34	48	nC	$I_D = 38\text{A}$ $V_{\text{DS}} = 50\text{V}$ $V_{\text{GS}} = 4.5\text{V}$ ③
Q_{gs}	Gate-to-Source Charge	—	10	—		
Q_{gd}	Gate-to-Drain ("Miller") Charge	—	15	—		
$t_{\text{d}(\text{on})}$	Turn-On Delay Time	—	24	—		
t_r	Rise Time	—	110	—	ns	$V_{\text{DD}} = 50\text{V}$ $I_D = 38\text{A}$ $R_G = 3.7\Omega$ $V_{\text{GS}} = 4.5\text{V}$ ③
$t_{\text{d}(\text{off})}$	Turn-Off Delay Time	—	33	—		
t_f	Fall Time	—	48	—		
L_D	Internal Drain Inductance	—	4.5	—		
L_S	Internal Source Inductance	—	7.5	—	nH	Between lead, 6mm (0.25in.) from package and center of die contact
C_{iss}	Input Capacitance	—	3980	—		
C_{oss}	Output Capacitance	—	310	—		
C_{rss}	Reverse Transfer Capacitance	—	130	—		
C_{oss}	Output Capacitance	—	1820	—	pF	$V_{\text{GS}} = 0\text{V}$ $V_{\text{DS}} = 25\text{V}$ $f = 1.0\text{MHz}$
C_{oss}	Output Capacitance	—	170	—		$V_{\text{GS}} = 0\text{V}$, $V_{\text{DS}} = 1.0\text{V}$, $f = 1.0\text{MHz}$
$C_{\text{oss eff.}}$	Effective Output Capacitance	—	320	—		$V_{\text{GS}} = 0\text{V}$, $V_{\text{DS}} = 80\text{V}$, $f = 1.0\text{MHz}$
						$V_{\text{GS}} = 0\text{V}$, $V_{\text{DS}} = 0\text{V}$ to 80V ④

Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	63	A	MOSFET symbol showing the integral reverse p-n junction diode.
	Pulsed Source Current (Body Diode) ①	—	—	250		
	V_{SD}	—	—	1.3		$T_J = 25^\circ\text{C}$, $I_S = 38\text{A}$, $V_{\text{GS}} = 0\text{V}$ ③
	t_{rr}	—	34	51		$T_J = 25^\circ\text{C}$, $I_F = 38\text{A}$, $V_{\text{DD}} = 50\text{V}$ $di/dt = 100\text{A}/\mu\text{s}$ ③
Q_{rr}	Reverse Recovery Charge	—	42	63	nC	
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11).
- ② Limited by T_{Jmax} , starting $T_J = 25^\circ\text{C}$, $L = 0.16\text{mH}$, $R_G = 25\Omega$, $I_{\text{AS}} = 38\text{A}$, $V_{\text{GS}} = 10\text{V}$. Part not recommended for use above this value.
- ③ Pulse width $\leq 1.0\text{ms}$; duty cycle $\leq 2\%$.
- ④ $C_{\text{oss eff.}}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS} .
- ⑤ Limited by T_{Jmax} , see Fig.12a, 12b, 15, 16 for typical repetitive avalanche performance.

- ⑥ This value determined from sample failure population. 100% tested to this value in production.
- ⑦ When mounted on 1" square PCB (FR-4 or G-10 Material).
- ⑧ R_θ is measured at T_J approximately 90°C .
- ⑨ Calculated continuous current based on maximum allowable junction temperature. Bond wire current limit is 42A. Note that current limitations arising from heating of the device leads may occur with some lead mounting arrangements.

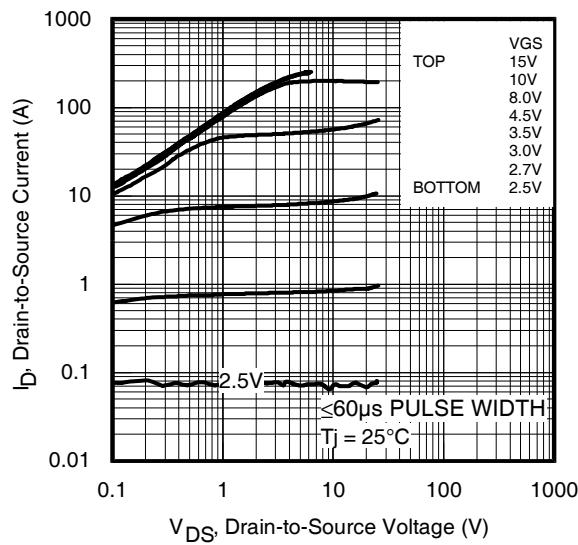


Fig 1. Typical Output Characteristics

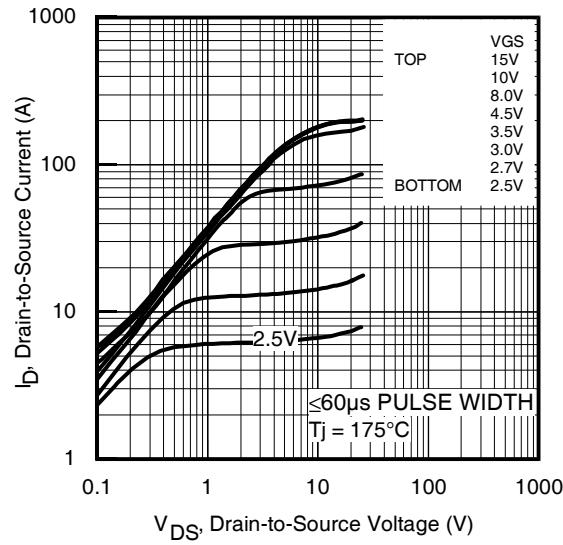


Fig 2. Typical Output Characteristics

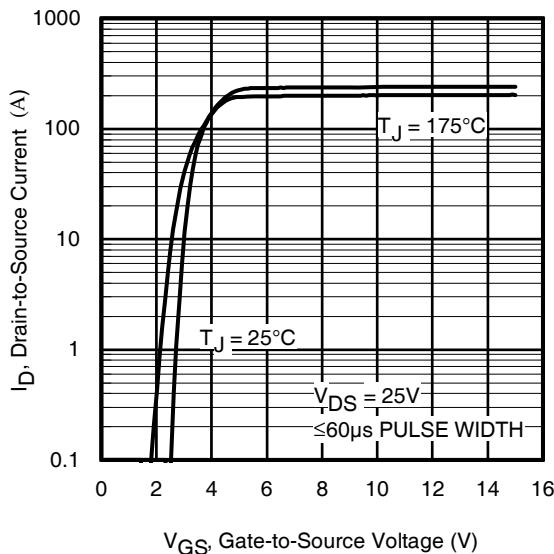


Fig 3. Typical Transfer Characteristics

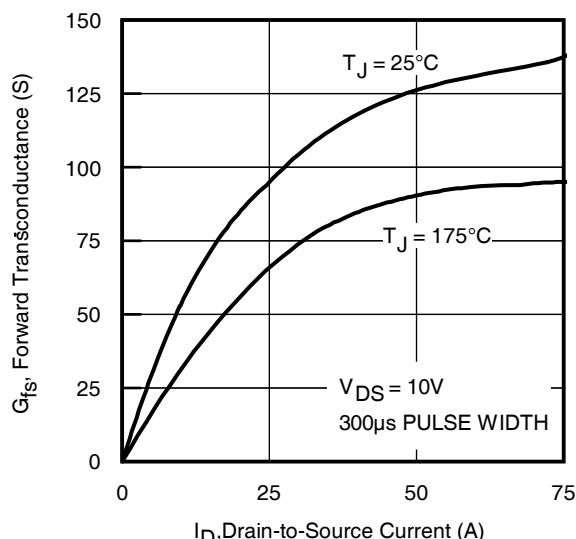


Fig 4. Typical Forward Transconductance vs. Drain Current

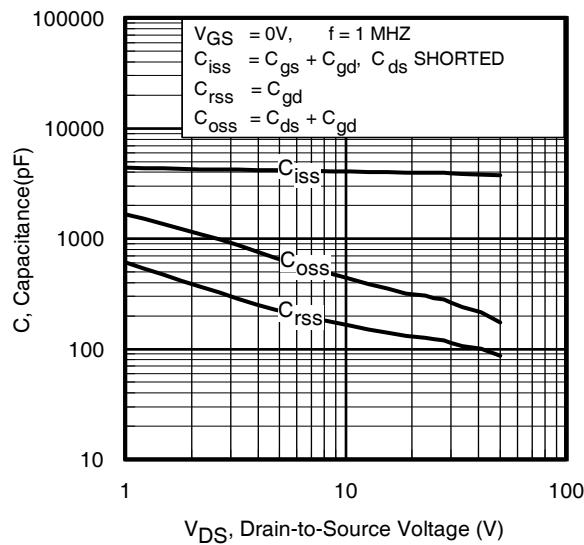


Fig 5. Typical Capacitance vs.
Drain-to-Source Voltage

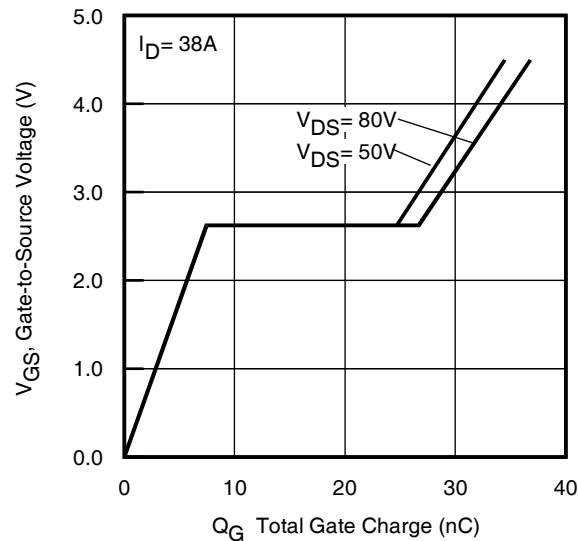


Fig 6. Typical Gate Charge vs.
Gate-to-Source Voltage

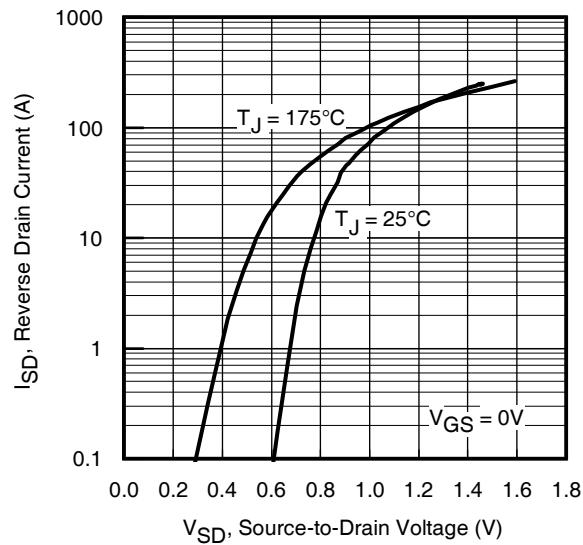


Fig 7. Typical Source-Drain Diode
Forward Voltage

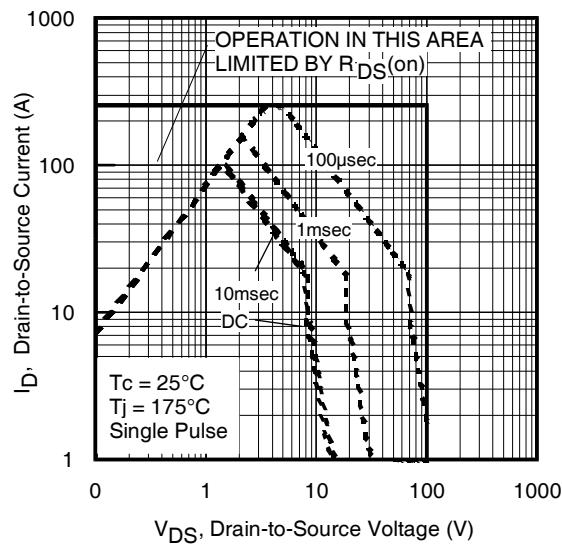


Fig 8. Maximum Safe Operating Area

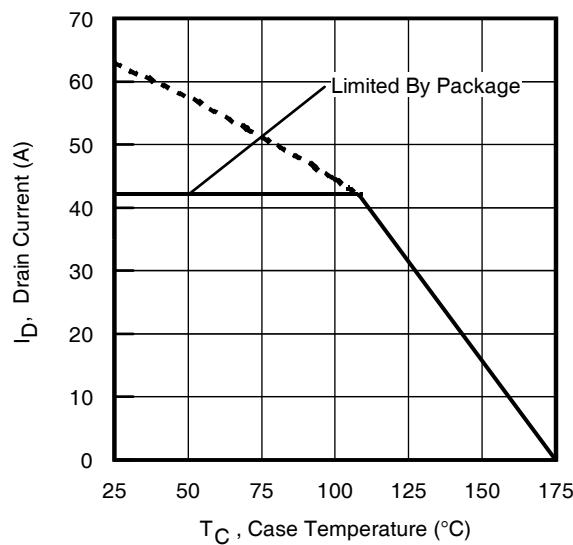


Fig 9. Maximum Drain Current vs. Case Temperature

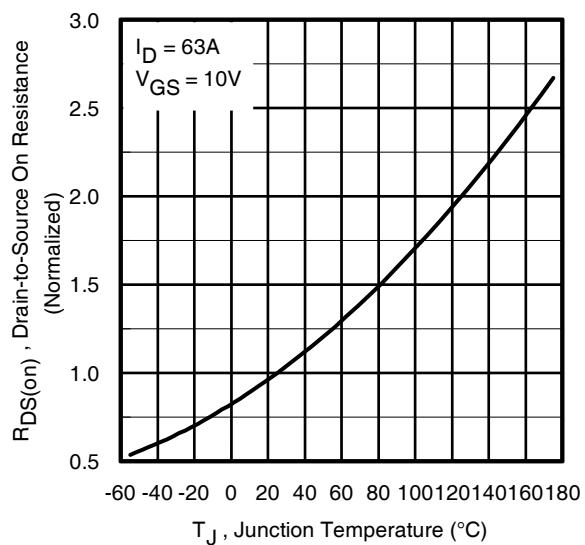


Fig 10. Normalized On-Resistance vs. Temperature

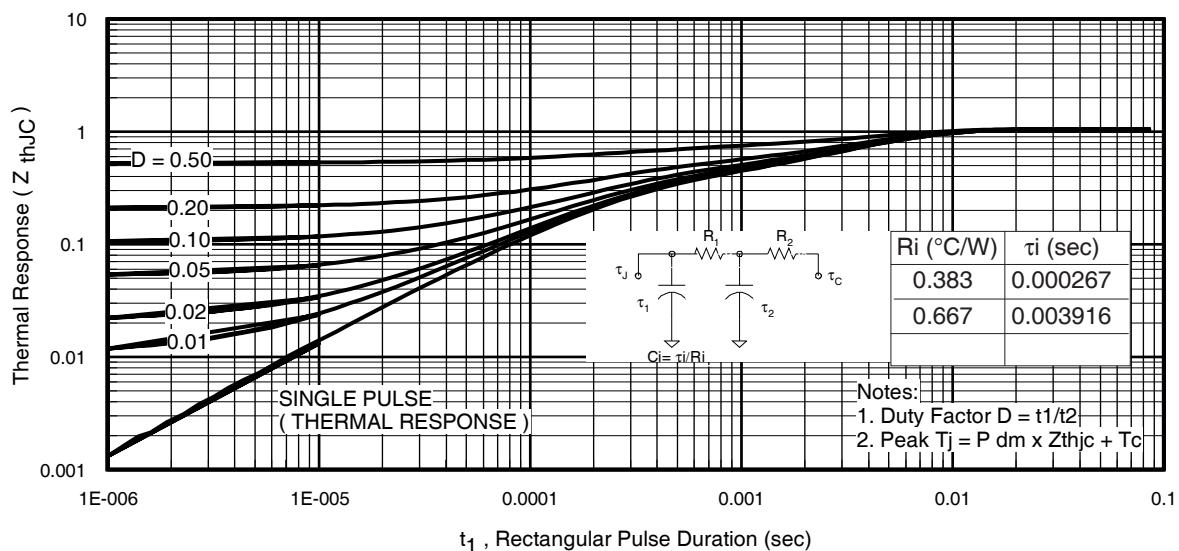


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

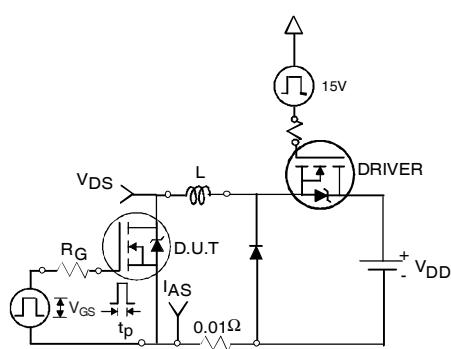


Fig 12a. Unclamped Inductive Test Circuit

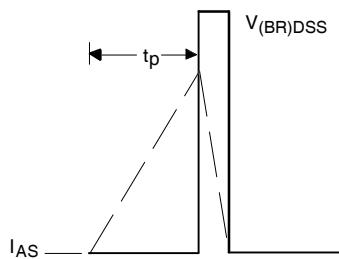


Fig 12b. Unclamped Inductive Waveforms

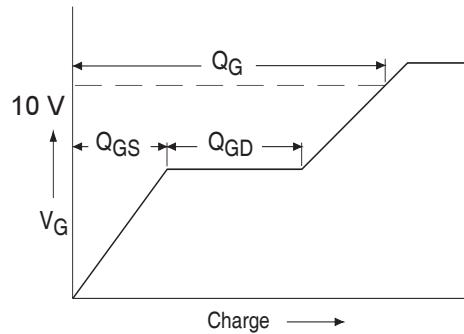


Fig 13a. Basic Gate Charge Waveform

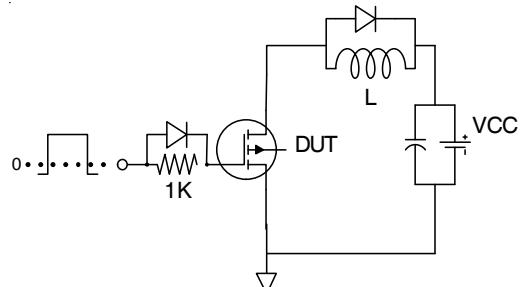


Fig 13b. Gate Charge Test Circuit

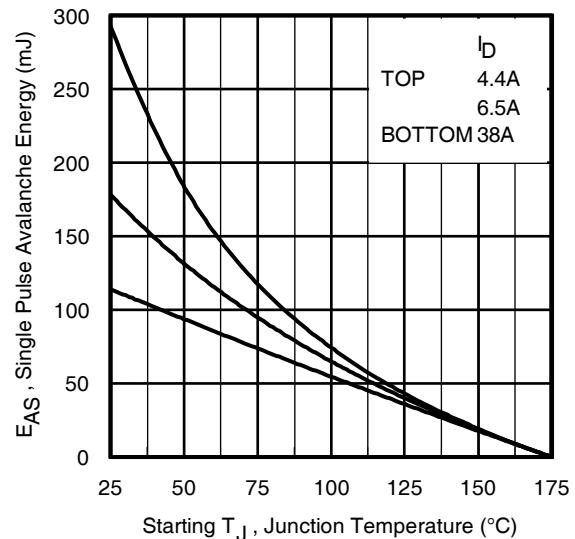


Fig 12c. Maximum Avalanche Energy vs. Drain Current

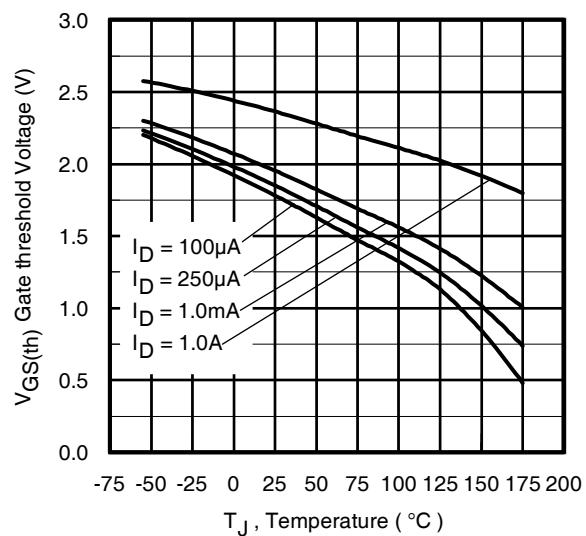


Fig 14. Threshold Voltage vs. Temperature

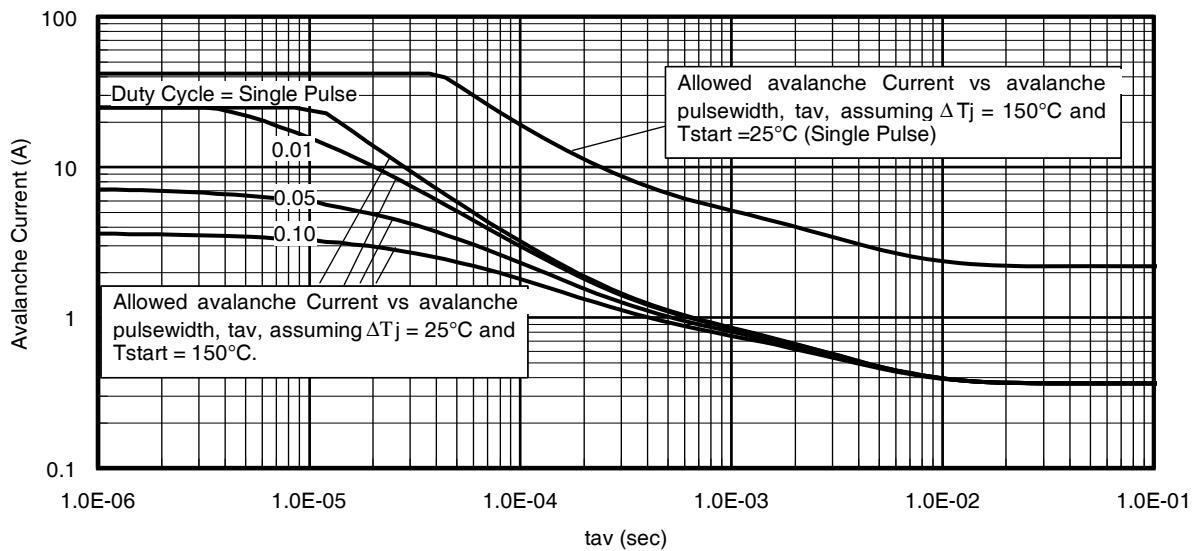


Fig 15. Typical Avalanche Current vs.Pulsewidth

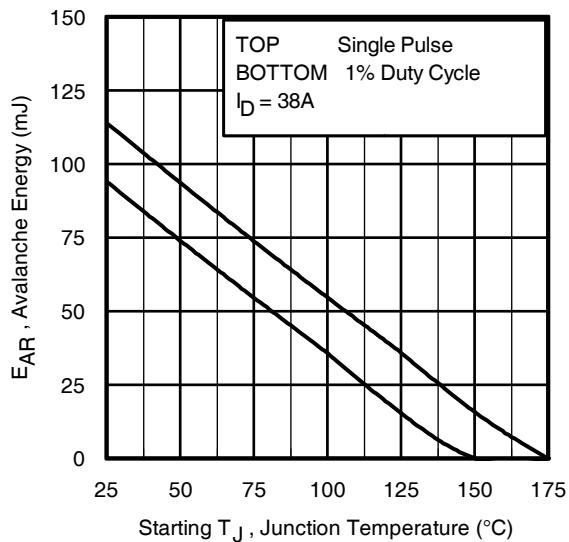


Fig 16. Maximum Avalanche Energy vs. Temperature

Notes on Repetitive Avalanche Curves , Figures 15, 16:
(For further info, see AN-1005 at www.irf.com)

1. Avalanche failures assumption:
Purely a thermal phenomenon and failure occurs at a temperature far in excess of T_{jmax} . This is validated for every part type.
2. Safe operation in Avalanche is allowed as long as neither T_{jmax} nor I_{av} (max) is exceeded.
3. Equation below based on circuit and waveforms shown in Figures 12a, 12b.
4. $P_D(\text{ave})$ = Average power dissipation per single avalanche pulse.
5. BV = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).
6. I_{av} = Allowable avalanche current.
7. ΔT = Allowable rise in junction temperature, not to exceed T_{jmax} (assumed as 25°C in Figure 15, 16).

t_{av} = Average time in avalanche.

D = Duty cycle in avalanche = $t_{av} \cdot f$

$Z_{thJC}(D, t_{av})$ = Transient thermal resistance, see figure 11)

$$P_D(\text{ave}) = 1/2 (1.3 \cdot BV \cdot I_{av}) = \Delta T / Z_{thJC}$$

$$I_{av} = 2\Delta T / [1.3 \cdot BV \cdot Z_{th}]$$

$$E_{AS(AR)} = P_D(\text{ave}) \cdot t_{av}$$

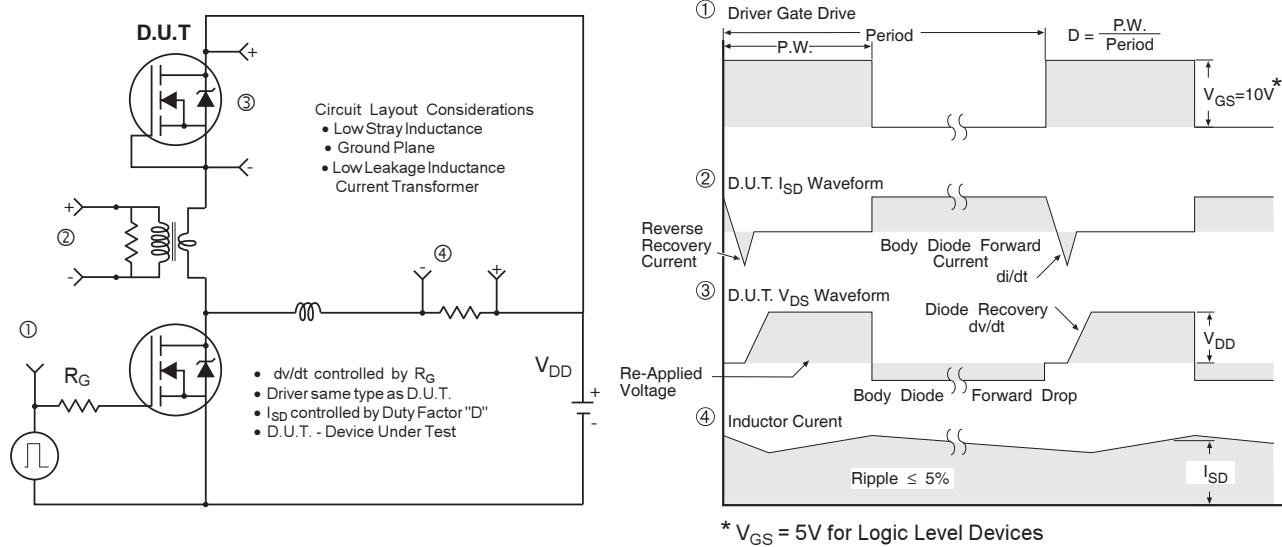


Fig 17. Peak Diode Recovery dv/dt Test Circuit for N-Channel HEXFET® Power MOSFETs

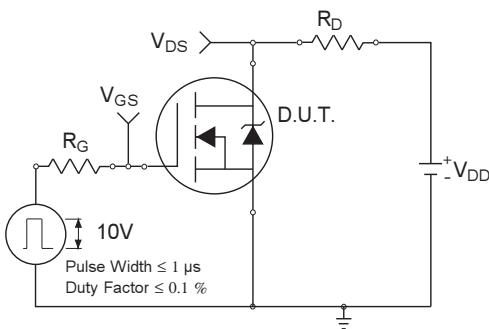


Fig 18a. Switching Time Test Circuit

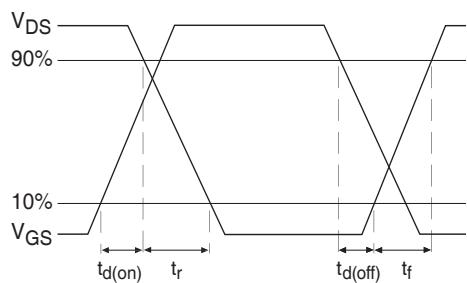
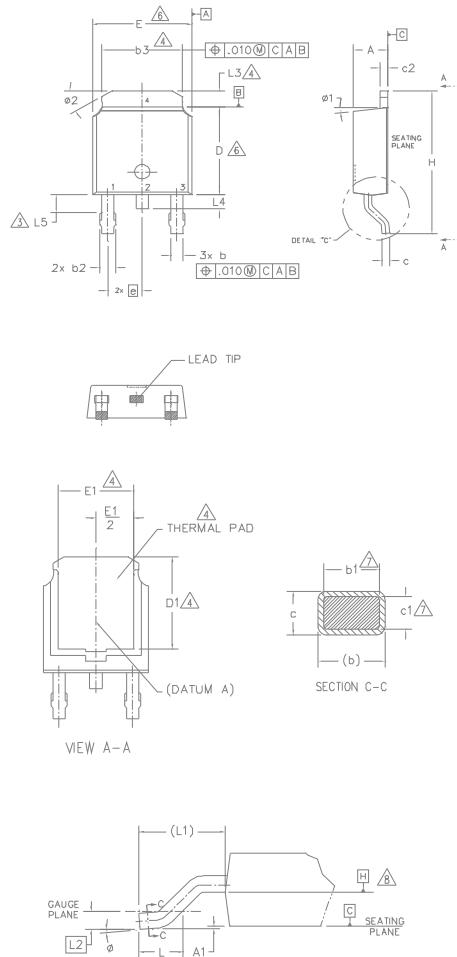


Fig 18b. Switching Time Waveforms

D-Pak (TO-252AA) Package Outline

Dimensions are shown in millimeters (inches)



NOTES:

1. - DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
2. - DIMENSION ARE SHOWN IN INCHES [MILLIMETERS].
3. - LEAD DIMENSION UNCONTROLLED IN L5.
4. - DIMENSION D1, E1, L3 & b3 ESTABLISH A MINIMUM MOUNTING SURFACE FOR THERMAL PAD.
5. - SECTION C-C DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN .005 AND 0.10 [0.13 AND 0.25] FROM THE LEAD TIP.
6. - DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .006 [0.15] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY.
7. - DIMENSION b1 & c1 APPLIED TO BASE METAL ONLY.
8. - DATUM A & B TO BE DETERMINED AT DATUM PLANE H.
9. - OUTLINE CONFORMS TO JEDEC OUTLINE TO-252AA.

SYMBOL	DIMENSIONS		NOTES
	MILLIMETERS	INCHES	
MIN.	MAX.	MIN.	MAX.
A	2.18	.239	.086 .094
A1	—	.13	— .005
b	0.64	.89	.025 .035
b1	0.64	.79	.025 .031
b2	0.76	1.14	.030 .045
b3	4.95	5.46	.195 .215
c	0.46	.61	.018 .024
c1	0.41	.56	.016 .022
c2	0.46	.89	.018 .035
D	5.97	6.22	.235 .245
D1	5.21	—	.205 —
E	6.35	6.73	.250 .265
E1	4.32	—	.170 —
e	2.29	BSC	.090 BSC
H	9.40	10.41	.370 .410
L	1.40	1.78	.055 .070
L1	2.74	BSC	.108 REF.
L2	0.51	BSC	.020 BSC
L3	0.89	1.27	.035 .050
L4	—	1.02	— .040
L5	1.14	1.52	.045 .060
Ø	0°	10°	0° 10°
Ø1	0°	15°	0° 15°
Ø2	25°	35°	25° 35°

LEAD ASSIGNMENTS

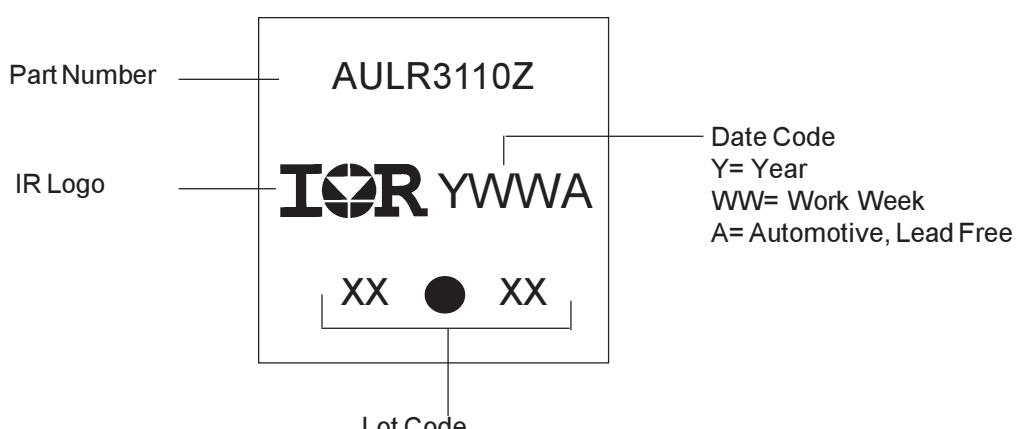
HEXFET

1. - GATE
2. - DRAIN
3. - SOURCE
4. - DRAIN

IGBT & CoPAK

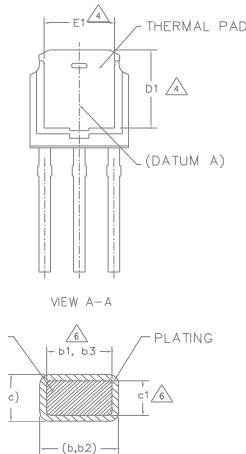
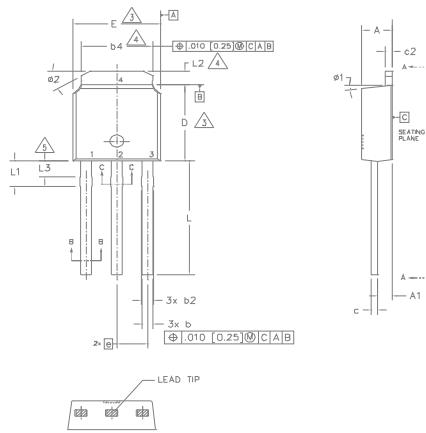
1. - GATE
2. - COLLECTOR
3. - Emitter
4. - COLLECTOR

D-Pak (TO-252AA) Part Marking Information



Note: For the most current drawing please refer to IR website at <http://www.irf.com/package/>

I-Pak (TO-251AA) Package Outline (Dimensions are shown in millimeters (inches))



SECTION B-B & C-C

NOTES:

- 1.- DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
- 2.- DIMENSION ARE SHOWN IN INCHES [MILLIMETERS].
- 3.- DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .005 [0.13] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY.
- 4.- THERMAL PAD CONTOUR OPTION WITHIN DIMENSION b4, L2, E1 & D1.
- 5.- LEAD DIMENSION UNCONTROLLED IN L3.
- 6.- DIMENSION b1, b3 & c1 APPLY TO BASE METAL ONLY.
- 7.- OUTLINE CONFORMS TO JEDEC OUTLINE TO-251AA (Date 06/02).
- 8.- CONTROLLING DIMENSION : INCHES.

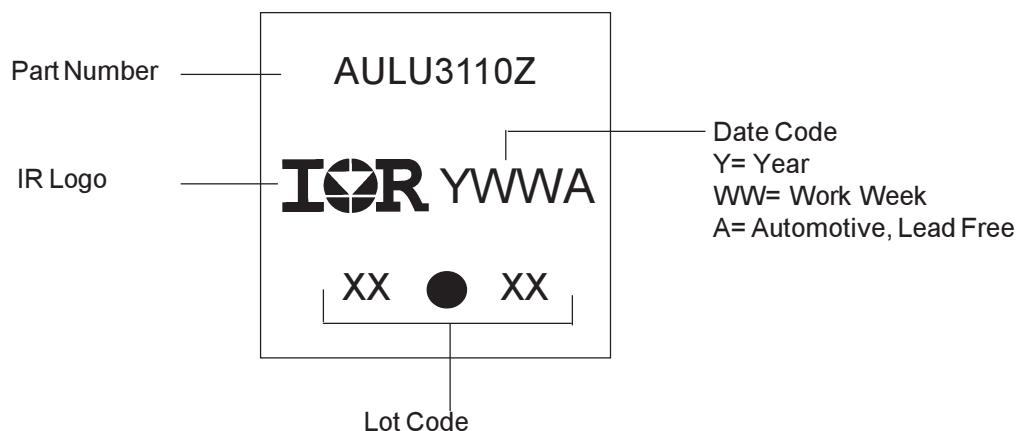
S Y M B O L	DIMENSIONS				N O T E S	
	MILLIMETERS		INCHES			
	MIN.	MAX.	MIN.	MAX.		
A	2.18	2.39	.086	.094		
A1	0.89	1.14	.035	.045		
b	0.64	0.89	.025	.035		
b1	0.65	0.79	.025	.031	6	
b2	0.76	1.14	.030	.045		
b3	0.76	1.04	.030	.041	6	
b4	4.95	5.46	.195	.215	4	
c	0.46	0.61	.018	.024		
c1	0.41	0.56	.016	.022	6	
c2	0.46	0.89	.018	.035		
D	5.97	6.22	.235	.245	3	
D1	5.21	—	.205	—	4	
E	6.35	6.73	.250	.265	3	
E1	4.32	—	.170	—	4	
e	2.29	BSC	.090	BSC		
L	8.89	9.65	.350	.380		
L1	1.91	2.29	.045	.090		
L2	0.89	1.27	.035	.050	4	
L3	0.89	1.52	.035	.060	5	
Ø1	0°	15°	0°	15°		
Ø2	25°	35°	25°	35°		

LEAD ASSIGNMENTS

HEXFET

- 1.- GATE
- 2.- DRAIN
- 3.- SOURCE
- 4.- DRAIN

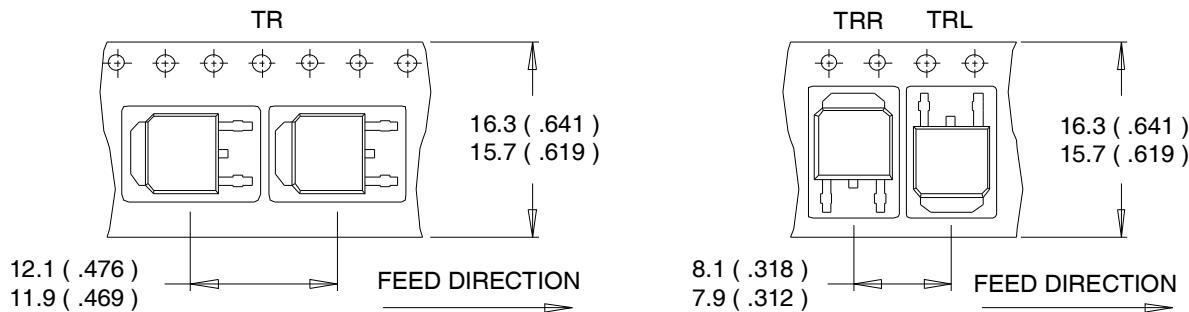
I-Pak (TO-251AA) Part Marking Information



Note: For the most current drawing please refer to IR website at <http://www.irf.com/package/>

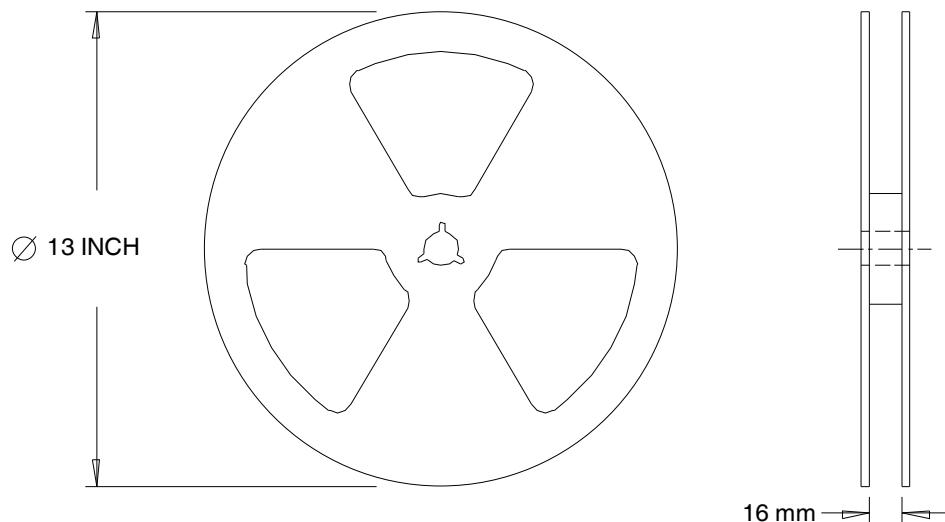
D-Pak (TO-252AA) Tape & Reel Information

Dimensions are shown in millimeters (inches)



NOTES :

1. CONTROLLING DIMENSION : MILLIMETER.
2. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS (INCHES).
3. OUTLINE CONFORMS TO EIA-481 & EIA-541.



NOTES :

1. OUTLINE CONFORMS TO EIA-481.

Note: For the most current drawing please refer to IR website at <http://www.irf.com/package/>

Qualification Information[†]

		Automotive (per AEC-Q101) ^{††}	
Qualification Level		Comments: This part number(s) passed Automotive qualification. IR's Industrial and Consumer qualification level is granted by extension of the higher Automotive level.	
Moisture Sensitivity Level		3L-D PAK	MSL1
ESD	Machine Model	3L-I PAK Class M4(+/- 700V) ^{†††} (per AEC-Q101-002)	
	Human Body Model	Class H1C(+/- 2000V) ^{†††} (per AEC-Q101-001)	
	Charged Device Model	Class C5(+/- 2000V) ^{†††} (per AEC-Q101-005)	
RoHS Compliant		Yes	

[†] Qualification standards can be found at International Rectifier's web site: <http://www.irf.com/>

^{††} Exceptions to AEC-Q101 requirements are noted in the qualification report.

^{†††} Highest passing voltage

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For technical support, please contact IR's Technical Assistance Center
<http://www.irf.com/technical-info/>

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Revision History

Date	Comments
2/28/2014	<ul style="list-style-type: none">• Added "Logic Level Gate Drive" bullet in the features section on page 1• Updated data sheet with new IR corporate template
4/9/2014	<ul style="list-style-type: none">• Updated package outline on page 9 & page 10• Updated Qualification table- I-pak from "NVA" to "MSL1" on page 12