

BIT MAP LCD DRIVER

■ GENERAL DESCRIPTION

The NJU6452A is a bit map LCD driver to display graphics or characters.

It contains 2,560 bit display data RAM, microprocessor interface circuits, instruction decoder, and 16-common and 61-segment drivers.

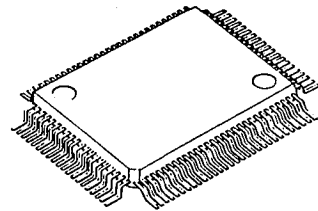
The bit image display data sent from 8- or 16-bit MPU are stored in the display data RAM and drives Dot Matrix LCD Panel by the common and segment drivers.

The 16-common and 61-segment drivers can drive graphics or 12-character 2-line with icon data.

The NJU6452A can combine with the NJU6452A or 6453A to expand the display capacity to 32 x 122 dots or 16 x 141 dots of graphics or character display by using the extension function of NJU6452A.

Furthermore, low current consumption due to the external clock input and wide operating voltage are useful apply to the small sized battery operated items.

■ PACKAGE OUTLINE

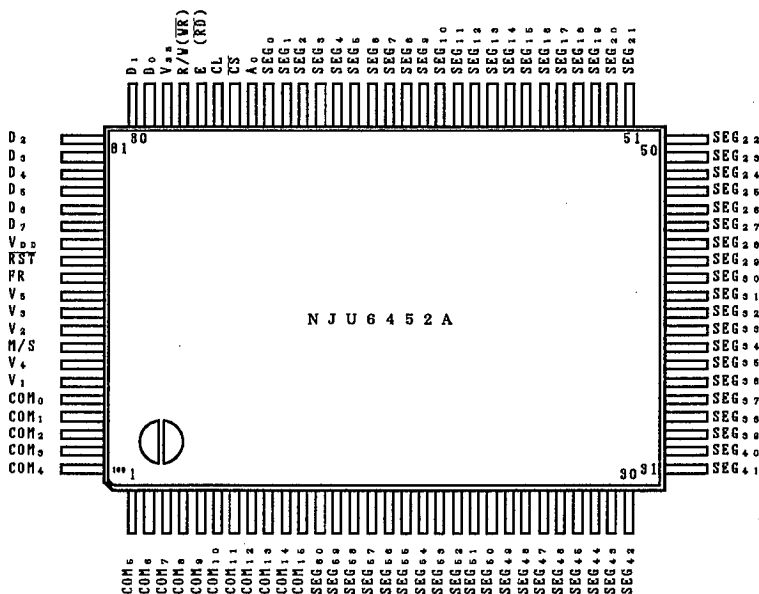


NJU6452AF

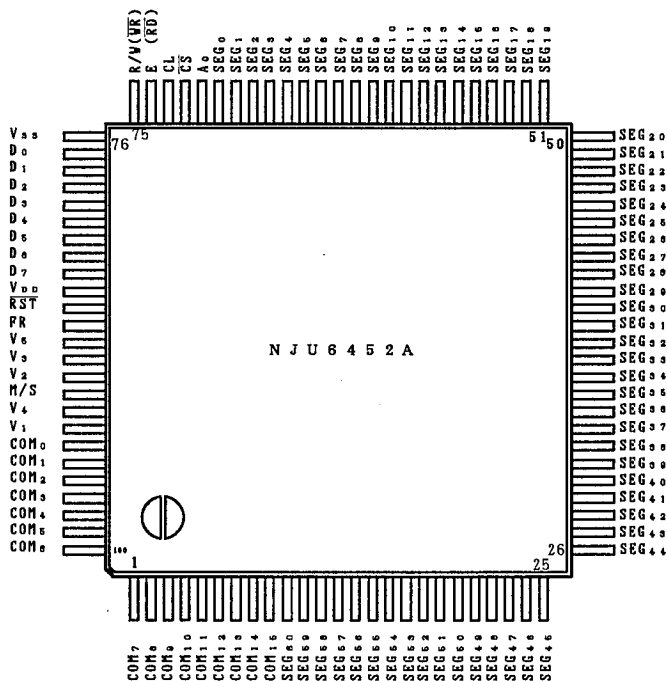
■ FEATURES

- Direct Correspondence between Display Data RAM and LCD Pixel
- Display Data RAM - 2,560 bits 80 x 8 x 4
- Direct Interface with 8- or 16-bit MPU
(Both of 68 and 80 type MPU can connect directly)
- Extension Function (can combine with NJU6452A or 6453A)
- Read Out From the Display Data RAM
- 16-common and 61-segment Drivers
- Programmable Duty Ratio ; 1/16 or 1/32 Duty
- Useful Instruction Set
Display Data Read/Write, Display ON/OFF Cont, Display Data RAM Address Set, Status Read, Display Starting Line Set, Static Drive ON/OFF, Duty Ratio Setting, and Read Modify Write,
- Low Power Consumption
- External Clock Input (2kHz)
- Operating Voltage --- 2.4V~6.0V
- LCD Driving Voltage --- 3.0V~13.5V
- Package Outline --- QFP 100 / Chip
- C-MOS Technology

PIN CONFIGURATION (NJU6452AFC1)

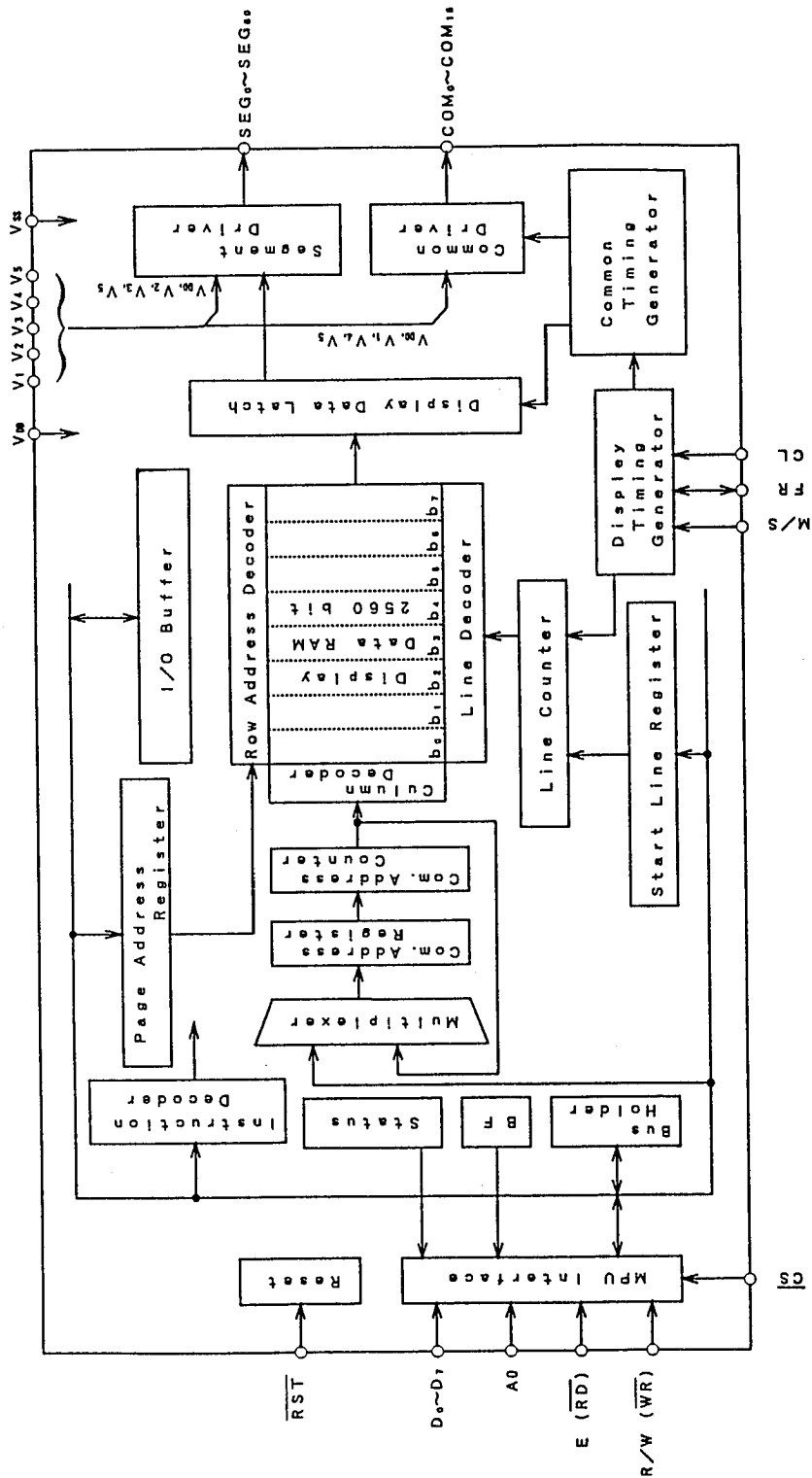


PIN CONFIGURATION (NJU6452AFG1)

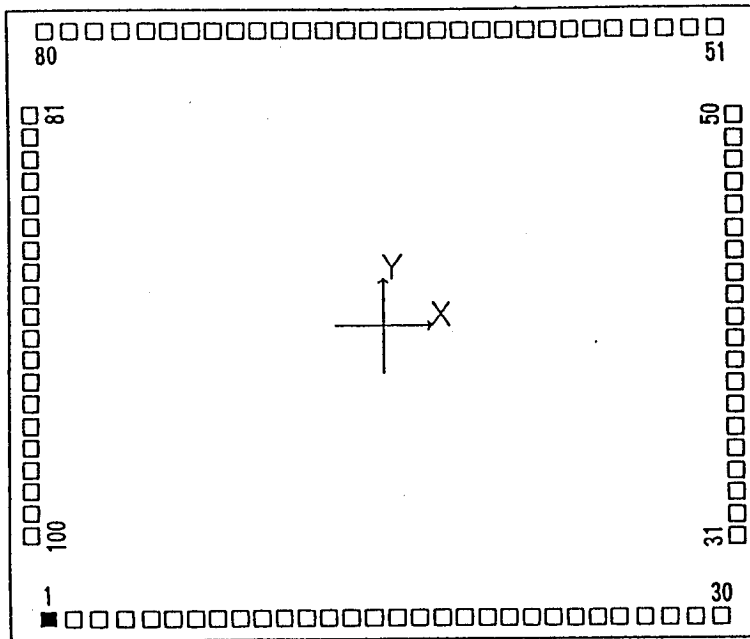


Note) Pin configuration of "FG1"package is different from "FC1"package.

■ BLOCK DIAGRAM



■ PAD LOCATION



Chip Center X=0um, Y=0um
 Chip Size 4860um x 4160um
 Chip Thickness 400um $\pm$ 30um
 Pad Size 92um x 92um

■ PAD COORDINATES

Chip Size 4860um x 4160um(Chip Center X=0um, Y=0um)

No.	Terminal Name	X=(um)	Y=(um)
1	COM ₅	-2130	-1865
2	COM ₆	-1970	-1865
3	COM ₇	-1810	-1865
4	COM ₈	-1650	-1865
5	COM ₉	-1490	-1865
6	COM ₁₀	-1330	-1865
7	COM ₁₁	-1190	-1865
8	COM ₁₂	-1050	-1865
9	COM ₁₃	- 910	-1865
10	COM ₁₄	- 770	-1865
11	COM ₁₅	- 630	-1865
12	SEG ₆₀	- 490	-1865
13	SEG ₅₉	- 350	-1865
14	SEG ₅₈	- 210	-1865
15	SEG ₅₇	- 70	-1865
16	SEG ₅₆	70	-1865
17	SEG ₅₅	210	-1865
18	SEG ₅₄	350	-1865
19	SEG ₅₃	490	-1865
20	SEG ₅₂	630	-1865
21	SEG ₅₁	770	-1865
22	SEG ₅₀	910	-1865
23	SEG ₄₉	1050	-1865
24	SEG ₄₈	1190	-1865
25	SEG ₄₇	1330	-1865
26	SEG ₄₆	1490	-1865
27	SEG ₄₅	1650	-1865
28	SEG ₄₄	1810	-1865
29	SEG ₄₃	1970	-1865
30	SEG ₄₂	2130	-1865
31	SEG ₄₁	2213	-1354
32	SEG ₄₀	2213	-1214
33	SEG ₃₉	2213	-1074
34	SEG ₃₈	2213	- 934
35	SEG ₃₇	2213	- 794
36	SEG ₃₆	2213	- 654
37	SEG ₃₅	2213	- 514
38	SEG ₃₄	2213	- 374
39	SEG ₃₃	2213	- 234
40	SEG ₃₂	2213	- 94
41	SEG ₃₁	2213	46
42	SEG ₃₀	2213	186
43	SEG ₂₉	2213	326
44	SEG ₂₈	2213	466
45	SEG ₂₇	2213	606
46	SEG ₂₆	2213	746
47	SEG ₂₅	2213	886
48	SEG ₂₄	2213	1026
49	SEG ₂₃	2213	1166
50	SEG ₂₂	2213	1306

No.	Terminal Name	X=(um)	Y=(um)
51	SEG ₂₁	2130	1865
52	SEG ₂₀	1970	1865
53	SEG ₁₉	1810	1865
54	SEG ₁₈	1650	1865
55	SEG ₁₇	1490	1865
56	SEG ₁₆	1330	1865
57	SEG ₁₅	1190	1865
58	SEG ₁₄	1050	1865
59	SEG ₁₃	910	1865
60	SEG ₁₂	770	1865
61	SEG ₁₁	630	1865
62	SEG ₁₀	490	1865
63	SEG ₉	350	1865
64	SEG ₈	210	1865
65	SEG ₇	70	1865
66	SEG ₆	- 70	1865
67	SEG ₅	- 210	1865
68	SEG ₄	- 350	1865
69	SEG ₃	- 490	1865
70	SEG ₂	- 630	1865
71	SEG ₁	- 770	1865
72	SEG ₀	- 910	1865
73	A ₀	-1050	1865
74	OSC ₁	-1190	1865
75	OSC ₂	-1330	1865
76	E	-1490	1865
77	R/W	-1650	1865
78	V _{SS}	-1810	1865
79	DB ₀	-1970	1865
80	DB ₁	-2130	1865
81	DB ₂	-2213	1330
82	DB ₃	-2213	1190
83	DB ₄	-2213	1050
84	DB ₅	-2213	910
85	DB ₆	-2213	770
86	DB ₇	-2213	630
87	V _{DD}	-2213	490
88	RST	-2213	350
89	FR	-2213	210
90	V ₅	-2213	70
91	V ₃	-2213	- 70
92	V ₂	-2213	- 210
93	M/S	-2213	- 350
94	V ₄	-2213	- 490
95	V ₁	-2213	- 630
96	COM ₀	-2213	- 770
97	COM ₁	-2213	- 910
98	COM ₂	-2213	-1050
99	COM ₃	-2213	-1190
100	COM ₄	-2213	-1330

* Pad Size 92um x 92um

■ Terminal Description

No.		Symbol	F u n c t i o n															
FG1	FC1																	
85	87	V _{DD}	Power Supply : V _{DD} =+5V															
76	78	V _{SS}	GND : V _{SS} = 0V															
88, 89 90, 92, 93	90, 91 92, 94, 95	V ₅ , V ₄ V ₃ , V ₂ , V ₁	LCD Driving Voltage Supplying Terminal. Following relation must be maintained. V _{DD} ≥V ₁ ≥V ₂ ≥V ₃ ≥V ₄ ≥V ₅															
72	74	CS	Chip Select Signal Input Terminal. Normally input the decoded signal of Address Bus Signal. Active "L".															
73	75	CL	Display Data Latch Signal Input Terminal. The Line Counter also count up by this signal rising timing. The synchronized signal of the NJU6450A is required.															
74	76	E (RD)	<When connect to the 68 type MPU> Connect to Enable Clock Input Terminal of 68 type MPU. Active "H". <When connect to the 80 type MPU> Connect to RD Signal Input Terminal of 80 type MPU. Active "L" During this terminal is "L", the Data Bus is output state.															
75	77	R/W (WR)	<When connect to the 68 type MPU> Connect to READ/WRITE Control Signal Input Terminal of 68 type MPU. <table border="1"><tr><td>R/W</td><td>H</td><td>L</td></tr><tr><td>Status</td><td>Read</td><td>Write</td></tr></table> <When connect to the 80 type MPU> Connect to WR Signal connecting terminal of 80 type MPU. Active "L". The data on the Data Bus is fetch at the rising edge of this signal.	R/W	H	L	Status	Read	Write									
R/W	H	L																
Status	Read	Write																
71	73	AO	Connect to the Address Bus of MPU. The data on the D ₀ ~D ₇ is distinguished between Display Data and Instruction by this signal. <table border="1"><tr><td>AO</td><td>H</td><td>L</td></tr><tr><td>Data</td><td>Display Data</td><td>Instruction</td></tr></table>	AO	H	L	Data	Display Data	Instruction									
AO	H	L																
Data	Display Data	Instruction																
77~84	79~86	D ₀ ~D ₇	Tri-state bilateral Data Bus. The data transmission between 8- or 16-bit MPU and NJU6452A is executed by this Bus.															
87	89	FR	Alternating signal for LCD Driving output or input terminal. Output or input is determined by master or slave mode which selected by M/S terminal. <table border="1"><tr><td>M/S</td><td>Master</td><td>Slave</td></tr><tr><td>FR</td><td>Output</td><td>Input</td></tr></table>	M/S	Master	Slave	FR	Output	Input									
M/S	Master	Slave																
FR	Output	Input																
94~100 1~9	96~100 1~11	COM ₀ ~COM ₁₅ (COM ₃₁ ~COM ₁₆) (Note)	Common output terminal. One output level out of V _{DD} , V ₁ , V ₄ , V ₅ is selected by combination of FR and data of common counter. <table border="1"><tr><td>FR</td><td colspan="2">H</td><td colspan="2">L</td></tr><tr><td>Data</td><td>H</td><td>L</td><td>H</td><td>L</td></tr><tr><td>Output</td><td>V₅</td><td>V₁</td><td>V_{DD}</td><td>V₄</td></tr></table>	FR	H		L		Data	H	L	H	L	Output	V ₅	V ₁	V _{DD}	V ₄
FR	H		L															
Data	H	L	H	L														
Output	V ₅	V ₁	V _{DD}	V ₄														
70~10	72~12	SEG ₀ ~SEG ₆₀	Segment output terminal. One output level out of V _{DD} , V ₂ , V ₃ , V ₅ is selected by combination of FR and data of Display RAM. <table border="1"><tr><td>FR</td><td colspan="2">H</td><td colspan="2">L</td></tr><tr><td>Data</td><td>H</td><td>L</td><td>H</td><td>L</td></tr><tr><td>Output</td><td>V_{DD}</td><td>V₂</td><td>V₅</td><td>V₃</td></tr></table>	FR	H		L		Data	H	L	H	L	Output	V _{DD}	V ₂	V ₅	V ₃
FR	H		L															
Data	H	L	H	L														
Output	V _{DD}	V ₂	V ₅	V ₃														
86	88	RST	Reset and Interface type select terminal. The reset operation is performed by rise or fall edge of this signal. The input level after initialization selects the interface type of 68 or 80 type of MPU. <table border="1"><tr><td>MPU</td><td>Edge</td><td>Input Level after Initialization</td></tr><tr><td>68 Type</td><td>Rise</td><td>H</td></tr><tr><td>80 Type</td><td>Fall</td><td>L</td></tr></table>	MPU	Edge	Input Level after Initialization	68 Type	Rise	H	80 Type	Fall	L						
MPU	Edge	Input Level after Initialization																
68 Type	Rise	H																
80 Type	Fall	L																
91	93	M/S (Note)	Master or Slave operation selecting terminal. Connect to V _{DD} or V _{SS} . M/S=V _{DD} : Master, M/S=V _{SS} : Slave The function of FR, COM ₀ ~COM ₁₅ , OSC ₁ , and OSC ₂ is changed by M/S. <table border="1"><tr><td>M/S</td><td>FR</td><td>Common Output</td><td>OSC₁</td><td>OSC₂</td></tr><tr><td>Master</td><td>Out</td><td>COM₀ ~COM₁₅</td><td>In</td><td>Out</td></tr><tr><td>Slave</td><td>In</td><td>COM₃₁ ~COM₁₆</td><td>NC</td><td>In</td></tr></table>	M/S	FR	Common Output	OSC ₁	OSC ₂	Master	Out	COM ₀ ~COM ₁₅	In	Out	Slave	In	COM ₃₁ ~COM ₁₆	NC	In
M/S	FR	Common Output	OSC ₁	OSC ₂														
Master	Out	COM ₀ ~COM ₁₅	In	Out														
Slave	In	COM ₃₁ ~COM ₁₆	NC	In														

(Note) The common scanning order of slave LSI is inverted against the master LSI.

■ Functional Description

(1) Description for each blocks

(1-1) Busy Flag (BF)

When the internal circuits are in the operation mode, the busy flag(BF) is "1", and any instruction except the status read are inhibited.

The busy flag is output at D₇ terminal when status read instruction is executed.

If enough cycle time over than t_{cyo} is kept, no need to check the busy flag.

(1-2) Display Start Line Register

The Display Start Line Register is a pointer register which indicate the address in the Display Data RAM corresponded with COM₀ (normally it display the top line in the LCD Panel).

This register can use for scroll the screen, change the display page and so on.

The Display Start Line instruction set the display start address of the Display Data RAM represented in 5-bit to this register.

(1-3) Line Counter

The Display Start Address stored in the Display Start Line Register is set to the Line Counter when the FR signal out from the NJU6452A is changing.

The Line Counter count up by synchronizing common signal out from NJU6452A and generate the line address which addressing the read out line of Display Data RAM.

(1-4) Column Address Counter

The column address counter is 7-bit presettable counter which addressing the column address as shown as Fig. 1.

This counter increments "1" up to 50H when the Display Data Read/Write instruction is executed. The count up is stop at 50H (over 50H is non existing address) automatically by the count lock function.

Furthermore, this counter is independent with the Page Register.

(1-5) Page Register

This register gives page address of Display Data RAM as shown Fig. 1.

When the MPU access the data by changing the page, the page address set instruction is required.

(1-6) Display Data RAM

Display Data Ram consist of 2,560 bits stores the bit image display data (each bit correspond to the each pixel so called bit map method). This RAM and MPU are operating independently, therefore, there is

no influence by the unsynchronize rewriting.

The each bit in the Display Data RAM correspond to the each dot of the LCD panel.

On = "1"

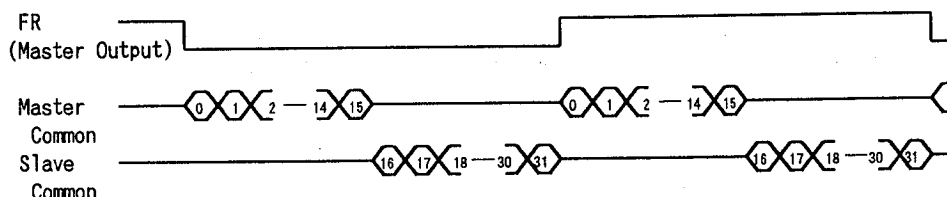
Off = "0"

The relation between column address and segment output can inverse by the Address Inverse Instruction ADC as shown Fig. 1.

(1-7) Timing Generator

This Generator generates the common timing and frame signal for 1/16 and 1/32 duty selecting by Duty Select Instruction from the master clock.

In the case of the 1/32 duty, 2 chip of master and slave chip should be combined, and both of common are synchronized by the common multi-chip method. (Refer the figure shown below)



(1-8) Display Data Latch

Display Data Latch stores 80-bit of one line display data for each common cycle which read out from the Display Data RAM temporary and transfer this data to the LCD Driver.

The Display On/Off and Static Drive On/Off controls the latched data only, therefore, the data in the Display Data RAM is no change and keep on remaining.

(1-9) LCD Driving Circuits

This Driver is consists of 80-multiplexer which output the 4-level of LCD driving voltage.

The output waveform is determined by the combination of the data in the Display Data Latch, Common Timing Generator and FR signal

(1-10) Display Timing Generator

This Generator generates the timing signal for the display system by combination of the master clock and Frame Driving Signal FR. The Frame Driving Signal FR has a function to generate the 2 frame alternative driving method waveform for the LCD panel, and synchronizing the line counter and common timing generator to the master LSI. Therefore, the FR signal must be 50% duty ratio clock signal which synchronized with the frame signal.

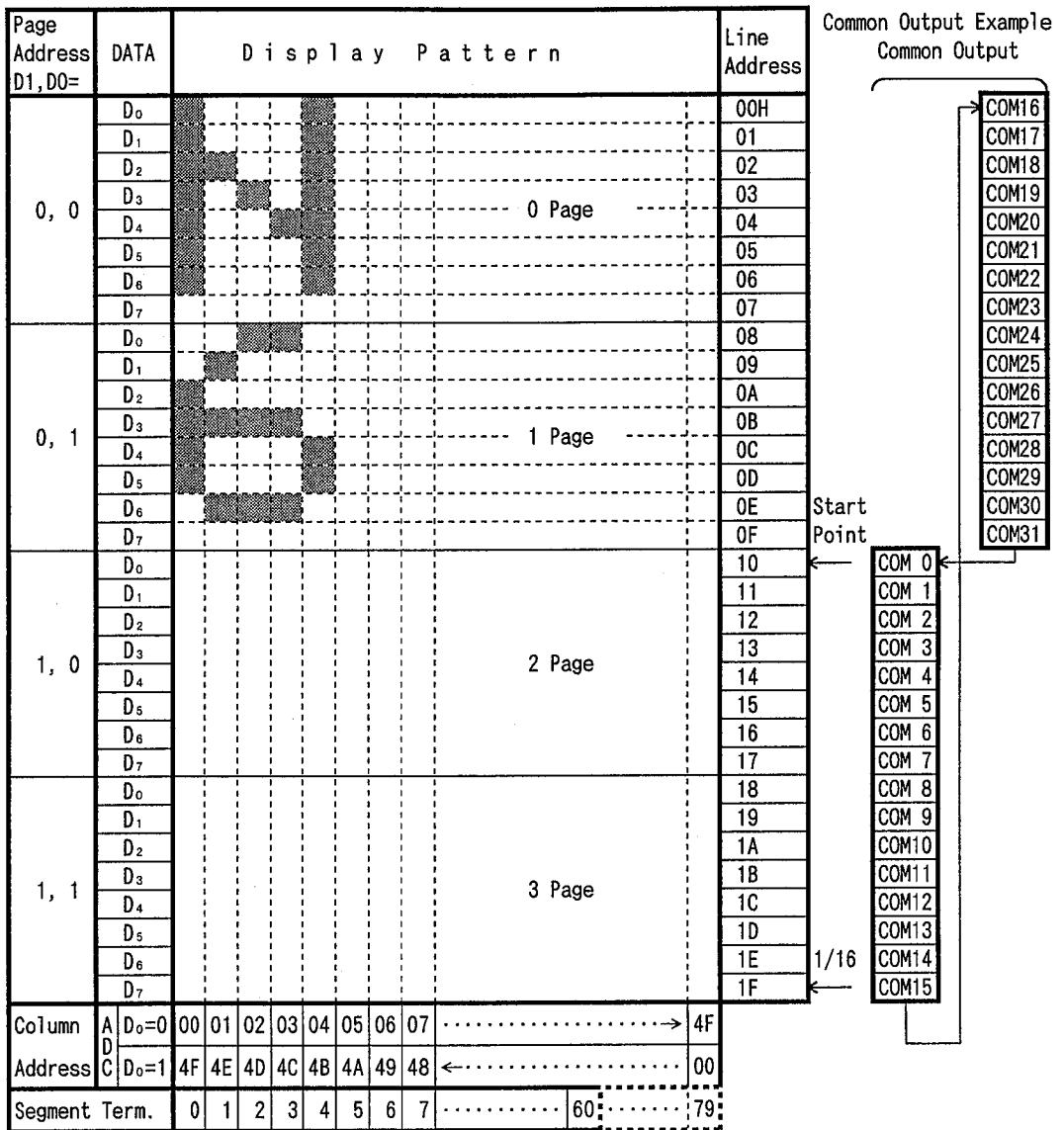


Fig. 1. Correspondence with Display Data RAM and address (For example the display start line is 10th and 1/32 duty)

(1-11) Reset Circuits

The NJU6452A performs following initialization by detecting the rising or falling edge of the $\overline{\text{RST}}$ input after the power turns on.

Initialization

- ① Display Off
- ② Set the 1st line to the Display Start Register
- ③ Static Drive Off
- ④ Set the address "0" to the Column Address Counter
- ⑤ Set the page "3" to the Page Address Register
- ⑥ Select the 1/32 duty
- ⑦ Select the ADC : Counterclockwise output
(ADC instruction $D_0 = "0"$, ADC status flag "1")
- ⑧ Read Modify Write Mode Off

The $\overline{\text{RST}}$ terminal input level is used to select the interface of 80 or 68 type MPU as shown in Table. 2. Therefore, the "H" level input through the inverter is required when connecting the 80 type MPU, and "L" level input is required when connecting the 68 type MPU as shown in application circuits 1.

The $\overline{\text{RST}}$ terminal must be connect to the Reset Terminal of MPU and reset at same time with it. The dead-lock may occur if the no initialization by the $\overline{\text{RST}}$ terminal when the power terns on. By the RESET instruction, the initialization of ② and ⑤ mentioned above are executed.

(2) Instruction

The NJU6452A distinguish the signal on the data bus by combination of A0 and R/W($\overline{\text{RD}}$, $\overline{\text{WR}}$).

Normally, the busy check is not required as the NJU6452A is operating so first because of the decode of the instruction and execution are performs only depend on the internal timing which not depend on the external clock.

The Table. 1 shows the instruction codes of the NJU6452A.

Table 1. Instruction Code

Instruction	C o d e											Description
	AO	RD	WR	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	
Display On / Off	0	1	0	1	0	1	0	1	1	1	0/1	Whole Display On/Off. 1:On,0:Off(Power Save mode if the static Drive On)
Display Start Line	0	1	0	1	1	0	Display Start Address (1~31)				Determine the Display Line correspond to the COM ₀ .	
Page Address Set	0	1	0	1	0	1	1	1	0	Page (0~3)		Set the Page of Disp. Data RAM to the Page Register.
Column Address Set	0	1	0	0	Column Address (0~79)						Set the Column Address of Display Data RAM to the Column Register.	
Status Read	0	0	1	B U S Y	A D C	ON / OFF	R E S E T	0	0	0	0	Read the status. BUSY 1:Working 0:Ready ADC 1:Clockwise Output 0:Counterclockwise ON/OFF1:Disp Off 0:Disp On RESET 1:Reset 0:Normal
Write Display Data	1	1	0	Write Data							Write the data to the Display Data RAM.	Access the predetermined address of the Display Data RAM. The Column address increment "1" after read or write.
Read Display Data	1	0	1	Read Data							Read the data from the Display Data RAM.	
ADC Select	0	1	0	1	0	1	0	0	0	0	0/1	Determine the clockwise or counterclockwise reading of the Display Data RAM. 0:Clockwise Output 1:Counterclockwise Output
Static Drive On / Off	0	1	0	1	0	1	0	0	1	0	0/1	Select the Dynamic or Static Driving. 1:Static Driving (Power Saving) 0:Dynamic Driving
Duty Ratio Select	0	1	0	1	0	1	0	1	0	0	0/1	Select the duty ratio. 1:1/32 Duty 0:1/16 Duty
Read Modify Write	0	1	0	1	1	1	0	0	0	0	0	Increment the Column Address register when writing but no-change when reading.
End	0	1	0	1	1	1	0	1	1	1	0	Release from the Read Modify Write Mode.
Reset	0	1	0	1	1	1	0	0	0	1	0	Set the Display Start Line Register to 1st line, Page Add. Register to "3".
Power Save (Dual Command)	0	1	0	1	0	1	0	1	1	1	0	Set the power save mode by selecting Display Off and Static Driving On.
	0	1	0	1	0	1	0	0	1	0	1	

(3) Explanation of Instruction Code.

(a) Display On/Off

This instruction executes whole display On/Off no relation with the data in the Display Data RAM and internal conditions.

Code	A0	R/W	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
	RD	WR								
	0	1	0	1	0	1	0	1	1	D

D 0 : Display On
1 : Display Off

When the static driving mode is selected (static drive On) in display Off status, the internal circuits put on the power save mode.

(b) Display Start Line

This instruction set the line address as shown Fig. 1. The selected line in the Display Data RAM correspond to the COM₀ which display at the top of LCD panel.

The display area is set automatically from the selected line to the line which increased the number of duty ratio.

Therefore, the smooth scroll for vertical direction by changing the start line address one by one or page switching are available by this instruction.

Code	A0	R/W	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
	RD	WR								
	0	1	0	1	1	0	A ₄	A ₃	A ₂	A ₁

A ₄	A ₃	A ₂	A ₁	A ₀	Line Address
0	0	0	0	0	0
				1	1
1	1	1	1	0	1E
1	1	1	1	1	1F

(c) Page Address Set

When MPU access the Display Data RAM, the page address corresponded to the row address must be selected.

The access in the Display Data RAM is available by setting the page and column address. (Refer the Fig. 1.)

The display is no change when the page address is changed.

Code	A0	R/W	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
	RD	WR								
	0	1	0	1	0	1	1	1	0	A ₁

A ₁	A ₀	Page
0	0	0
0	1	1
1	0	2
1	1	3

(d) Column Address Set

This instruction set the column address in the Display Data RAM.(See Fig.1.)

When the MPU access the Display Data RAM continuously, the column address increase "1" automatically, therefore, the MPU can access the data only without address setting.

The increment of the column address is stopped by the address of 50H automatically, but the page address is no change even if the column address increase to 50H and stop.

Code	R/W		D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
	A ₀	$\overline{RD}$ WR								
	0	1 0	0	A ₆	A ₅	A ₄	A ₃	A ₂	A ₁	A ₀

A ₆	A ₅	A ₄	A ₃	A ₂	A ₁	A ₀	Column Add.
0	0	0	0	0	0	0	0
0	0	0	0	0	0	1	1
1	0	0	1	1	1	0	4E
1	0	0	1	1	1	1	4F

(e) Status Read

This instruction read out the internal status.

Code	R/W		D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
	A ₀	$\overline{RD}$ WR								
	0	0 1	BUSY	ADC	ON/OFF	RESET	0	0	0	0

BUSY : BUSY=1 indicate the operating or the Reset cycle.

The instruction can be input after the BUSY status change to "0".

ADC : Indicate the output correspondence of column(segment) address and segment driver.

0 : Counterclockwise Output(Inverse) Column Address 79-n $\longleftrightarrow$ Segment Driver n

1 : Clockwise Output (Normal) Column Address n $\longleftrightarrow$ Segment Driver n

ON/OFF : Indicate the whole display On/Off status.

0 : Whole Display "On"

1 : Whole Display "Off"

(Note) The data "0=On" and "1=Off" of Display On/Off status read out is inverted with the Display On/Off instruction data of "1=On" and "0=Off".

RESET : Indicate the initialization period by $\overline{RST}$ signal or reset instruction.

0 : —

1 : Initialization Period

(f) Write Display Data

This instruction write the 8-bit data on the data bus into the Display Data RAM.

The column(segment) address increase "1" automatically when writing, therefore, the MPU can write the 8-bit data into the Display Data RAM without address setting.

	R/W										
	A0	$\overline{RD}$	$\overline{WR}$	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
Code	1	1	0	Write Data							

(g) Read Display Data

This instruction read out the 8-bit data from Display Data RAM which addressed by the column and page address. In case of the Read Modify Write Mode is Off, the column address increase "1" automatically after each read out, therefore, the MPU can read out the 8-bit data from the Display Data RAM continuously without address setting. One time of dummy read must be required after column address set as explain in (4-3).

	A0	$\overline{RD}$	R/W WR	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
Code	1	0	1	Read Data							

(h) ADC Select

This instruction set the correspondence of column address in the Display Data RAM and segment driver output. (See Fig. 1.) Therefore, the order of segment output can be changed by the software, and no restriction of the LSI placement against the LCD panel.

	A0	$\overline{RD}$	R/W WR	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
Code	0	1	0	1	0	1	0	0	0	0	D

D 0 : Clockwise Output (Inverse)
1 : CounterClockwise Output (Normal)

(i) Static Drive On/Off

This instruction executes the all common output turns on and whole display on obligatory.

	A0	$\overline{RD}$	R/W WR	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
Code	0	1	0	1	0	1	0	0	1	0	D

D 0 : Static Drive Off (Normal Operation)
1 : Static Drive On (Whole Display Turns On)

When the Display Off mode is selected (Display Off) in Static Drive On status, the internal circuits put on the power save mode.

(j) Duty Select

This instruction set the LCD driving duty ratio.

	A0	$\overline{RD}$	R/W WR	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
Code	0	1	0	1	0	1	0	1	0	0	D

D 0 : 1/16 duty
1 : 1/32 duty

(k) Read Modify Write

After this instruction is executed, the column address increase "1" automatically when Display Data Write Instruction execution, but the address is not changed when the Display Data Read Instruction execution.

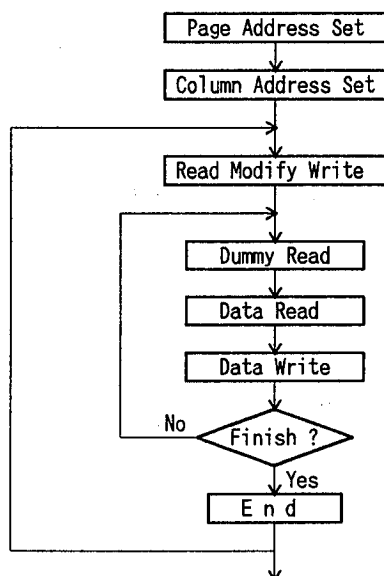
This status continues during End instruction execution. When the End instruction is entered the column address back to the address where Read Modify Write instruction entering.

By this function, the load of MPU for example cyclic data writing operation like as cursor blink etc., can be reduced.

	A0	$\overline{RD}$	$\overline{WR}$	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
Code	0	1	0	1	1	1	0	0	0	0	0

Note) During the Read Modify Write mode, any instruction except Column Address Set can be executed.

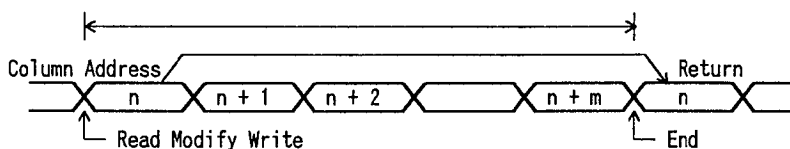
(1) Sequence of cursor display



(m) End

This instruction release the Read Modify Write mode and the column address back to the address where the read modify write mode setting.

	A0	$\overline{RD}$	$\overline{WR}$	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
Code	0	1	0	1	1	1	0	1	1	1	0



(n) Reset

This instruction executes the following initialization.

Initialization

- ① Set the 1st line in the Display Start Line Register.
- ② Set the page 3 in the Page Register.

In this time, there are no influence to the Display Data RAM.

	A0	$\overline{RD}$	R/W WR	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
Code	0	1	0	1	1	1	0	0	0	1	0

The reset signal input to the $\overline{RST}$ terminal must be required for the initialization when the power turns on.

(Note) The initialization when the power turns on can not be executed by Reset instruction.

(o) Power Save(Dual Command)

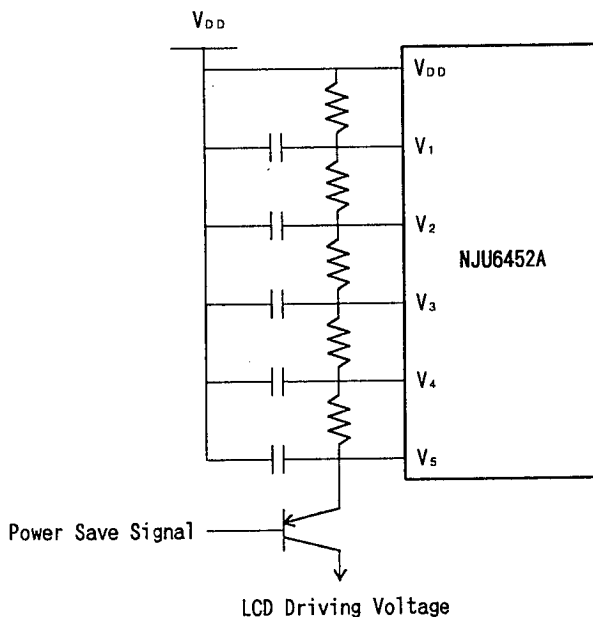
When both of Display Off and Static Drive On are executed, the internal circuits put on the power save mode and the current consumption is reduced as same as stand by current.

The internal status in this mode are as follows;

- ① Stop the LCD driving. Segment and Common drivers output V_{DD} level.
- ② Stop the oscillation or inhibit the external clock input. Then the terminal OSC₂ becomes floating status.
- ③ Keeping the display data and operating mode.

The power save mode is released by Display on or static drive off instruction.

To reduce the total power consumption, the current flow on the bleeder resistance must be cut by the transistor etc. during the power save mode as shown below.



(4) MPU Interface

(4-1) 68 or 80 type MPU interface selection.

The NJU6452A can interface both of 68 or 80 type MPU bus directly by setting the $\overline{\text{RST}}$ level after reset instruction entered as shown Table. 2.

The data transfer is executed between $\text{D}_0 \sim \text{D}_7$ of NJU6452A and the MPU data bus.

During the CS signal is "H", the NJU6452A released from the MPU and becomes stand-by mode. But the reset instruction can be input though the internal status of NJU6451A.

Table. 2.

Level of $\overline{\text{RST}}$	Type of MPU	A0	E	R/W	$\text{D}_0 \sim \text{D}_7$
"H"	68 type	↑	↑	↑	↑
"L"	80 type	↑	$\overline{\text{RD}}$	$\overline{\text{WR}}$	↑

(4-2) Discrimination of the data bus signal.

The NJU6452A discriminates the data bus signal by combination of A0, E($\overline{\text{RD}}$), and R/W($\overline{\text{WR}}$) signals as shown Table. 3.

Table. 3.

Common	68 type	80 type		Function
A0	R/W	$\overline{\text{RD}}$	$\overline{\text{WR}}$	
1	1	0	1	Display Data Read out
1	0	1	0	Display Data Write
0	1	0	1	Status Read
0	0	1	0	Command Input to the Register

(4-3) Access to the Display Data RAM and Internal Register.

The NJU6452A is operating as one of Pipe-line processor by the bus-holder connecting to the internal data bus to adjust the operation frequency between MPU and the Display Data RAM or Internal Register.

For example, when the MPU write the data into the Display Data RAM, the data is held in the bus-holder at once then write into the Display Data RAM by next data write cycle.

Therefore high speed data transmission between MPU and NJU6452A is available because of the limitation of access time of NJU6452A locking from MPU is just determined by the cycle time only which ignored the access time of t_{ACC} and t_{DS} of Display Data RAM.

If the cycle time can not be kept in the MPU operation, NOP operation cycle must be insert which equivalent to the waiting operation.

Please note that the read out data is a address data when the read out execution just after the address setting. Therefore, one dummy read is required after address setting or write cycle as shown in Fig. 2.

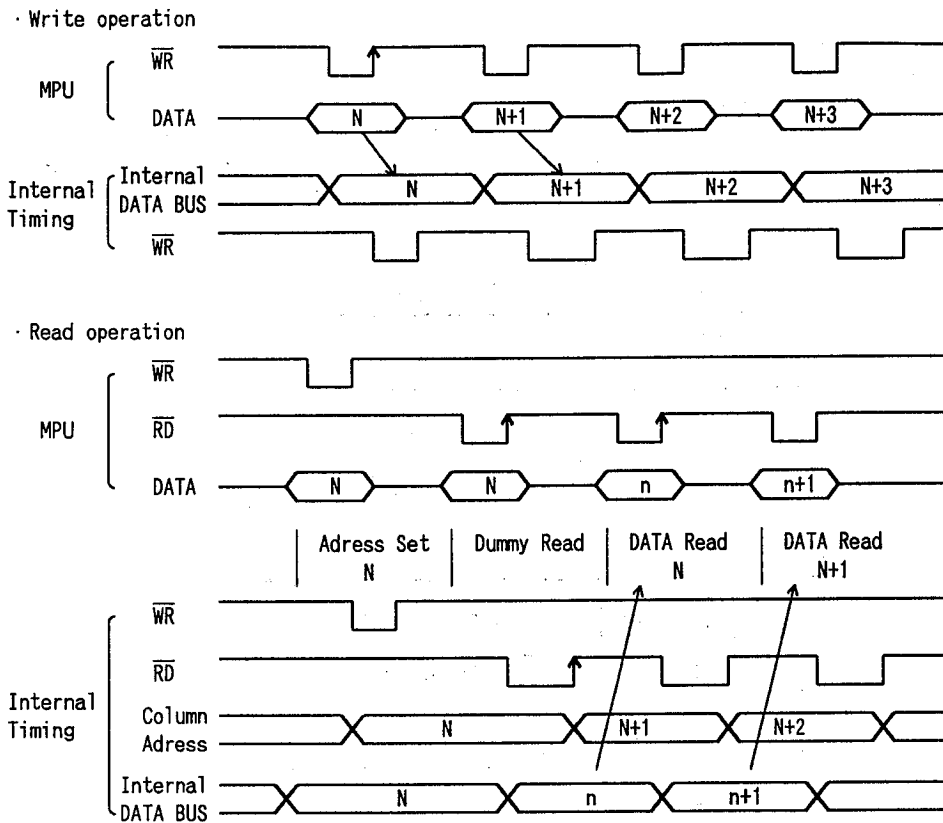


Fig.2 MPU Interface Timing

■ ABSOLUTE MAXIMUM RATINGS

(Ta=25°C)

P A R A M E T E R	S Y M B O L	R A T I N G S	U N I T
Supply Voltage (1)	V _{DD}	- 0.3 ~ + 7.0	V
Supply Voltage (2)	V ₁ ~ V ₅ (3)	V _{DD} -13.5 ~ V _{DD} +0.3	V
Input Voltage	V _{IN}	- 0.3 ~ V _{DD} +0.3	V
Operating Temperature	Topr	- 30 ~ + 80	°C
Storage Temperature	Tstg	- 55 ~ + 125	°C

Note 1) If the LSI are used on condition above the absolute maximum ratings, the LSI may be destroyed. Using the LSI within electrical characteristics is strongly recommended for normal operation. Use beyond the electric characteristics conditions will cause malfunction and poor reliability.

Note 2) All voltage values are specified as V_{SS} = 0 V.

Note 3) The relation : V_{DD} ≥ V₁ ≥ V₂ ≥ V₃ ≥ V₄ ≥ V₅ must be maintained.

■ ELECTRICAL CHARACTERISTICS

(V_{DD}=5V±10%, V_{SS}=0V, Ta=-20~+75°C)

P A R A M E T E R		SYMBOL	C O N D I T I O N S		MIN	TYP	MAX	UNIT	Note
Operating Voltage(1)	Recommend	V _{DD}			4.5	5.0	5.5	V	4
	Available				2.4		5.5		
Operating Voltage(2)	Recommend	V ₅			V _{DD} -13.5		V _{DD} -3.5	V	
	Available				V _{DD} -13.5				
	Available	V _{LCD} =V _{DD} -V ₅	V _{DD} -0.6xV _{LCD}			V _{DD}			
	Available		V ₅		V _{DD} -0.4xV _{LCD}				
Input Voltage	1	V _{IHT}	CS, AO, D ₀ ~D ₇ , E, R/W		2.0		V _{DD}	V	
		V _{ILT}	Terminals		V _{SS}		0.8		
	2	V _{IHC}	CL, FR, $\overline{\text{RST}}$		0.8xV _{DD}		V _{DD}		
		V _{ILC}	Terminals		V _{SS}		0.2xV _{DD}		
Output Voltage		V _{OHT}	D ₀ ~D ₇	I _{OH} =-3.0mA	2.4			V	
		V _{OLT}	Terminals	I _{OL} = 3.0mA			0.4		
	1	V _{OHC1}	FR Terminal	I _{OH} =-2.0mA	2.4				
		V _{OLC1}		I _{OL} = 2.0mA			0.4		
Input Leakage Current		I _{LI}	AO, E, R/W, CS, CL, $\overline{\text{RST}}$		-1.0		1.0	uA	5
		I _{LO}	D ₀ ~D ₇ , FR Terminals		-3.0		3.0		
Driver On-resistance		R _{ON}	Ta=25°C	V ₅ =V _{DD} -5.0V		5.0	7.5	kΩ	6
				V ₅ =V _{DD} -3.5V					
Stand-by Current		I _{DDQ}	CS=CL=V _{DD}			0.05	1.0	uA	
Operating Current		I _{DD1}	Display V ₅ =V _{DD} -5.0V, f _{CL} =2kHz			2.0	5.0	uA	7
		I _{DD2}	Accessing, tcyc=200kHz			300	500		
Reset time		t _r	$\overline{\text{RST}}$ Terminal		1.0		1000	us	

Note 4) NJU6452A can operate wide operating range, but it is not guarantee immediate voltage changing during the accessing of the MPU.

- Note 5) Apply to the High-impedance state of D0 to D7 and FR terminals.
- Note 6) R_{ON} is the resistance values between power supply terminals(V_1, V_2, V_3, V_4) and each output terminals of common and segment supplied by 0.1V.
- Note 7) The $IDD2$ is specified under the condition of cyclic($tcyc$)inverted data input continuously. The operating current during the accessing is proportionate to the frequency of $tcyc$. In the no accessing it is as same as $IDD1$.

BUS TIMING CHARACTERISTICS

Read / Write operation sequence (68 Type MPU)

($V_{DD}=5.0V \pm 10\%$, $V_{SS}=0V$, $T_a=-20 \sim +75^\circ C$)

P A R A M E T E R		SYMBOL	MIN	MAX	CONDITION	UNIT
Address Set Up Time	A0, R/W Terminals	t_{AW6}	20		$C_L=100pF$	ns
Address Hold Time		t_{AH6}	10			
System Cycle Time		t_{CYC6}	1000			
Enable	E Terminal	t_{EW}	100			
Pulse Width			80			
Data Set Up Time	D ₀ ~D ₇ Terminals	t_{DS6}	80			
Data Hold Time		t_{DH6}	10			
Access Time		t_{ACC6}		90		
Output Disable Time		t_{CH6}	10	60		

Note 8) Input signal rise time(t_r) and fall time(t_f) are less than 15ns.

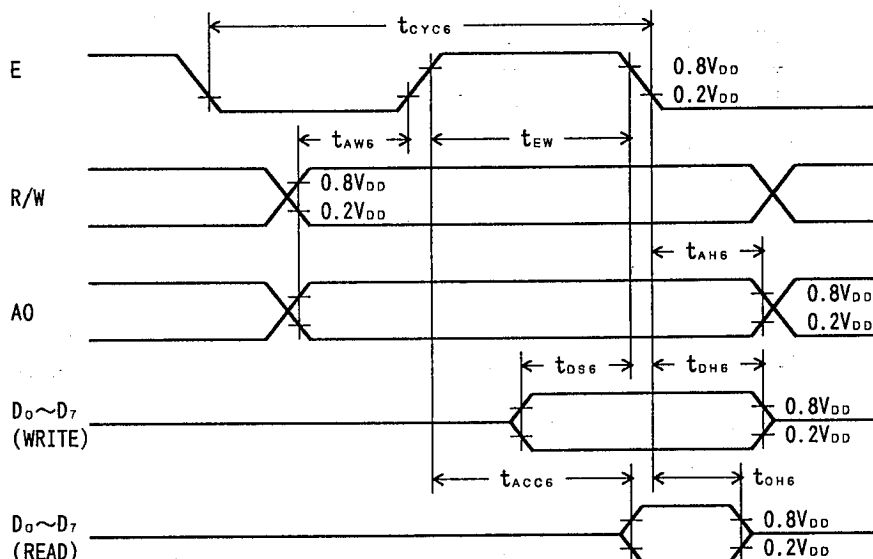


fig.3 Bus Read / Write operation sequence (68 Type MPU)

· Read / Write operation sequence (80 Type MPU)

($V_{DD}=5.0V \pm 10\%$, $V_{SS}=0V$, $T_a=-20 \sim +75^\circ C$)

P A R A M E T E R		SYMBOL	MIN	MAX	CONDITION	UNIT
Address Set Up Time	A0	t_{AWB}	20			ns
Address Hold Time	Terminal	t_{AHB}	10			
System Cycle Time	RW, WR	t_{CYCB}	1000			
Control Pulse Width	Terminals	t_{CC}	200			
Data Set Up Time	$D_0 \sim D_7$	t_{DSB}	80			
Data Hold Time		t_{DHB}	10			
RD Access Time		t_{ACCB}		90	$C_L=100pF$	
Output Disable Time	Terminals	t_{CHB}	10	60		

Note 9) Input signal rise time(t_r) and fall time(t_f) are less than 15ns.

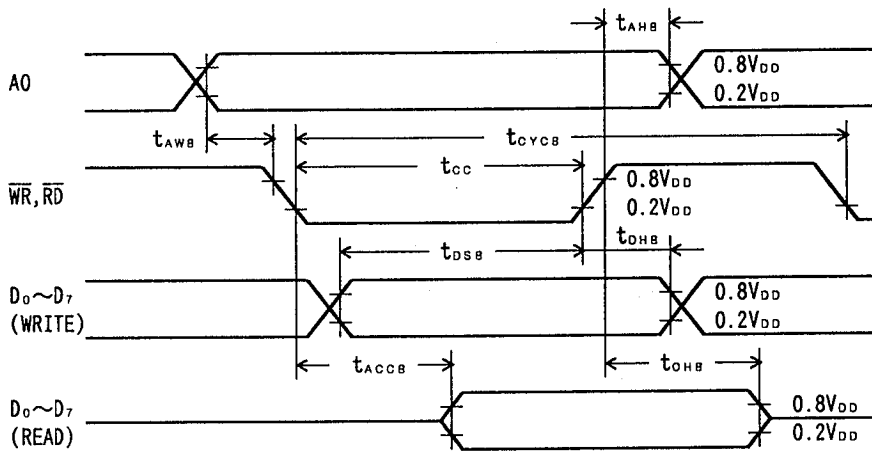


fig.4 Bus Read / Write operation sequence (80 Type MPU)

· Display control timing characteristics (Both of 68 and 80 type MPU)

Input Timing

($V_{DD}=5.0V \pm 10\%$, $V_{SS}=0V$, $T_a=-20 \sim +75^\circ C$)

PARAMETER	SYMBOL	MIN	TYP	MAX	CONDITION	UNIT
"L" level Pulse Width	t_{WLCL}	35				μs
"H" level Pulse Width	t_{WHCL}	35				
Rise Time	t_r		30	150		ns
Fall Time	t_f		30	150		
FR Delay Time (NJU6452A Slave)	t_{DFR}	-2.0		2.0		μs

Output Timing

PARAMETER	SYMBOL	MIN	TYP	MAX	CONDITION	UNIT
FR Delay Time (NJU6452A Master)	t_{DFR}		0.2	0.4	$C_L=100pF$	μs

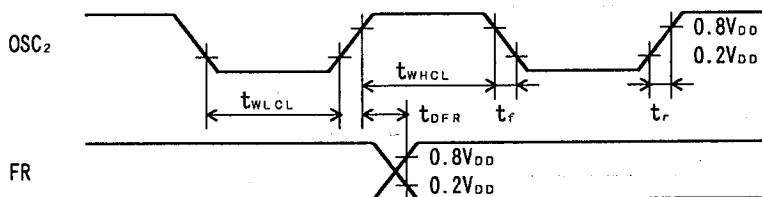
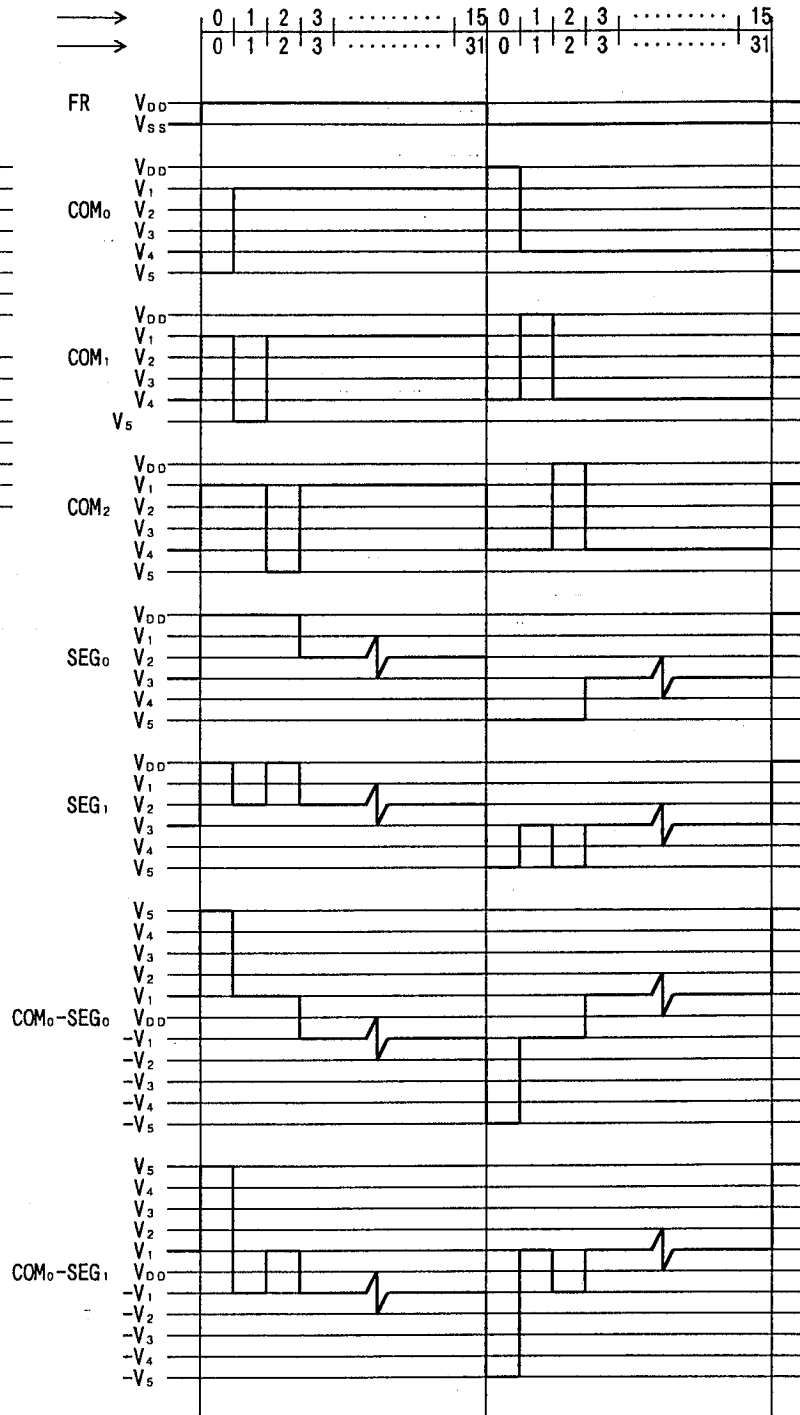
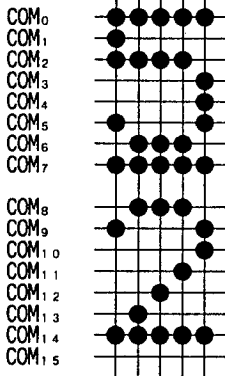


fig.5 Display control timing characteristics

LCD DRIVING WAVEFORM

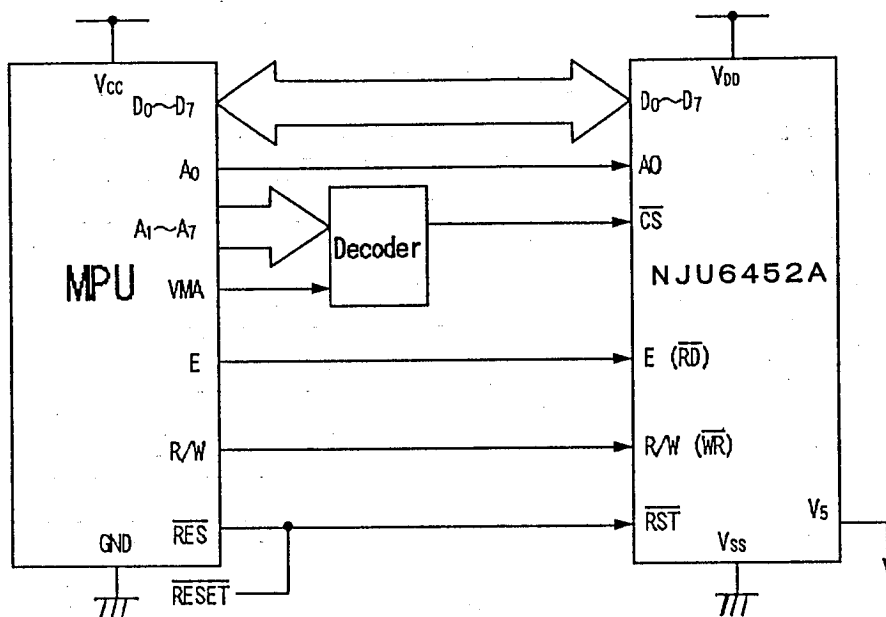
1/5 BIAS, 1/16 DUTY

1/6 BIAS, 1/32 DUTY

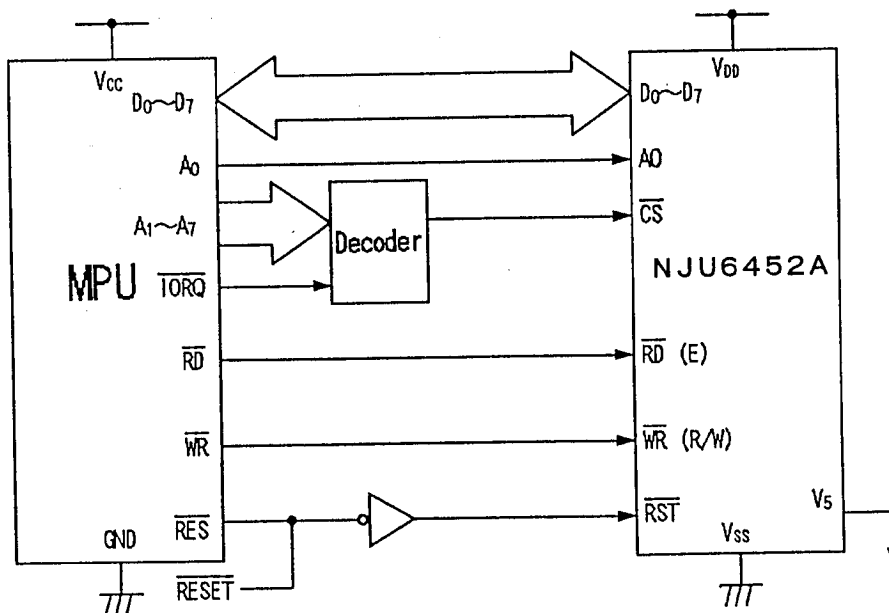


■ APPLICATION CIRCUITS 1

· 68 type MPU Interface

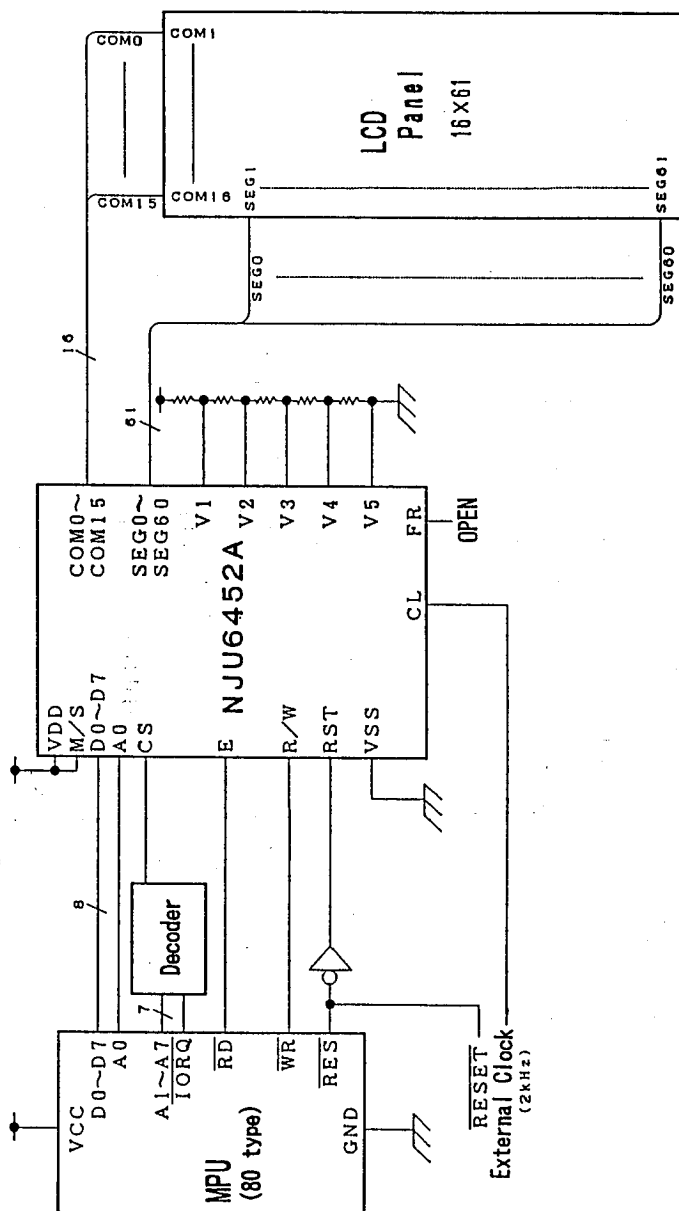


· 80 type MPU Interface



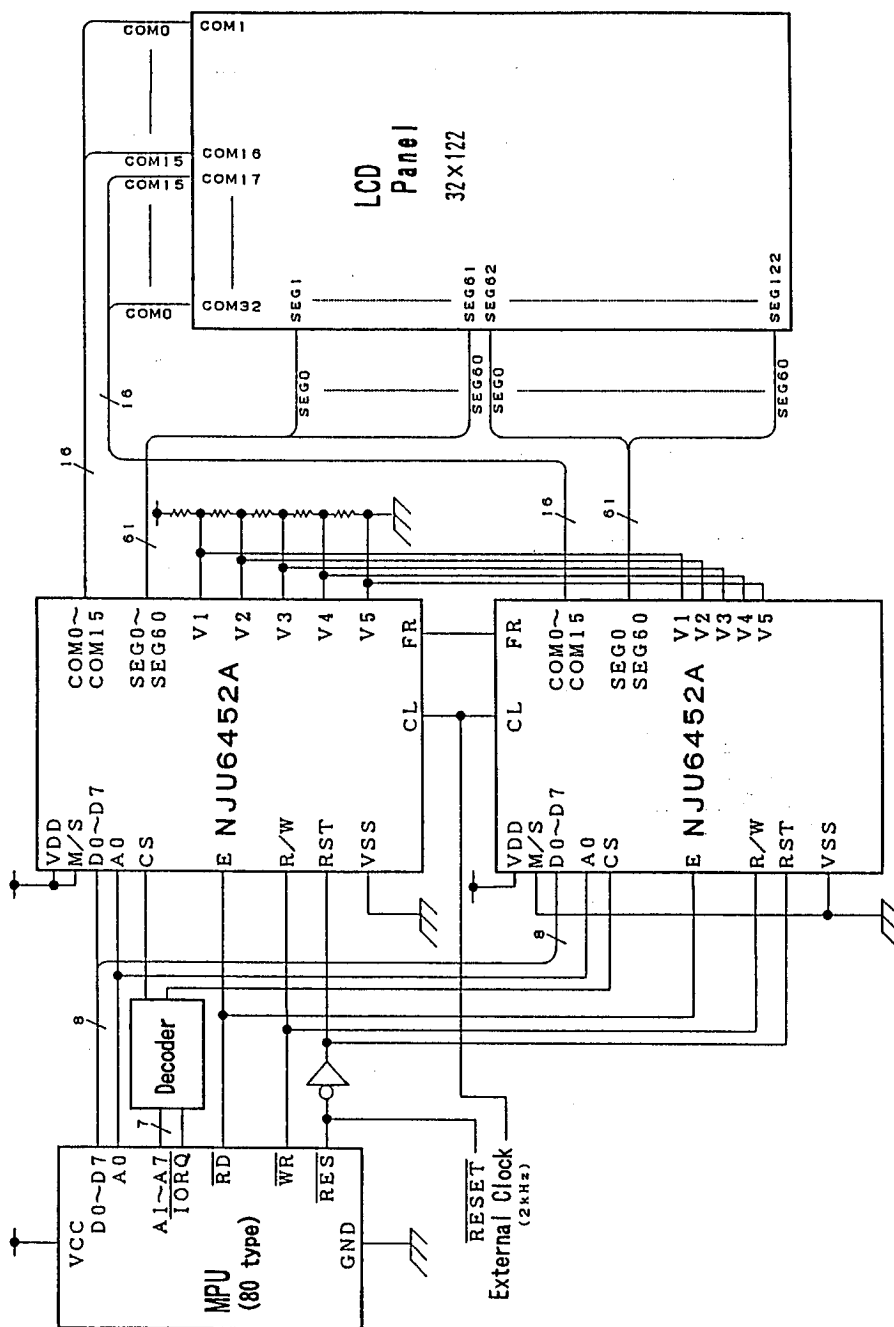
APPLICATION CIRCUITS 2

(1) 16 x 61 dots Driving Application Circuits (NJU6452A Single Operation)



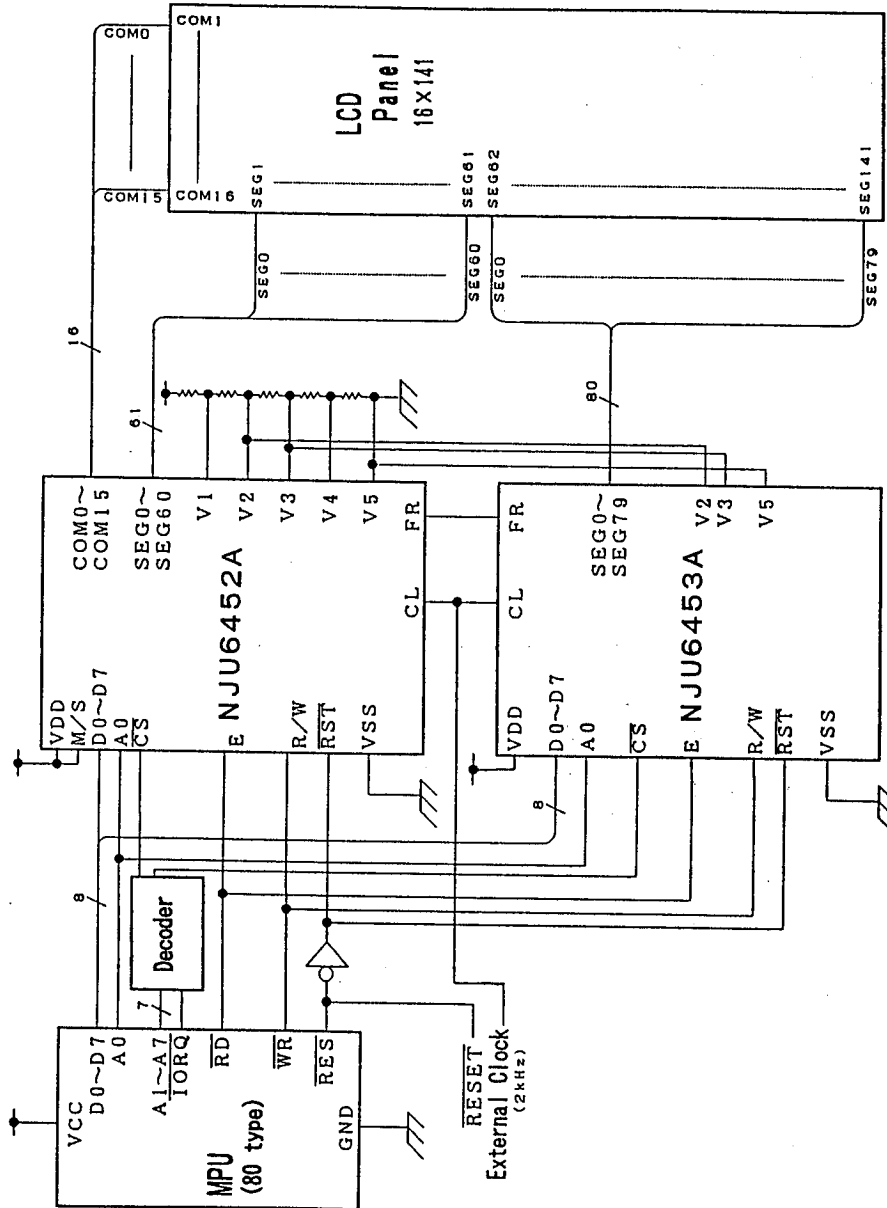
(2) 32 x 122 dots Driving Application Circuits

(Common and Segment Drivers Extension by using two of NJU6452A)



(3) 16 x 141 dots Driving Application Circuits

(Segment Drivers Extension by using NJU6453A)



MEMO

[CAUTION]

The specifications on this databook are only given for information, without any guarantee as regards either mistakes or omissions. The application circuits in this databook are described only to show representative usages of the product and not intended for the guarantee or permission of any right including the industrial rights.