

- ◇ STRUCTURE Silicon Monolithic Integrated Circuit
- ◇ PRODUCT Microwire BUS 4Kbit (256 × 16bit) EEPROM
- ◇ PART NUMBER **BR93H66-W Series**

PART NUMBER	PACKAGE
BR93H66RF-W	SOP8
BR93H66RFJ-W	SOP-J8

- ◇ FEATURES Microwire BUS EEPROM
- Wide action range -40~+125°C
- Electrostatic withstand voltage 8kV, about twice of other series (HBM method typ.)

- ◇ ABSOLUTE MAXIMUM RATING (Ta=25°C)

Parameter	Symbol	Rating	Unit
Supply Voltage	Vcc	-0.3~6.5	V
Power Dissipation	Pd	450 (BR93H66RF-W) *1	mW
		450 (BR93H66RFJ-W) *2	
Storage Temperature	Tstg	-65~150	°C
Operating Temperature	Topr	-40~125	°C
Terminal Voltage	—	-0.3~Vcc+0.3	V

* Degradation is done at 3.6mW for operation above 25°C

- ◇ RECOMMENDED OPERATING CONDITION

Parameter	Symbol	Rating	Unit
Supply Voltage	Vcc	2.7~5.5	V
Input Voltage	VIN	0~Vcc	V

Status of this document

The Japanese version of this document is the formal specification.

A customer may use this translation version only for a reference to help reading the formal version.

If there are any differences in translation version of this document, formal version takes priority.

◇ MEMORY CELL CHARACTERISTICS ($V_{CC}=2.7\sim 5.5V$)

Parameter		Specification			Unit	Test Condition
		Min.	Typ.	Max.		
Erase/Write Cycle	※1	1,000,000	—	—	Cycles	$T_a \leq 85^\circ C$
		500,000	—	—	Cycles	$T_a \leq 105^\circ C$
		300,000	—	—	Cycles	$T_a \leq 125^\circ C$
Data Retention	※1	40	—	—	Years	$T_a \leq 25^\circ C$
		10	—	—	Years	$T_a \leq 50^\circ C$

○Initial Data FFFFh in all address. ※1 Not 100% TESTED

◇ DC OPERATING CHARACTERISTICS

(Unless otherwise specified $T_a=-40\sim 125^\circ C$, $V_{CC}=2.7\sim 5.5V$)

Parameter	Symbol	Specification			Unit	Test Condition
		Min.	Typ.	Max.		
"L" Input Voltage	VIL	-0.3	—	$0.3 \times V_{CC}$	V	
"H" Input Voltage	VIH	$0.7 \times V_{CC}$	—	$V_{CC}+0.3$	V	
"L" Output Voltage1	VOL1	0	—	0.4	V	$I_{OL}=2.1mA$, $4.0 \leq V_{CC} \leq 5.5$
"L" Output Voltage2	VOL2	0	—	0.2	V	$I_{OL}=100\mu A$, $2.7 \leq V_{CC} \leq 4.0$
"H" Output Voltage1	VOH1	2.4	—	V_{CC}	V	$I_{OH}=-0.4mA$, $4.0 \leq V_{CC} \leq 5.5$
"H" Output Voltage2	VOH2	$V_{CC}-0.2$	—	V_{CC}	V	$I_{OH}=-100\mu A$, $2.7 \leq V_{CC} \leq 4.0$
Input Leakage Current	ILI	-10	—	10	μA	$V_{IN}=0\sim V_{CC}$
Output Leakage Current	ILO	-10	—	10	μA	$V_{OUT}=0\sim V_{CC}$, $CS=0V$
Operating Current	ICC1	—	—	3.0	mA	fSK=1.25MHz, tE/W=10ms (WRITE)
	ICC2	—	—	1.5	mA	fSK=1.25MHz (READ)
	ICC3	—	—	4.5	mA	fSK=1.25MHz, tE/W=10ms (WRAL)
Standby Current	ISB	—	0.1	10	μA	$CS=0V$, $DO=OPEN$

○This product is not designed for protection against radioactive rays.

◇ AC OPERATING CHARACTERISTICS

(Unless otherwise specified $T_a=-40\sim 125^\circ C$, $V_{CC}=2.7\sim 5.5V$)

Parameter	Symbol	2.7V $\leq V_{CC} \leq 5.5V$			Unit
		Min.	Typ.	Max.	
SK Clock Frequency	fSK	—	—	1.25	MHz
SK High Time	tSKH	250	—	—	ns
SK Low Time	tSKL	250	—	—	ns
CS Low Time	tCS	200	—	—	ns
CS Setup Time	tCSS	200	—	—	ns
DI Setup Time	tDIS	100	—	—	ns
CS Hold Time	tCSH	0	—	—	ns
DI Hold Time	tDIH	100	—	—	ns
Data "1" Output Delay Time	tPD1	—	—	300	ns
Data "0" Output Delay Time	tPD0	—	—	300	ns
CS to Status Valid	tSV	—	—	200	ns
CS to Output High-Z	tDF	—	—	200	ns
Write Cycle time	tE/W	—	7	10	ms

◇ BLOCK DIAGRAM

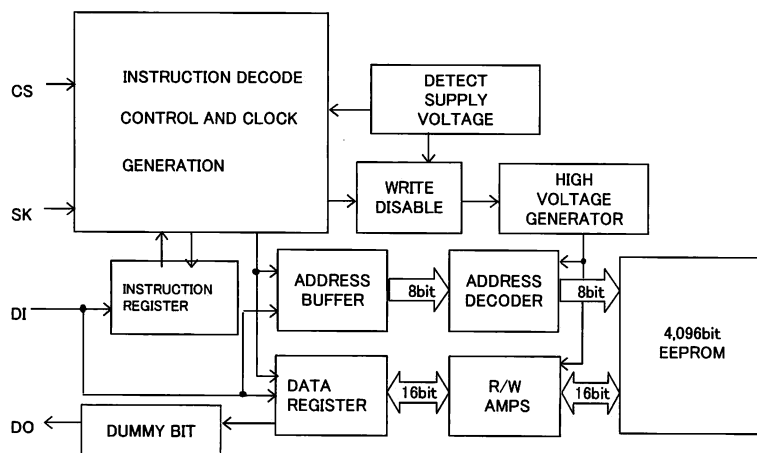


Fig.-1 BLOCK DIAGRAM

◇ PIN No. / PIN NAME

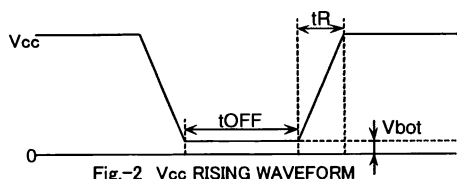
PIN No.	PIN NAME
1	CS
2	SK
3	DI
4	DO
5	GND
6	TEST1
7	TEST2
8	Vcc

◇ NOTES FOR POWER SUPPLY

This IC has a POR (Power On Reset) circuit as mistake write countermeasure.

After POR action, it gets in write disable status. The POR circuit is valid only when power is ON, and does not work when power is OFF. However, if CS is "H" at power ON/OFF, it may become write enable status owing to noises and the likes. For secure operations, observe the following conditions.

1. Set CS = "L".
2. Turn on power so as to satisfy the recommended conditions of t_R , t_{OFF} , V_{bot} for POR circuit operation.



◇ Recommended conditions of t_R , t_{OFF} , V_{bot}

t_R	t_{OFF}	V_{bot}
Below 10ms	Above 10ms	Below 0.3V
Below 100ms	Above 10ms	Below 0.2V

◇ NOTES AT TEST PIN WRONG INPUT

There is no influence of external input upon TEST2 pin.

As for TEST1 pin, input must be GND or OPEN. If "H" level is input, the following may occur.

1. At WEN, WDS, READ command input
There is no influence by TEST1 pin.
2. WRITE, WRAL command input

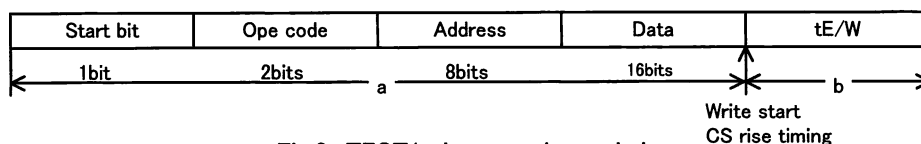


Fig.3 TEST1 pin wrong input timing

- a. There is no influence by TEST1 pin.
- b. If "H" during write execution, it may not be written correctly. And "H" area remains BUSY and READY does not go back. Avoid noise input, and at use, be sure to connect it to GND terminal or set it OPEN.

◇ CAUTIONS ON USE

(1) Absolute Maximum Ratings

If the absolute maximum ratings such as impressed voltage and action temperature range and so forth are exceeded, LSI may be destructed. Do not impress voltage and temperature exceeding the absolute maximum ratings. In the case of fear exceeding the absolute maximum ratings, take physical safety countermeasures such as fuses, and see to it that conditions exceeding the absolute maximum ratings should not be impressed to LSI.

(2) GND electric potential

Set the voltage of GND terminal lowest at any action condition. Make sure that each terminal voltage is not lower than that of GND terminal in consideration of transition status.

(3) Heat design

In consideration of allowable loss in actual use condition, carry out heat design with sufficient margin.

(4) Terminal to terminal shortcircuit and wrong packaging

When to package LSI onto a board, pay sufficient attention to LSI direction and displacement. Wrong packaging may destruct LSI. And in the case of shortcircuit between LSI terminals and terminals and power source, terminal and GND owing to foreign matter, LSI may be destructed.

(5) Use in a strong electromagnetic field may cause malfunction, therefore, evaluated design sufficiently.

◇ PHYSICAL DIMENSION

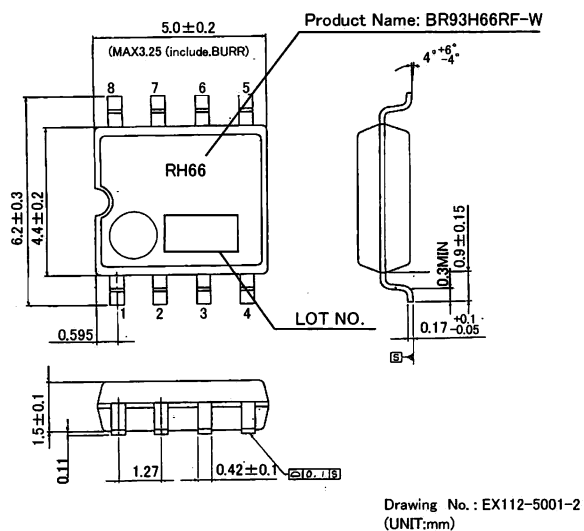


Fig.4-(a) PHYSICAL DIMENSION SOP8 (BR93H66RF-W)

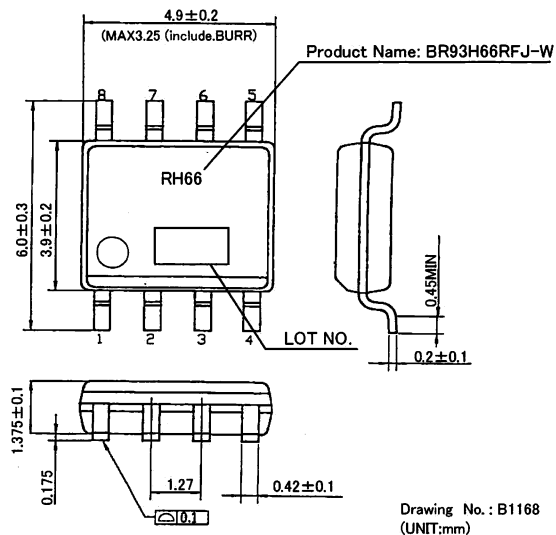


Fig.4-(b) PHYSICAL DIMENSION SOP-J8 (BR93H66RFJ-W)

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