# FAMILY OF 600µA/Ch 2.8MHz RAIL-TO-RAIL INPUT/OUTPUT HIGH-DRIVE OPERATIONAL AMPLIFIERS WITH SHUTDOWN

## FEATURES

- **CMOS Rail-To-Rail Input/Output**
- **Input Bias Current: 2.5pA**
- **Low Supply Current: 600µA/Channel**
- **Ultra-Low Power Shutdown Mode:**
  **$I_{DD(SHDN)}$: 350nA/ch at 3V**
  **$I_{DD(SHDN)}$: 1000nA/ch at 5V**
- **Gain-Bandwidth Product: 2.8MHz**
- **High Output Drive Capability:**
  - **±10mA at 180mV**
  - **±35mA at 500mV**
- **Input Offset Voltage: 250µV (typ)**
- **Supply Voltage Range: 2.7V to 6V**
- **Ultra-Small Packaging**
  - **SOT23-5 or -6 (TLV2470/1)**
  - **MSOP-8 or -10 (TLV2472/3)**

## DESCRIPTION

The TLV247x is a family of CMOS rail-to-rail input/output operational amplifiers that establishes a new performance point for supply current versus ac performance. These devices consume just 600µA/channel while offering 2.8MHz of gain-bandwidth product. Along with increased ac performance, the amplifier provides high output drive capability, solving a major shortcoming of older micropower operational amplifiers. The TLV247x can swing to within 180mV of each supply rail while driving a 10mA load. For non-RRO applications, the TLV247x can supply ±35mA at 500mV off the rail. Both the inputs and outputs swing rail-to-rail for increased dynamic range in low-voltage applications. This performance makes the TLV247x family ideal for sensor interface, portable medical equipment, and other data acquisition circuits.

### FAMILY PACKAGE TABLE

| DEVICE | NUMBER OF CHANNELS | PACKAGE TYPES | | | | | SHUTDOWN | UNIVERSAL EVM BOARD |
|---|---|---|---|---|---|---|---|---|
| | | PDIP | SOIC | SOT23 | TSSOP | MSOP | | |
| TLV2470 | 1 | 8 | 8 | 6 | — | — | Yes | Refer to the EVM Selection Guide (SLOU060) |
| TLV2471 | 1 | 8 | 8 | 5 | — | — | — | |
| TLV2472 | 2 | 8 | 8 | — | — | 8 | — | |
| TLV2473 | 2 | 14 | 14 | — | — | 10 | Yes | |
| TLV2474 | 4 | 14 | 14 | — | 14 | — | — | |
| TLV2475 | 4 | 16 | 16 | — | 16 | — | Yes | |

### A SELECTION OF SINGLE-SUPPLY OPERATIONAL AMPLIFIER PRODUCTS(1)

| DEVICE | $V_{DD}$ (V) | $V_{IO}$ (µV) | BW (MHz) | SLEW RATE (V/µs) | $I_{DD}$ (per channel) (µA) | OUTPUT DRIVE | RAIL-TO-RAIL |
|---|---|---|---|---|---|---|---|
| TLV247X | 2.7 – 6.0 | 250 | 2.8 | 1.5 | 600 | ±35mA | I/O |
| TLV245X | 2.7 – 6.0 | 20 | 0.22 | 0.11 | 23 | ±10mA | I/O |
| TLV246X | 2.7 – 6.0 | 150 | 6.4 | 1.6 | 550 | ±90mA | I/O |
| TLV277X | 2.5 – 6.0 | 360 | 5.1 | 10.5 | 1000 | ±10mA | O |

(1) All specifications measured at 5V.

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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## TLV2470 and TLV2471 AVAILABLE OPTIONS(1)

| $T_A$ | PACKAGED DEVICES | | | |
|---|---|---|---|---|
| | SMALL OUTLINE (D)(2) | SOT23 | | PLASTIC DIP (P) |
| | | (DBV)(2) | SYMBOL | |
| 0°C to +70°C | TLV2470CD<br>TLV2471CD | TLV2470CDBV<br>TLV2471CDBV | VAUC<br>VAVC | TLV2470CP<br>TLV2471CP |
| –40°C to +125°C | TLV2470ID<br>TLV2471ID | TLV2470IDBV<br>TLV2471IDBV | VAUI<br>VAVI | TLV2470IP<br>TLV2471IP |
| | TLV2470AID<br>TLV2471AID | — | — | TLV2470AIP<br>TLV2471AIP |

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) This package is available taped and reeled. To order this packaging option, add an R suffix to the part number (for example, TLV2470CDR).

## TLV2472 AND TLV2473 AVAILABLE OPTIONS(1)

| $T_A$ | PACKAGED DEVICES | | | | | | |
|---|---|---|---|---|---|---|---|
| | SMALL OUTLINE (D)(2) | MSOP | | MSOP | | PLASTIC DIP (N) | PLASTIC DIP (P) |
| | | (DGN)(2) | SYMBOL(3) | (DGQ)(2) | SYMBOL(3) | | |
| 0°C to +70°C | TLV2472CD<br>TLV2473CD | TLV2472CDGN<br>— | xxTIABU<br>— | —<br>TLV2473CDGQ | —<br>xxTIABW | —<br>TLV2473CN | TLV2472CP<br>— |
| –40°C to +125°C | TLV2472ID<br>TLV2473ID | TLV2472IDGN<br>— | xxTIABV<br>— | —<br>TLV2473IDGQ | —<br>xxTIABX | —<br>TLV2473IN | TLV2472IP<br>— |
| | TLV2472AID<br>TLV2473AID | — | — | — | — | —<br>TLV2473AIN | TLV2472AIP<br>— |

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) This package is available taped and reeled. To order this packaging option, add an R suffix to the part number (for example, TLV2472CDR).
(3) xx represents the device date code.

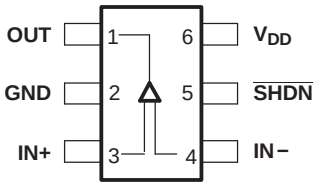
## TLV2474 and TLV2475 AVAILABLE OPTIONS(1)

| $T_A$ | PACKAGED DEVICES | | |
|---|---|---|---|
| | SMALL OUTLINE (D)(2) | PLASTIC DIP (N) | TSSOP (PWP)(2) |
| 0°C to +70°C | TLV2474CD<br>TLV2475CD | TLV2474CN<br>TLV2475CN | TLV2474CPWP<br>TLV2475CPWP |
| –40°C to +125°C | TLV2474ID<br>TLV2475ID | TLV2474IN<br>TLV2475IN | TLV2474IPWP<br>TLV2475IPWP |
| | TLV2474AID<br>TLV2475AID | TLV2474AIN<br>TLV2475AIN | TLV2474AIPWP<br>TLV2475AIPWP |

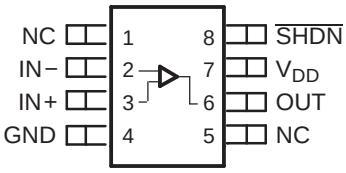
(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) This package is available taped and reeled. To order this packaging option, add an R suffix to the part number (for example, TLV2474CDR).

## TLV247X PACKAGE PINOUTS

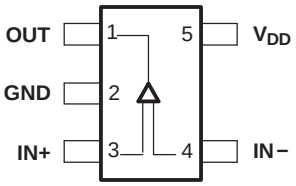
**TLV2470**
**DBV PACKAGE**
**(TOP VIEW)**



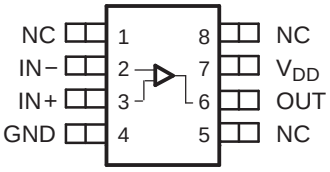

**TLV2470**
**D OR P PACKAGE**
**(TOP VIEW)**



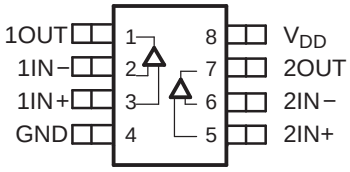

**TLV2471**
**DBV PACKAGE**
**(TOP VIEW)**



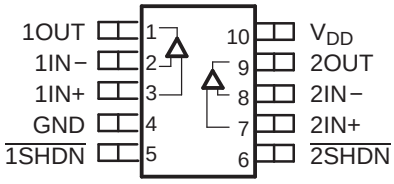

**TLV2471**
**D OR P PACKAGE**
**(TOP VIEW)**



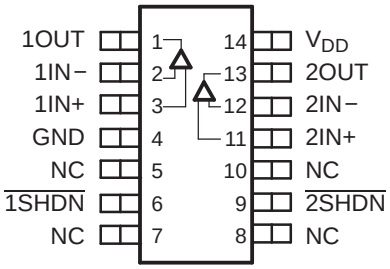

**TLV2472**
**D, DGN, OR P PACKAGE**
**(TOP VIEW)**



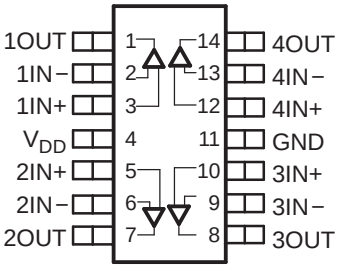

**TLV2473**
**DGQ PACKAGE**
**(TOP VIEW)**



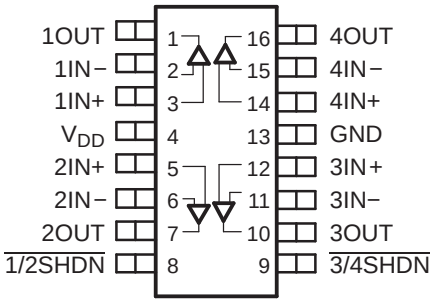

**TLV2473**
**D OR N PACKAGE**
**(TOP VIEW)**




**TLV2474**
**D, N, OR PWP PACKAGE**
**(TOP VIEW)**

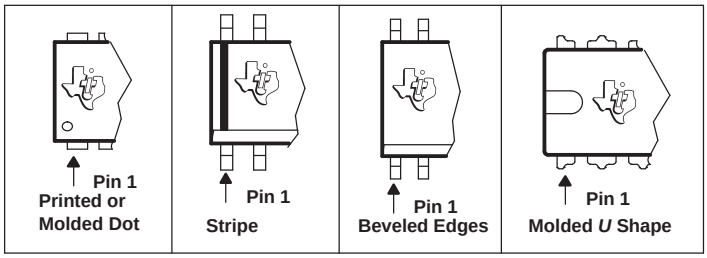



**TLV2475**
**D, N, OR PWP PACKAGE**
**(TOP VIEW)**




NC − No internal connection

**TYPICAL PIN 1 INDICATORS**



## DESCRIPTION (CONTINUED)

Three members of the family (TLV2470/3/5) offer a shutdown terminal for conserving battery life in portable applications. During shutdown, the outputs are placed in a high-impedance state and the amplifier consumes only 350nA/channel. The family is fully specified at 3V and 5V across an expanded industrial temperature range (–40°C to +125°C). The singles and duals are available in the SOT23 and MSOP packages, while the quads are available in TSSOP. The TLV2470 offers an amplifier with shutdown functionality all in a SOT23-6 package, making it perfect for high-density power-sensitive circuits.

## ABSOLUTE MAXIMUM RATINGS(1)

Over operating free-air temperature range, unless otherwise noted.

| | | UNIT |
|---|---|---|
| Supply voltage, $V_{DD}$(2) | | 7V |
| Differential input voltage, $V_{ID}$ | | $\pm V_{DD}$ |
| Continuous total power dissipation | | See Dissipation Rating table |
| Operating free-air temperature range, $T_A$ | C-suffix | 0°C to +70°C |
| | I-suffix | –40°C to +125°C |
| Maximum junction temperature, $T_J$ | | +150°C |
| Storage temperature range, $T_{stg}$ | | –65°C to +150°C |
| Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds | | +260°C |

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under*recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential voltages, are with respect to GND.

## DISSIPATION RATING TABLE

| PACKAGE | $\theta_{JC}$ (°C/W) | $\theta_{JA}$ (°C/W) | $T_A \leq +25°C$ POWER RATING |
|---|---|---|---|
| D (8) | 38.3 | 176 | 710mW |
| D (14) | 26.9 | 122.3 | 1022mW |
| D (16) | 25.7 | 114.7 | 1090mW |
| DBV (5) | 55 | 324.1 | 385mW |
| DBV (6) | 55 | 294.3 | 425mW |
| DGN (8) | 4.7 | 52.7 | 2.37W |
| DGQ (10) | 4.7 | 52.3 | 2.39W |
| N (14, 16) | 32 | 78 | 1600mW |
| P (8) | 41 | 104 | 1200mW |
| PWP (14) | 2.07 | 30.7 | 4.07W |
| PWP (16) | 2.07 | 29.7 | 4.21W |

## RECOMMENDED OPERATING CONDITIONS

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| Supply voltage, $V_{DD}$ | Single supply | 2.7 | 6 | V |
| | Split supply | ±1.35 | ±3 | |
| Common-mode input voltage range, $V_{ICR}$ | | 0 | $V_{DD}$ | V |
| Operating free-air temperature, $T_A$ | C-suffix | 0 | +70 | °C |
| | I-suffix | –40 | +125 | |
| Shutdown on/off voltage level(1) | $V_{IH}$ | 2 | | V |
| | $V_{IL}$ | | 0.8 | |

(1) Relative to GND.

## ELECTRICAL CHARACTERISTICS

At specified free-air temperature, $V_{DD}$ = 3V, unless otherwise noted.

| PARAMETER | | TEST CONDITIONS | | $T_A$ (1) | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| $V_{IO}$ | Input offset voltage | $V_{IC} = V_{DD}/2$, $V_O = V_{DD}/2$, $R_S = 50\Omega$ | TLV247x | +25°C | | 250 | 2200 | µV |
| | | | | Full range | | | 2400 | |
| | | | TLV247xA | +25°C | | 250 | 1600 | |
| | | | | Full range | | | 1800 | |
| $\alpha_{VIO}$ | Temperature coefficient of input offset voltage | | | | | 0.4 | | µV/°C |
| $I_{IO}$ | Input offset current | | | 25°C | | 1.5 | 50 | pA |
| | | | TLV247xC | Full range | | | 100 | |
| | | | TLV247xI | Full range | | | 300 | |
| $I_{IB}$ | Input bias current | | | +25°C | | 2 | 50 | |
| | | | TLV247xC | Full range | | | 100 | |
| | | | TLV247xI | Full range | | | 300 | |
| $V_{OH}$ | High-level output voltage | $V_{IC} = V_{DD}/2$ | $I_{OH}$ = –2.5mA | +25°C | 2.85 | 2.94 | | V |
| | | | | Full range | 2.8 | | | |
| | | | $I_{OH}$ = –10mA | +25°C | 2.6 | 2.74 | | |
| | | | | Full range | 2.5 | | | |
| $V_{OL}$ | Low-level output voltage | $V_{IC} = V_{DD}/2$ | $I_{OL}$ = 2.5mA | +25°C | | 0.07 | 0.15 | V |
| | | | | Full range | | | 0.2 | |
| | | | $I_{OL}$ = 10mA | +25°C | | 0.2 | 0.35 | |
| | | | | Full range | | | 0.5 | |
| $I_{OS}$ | Short-circuit output current | Sourcing | | +25°C | 30 | | | mA |
| | | | | Full range | 20 | | | |
| | | Sinking | | +25°C | 30 | | | |
| | | | | Full range | 20 | | | |
| $I_O$ | Output current | $V_O$ = 0.5V from rail | | +25°C | | ±22 | | mA |
| $A_{VD}$ | Large-signal differential voltage amplification | $V_{O(PP)}$ = 1V, $R_L$ = 10kΩ | | +25°C | 90 | 116 | | dB |
| | | | | Full range | 88 | | | |
| $r_{i(d)}$ | Differential input resistance | | | +25°C | | $10^{12}$ | | Ω |
| $C_{IC}$ | Common-mode input capacitance | f = 10kHz | | +25°C | | 19.3 | | pF |
| $z_o$ | Closed-loop output impedance | f = 10kHz, $A_V$ = 10 | | +25°C | | 2 | | Ω |
| CMRR | Common-mode rejection ratio | $V_{IC}$ = 0V to 3V, $R_S$ = 50Ω | | +25°C | 61 | 78 | | dB |
| | | | TLV247xC | Full range | 59 | | | |
| | | | TLV247xI | Full range | 58 | | | |

(1) Full range is 0°C to +70°C for C-suffix and –40°C to +125°C for I-suffix. If not specified, full range is –40°C to +125°C.

## ELECTRICAL CHARACTERISTICS (continued)

At specified free-air temperature, $V_{DD}$ = 3V, unless otherwise noted.

| PARAMETER | | TEST CONDITIONS | | $T_A$ (1) | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| $k_{SVR}$ | Supply voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$) | $V_{DD}$ = 2.7V to 6V, $V_{IC}$ = $V_{DD}$/2, No load | | +25°C | 74 | 90 | | dB |
| | | | | Full range | 66 | | | |
| | | $V_{DD}$ = 3V to 5V, $V_{IC}$ = $V_{DD}$/2, No load | | +25°C | 77 | 92 | | |
| | | | | Full range | 68 | | | |
| $I_{DD}$ | Supply current (per channel) | $V_O$ = 1.5V, No load | | +25°C | | 550 | 750 | µA |
| | | | | Full range | | | 800 | |
| $I_{DD(SHDN)}$ | Supply current in shutdown mode (TLV2470, TLV2473, TLV2475) (per channel) | $\overline{SHDN}$ = 0V | | +25°C | | 350 | 1500 | nA |
| | | | TLV247xC | Full range | | | 2000 | |
| | | | TLV247xI | Full range | | | 4000 | |

(1) Full range is 0°C to +70°C for C-suffix and –40°C to +125°C for I-suffix. If not specified, full range is –40°C to +125°C.

## OPERATING CHARACTERISTICS

At specified free-air temperature, $V_{DD}$ = 3V, unless otherwise noted.

| PARAMETER | | TEST CONDITIONS | | $T_A$ (1) | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| SR | Slew rate at unity gain | $V_{O(PP)}$ = 0.8V, $C_L$ = 150pF, $R_L$= 10kΩ | | +25°C | 1.1 | 1.4 | | V/µs |
| | | | | Full range | 0.6 | | | |
| $V_n$ | Equivalent input noise voltage | f = 100Hz | | +25°C | | 28 | | nV/√Hz |
| | | f = 1kHz | | +25°C | | 15 | | |
| $I_n$ | Equivalent input noise current | f = 1kHz | | +25°C | | 0.405 | | pA/√Hz |
| THD+N | Total harmonic distortion plus noise | $V_{O(PP)}$ = 2V, $R_L$= 10kΩ, f = 1kHz | $A_V$ = 1 | +25°C | | 0.02% | | |
| | | | $A_V$ = 10 | | | 0.1% | | |
| | | | $A_V$ = 100 | | | 0.5% | | |
| $t_{(on)}$ | Amplifier turn-on time | $R_L$= OPEN (2) | | +25°C | | 5 | | µs |
| $t_{(off)}$ | Amplifier turn-off time | | | +25°C | | 250 | | ns |
| | Gain-bandwidth product | f = 10kHz, $R_L$ = 600Ω | | +25°C | | 2.8 | | MHz |
| $t_s$ | Settling time | $V_{(STEP)PP}$ = 2V, $A_V$ = –1, $C_L$ = 10pF, $R_L$ = 10kΩ | 0.1% | +25°C | | 1.5 | | µs |
| | | | 0.01% | | | 3.9 | | |
| | | $V_{(STEP)PP}$ = 2V, $A_V$ = –1, $C_L$ = 56pF, $R_L$ = 10kΩ | 0.1% | | | 1.6 | | |
| | | | 0.01% | | | 4 | | |
| $\Phi_m$ | Phase margin | $R_L$ = 10kΩ, $C_L$ = 1000pF | | +25°C | | 61 | | ° |
| | Gain margin | $R_L$ = 10kΩ, $C_L$ = 1000pF | | +25°C | | 15 | | dB |

(1) Full range is 0°C to +70°C for C-suffix and –40°C to +125°C for I-suffix. If not specified, full range is –40°C to +125°C.
(2) Disable and enable time are defined as the interval between application of logic signal to $\overline{SHDN}$ and the point at which the supply current has reached half its final value.

## ELECTRICAL CHARACTERISTICS

At specified free-air temperature, $V_{DD}$ = 5V, unless otherwise noted.

| PARAMETER | | TEST CONDITIONS | | $T_A$ (1) | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| $V_{IO}$ | Input offset voltage | $V_{IC} = V_{DD}/2$, $V_O = V_{DD}/2$, $R_S = 50\Omega$ | TLV247x | +25°C | | 250 | 2200 | μV |
| | | | | Full range | | | 2400 | |
| | | | TLV247xA | +25°C | | 250 | 1600 | |
| | | | | Full range | | | 2000 | |
| $\alpha_{VIO}$ | Temperature coefficient of input offset voltage | | | | | 0.4 | | μV/°C |
| $I_{IO}$ | Input offset current | | | +25°C | | 1.7 | 50 | pA |
| | | | TLV247xC | Full range | | | 100 | |
| | | | TLV247xI | Full range | | | 300 | |
| $I_{IB}$ | Input bias current | | | +25°C | | 2.5 | 50 | |
| | | | TLV247xC | Full range | | | 100 | |
| | | | TLV247xI | Full range | | | 300 | |
| $V_{OH}$ | High-level output voltage | $V_{IC} = V_{DD}/2$ | $I_{OH}$ = –2.5mA | +25°C | 4.85 | 4.96 | | V |
| | | | | Full range | 4.8 | | | |
| | | | $I_{OH}$ = –10mA | +25°C | 4.72 | 4.82 | | |
| | | | | Full range | 4.65 | | | |
| $V_{OL}$ | Low-level output voltage | $V_{IC} = V_{DD}/2$ | $I_{OL}$ = 2.5mA | +25°C | | 0.07 | 0.15 | V |
| | | | | Full range | | | 0.2 | |
| | | | $I_{OL}$ = 10mA | +25°C | | 0.178 | 0.28 | |
| | | | | Full range | | | 0.35 | |
| $I_{OS}$ | Short-circuit output current | Sourcing | | +25°C | 110 | | | mA |
| | | | | Full range | 60 | | | |
| | | Sinking | | +25°C | 90 | | | |
| | | | | Full range | 60 | | | |
| $I_O$ | Output current | $V_O$ = 0.5V from rail | | +25°C | | ±35 | | mA |
| $A_{VD}$ | Large-signal differential voltage amplification | $V_{O(PP)}$ = 3V, $R_L$ = 10kΩ | | +25°C | 92 | 120 | | dB |
| | | | | Full range | 91 | | | |
| $r_{i(d)}$ | Differential input resistance | | | +25°C | | $10^{12}$ | | Ω |
| $C_{IC}$ | Common-mode input capacitance | f = 10kHz | | +25°C | | 18.9 | | pF |
| $z_o$ | Closed-loop output impedance | f = 10kHz, $A_V$ = 10 | | +25°C | | 1.8 | | Ω |
| CMRR | Common-mode rejection ratio | $V_{IC}$ = 0V to 5V, $R_S$ = 50Ω | | +25°C | 64 | 84 | | dB |
| | | | TLV247xC | Full range | 63 | | | |
| | | | TLV247xI | Full range | 58 | | | |
| $k_{SVR}$ | Supply voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$) | $V_{DD}$ = 2.7V to 6V, $V_{IC} = V_{DD}/2$, No load | | +25°C | 74 | 90 | | dB |
| | | | | Full range | 66 | | | |
| | | $V_{DD}$ = 3V to 5V, $V_{IC} = V_{DD}/2$, No load | | +25°C | 77 | 92 | | |
| | | | | Full range | 66 | | | |
| $I_{DD}$ | Supply current (per channel) | $V_O$ = 2.5V, No load | | +25°C | | 600 | 900 | μA |
| | | | | Full range | | | 1000 | |

(1) Full range is 0°C to +70°C for C-suffix and –40°C to +125°C for I-suffix. If not specified, full range is –40°C to +125°C.

## ELECTRICAL CHARACTERISTICS (continued)

At specified free-air temperature, $V_{DD}$ = 5V, unless otherwise noted.

| PARAMETER | | TEST CONDITIONS | | $T_A$ (1) | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| $I_{DD(SHDN)}$ | Supply current in shutdown mode (TLV2470, TLV2473, TLV2475) (per channel) | $\overline{SHDN}$ = 0V | | +25°C | | 1000 | 2500 | nA |
| | | | TLV247xC | Full range | | | 3000 | |
| | | | TLV247xI | Full range | | | 6000 | nA |

(1) Full range is 0°C to +70°C for C-suffix and –40°C to +125°C for I-suffix. If not specified, full range is –40°C to +125°C.

## OPERATING CHARACTERISTICS

At specified free-air temperature, $V_{DD}$ = 5V, unless otherwise noted.

| PARAMETER | | TEST CONDITIONS | | $T_A$ (1) | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| SR | Slew rate at unity gain | $V_{O(PP)}$ = 2V, $C_L$ = 150pF, $R_L$= 10kΩ | | +25°C | 1.1 | 1.5 | | V/μs |
| | | | | Full range | 0.7 | | | |
| $V_n$ | Equivalent input noise voltage | f = 100Hz | | +25°C | | 28 | | nV/√Hz |
| | | f = 1kHz | | +25°C | | 15 | | |
| $I_n$ | Equivalent input noise current | f = 1kHz | | +25°C | | 0.39 | | pA/√Hz |
| THD + N | Total harmonic distortion plus noise | $V_{O(PP)}$ = 4V, $R_L$= 10kΩ, f = 1kHz | $A_V$ = 1 | +25°C | | 0.01% | | |
| | | | $A_V$ = 10 | | | 0.05% | | |
| | | | $A_V$ = 100 | | | 0.3% | | |
| $t_{(on)}$ | Amplifier turn-on time | $R_L$= OPEN (2) | | +25°C | | 5 | | μs |
| $t_{(off)}$ | Amplifier turn-off time | | | +25°C | | 250 | | ns |
| | Gain-bandwidth product | f = 10kHz, $R_L$ = 600Ω | | +25°C | | 2.8 | | MHz |
| $t_s$ | Settling time | $V_{(STEP)PP}$ = 2V, $A_V$ = –1, $C_L$ = 10pF, $R_L$ = 10kΩ | 0.1% | +25°C | | 1.8 | | μs |
| | | | 0.01% | | | 3.3 | | |
| | | $V_{(STEP)PP}$ = 2V, $A_V$ = –1, $C_L$ = 56pF, $R_L$ = 10kΩ | 0.1% | | | 1.7 | | |
| | | | 0.01% | | | 3 | | |
| $\Phi_m$ | Phase margin | $R_L$ = 10kΩ, $C_L$ = 1000pF | | +25°C | | 68 | | °C |
| | Gain margin | $R_L$ = 10kΩ, $C_L$ = 1000pF | | +25°C | | 23 | | dB |

(1) Full range is 0°C to +70°C for C suffix and –40°C to +125°C for I suffix. If not specified, full range is –40°C to +125°C.
(2) Disable and enable time are defined as the interval between application of logic signal to $\overline{SHDN}$ and the point at which the supply current has reached half its final value.

## TYPICAL CHARACTERISTICS

### Table of Graphs

| | | | FIGURE |
|---|---|---|---|
| $V_{IO}$ | Input offset voltage | vs Common-mode input voltage | Figure 1, Figure 2 |
| $I_{IB}$ | Input bias current | vs Free-air temperature | Figure 3, Figure 4 |
| $I_{IO}$ | Input offset current | | |
| $V_{OH}$ | High-level output voltage | vs High-level output current | Figure 5, Figure 7 |
| $V_{OL}$ | Low-level output voltage | vs Low-level output current | Figure 6, Figure 8 |
| $Z_o$ | Output impedance | vs Frequency | Figure 9 |
| $I_{DD}$ | Supply current | vs Supply voltage | Figure 10 |
| PSRR | Power-supply rejection ratio | vs Frequency | Figure 11 |
| CMRR | Common-mode rejection ratio | vs Frequency | Figure 12 |
| $V_n$ | Equivalent input noise voltage | vs Frequency | Figure 13 |
| $V_{O(PP)}$ | Maximum peak-to-peak output voltage | vs Frequency | Figure 14, Figure 15 |
| $A_{VD}$ | Differential voltage gain and phase | vs Frequency | Figure 16, Figure 17 |
| $\Phi_m$ | Phase margin | vs Load capacitance | Figure 18, Figure 19 |
| | Gain margin | vs Load capacitance | Figure 20, Figure 21 |
| | Gain-bandwidth product | vs Supply voltage | Figure 22 |
| SR | Slew rate | vs Supply voltage | Figure 23 |
| | | vs Free-air temperature | Figure 24, Figure 25 |
| | Crosstalk | vs Frequency | Figure 26 |
| THD+N | Total harmonic distortion + noise | vs Frequency | Figure 27, Figure 28 |
| $V_O$ | Large and small signal follower | vs Time | Figure 29–Figure 32 |
| | Shutdown pulse response | vs Time | Figure 33, Figure 34 |
| | Shutdown forward and reverse isolation | vs Frequency | Figure 35, Figure 36 |
| $I_{DD(SHDN)}$ | Shutdown supply current | vs Supply voltage | Figure 37 |
| $I_{DD(SHDN)}$ | Shutdown supply current | vs Free-air temperature | Figure 38 |
| $I_{DD(SHDN)}$ | Shutdown pulse current | vs Time | Figure 39, Figure 40 |

## TYPICAL CHARACTERISTICS

### INPUT OFFSET VOLTAGE vs COMMON-MODE INPUT VOLTAGE

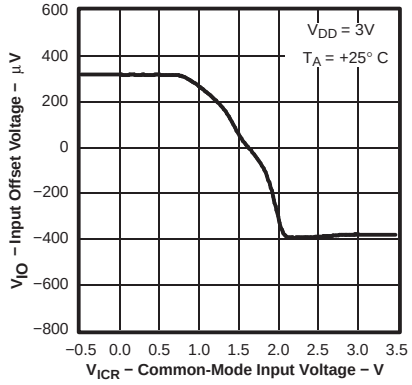



Figure 1.

### INPUT OFFSET VOLTAGE vs COMMON-MODE INPUT VOLTAGE

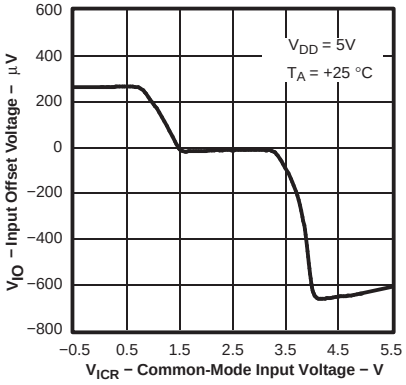



Figure 2.

### INPUT BIAS AND INPUT OFFSET CURRENTS vs FREE-AIR TEMPERATURE

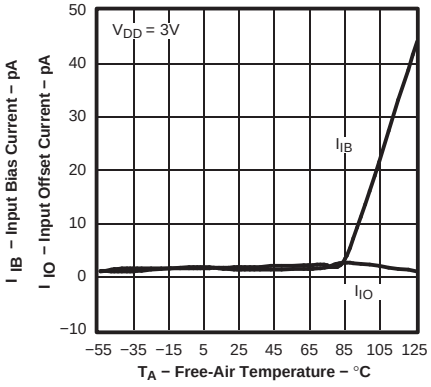



Figure 3.

### INPUT BIAS AND INPUT OFFSET CURRENTS vs FREE-AIR TEMPERATURE

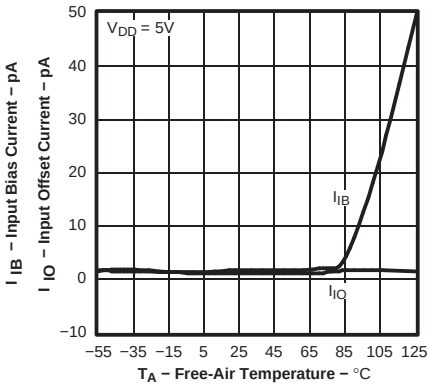



Figure 4.

### HIGH-LEVEL OUTPUT VOLTAGE vs HIGH-LEVEL OUTPUT CURRENT

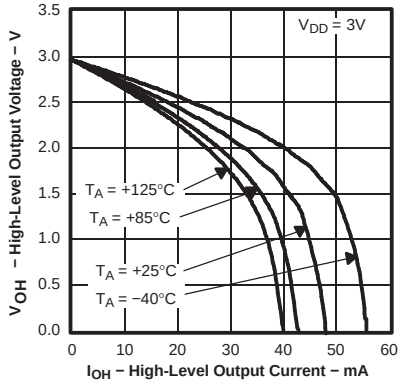



Figure 5.

### LOW-LEVEL OUTPUT VOLTAGE vs LOW-LEVEL OUTPUT CURRENT

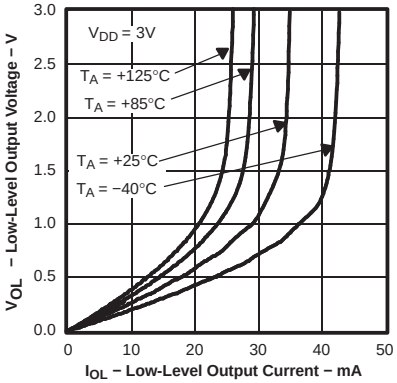



Figure 6.

### HIGH-LEVEL OUTPUT VOLTAGE vs HIGH-LEVEL OUTPUT CURRENT

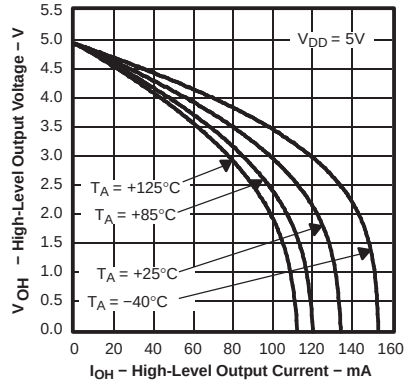



Figure 7.

### LOW-LEVEL OUTPUT VOLTAGE vs LOW-LEVEL OUTPUT CURRENT

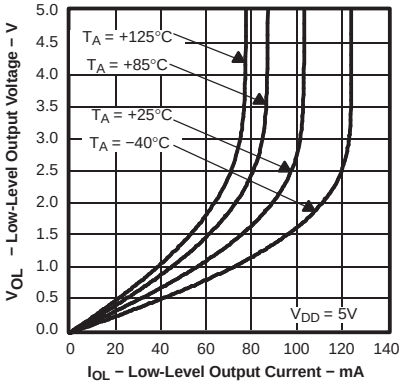



Figure 8.

### OUTPUT IMPEDANCE vs FREQUENCY

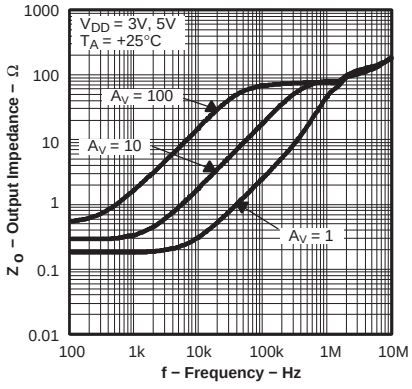



Figure 9.

## TYPICAL CHARACTERISTICS (continued)

**SUPPLY CURRENT vs SUPPLY VOLTAGE**

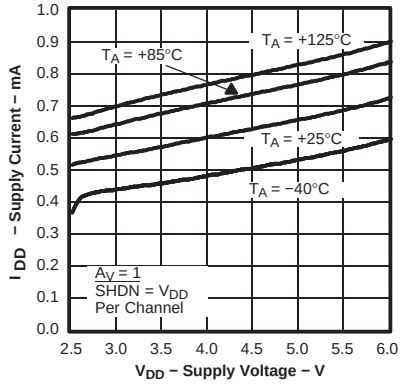



Figure 10.

**POWER-SUPPLY REJECTION RATIO vs FREQUENCY**

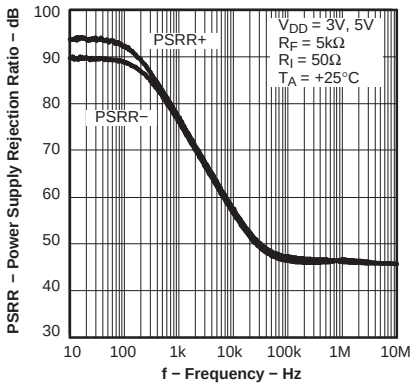



Figure 11.

**COMMON-MODE REJECTION RATIO vs FREQUENCY**

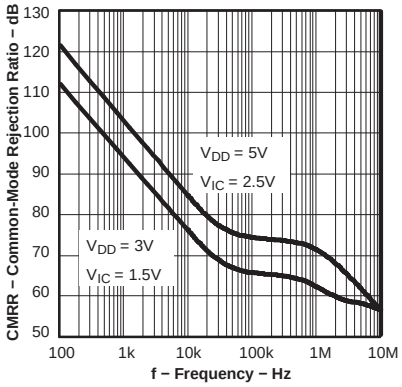



Figure 12.

**EQUIVALENT NOISE VOLTAGE vs FREQUENCY**

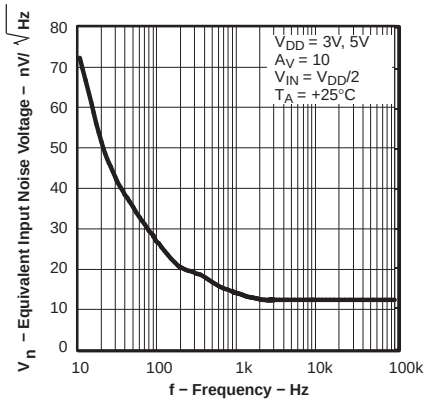



Figure 13.

**MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE vs FREQUENCY**

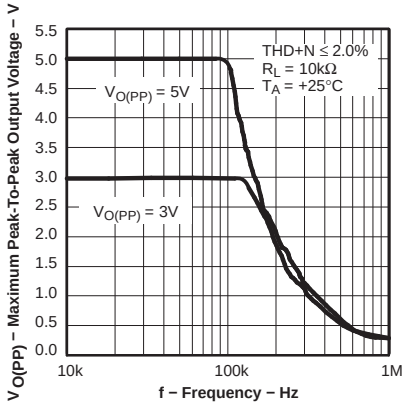



Figure 14.

**MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE vs FREQUENCY**

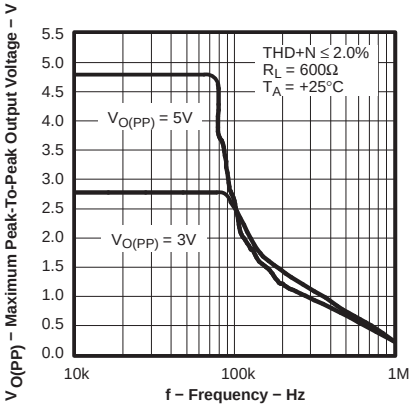



Figure 15.

**DIFFERENTIAL VOLTAGE GAIN AND PHASE vs FREQUENCY**

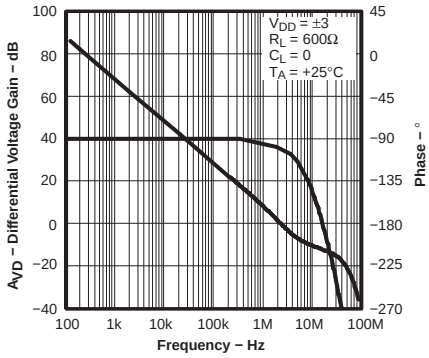



Figure 16.

**DIFFERENTIAL VOLTAGE GAIN AND PHASE vs FREQUENCY**

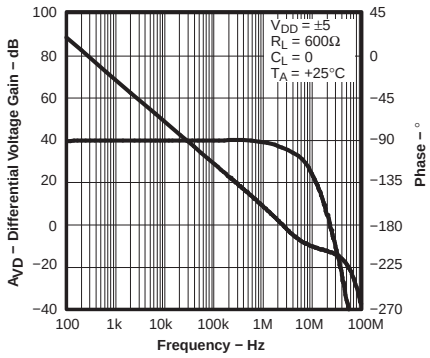



Figure 17.

## TYPICAL CHARACTERISTICS (continued)

**PHASE MARGIN vs LOAD CAPACITANCE**

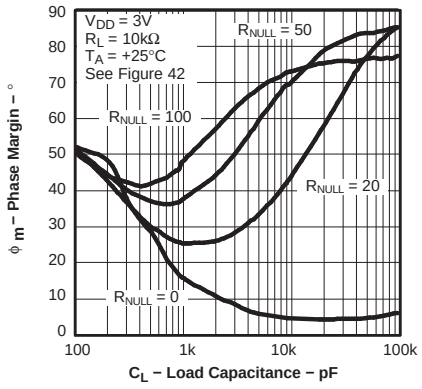



Figure 18.

**PHASE MARGIN vs LOAD CAPACITANCE**

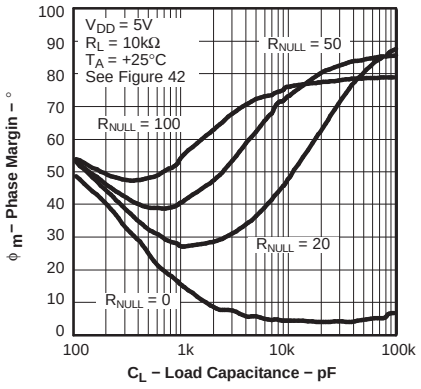



Figure 19.

**GAIN MARGIN vs LOAD CAPACITANCE**

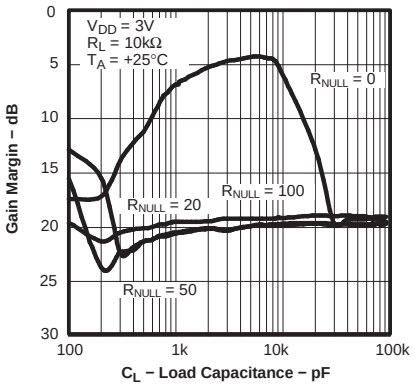



Figure 20.

**GAIN MARGIN vs LOAD CAPACITANCE**

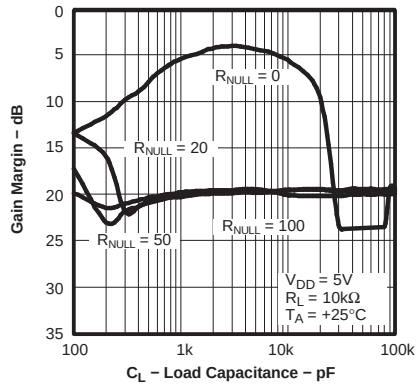



Figure 21.

**GAIN-BANDWIDTH PRODUCT vs SUPPLY VOLTAGE**

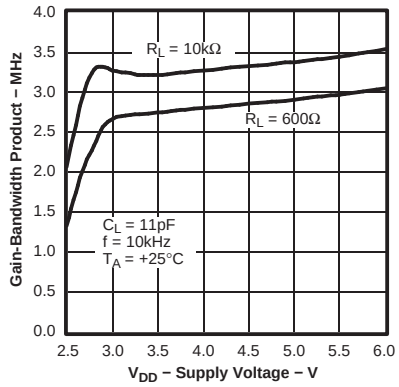



Figure 22.

**SLEW RATE vs SUPPLY VOLTAGE**

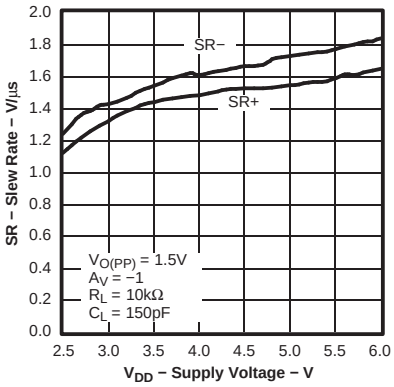



Figure 23.

**SLEW RATE vs FREE-AIR TEMPERATURE**

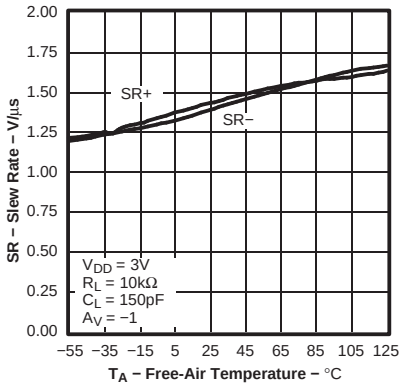



Figure 24.

**SLEW RATE vs FREE-AIR TEMPERATURE**

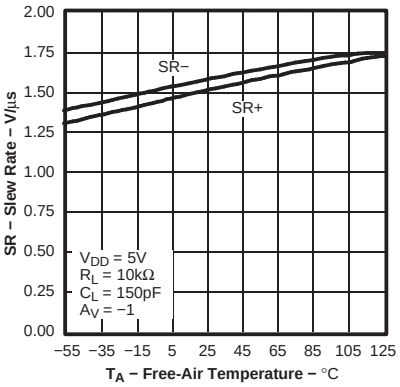



Figure 25.

## TYPICAL CHARACTERISTICS (continued)

**CROSSTALK vs FREQUENCY**

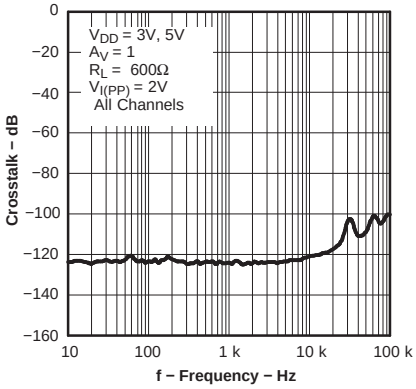



Figure 26.

**TOTAL HARMONIC DISTORTION PLUS NOISE vs FREQUENCY**

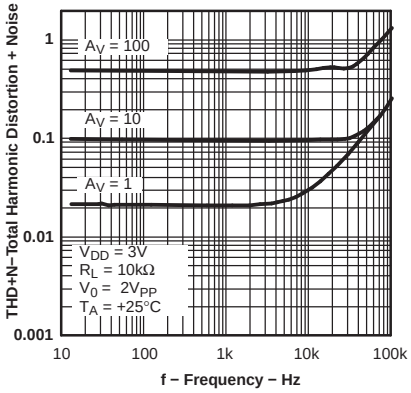



Figure 27.

**TOTAL HARMONIC DISTORTION PLUS NOISE vs FREQUENCY**

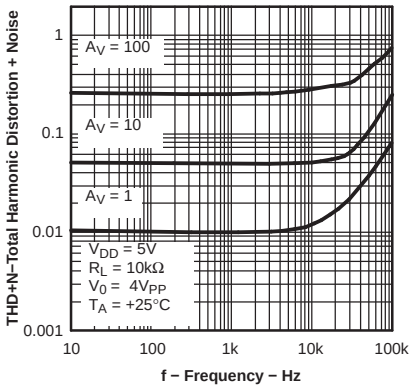



Figure 28.

**LARGE-SIGNAL FOLLOWER PULSE RESPONSE vs TIME**

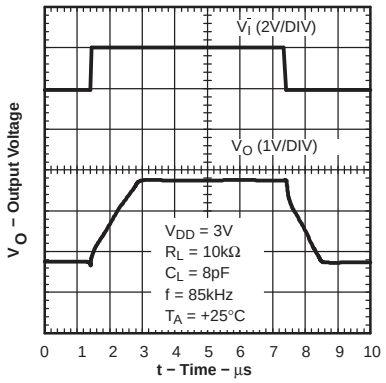



Figure 29.

**LARGE-SIGNAL FOLLOWER PULSE RESPONSE vs TIME**

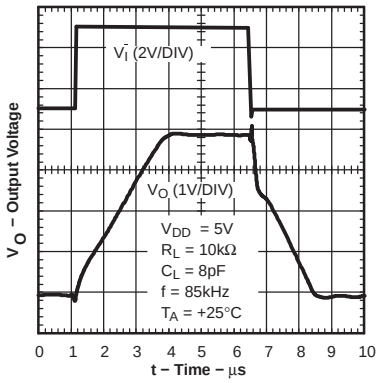



Figure 30.

**SMALL-SIGNAL FOLLOWER PULSE RESPONSE vs TIME**

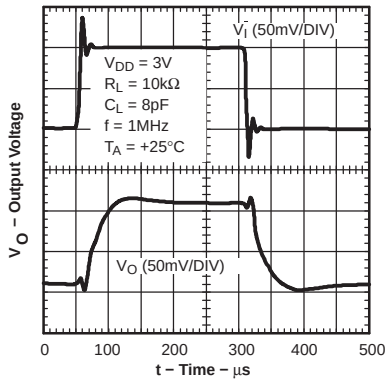



Figure 31.

**SMALL-SIGNAL FOLLOWER PULSE RESPONSE vs TIME**

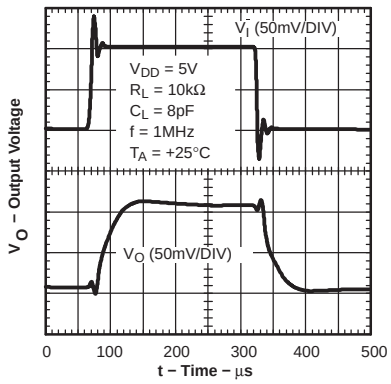



Figure 32.

**SHUTDOWN (ON AND OFF) PULSE RESPONSE vs TIME**

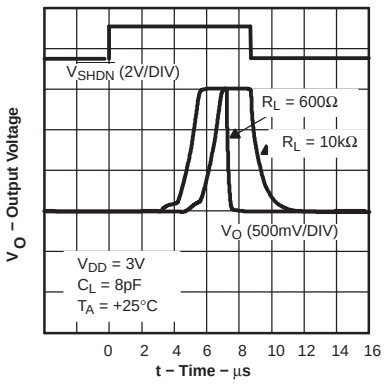



Figure 33.

**SHUTDOWN (ON AND OFF) PULSE RESPONSE vs TIME**

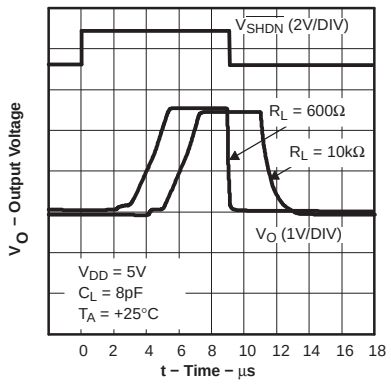



Figure 34.

## TYPICAL CHARACTERISTICS (continued)

**SHUTDOWN FORWARD ISOLATION vs FREQUENCY**

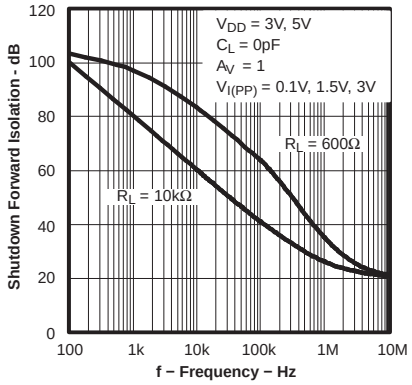



Figure 35.

**SHUTDOWN REVERSE ISOLATION vs FREQUENCY**

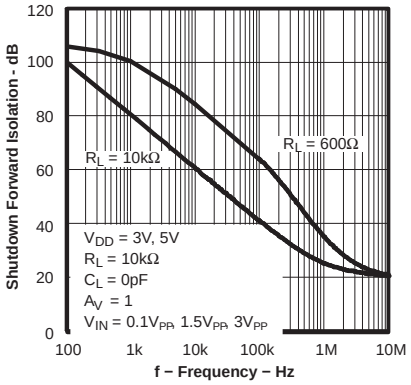



Figure 36.

**SHUTDOWN SUPPLY CURRENT vs SUPPLY VOLTAGE**

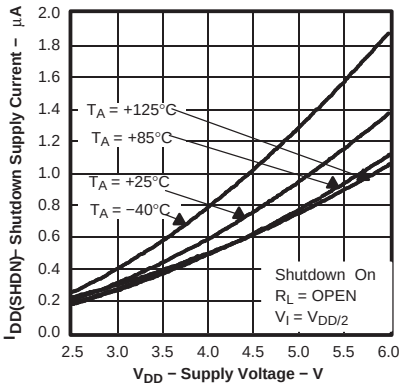



Figure 37.

**SHUTDOWN SUPPLY CURRENT vs FREE-AIR TEMPERATURE**

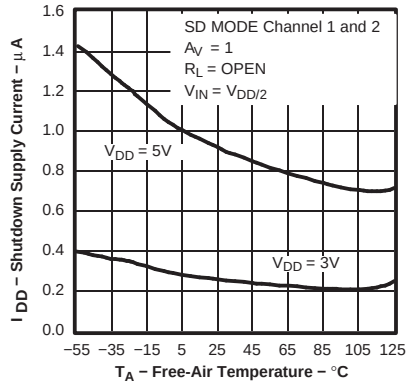



Figure 38.

**SHUTDOWN PULSE CURRENT vs TIME**

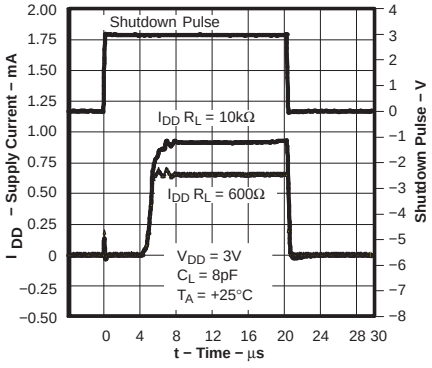



Figure 39.

**SHUTDOWN PULSE CURRENT vs TIME**

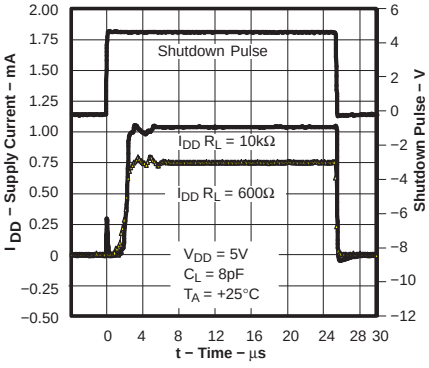



Figure 40.

## PARAMETER MEASUREMENT INFORMATION

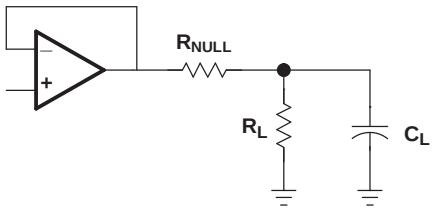



**Figure 41.**

## APPLICATION INFORMATION

### DRIVING A CAPACITIVE LOAD

When the amplifier is configured in this manner, capacitive loading directly on the output will decrease the device phase margin leading to high-frequency ringing or oscillations. Therefore, for capacitive loads of greater than 10pF, it is recommended that a resistor ($R_{NULL}$) be placed in series with the output of the amplifier, as shown in Figure 42. A minimum value of 20Ω should work well for most applications.

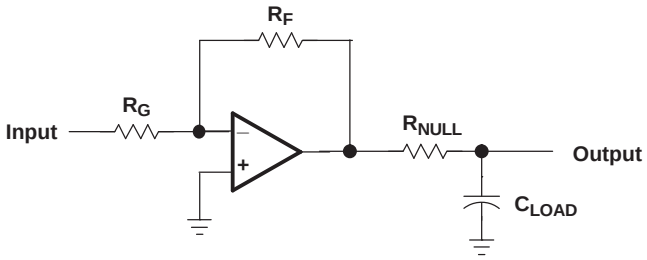
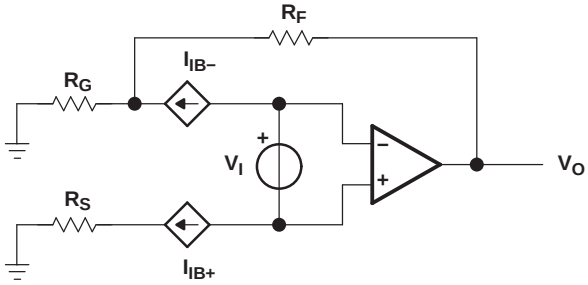



**Figure 42. Driving a Capacitive Load**

### OFFSET VOLTAGE

The output offset voltage ($V_{OO}$) is the sum of the input offset voltage ($V_{IO}$) and both input bias currents ($I_{IB}$) times the corresponding gains. The following schematic and formula can be used to calculate the output offset voltage:




$$V_{OO} = V_{IO}\left(1 + \left(\frac{R_F}{R_G}\right)\right) \pm I_{IB+} R_S \left(1 + \left(\frac{R_F}{R_G}\right)\right) \pm I_{IB-} R_F$$

**Figure 43. Output Offset Voltage Model**

## APPLICATION INFORMATION (continued)

### GENERAL CONFIGURATIONS

When receiving low-level signals, limiting the bandwidth of the incoming signals into the system is often required. The simplest way to accomplish this is to place an RC filter at the noninverting terminal of the amplifier (see Figure 44).

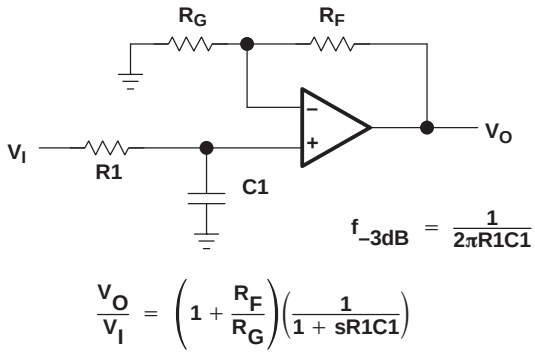



**Figure 44. Single-Pole Low-Pass Filter**

If even more attenuation is needed, a multiple pole filter is required. The Sallen-Key filter can be used for this task. For best results, the amplifier should have a bandwidth that is eight to ten times the filter frequency bandwidth. Failure to do this can result in phase shift of the amplifier.

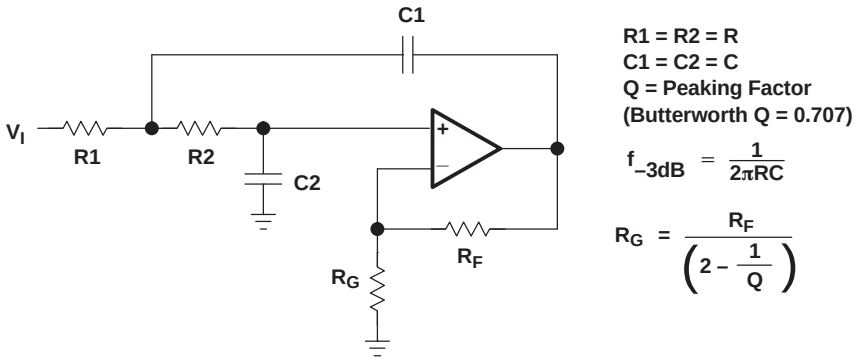



**Figure 45. 2-Pole Low-Pass Sallen-Key Filter**

### SHUTDOWN FUNCTION

Three members of the TLV247x family (TLV2470/3/5) have a shutdown terminal for conserving battery life in portable applications. When the shutdown terminal is tied low, the supply current is reduced to 350nA/channel, the amplifier is disabled, and the outputs are placed in a high impedance mode. To enable the amplifier, the shutdown terminal can either be left floating or pulled high. When the shutdown terminal is left floating, care should be taken to ensure that parasitic leakage current at the shutdown terminal does not inadvertently place the operational amplifier into shutdown. The shutdown terminal threshold is always referenced to $V_{DD}/2$. Therefore, when operating the device with split supply voltages (e.g., ±2.5V), the shutdown terminal needs to be pulled to $V_{DD}$– (not GND) to disable the operational amplifier.

The amplifier output with a shutdown pulse is shown in Figure 33 and Figure 34. The amplifier is powered with a single 5V supply and configured as a noninverting configuration with a gain of 5. The amplifier turn-on and turn-off times are measured from the 50% point of the shutdown pulse to the 50% point of the output waveform. The times for the single, dual, and quad versions are listed in the data tables.

## APPLICATION INFORMATION (continued)

Figure 35 and Figure 36 show the amplifier forward and reverse isolation in shutdown. The operational amplifier is powered by ±1.35V supplies and configured as a voltage follower ($A_V$= 1). The isolation performance is plotted across frequency using $0.1V_{PP}$, $1.5V_{PP}$, and $2.5V_{PP}$ input signals. During normal operation, the amplifier would not be able to handle a $2.5V_{PP}$ input signal with a supply voltage of ±1.35V since it exceeds the common-mode input voltage range ($V_{ICR}$). However, this curve illustrates that the amplifier remains in shutdown even under a worst case scenario.

## CIRCUIT LAYOUT CONSIDERATIONS

To achieve the levels of high performance of the TLV247x, follow proper printed circuit board (PCB) design techniques. A general set of guidelines is given below:

- Ground planes—It is highly recommended that a ground plane be used on the board to provide all components with a low inductive ground connection. However, in the areas of the amplifier inputs and output, the ground plane can be removed to minimize the stray capacitance.
- Proper power supply decoupling—Use a 6.8μF tantalum capacitor in parallel with a 0.1μF ceramic capacitor on each supply terminal. It may be possible to share the tantalum among several amplifiers depending on the application, but a 0.1μF ceramic capacitor should always be used on the supply terminal of every amplifier. In addition, the 0.1μF capacitor should be placed as close as possible to the supply terminal. As this distance increases, the inductance in the connecting trace makes the capacitor less effective. The designer should strive for distances of less than 0.1 inches between the device power terminals and the ceramic capacitors.
- Sockets—Sockets can be used but are not recommended. The additional lead inductance in the socket pins will often lead to stability problems. Surface-mount packages soldered directly to the printed-circuit board is the best implementation.
- Short trace runs/compact part placements—Optimum high performance is achieved when stray series inductance has been minimized. To realize this, the circuit layout should be made as compact as possible, thereby minimizing the length of all trace runs. Particular attention should be paid to the inverting input of the amplifier. Its length should be kept as short as possible. This will help to minimize stray capacitance at the input of the amplifier.
- Surface-mount passive components—Using surface-mount passive components is recommended for high-performance amplifier circuits for several reasons. First, because of the extremely low lead inductance of surface-mount components, the problem with stray series inductance is greatly reduced. Second, the small size of surface-mount components naturally leads to a more compact layout thereby minimizing both stray inductance and capacitance. If leaded components are used, it is recommended that the lead lengths be kept as short as possible.

## GENERAL PowerPAD™ DESIGN CONSIDERATIONS

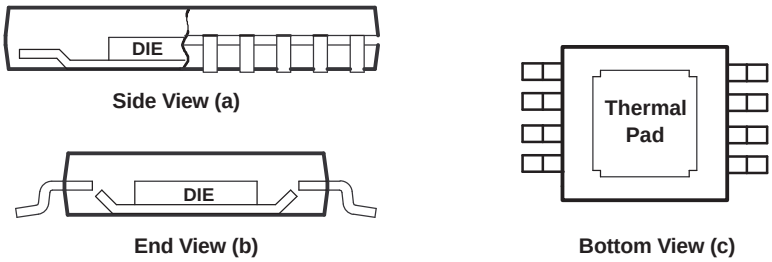
The TLV247x is available in a thermally-enhanced PowerPAD family of packages. These packages are constructed using a downset leadframe upon which the die is mounted (see Figure 46a and Figure 46b). This arrangement results in the lead frame being exposed as a thermal pad on the underside of the package (see Figure 46c). Because this thermal pad has direct thermal contact with the die, excellent thermal performance can be achieved by providing a good thermal path away from the thermal pad.

The PowerPAD package allows for both assembly and thermal management in one manufacturing operation. During the surface-mount solder operation (when the leads are being soldered), the thermal pad must be soldered to a copper area underneath the package. Through the use of thermal paths within this copper area, heat can be conducted away from the package into either a ground plane or other heat dissipating device.

Soldering the PowerPAD to the PCB is always recommended, even with applications that have low power dissipation. It provides the necessary mechanical and thermal connection between the lead frame die pad and the PCB.

The PowerPAD package represents a breakthrough in combining the small area and ease of assembly of surface mount with previously awkward mechanical methods of heatsinking.

## APPLICATION INFORMATION (continued)




The thermal pad is electrically isolated from all terminals in the package.

**Figure 46. Views of Thermally Enhanced DGN Package**

Although there are many ways to properly heatsink the PowerPAD package, the following steps illustrate the recommended approach.

1. The thermal pad must be connected to the most negative supply voltage on the device (GND pin).
2. Prepare the PCB with a top side etch pattern as illustrated in the thermal land pattern mechanical drawing at the end of this document. There should be etch for the leads as well as etch for the thermal pad.
3. Place holes in the area of the thermal pad as illustrated in the land pattern mechanical drawing at the end of this document. These holes should be 13mils (0.013 inches or 0.3302mm) in diameter. Keep them small so that solder wicking through the holes is not a problem during reflow.
4. Additional vias may be placed anywhere along the thermal plane outside of the thermal pad area. This helps dissipate the heat generated by the TLV247x IC. These additional vias may be larger than the 13mil diameter vias directly under the thermal pad. They can be larger because they are not in the thermal pad area to be soldered so that wicking is not a problem.
5. Connect all holes to the internal ground plane that is at the same voltage potential as the device GND pin.
6. When connecting these holes to the ground plane, **do not** use the typical web or spoke via connection methodology. Web connections have a high thermal resistance connection that is useful for slowing the heat transfer during soldering operations. This makes the soldering of vias that have plane connections easier. In this application, however, low thermal resistance is desired for the most efficient heat transfer. Therefore, the holes under the TLV247x PowerPAD package should make their connection to the internal ground plane with a complete connection around the entire circumference of the plated-through hole.
7. The top-side solder mask should leave the terminals of the package and the thermal pad area with its holes exposed. The bottom-side solder mask should cover the holes of the thermal pad area. This prevents solder from being pulled away from the thermal pad area during the reflow process.
8. Apply solder paste to the exposed thermal pad area and all of the IC terminals.
9. With these preparatory steps in place, the TLV247x IC is simply placed in position and run through the solder reflow operation as any standard surface-mount component. This results in a part that is properly installed.

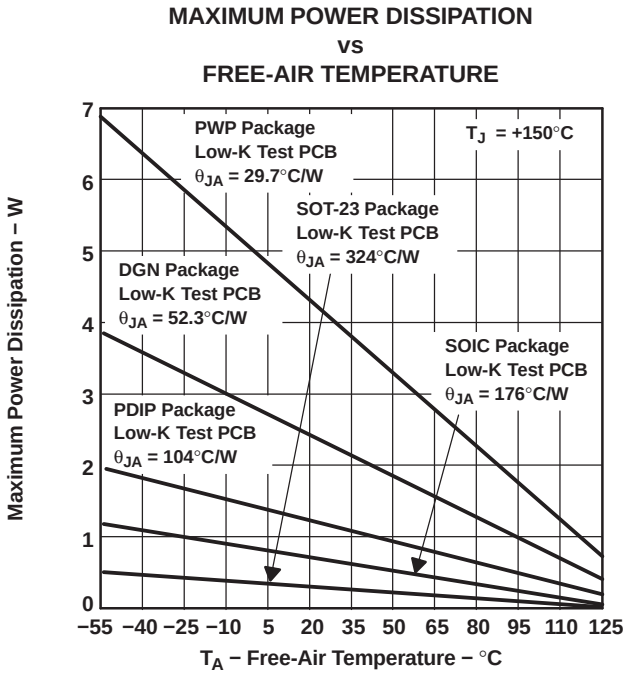
For a given $\theta_{JA}$, the maximum power dissipation is shown in Figure 47 and is calculated by Equation 1:

$$P_D = \left( \frac{T_{MAX} - T_A}{\theta_{JA}} \right) \quad (1)$$

Where:

- $P_D$ = Maximum power dissipation of TLV247x IC (watts)
- $T_{MAX}$ = Absolute maximum junction temperature (+150°C)
- $T_A$ = Free-ambient air temperature (°C)
- $\theta_{JA} = \theta_{JC} + \theta_{CA}$
  - $\theta_{JC}$ = Thermal coefficient from junction to case
  - $\theta_{CA}$ = Thermal coefficient from case to ambient air (°C/W)

## APPLICATION INFORMATION (continued)




Results are obtained with no air flow and using JEDEC Standard Low-K test PCB.

**Figure 47. Maximum Power Dissipation vs Free-Air Temperature**

The next consideration is the package constraints. The two sources of heat within an amplifier are quiescent power and output power. The designer should never forget about the quiescent heat generated within the device, especially multi-amplifier devices. Because these devices have linear output stages (Class A-B), most of the heat dissipation is at low output voltages with high output currents. Figure 48 to Figure 53 show this effect, along with the quiescent heat, with an ambient air temperature of +70°C and +125°C. When using $V_{DD}$ = 3V, there is generally not a heat problem with an ambient air temperature of +70°C. But, when using $V_{DD}$ = 5V, the package is severely limited in the amount of heat it can dissipate. The other key factor when looking at these graphs is how the devices are mounted on the PCB. The PowerPAD devices are extremely useful for heat dissipation. But the device should always be soldered to a copper plane to fully use the heat dissipation properties of the PowerPAD. The SOIC package, on the other hand, is highly dependent on how it is mounted on the PCB. As more trace and copper area is placed around the device, $\theta_{JA}$ decreases and the heat dissipation capability increases. The currents and voltages shown in these graphs are for the total package. For the dual or quad amplifier packages, the sum of the RMS output currents and voltages should be used to choose the proper package.

## APPLICATION INFORMATION (continued)

TLV2470, TLV2471(1)
MAXIMUM RMS OUTPUT CURRENT
vs
RMS OUTPUT VOLTAGE DUE TO THERMAL LIMITS

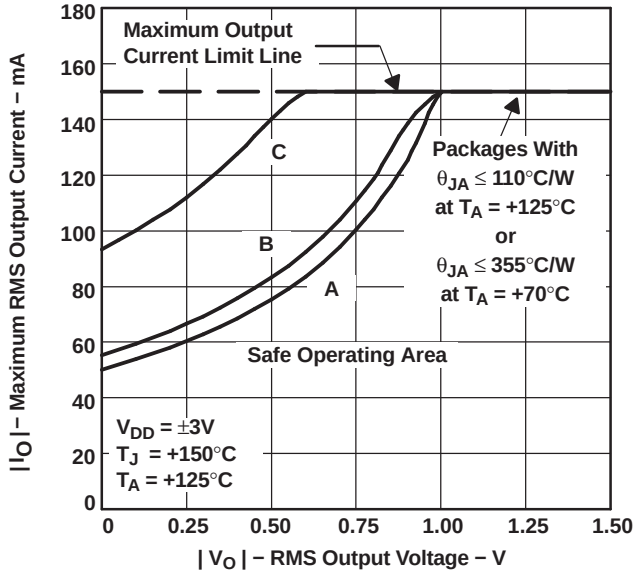



Figure 48.

TLV2470, TLV2471(1)
MAXIMUM RMS OUTPUT CURRENT
vs
RMS OUTPUT VOLTAGE DUE TO THERMAL LIMITS

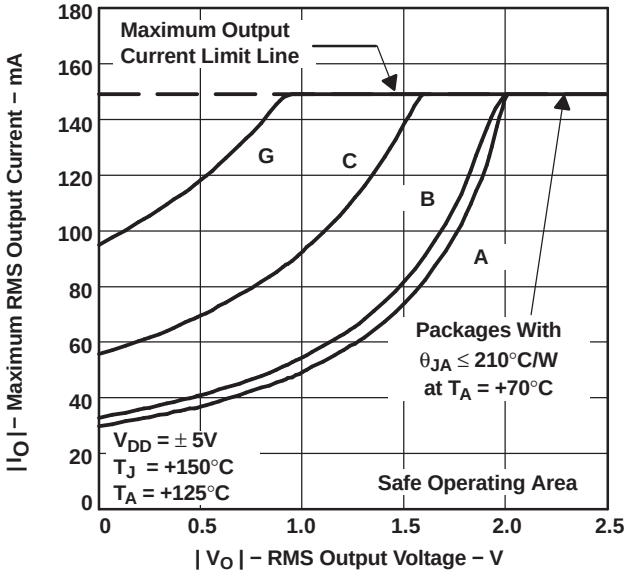



Figure 49.

TLV2472, TLV2473(1)
MAXIMUM RMS OUTPUT CURRENT
vs
RMS OUTPUT VOLTAGE DUE TO THERMAL LIMITS

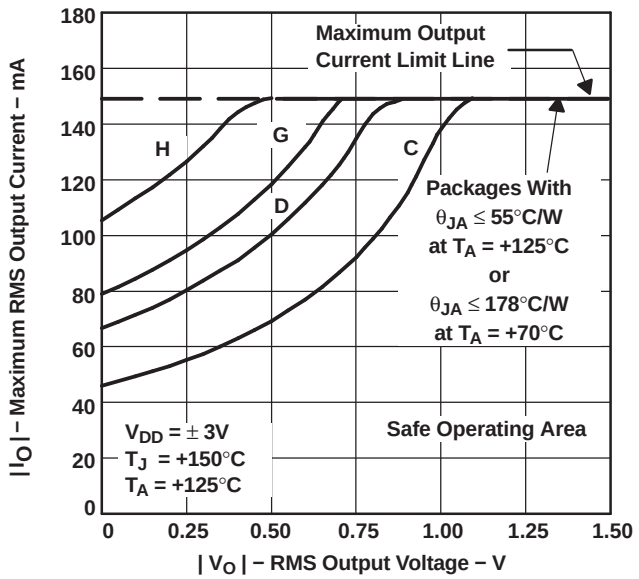



Figure 50.

TLV2472, TLV2473(1)
MAXIMUM RMS OUTPUT CURRENT
vs
RMS OUTPUT VOLTAGE DUE TO THERMAL LIMITS

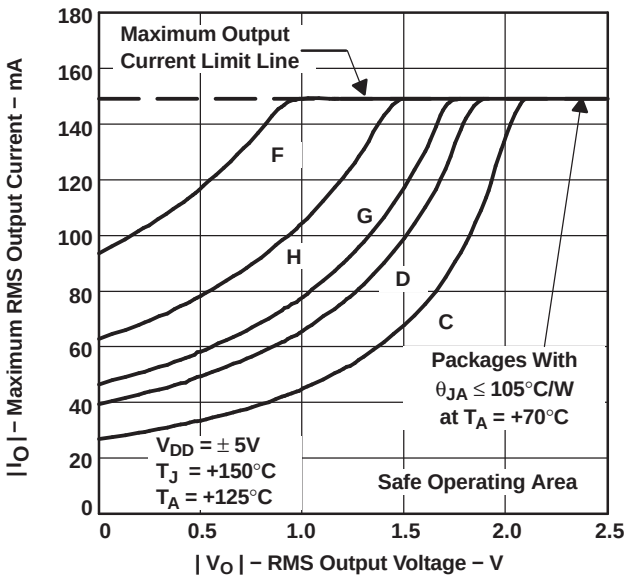



Figure 51.

Note: (1) A - SOT23 (5); B - SOT23 (6); C - SOIC (8); D - SOIC (14); E - SOIC (16); F - MSOP PP (8); G - PDIP (8); H - PDIP (14): I - PDIP (16); J - TSSOP PP (14/16)

## APPLICATION INFORMATION (continued)

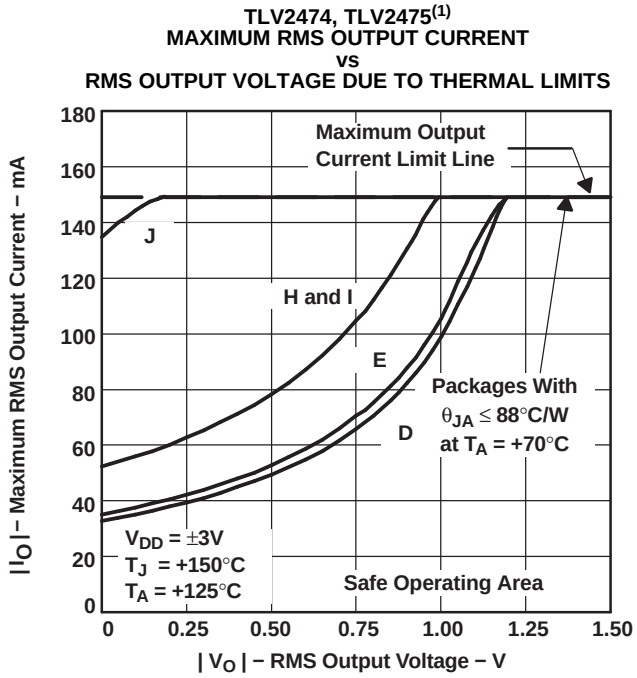



Figure 52.

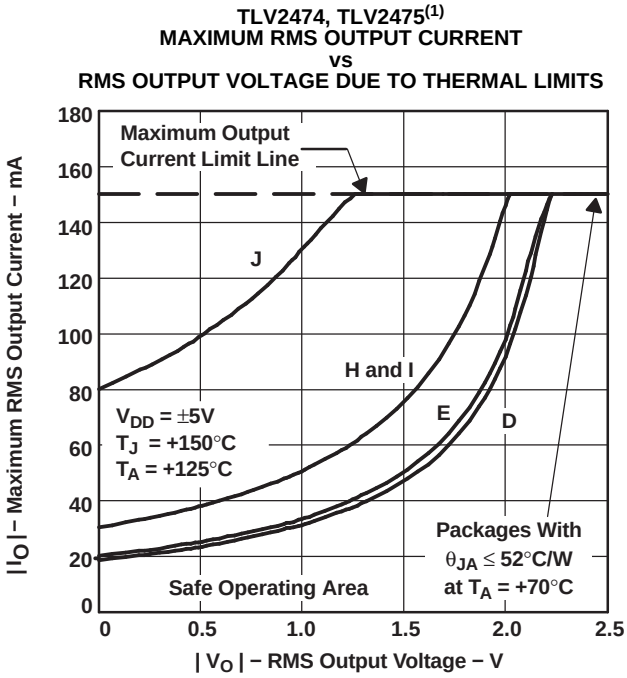



Figure 53.

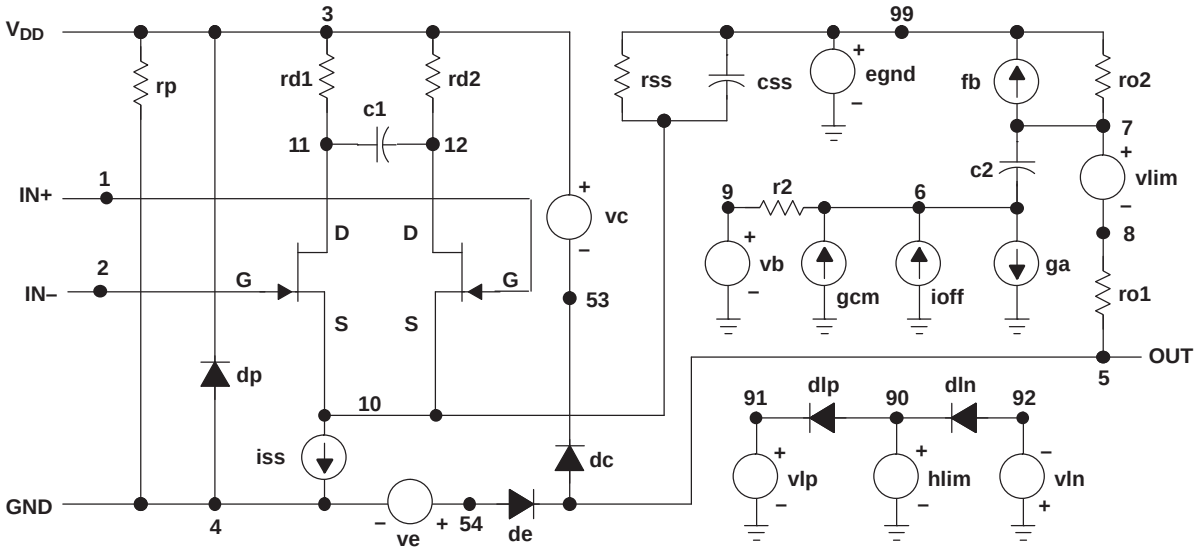
NOTE: (1) A - SOT23 (5); B - SOT23 (6); C - SOIC (8); D - SOIC (14); E - SOIC (16); F - MSOP PP (8); G - PDIP (8); H - PDIP (14): I - PDIP (16); J - TSSOP PP (14/16)

## APPLICATION INFORMATION (continued)

### MACROMODEL INFORMATION

Macromodel information provided was derived using Microsim PARTS™, the model generation software used with Microsim PSpice®. The Boyle macromodel and subcircuit in Figure 54 are generated using the TLV247x typical electrical and operating characteristics at $T_A$ = 25°C. Using this information, output simulations of the following key parameters can be generated to a tolerance of 20% (in most cases):

- Maximum positive output voltage swing
- Maximum negative output voltage swing
- Slew rate
- Quiescent power dissipation
- Input bias current
- Open-loop voltage amplification
- Unity-gain frequency
- Common-mode rejection ratio
- Phase margin
- DC output resistance
- AC output resistance
- Short-circuit output current limit




```
* TLV247x operational amplifier "macromodel" subcircuit
* created using Parts release 8.0 on 4/27/99 at 14:31
* Parts is a MicroSim product.
*
* connections:   non–inverting input
*                | inverting input
*                | | positive power supply
*                | | | negative power supply
*                | | | | output
*                | | | | |
.subckt  TLV247x 1 2 3 4 5
*
c1          11      12      1.1094E–12
c2          6       7       5.5000E–12
css         10      99      556.53E–15
dc          5       53      dy
de          54      5       dy
dlp         90      91      dx
dln         92      90      dx
dp          4       3       dx
egnd        99      0       poly(2) (3,0) (4,0) 0 .5 .5
fb          7       99      poly(5) vb vc ve vlp vln 0
+ 39.614E6 –1E3 1E3 40E6 –40E6
ga          6       0       11      12      79.828E–6
gcm         0       6       10      99      32.483E–9
iss         10      4       dc      10.714E–6
hlim        90      0       vlim 1K
ioff        0       6       dc      75E–9
j1          11      2       10 jx1
j2          12      1       10 jx2
r2          6       9       100.00E3
rd1         3       11      12.527E3
rd2         3       12      12.527E3
ro1         8       5       10
ro2         7       99      10
rp          3       4       3.8023E3
rss         10      99      18.667E6
vb          9       0       dc 0
vc          3       53      dc .842
ve          54      4       dc .842
vlim        7       8       dc 0
vlp         91      0       dc 110
vln         0       92      dc 110
.model      dx      D(Is=800.00E–18)
.model      dy      D(Is=800.00E–18 Rs=1m Cjo=10p)
.model      jx1     NJF(Is=1.0825E–12 Beta=594.78E–06 + Vto=–1)
.model      jx2     NJF(Is=1.0825E–12 Beta=594.78E–06 + Vto=–1)
.ends
*$
```

G. R. Boyle, B. M. Cohn, D. O. Pederson, and J. E. Solomon, "Macromodeling of Integrated Circuit Operational Amplifiers, "*IEEE Journal of Solid-State Circuits,* SC-9, 353 (1974).

**Figure 54. Boyle Macromodel and Subcircuit**

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| TLV2470AID | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 2470AI | Samples |
| TLV2470AIDG4 | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 2470AI | Samples |
| TLV2470AIDR | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 2470AI | Samples |
| TLV2470AIP | ACTIVE | PDIP | P | 8 | 50 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | -40 to 125 | TLV2470AI | Samples |
| TLV2470AIPE4 | ACTIVE | PDIP | P | 8 | 50 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | -40 to 125 | TLV2470AI | Samples |
| TLV2470CD | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | 2470C | Samples |
| TLV2470CDBVR | ACTIVE | SOT-23 | DBV | 6 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | VAUC | Samples |
| TLV2470CDBVT | ACTIVE | SOT-23 | DBV | 6 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | VAUC | Samples |
| TLV2470CDR | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | 2470C | Samples |
| TLV2470CDRG4 | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | 2470C | Samples |
| TLV2470CP | ACTIVE | PDIP | P | 8 | 50 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | 0 to 70 | TLV2470C | Samples |
| TLV2470ID | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 2470I | Samples |
| TLV2470IDBVR | ACTIVE | SOT-23 | DBV | 6 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | VAUI | Samples |
| TLV2470IDBVRG4 | ACTIVE | SOT-23 | DBV | 6 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | VAUI | Samples |
| TLV2470IDBVT | ACTIVE | SOT-23 | DBV | 6 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | VAUI | Samples |
| TLV2470IDBVTG4 | ACTIVE | SOT-23 | DBV | 6 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | VAUI | Samples |
| TLV2470IDR | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 2470I | Samples |

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| TLV2471AID | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 2471AI | Samples |
| TLV2471AIDR | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 2471AI | Samples |
| TLV2471AIP | ACTIVE | PDIP | P | 8 | 50 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | -40 to 125 | TLV2471AI | Samples |
| TLV2471CD | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | 2471C | Samples |
| TLV2471CDBVR | ACTIVE | SOT-23 | DBV | 5 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | VAVC | Samples |
| TLV2471CDBVRG4 | ACTIVE | SOT-23 | DBV | 5 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | VAVC | Samples |
| TLV2471CDBVT | ACTIVE | SOT-23 | DBV | 5 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | VAVC | Samples |
| TLV2471CDBVTG4 | ACTIVE | SOT-23 | DBV | 5 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | VAVC | Samples |
| TLV2471CDG4 | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | 2471C | Samples |
| TLV2471CDR | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | 2471C | Samples |
| TLV2471CP | ACTIVE | PDIP | P | 8 | 50 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | 0 to 70 | TLV2471C | Samples |
| TLV2471ID | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 2471I | Samples |
| TLV2471IDBVR | ACTIVE | SOT-23 | DBV | 5 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | VAVI | Samples |
| TLV2471IDBVRG4 | ACTIVE | SOT-23 | DBV | 5 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | VAVI | Samples |
| TLV2471IDBVT | ACTIVE | SOT-23 | DBV | 5 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | VAVI | Samples |
| TLV2471IDBVTG4 | ACTIVE | SOT-23 | DBV | 5 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | VAVI | Samples |
| TLV2471IDR | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 2471I | Samples |
| TLV2471IP | ACTIVE | PDIP | P | 8 | 50 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | -40 to 125 | TLV2471I | Samples |

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| TLV2472AID | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 2472AI | Samples |
| TLV2472AIDG4 | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 2472AI | Samples |
| TLV2472AIDR | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 2472AI | Samples |
| TLV2472AIDRG4 | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 2472AI | Samples |
| TLV2472AIP | ACTIVE | PDIP | P | 8 | 50 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | -40 to 125 | TLV2472AI | Samples |
| TLV2472CD | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | 2472C | Samples |
| TLV2472CDG4 | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | 2472C | Samples |
| TLV2472CDGN | ACTIVE | MSOP-PowerPAD | DGN | 8 | 80 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | ABU | Samples |
| TLV2472CDGNR | ACTIVE | MSOP-PowerPAD | DGN | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | ABU | Samples |
| TLV2472CDGNRG4 | ACTIVE | MSOP-PowerPAD | DGN | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | ABU | Samples |
| TLV2472CDR | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | 2472C | Samples |
| TLV2472CDRG4 | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | 2472C | Samples |
| TLV2472CP | ACTIVE | PDIP | P | 8 | 50 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | 0 to 70 | TLV2472CP | Samples |
| TLV2472ID | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 2472I | Samples |
| TLV2472IDG4 | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 2472I | Samples |
| TLV2472IDGN | ACTIVE | MSOP-PowerPAD | DGN | 8 | 80 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | ABV | Samples |
| TLV2472IDGNG4 | ACTIVE | MSOP-PowerPAD | DGN | 8 | 80 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | ABV | Samples |
| TLV2472IDGNR | ACTIVE | MSOP-PowerPAD | DGN | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | ABV | Samples |

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| TLV2472IDGNRG4 | ACTIVE | MSOP-PowerPAD | DGN | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | ABV | Samples |
| TLV2472IDR | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 2472I | Samples |
| TLV2472IDRG4 | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 2472I | Samples |
| TLV2472IP | ACTIVE | PDIP | P | 8 | 50 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | -40 to 125 | TLV2472IP | Samples |
| TLV2473AID | ACTIVE | SOIC | D | 14 | 50 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | TLV2473AI | Samples |
| TLV2473AIDR | ACTIVE | SOIC | D | 14 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | TLV2473AI | Samples |
| TLV2473AIN | ACTIVE | PDIP | N | 14 | 25 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | -40 to 125 | TLV2473AIN | Samples |
| TLV2473CD | ACTIVE | SOIC | D | 14 | 50 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | TLV2473C | Samples |
| TLV2473CDGQR | ACTIVE | MSOP-PowerPAD | DGQ | 10 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU \| CU NIPDAUAG | Level-1-260C-UNLIM | 0 to 70 | ABW | Samples |
| TLV2473CDR | ACTIVE | SOIC | D | 14 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | TLV2473C | Samples |
| TLV2473IDGQR | ACTIVE | MSOP-PowerPAD | DGQ | 10 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | ABX | Samples |
| TLV2473IDGQRG4 | ACTIVE | MSOP-PowerPAD | DGQ | 10 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | ABX | Samples |
| TLV2473IN | ACTIVE | PDIP | N | 14 | 25 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | -40 to 125 | TLV2473IN | Samples |
| TLV2474AID | ACTIVE | SOIC | D | 14 | 50 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 2474AI | Samples |
| TLV2474AIDG4 | ACTIVE | SOIC | D | 14 | 50 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 2474AI | Samples |
| TLV2474AIDR | ACTIVE | SOIC | D | 14 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 2474AI | Samples |
| TLV2474AIDRG4 | ACTIVE | SOIC | D | 14 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 2474AI | Samples |
| TLV2474AIN | ACTIVE | PDIP | N | 14 | 25 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | -40 to 125 | TLV2474AI | Samples |

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| TLV2474AINE4 | ACTIVE | PDIP | N | 14 | 25 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | -40 to 125 | TLV2474AI | Samples |
| TLV2474AIPWP | ACTIVE | HTSSOP | PWP | 14 | 90 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | 2474AI | Samples |
| TLV2474AIPWPG4 | ACTIVE | HTSSOP | PWP | 14 | 90 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | 2474AI | Samples |
| TLV2474AIPWPR | ACTIVE | HTSSOP | PWP | 14 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | 2474AI | Samples |
| TLV2474AIPWR | ACTIVE | TSSOP | PW | 14 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 2474AI | Samples |
| TLV2474AIPWRG4 | ACTIVE | TSSOP | PW | 14 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 2474AI | Samples |
| TLV2474CD | ACTIVE | SOIC | D | 14 | 50 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | 2474C | Samples |
| TLV2474CDG4 | ACTIVE | SOIC | D | 14 | 50 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | 2474C | Samples |
| TLV2474CDR | ACTIVE | SOIC | D | 14 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | 2474C | Samples |
| TLV2474CDRG4 | ACTIVE | SOIC | D | 14 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | 2474C | Samples |
| TLV2474CN | ACTIVE | PDIP | N | 14 | 25 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | 0 to 70 | TLV2474C | Samples |
| TLV2474CPWP | ACTIVE | HTSSOP | PWP | 14 | 90 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | 0 to 70 | 2474C | Samples |
| TLV2474CPWPR | ACTIVE | HTSSOP | PWP | 14 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | 0 to 70 | 2474C | Samples |
| TLV2474ID | ACTIVE | SOIC | D | 14 | 50 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 2474I | Samples |
| TLV2474IDG4 | ACTIVE | SOIC | D | 14 | 50 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 2474I | Samples |
| TLV2474IDR | ACTIVE | SOIC | D | 14 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 2474I | Samples |
| TLV2474IDRG4 | ACTIVE | SOIC | D | 14 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 2474I | Samples |
| TLV2474IN | ACTIVE | PDIP | N | 14 | 25 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | -40 to 125 | TLV2474I | Samples |

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| TLV2474IPWP | ACTIVE | HTSSOP | PWP | 14 | 90 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | 2474I | Samples |
| TLV2474IPWPR | ACTIVE | HTSSOP | PWP | 14 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | 2474I | Samples |
| TLV2474IPWPRG4 | ACTIVE | HTSSOP | PWP | 14 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | 2474I | Samples |
| TLV2475AIDR | ACTIVE | SOIC | D | 16 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | TLV2475AI | Samples |
| TLV2475AIN | ACTIVE | PDIP | N | 16 | 25 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | -40 to 125 | TLV2475AI | Samples |
| TLV2475AINE4 | ACTIVE | PDIP | N | 16 | 25 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | -40 to 125 | TLV2475AI | Samples |
| TLV2475AIPWP | ACTIVE | HTSSOP | PWP | 16 | 90 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | 2475AI | Samples |
| TLV2475AIPWPR | ACTIVE | HTSSOP | PWP | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | 2475AI | Samples |
| TLV2475CD | ACTIVE | SOIC | D | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | TLV2475C | Samples |
| TLV2475CDR | ACTIVE | SOIC | D | 16 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | TLV2475C | Samples |
| TLV2475CN | ACTIVE | PDIP | N | 16 | 25 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | 0 to 70 | TLV2475C | Samples |
| TLV2475CPWPR | ACTIVE | HTSSOP | PWP | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | 0 to 70 | 2475C | Samples |
| TLV2475IDR | OBSOLETE | SOIC | D | 16 | | TBD | Call TI | Call TI | -40 to 125 | TLV2475I | |
| TLV2475IDRG4 | OBSOLETE | SOIC | D | 16 | | TBD | Call TI | Call TI | -40 to 125 | | |
| TLV2475IPWPR | ACTIVE | HTSSOP | PWP | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | 2475I | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF TLV2471, TLV2471A, TLV2472, TLV2472A, TLV2474, TLV2474A :**

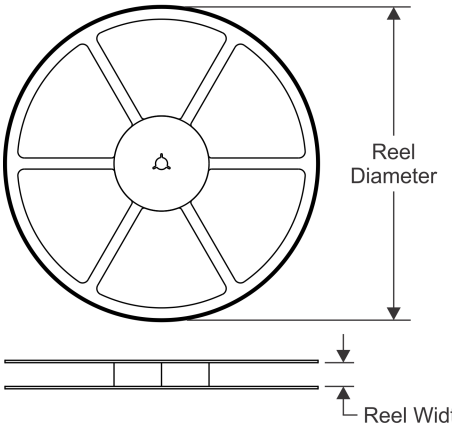
- Automotive: TLV2471-Q1, TLV2471A-Q1, TLV2472-Q1, TLV2472A-Q1, TLV2474-Q1, TLV2474A-Q1

NOTE: Qualified Version Definitions:

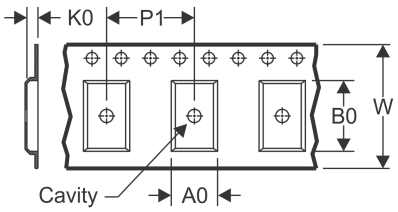
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

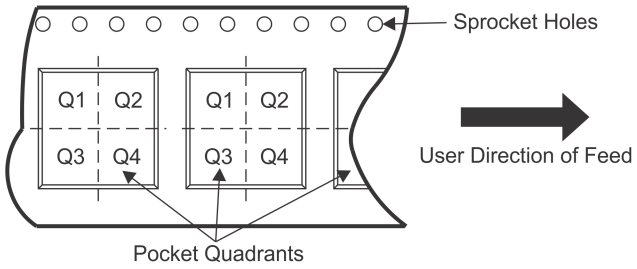



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**

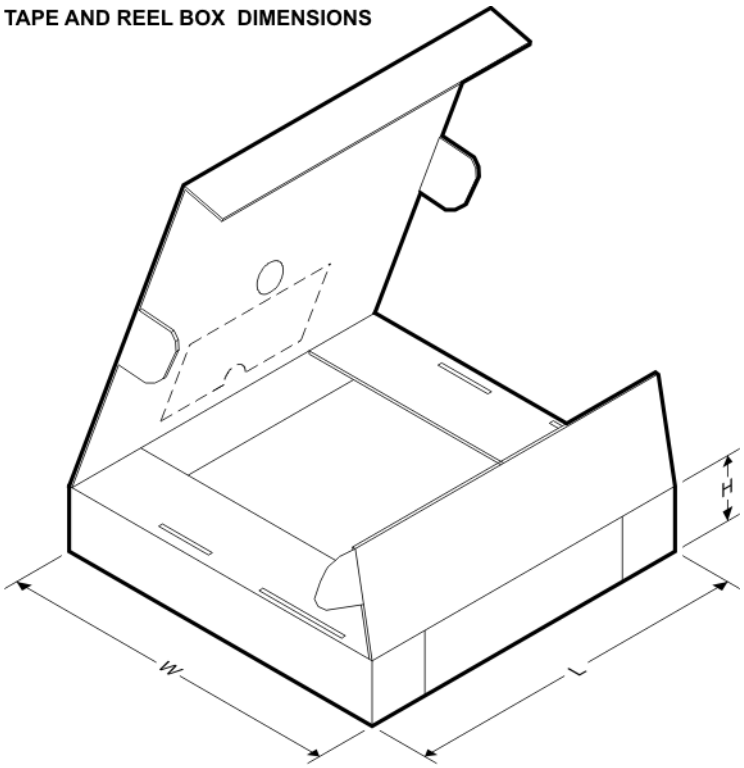



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TLV2470AIDR | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| TLV2470CDBVR | SOT-23 | DBV | 6 | 3000 | 178.0 | 9.0 | 3.23 | 3.17 | 1.37 | 4.0 | 8.0 | Q3 |
| TLV2470CDBVT | SOT-23 | DBV | 6 | 250 | 178.0 | 9.0 | 3.23 | 3.17 | 1.37 | 4.0 | 8.0 | Q3 |
| TLV2470CDR | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| TLV2470IDBVR | SOT-23 | DBV | 6 | 3000 | 178.0 | 9.0 | 3.23 | 3.17 | 1.37 | 4.0 | 8.0 | Q3 |
| TLV2470IDBVT | SOT-23 | DBV | 6 | 250 | 178.0 | 9.0 | 3.23 | 3.17 | 1.37 | 4.0 | 8.0 | Q3 |
| TLV2470IDR | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| TLV2470IDR | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| TLV2471AIDR | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| TLV2471CDBVR | SOT-23 | DBV | 5 | 3000 | 180.0 | 9.0 | 3.15 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| TLV2471CDBVT | SOT-23 | DBV | 5 | 250 | 180.0 | 9.0 | 3.15 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| TLV2471CDR | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| TLV2471IDBVR | SOT-23 | DBV | 5 | 3000 | 180.0 | 9.0 | 3.15 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| TLV2471IDBVT | SOT-23 | DBV | 5 | 250 | 180.0 | 9.0 | 3.15 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| TLV2471IDR | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| TLV2472AIDR | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| TLV2472CDGNR | MSOP-Power | DGN | 8 | 2500 | 330.0 | 12.4 | 5.3 | 3.4 | 1.4 | 8.0 | 12.0 | Q1 |

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | PAD | | | | | | | | | | | |
| TLV2472CDR | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| TLV2472IDGNR | MSOP-Power PAD | DGN | 8 | 2500 | 330.0 | 12.4 | 5.3 | 3.4 | 1.4 | 8.0 | 12.0 | Q1 |
| TLV2472IDR | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| TLV2473AIDR | SOIC | D | 14 | 2500 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |
| TLV2473CDGQR | MSOP-Power PAD | DGQ | 10 | 2500 | 330.0 | 12.4 | 5.3 | 3.4 | 1.4 | 8.0 | 12.0 | Q1 |
| TLV2473CDGQR | MSOP-Power PAD | DGQ | 10 | 2500 | 330.0 | 12.4 | 5.3 | 3.4 | 1.4 | 8.0 | 12.0 | Q1 |
| TLV2473CDR | SOIC | D | 14 | 2500 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |
| TLV2473IDGQR | MSOP-Power PAD | DGQ | 10 | 2500 | 330.0 | 12.4 | 5.3 | 3.4 | 1.4 | 8.0 | 12.0 | Q1 |
| TLV2474AIDR | SOIC | D | 14 | 2500 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |
| TLV2474AIPWPR | HTSSOP | PWP | 14 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| TLV2474AIPWR | TSSOP | PW | 14 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| TLV2474CDR | SOIC | D | 14 | 2500 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |
| TLV2474CPWPR | HTSSOP | PWP | 14 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| TLV2474IDR | SOIC | D | 14 | 2500 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |
| TLV2474IPWPR | HTSSOP | PWP | 14 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| TLV2475AIDR | SOIC | D | 16 | 2500 | 330.0 | 16.4 | 6.5 | 10.3 | 2.1 | 8.0 | 16.0 | Q1 |
| TLV2475AIPWPR | HTSSOP | PWP | 16 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| TLV2475CDR | SOIC | D | 16 | 2500 | 330.0 | 16.4 | 6.5 | 10.3 | 2.1 | 8.0 | 16.0 | Q1 |
| TLV2475CPWPR | HTSSOP | PWP | 16 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| TLV2475IPWPR | HTSSOP | PWP | 16 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |

**TAPE AND REEL BOX DIMENSIONS**

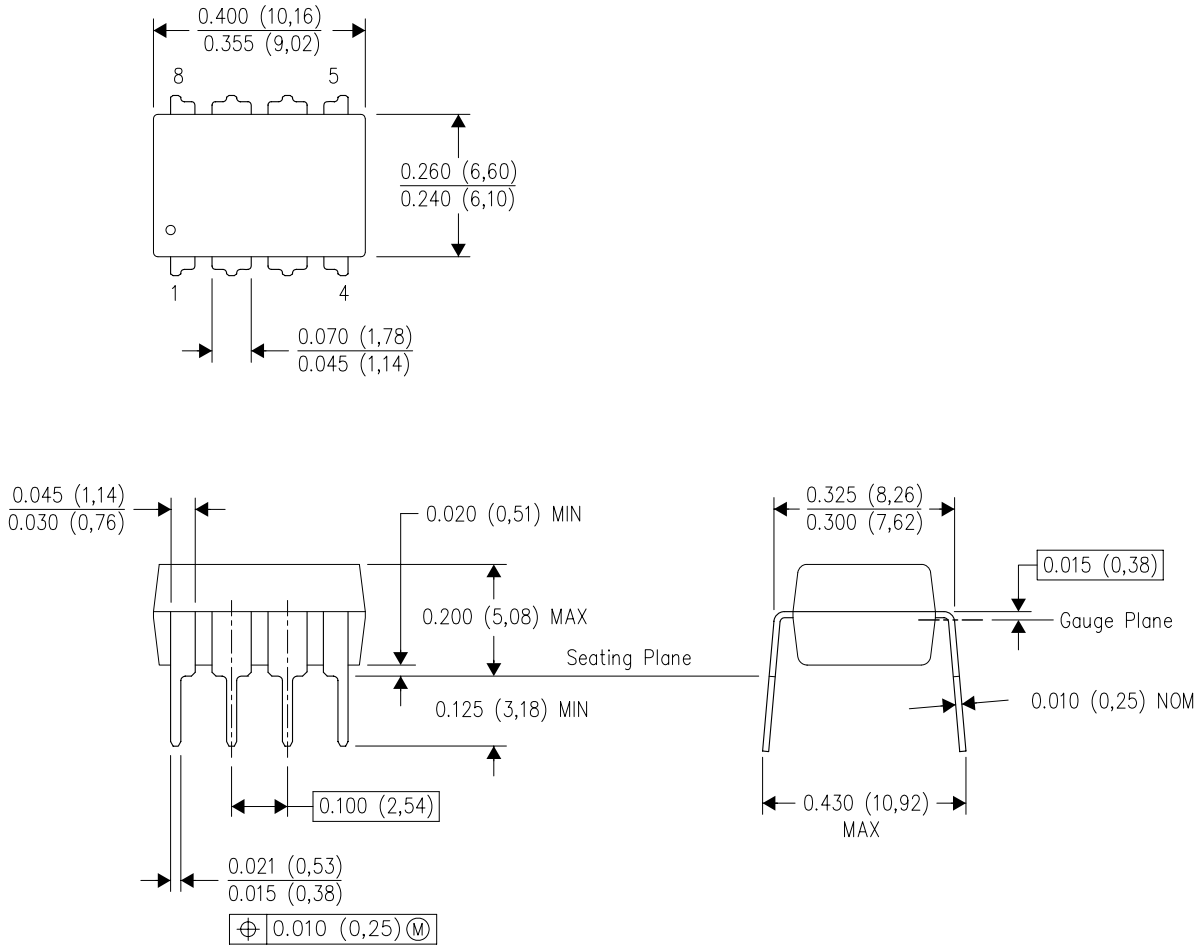



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| TLV2470AIDR | SOIC | D | 8 | 2500 | 340.5 | 338.1 | 20.6 |
| TLV2470CDBVR | SOT-23 | DBV | 6 | 3000 | 180.0 | 180.0 | 18.0 |
| TLV2470CDBVT | SOT-23 | DBV | 6 | 250 | 180.0 | 180.0 | 18.0 |
| TLV2470CDR | SOIC | D | 8 | 2500 | 340.5 | 338.1 | 20.6 |
| TLV2470IDBVR | SOT-23 | DBV | 6 | 3000 | 180.0 | 180.0 | 18.0 |
| TLV2470IDBVT | SOT-23 | DBV | 6 | 250 | 180.0 | 180.0 | 18.0 |
| TLV2470IDR | SOIC | D | 8 | 2500 | 340.5 | 338.1 | 20.6 |
| TLV2470IDR | SOIC | D | 8 | 2500 | 367.0 | 367.0 | 35.0 |
| TLV2471AIDR | SOIC | D | 8 | 2500 | 340.5 | 338.1 | 20.6 |
| TLV2471CDBVR | SOT-23 | DBV | 5 | 3000 | 182.0 | 182.0 | 20.0 |
| TLV2471CDBVT | SOT-23 | DBV | 5 | 250 | 182.0 | 182.0 | 20.0 |
| TLV2471CDR | SOIC | D | 8 | 2500 | 340.5 | 338.1 | 20.6 |
| TLV2471IDBVR | SOT-23 | DBV | 5 | 3000 | 182.0 | 182.0 | 20.0 |
| TLV2471IDBVT | SOT-23 | DBV | 5 | 250 | 182.0 | 182.0 | 20.0 |
| TLV2471IDR | SOIC | D | 8 | 2500 | 340.5 | 338.1 | 20.6 |
| TLV2472AIDR | SOIC | D | 8 | 2500 | 340.5 | 338.1 | 20.6 |
| TLV2472CDGNR | MSOP-PowerPAD | DGN | 8 | 2500 | 358.0 | 335.0 | 35.0 |
| TLV2472CDR | SOIC | D | 8 | 2500 | 340.5 | 338.1 | 20.6 |
| TLV2472IDGNR | MSOP-PowerPAD | DGN | 8 | 2500 | 358.0 | 335.0 | 35.0 |
| TLV2472IDR | SOIC | D | 8 | 2500 | 340.5 | 338.1 | 20.6 |

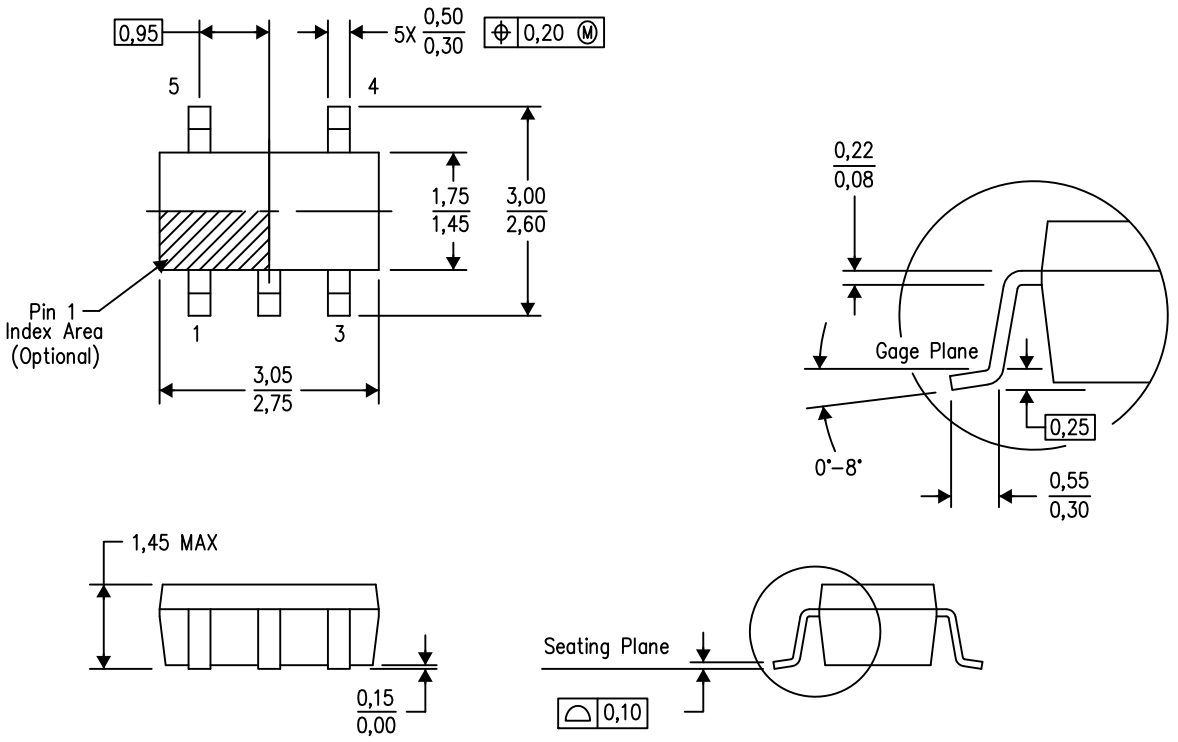
| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| TLV2473AIDR | SOIC | D | 14 | 2500 | 367.0 | 367.0 | 38.0 |
| TLV2473CDGQR | MSOP-PowerPAD | DGQ | 10 | 2500 | 358.0 | 335.0 | 35.0 |
| TLV2473CDGQR | MSOP-PowerPAD | DGQ | 10 | 2500 | 364.0 | 364.0 | 27.0 |
| TLV2473CDR | SOIC | D | 14 | 2500 | 367.0 | 367.0 | 38.0 |
| TLV2473IDGQR | MSOP-PowerPAD | DGQ | 10 | 2500 | 358.0 | 335.0 | 35.0 |
| TLV2474AIDR | SOIC | D | 14 | 2500 | 367.0 | 367.0 | 38.0 |
| TLV2474AIPWPR | HTSSOP | PWP | 14 | 2000 | 367.0 | 367.0 | 35.0 |
| TLV2474AIPWR | TSSOP | PW | 14 | 2000 | 367.0 | 367.0 | 35.0 |
| TLV2474CDR | SOIC | D | 14 | 2500 | 367.0 | 367.0 | 38.0 |
| TLV2474CPWPR | HTSSOP | PWP | 14 | 2000 | 367.0 | 367.0 | 35.0 |
| TLV2474IDR | SOIC | D | 14 | 2500 | 367.0 | 367.0 | 38.0 |
| TLV2474IPWPR | HTSSOP | PWP | 14 | 2000 | 367.0 | 367.0 | 35.0 |
| TLV2475AIDR | SOIC | D | 16 | 2500 | 367.0 | 367.0 | 38.0 |
| TLV2475AIPWPR | HTSSOP | PWP | 16 | 2000 | 367.0 | 367.0 | 35.0 |
| TLV2475CDR | SOIC | D | 16 | 2500 | 367.0 | 367.0 | 38.0 |
| TLV2475CPWPR | HTSSOP | PWP | 16 | 2000 | 367.0 | 367.0 | 35.0 |
| TLV2475IPWPR | HTSSOP | PWP | 16 | 2000 | 367.0 | 367.0 | 35.0 |

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE




NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.

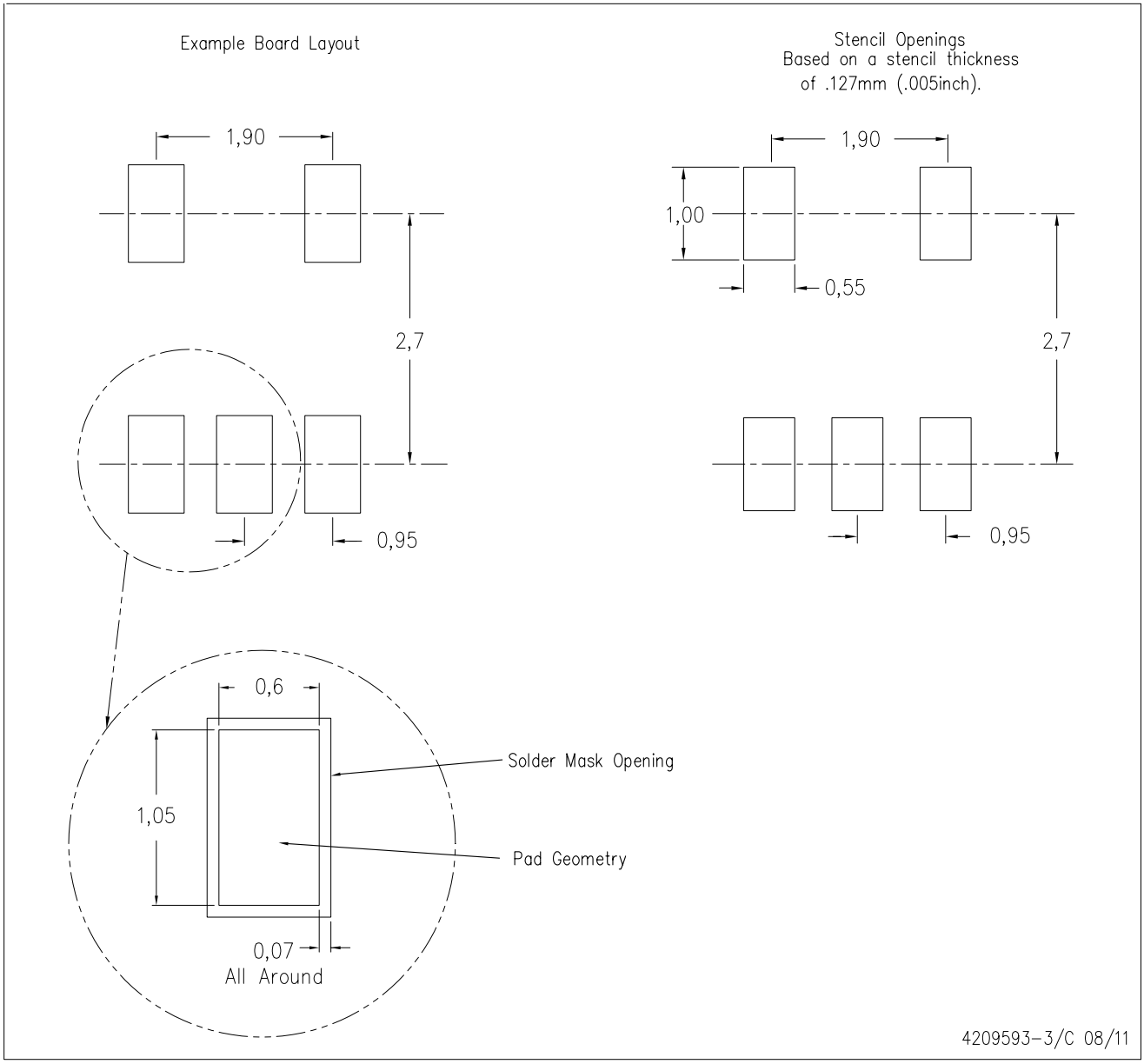
DBV (R–PDSO–G5) PLASTIC SMALL–OUTLINE PACKAGE




4073253–4/L 08/2013

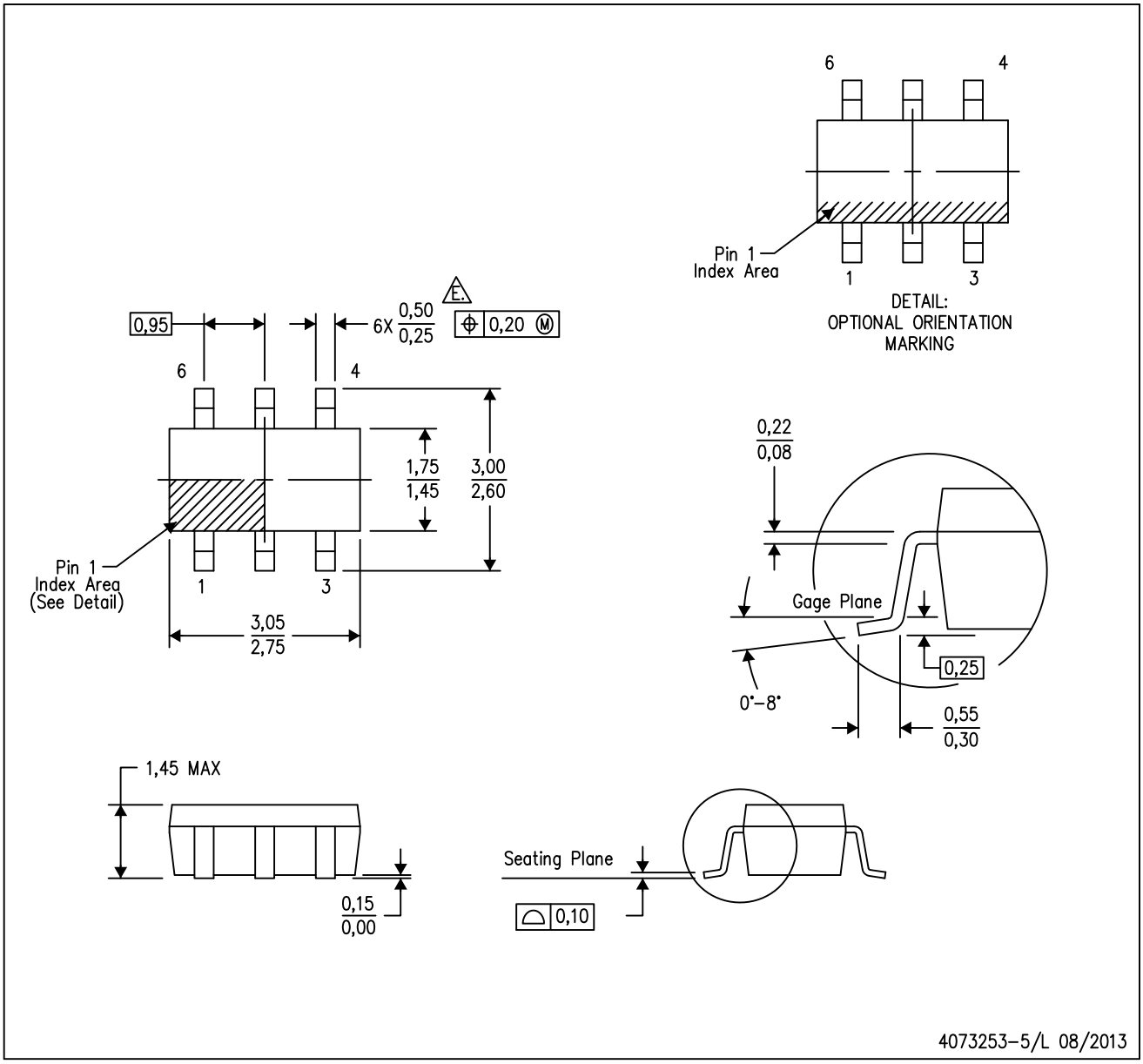
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO–178 Variation AA.

DBV (R–PDSO–G5) PLASTIC SMALL OUTLINE



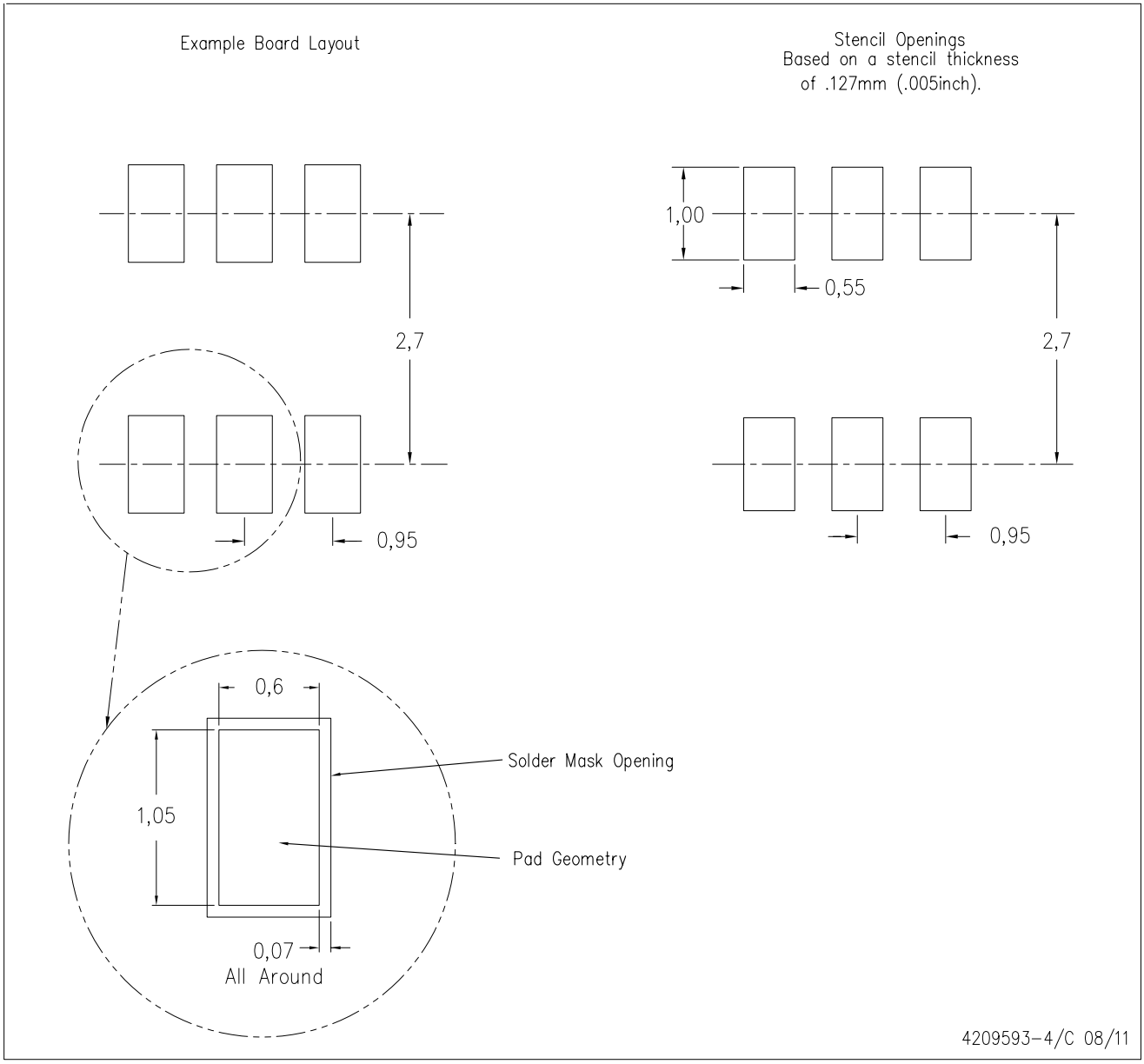

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

DBV (R–PDSO–G6) PLASTIC SMALL–OUTLINE PACKAGE



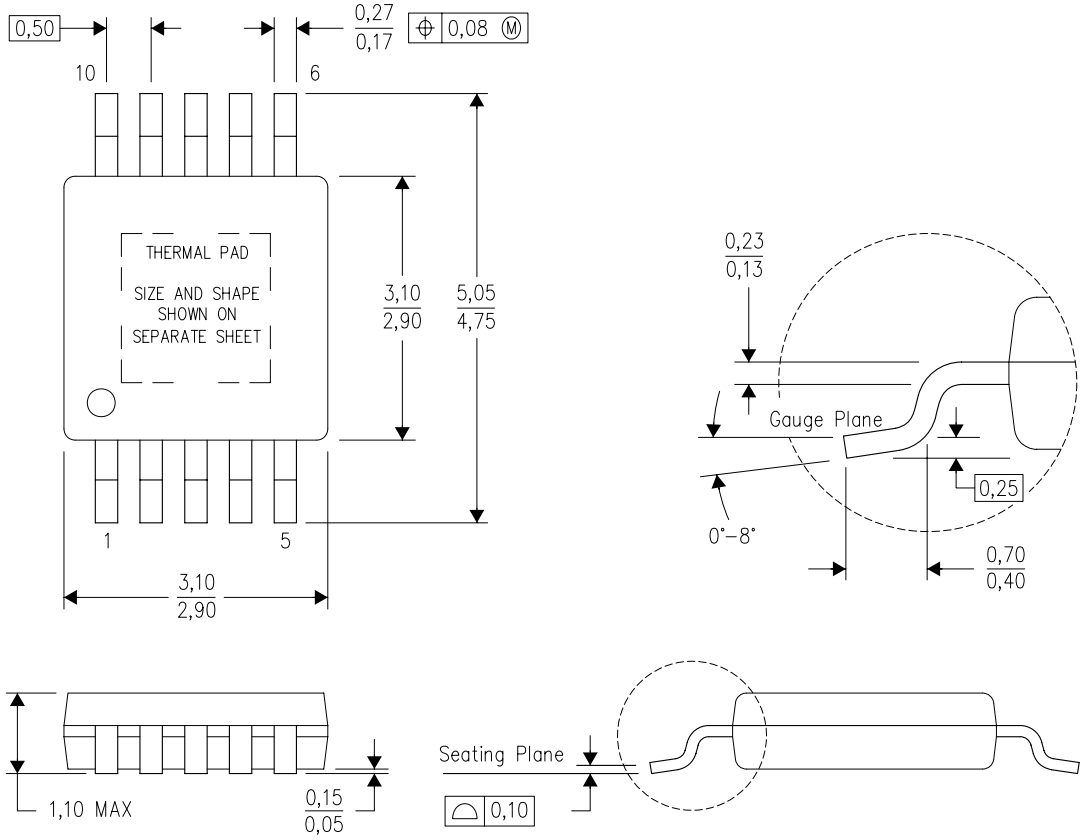

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
E. Falls within JEDEC MO–178 Variation AB, except minimum lead width.

DBV (R–PDSO–G6) PLASTIC SMALL OUTLINE




NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

DGQ (S–PDSO–G10) PowerPAD™ PLASTIC SMALL OUTLINE




4073273/F 11/11

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–187 variation BA–T.

**PowerPAD is a trademark of Texas Instruments.**

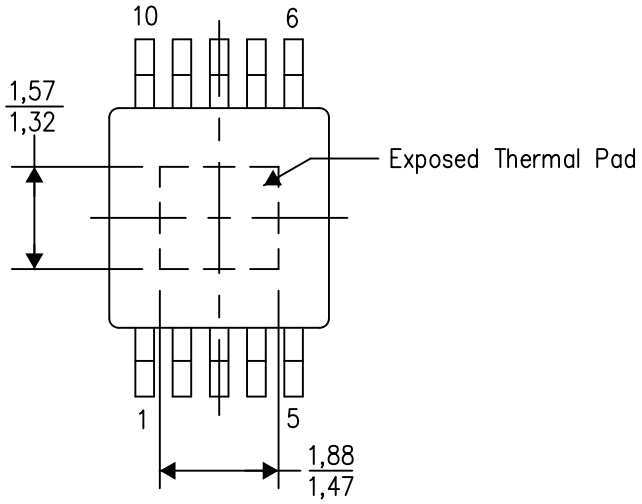
DGQ (S–PDSO–G10) PowerPAD™ PLASTIC SMALL OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.




Top View

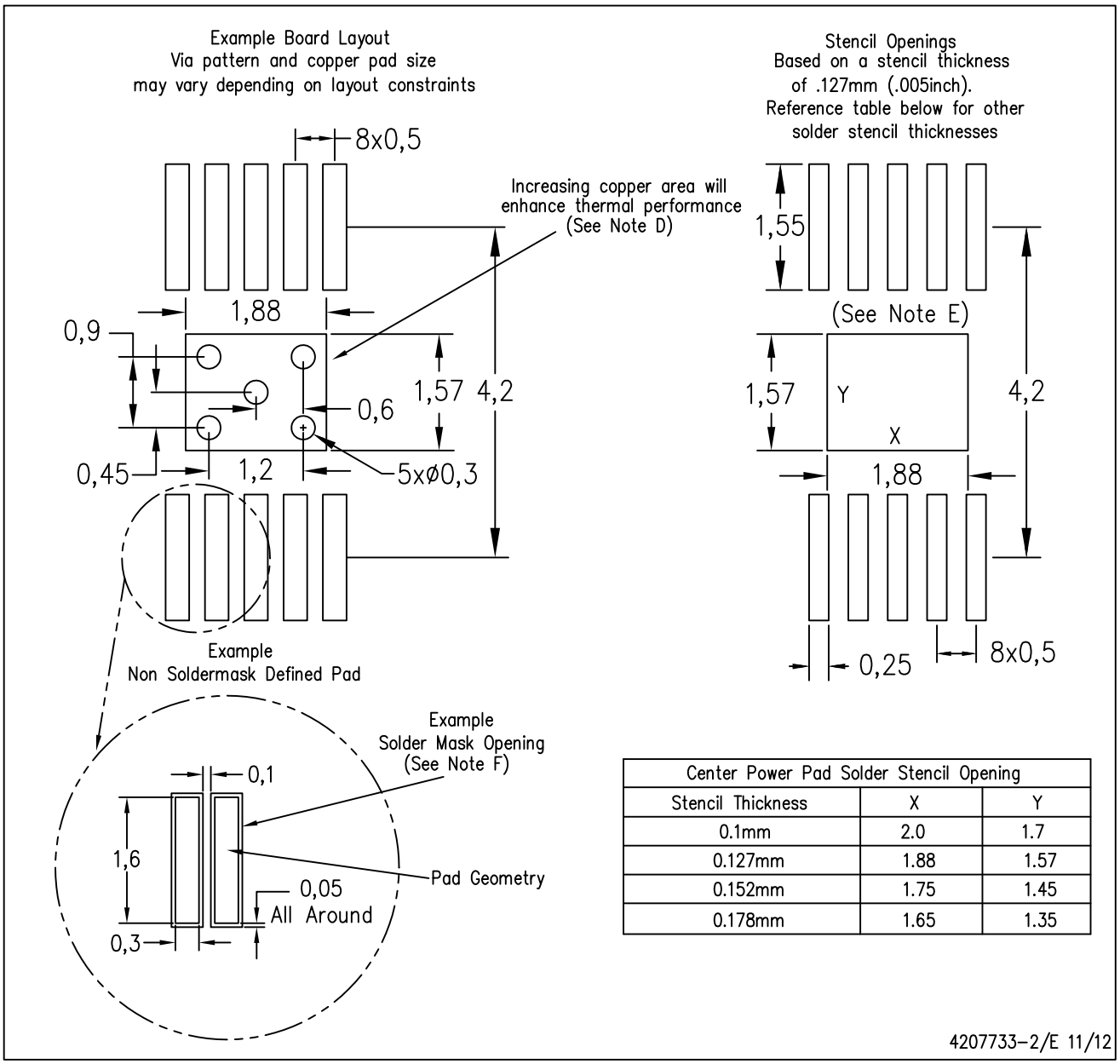
Exposed Thermal Pad Dimensions

4206324–2/G 05/13

NOTE: A. All linear dimensions are in millimeters

PowerPAD is a trademark of Texas Instruments

# DGQ (S–PDSO–G10) PowerPAD™ PLASTIC SMALL OUTLINE



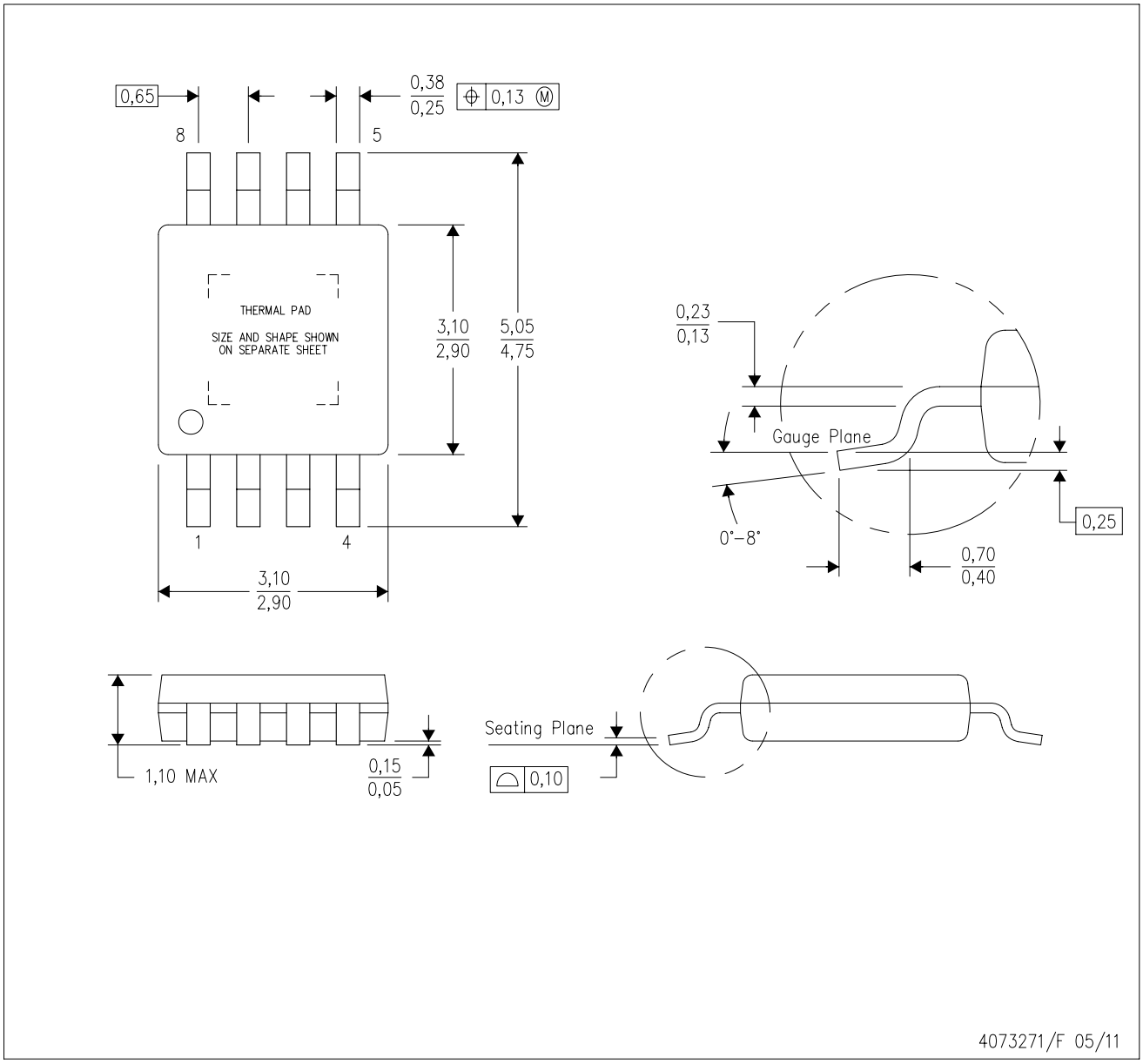

| Center Power Pad Solder Stencil Opening | | |
|---|---|---|
| Stencil Thickness | X | Y |
| 0.1mm | 2.0 | 1.7 |
| 0.127mm | 1.88 | 1.57 |
| 0.152mm | 1.75 | 1.45 |
| 0.178mm | 1.65 | 1.35 |

4207733–2/E 11/12

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PowerPAD is a trademark of Texas Instruments

DGN (S–PDSO–G8) PowerPAD™ PLASTIC SMALL OUTLINE




NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–187 variation AA–T

**PowerPAD is a trademark of Texas Instruments.**

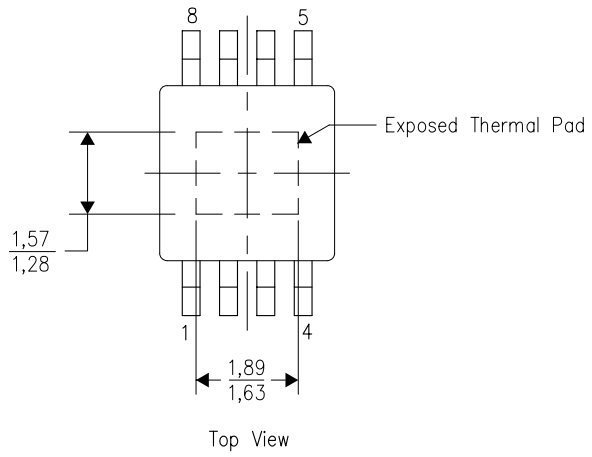
DGN (S–PDSO–G8) PowerPAD™ PLASTIC SMALL OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.




Top View

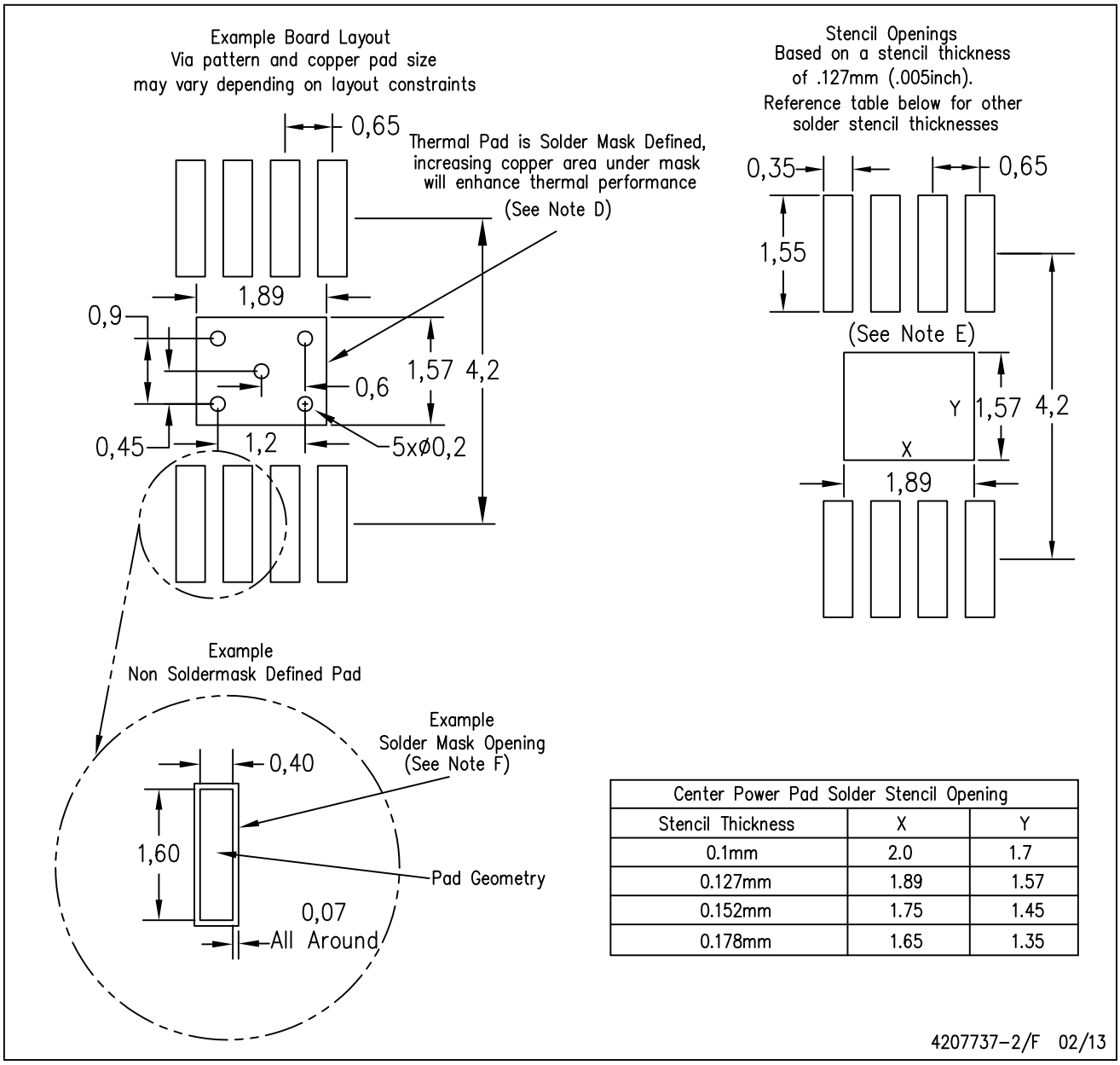
Exposed Thermal Pad Dimensions

4206323–2/I 12/11

NOTE: All linear dimensions are in millimeters

PowerPAD is a trademark of Texas Instruments

# DGN (R–PDSO–G8) PowerPAD™ PLASTIC SMALL OUTLINE



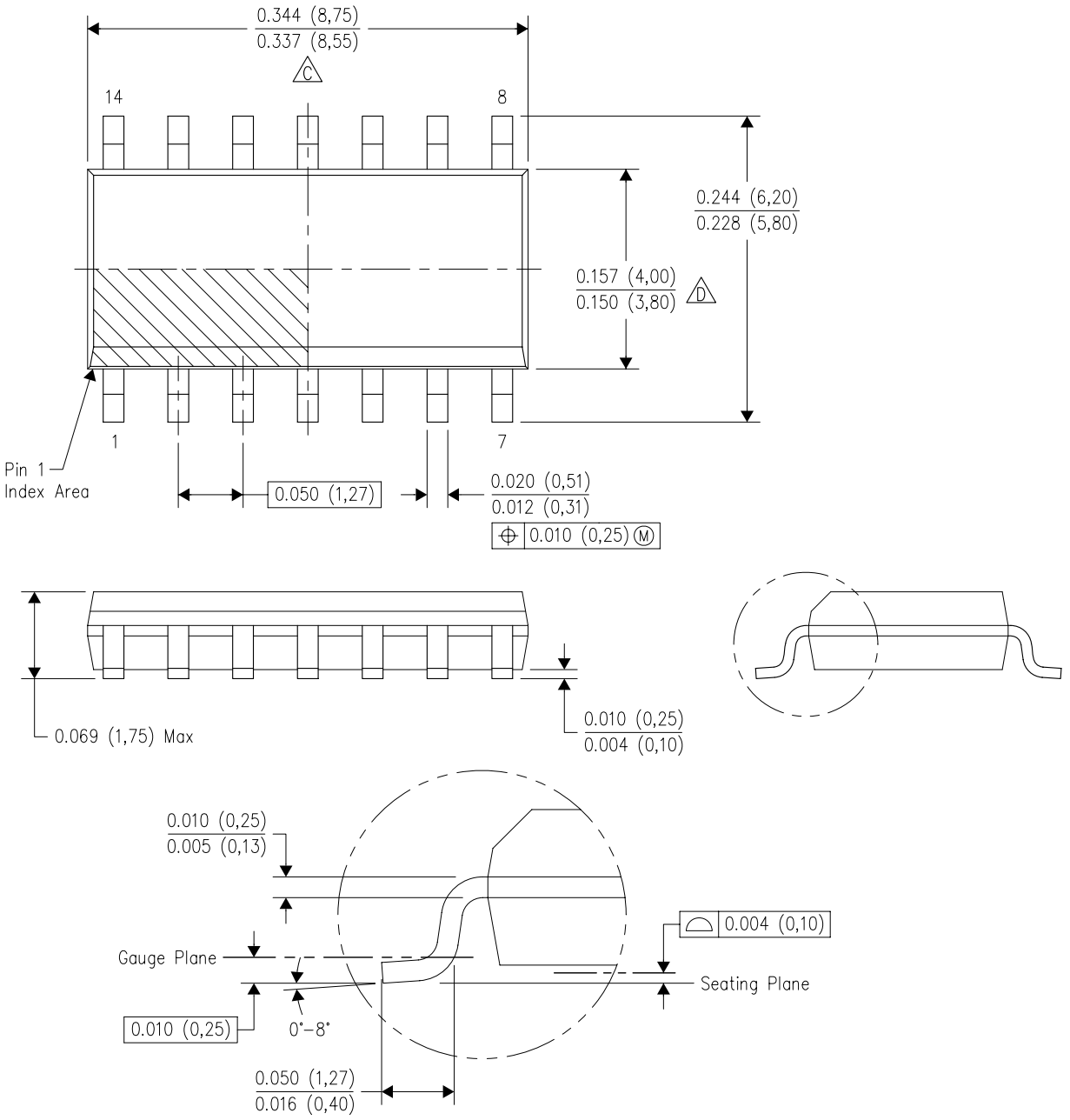

| Center Power Pad Solder Stencil Opening | | |
|---|---|---|
| Stencil Thickness | X | Y |
| 0.1mm | 2.0 | 1.7 |
| 0.127mm | 1.89 | 1.57 |
| 0.152mm | 1.75 | 1.45 |
| 0.178mm | 1.65 | 1.35 |

4207737–2/F 02/13

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

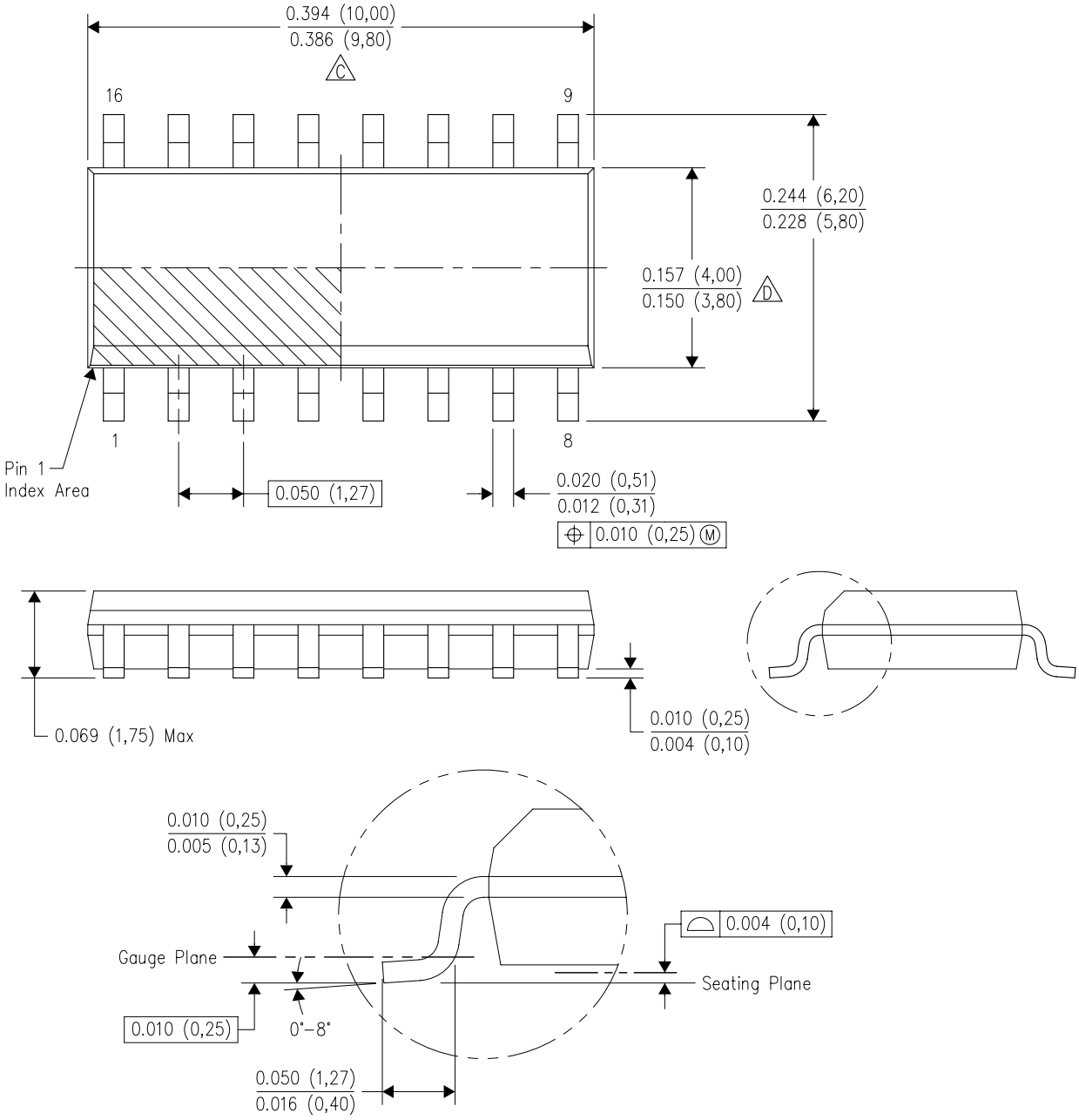
**PowerPAD is a trademark of Texas Instruments**

D (R–PDSO–G14) PLASTIC SMALL OUTLINE



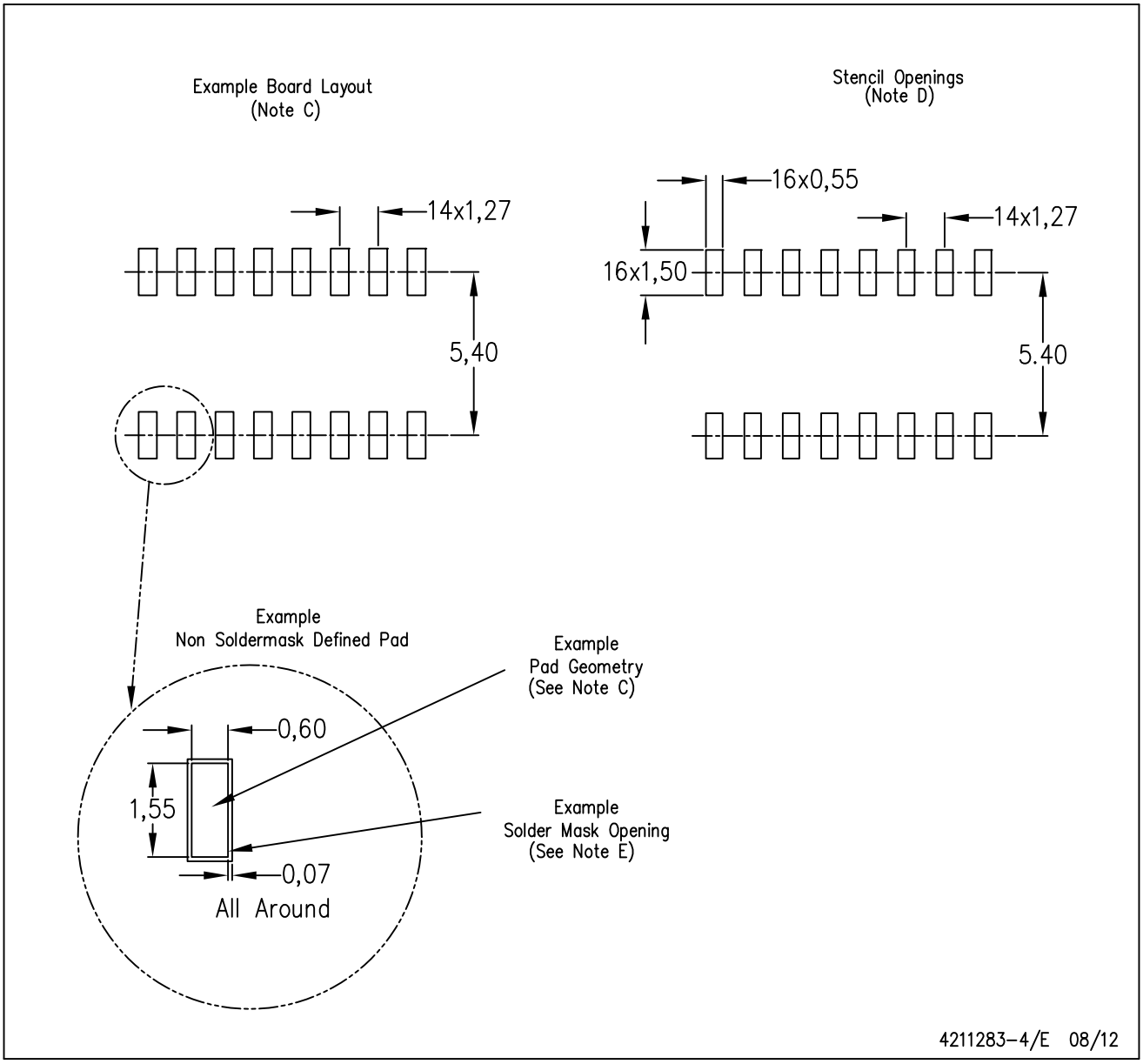

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AB.

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



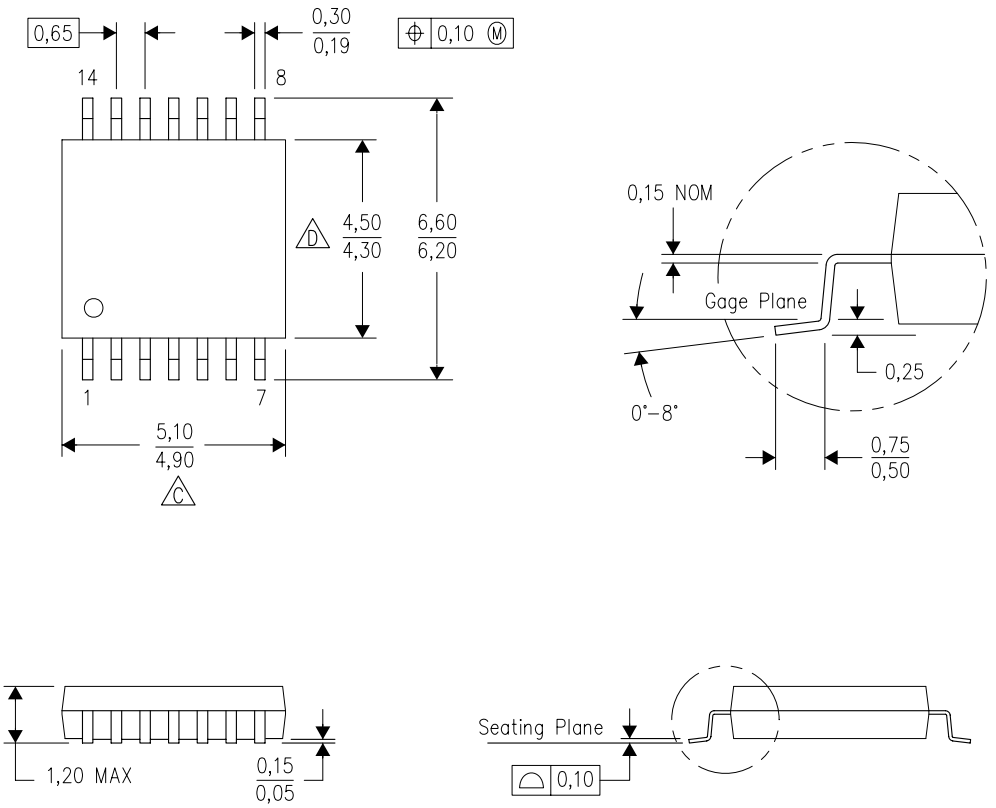

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

D (R–PDSO–G16) PLASTIC SMALL OUTLINE




NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

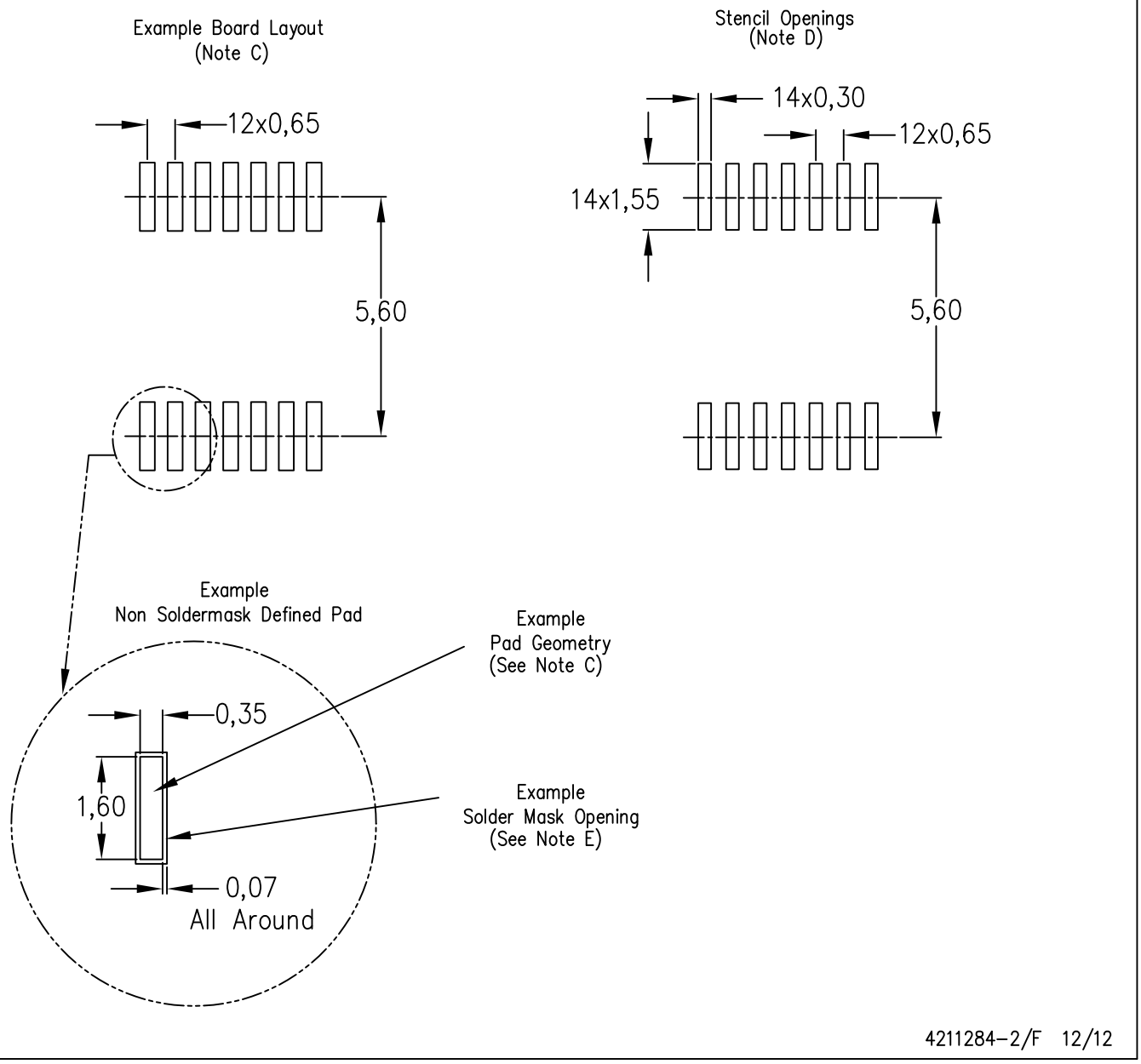
PW (R–PDSO–G14) PLASTIC SMALL OUTLINE




4040064–3/G 02/11

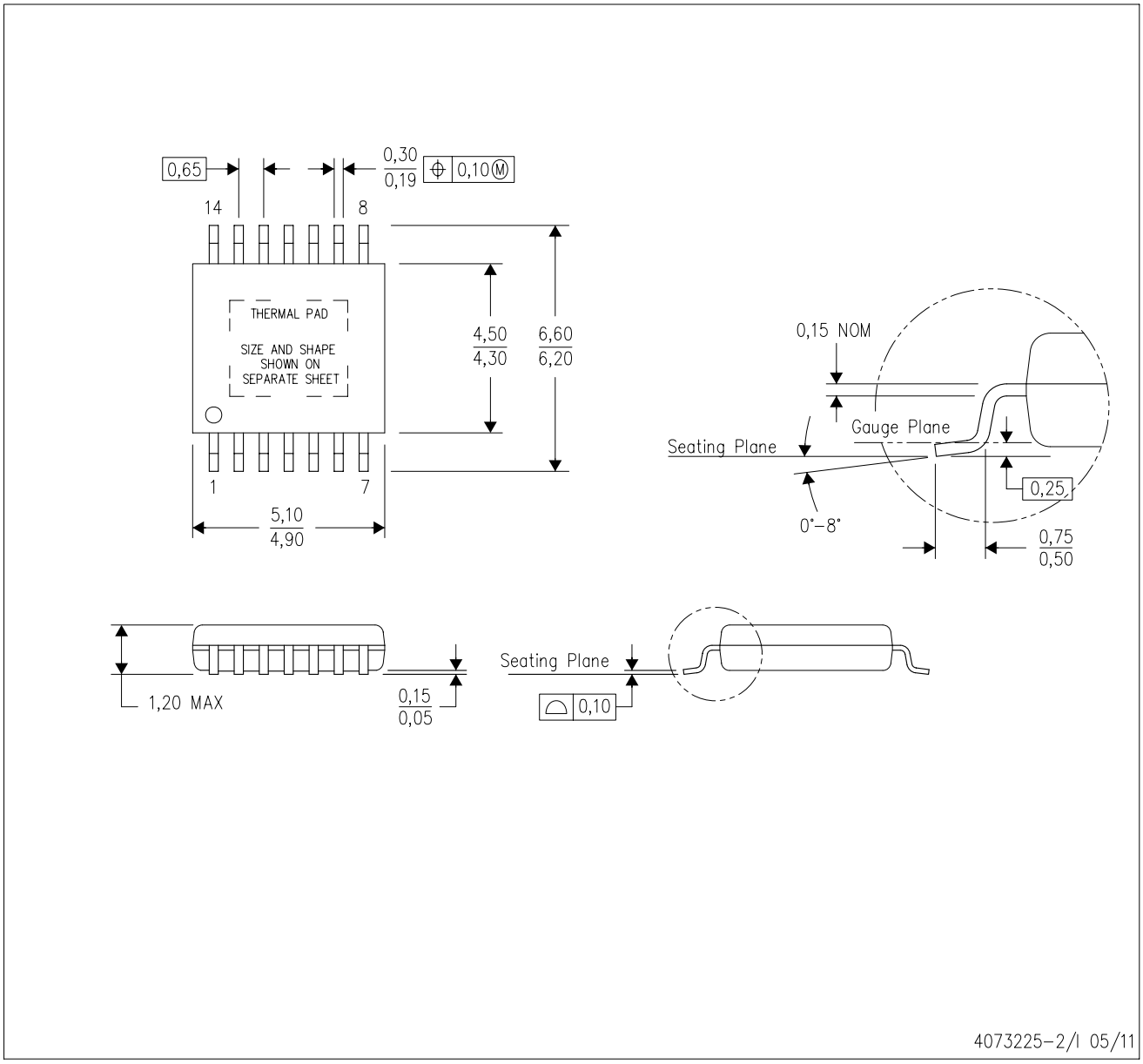
NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PW (R–PDSO–G14) PLASTIC SMALL OUTLINE




NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PWP (R–PDSO–G14) PowerPAD™ PLASTIC SMALL OUTLINE




NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.15 per side.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
E. Falls within JEDEC MO–153

**PowerPAD is a trademark of Texas Instruments.**

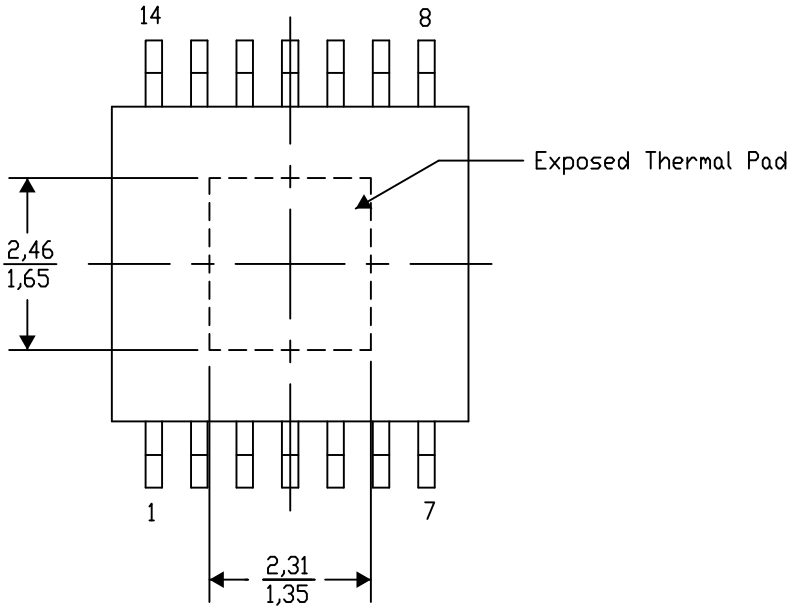
PWP (R–PDSO–G14) PowerPAD™ SMALL PLASTIC OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.




Top View

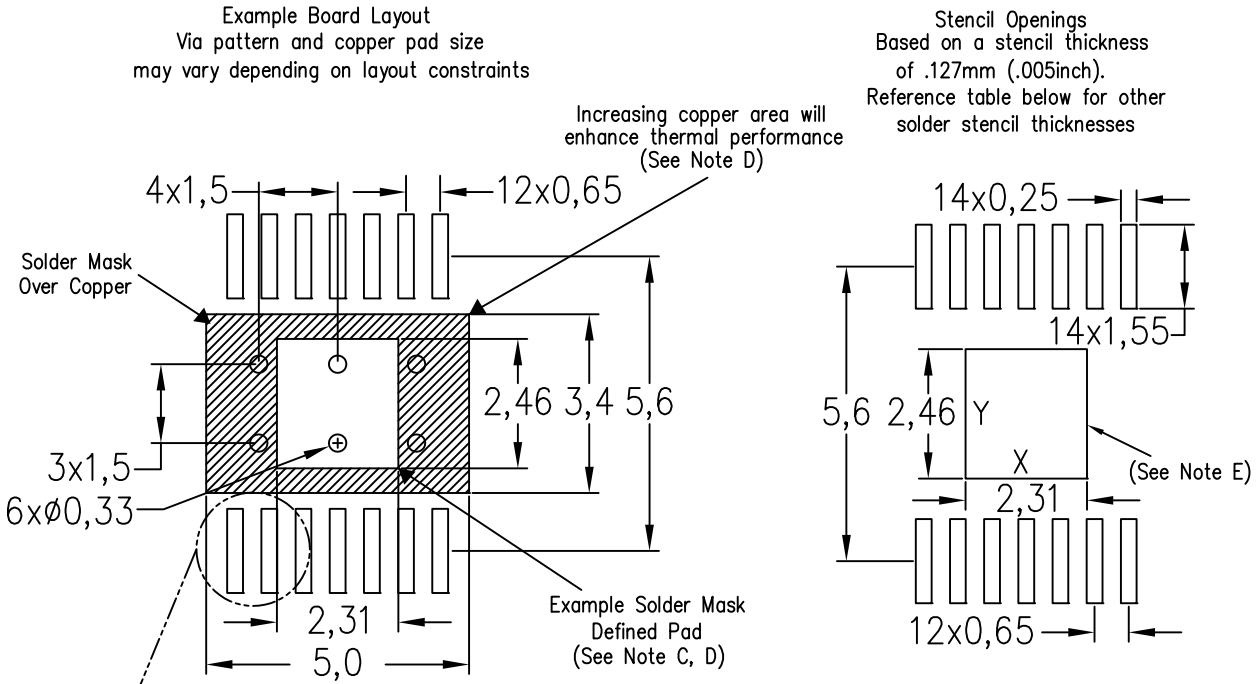
Exposed Thermal Pad Dimensions

4206332–2/AH 11/13

NOTE: A. All linear dimensions are in millimeters

PowerPAD is a trademark of Texas Instruments

## PWP (R–PDSO–G14) PowerPAD™ PLASTIC SMALL OUTLINE




| Center Power Pad Solder Stencil Opening | | |
|---|---|---|
| Stencil Thickness | X | Y |
| 0.1mm | 2.5 | 2.65 |
| 0.127mm | 2.31 | 2.46 |
| 0.152mm | 2.15 | 2.3 |
| 0.178mm | 2.05 | 2.15 |

4207609–2/T 08/13

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

# PWP (R–PDSO–G14) PowerPAD™ SMALL PLASTIC OUTLINE

## THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

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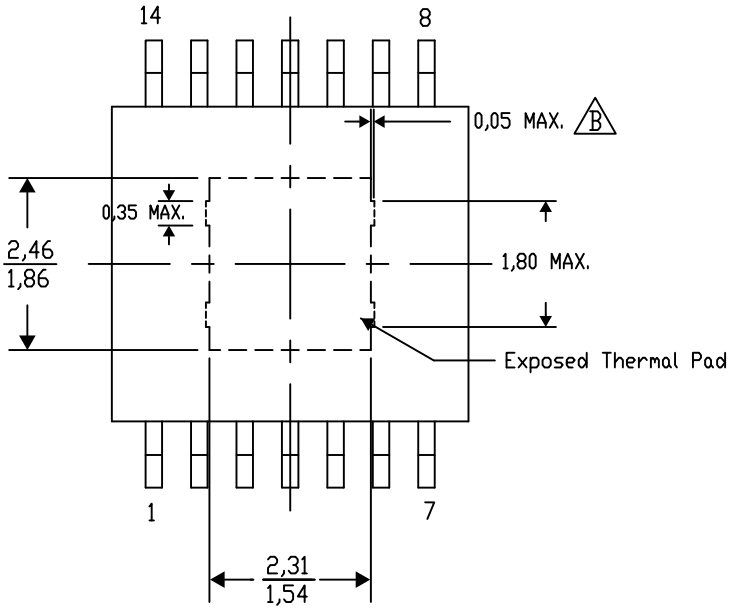
The exposed thermal pad dimensions for this package are shown in the following illustration.




Top View

Exposed Thermal Pad Dimensions

4206332–44/AH 11/13

NOTE: A. All linear dimensions are in millimeters

B. Exposed tie strap features may not be present.

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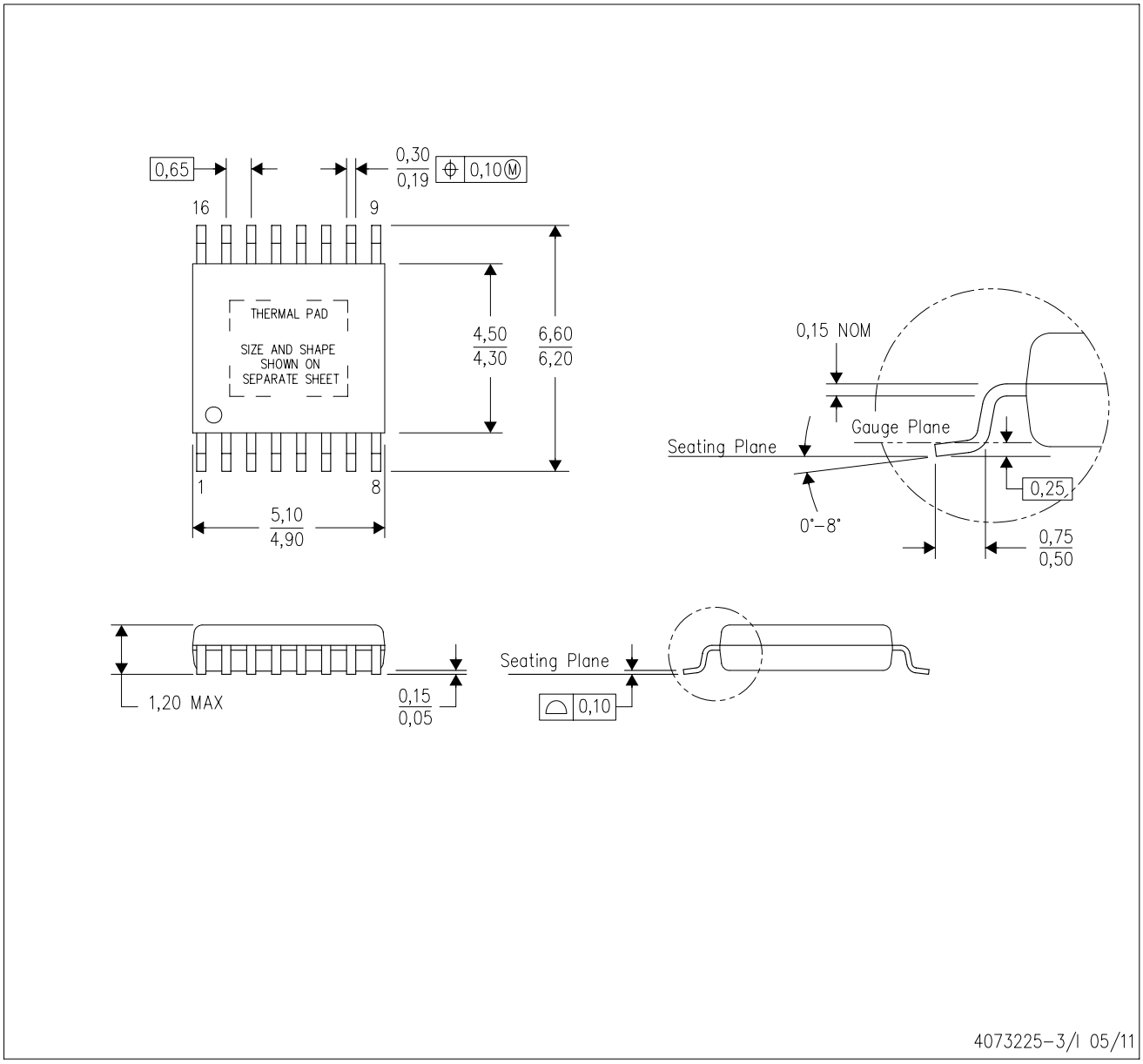
PWP (R–PDSO–G16) PowerPAD™ PLASTIC SMALL OUTLINE




NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.15 per side.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
E. Falls within JEDEC MO–153

**PowerPAD is a trademark of Texas Instruments.**

PWP (R–PDSO–G16) PowerPAD™ SMALL PLASTIC OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

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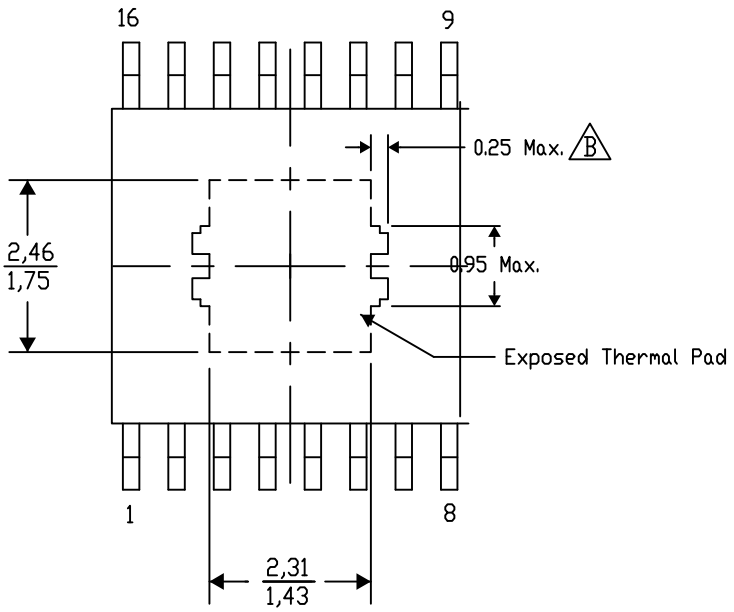
The exposed thermal pad dimensions for this package are shown in the following illustration.




Top View

Exposed Thermal Pad Dimensions

4206332–6/AH 11/13

NOTE: A. All linear dimensions are in millimeters

B. Exposed tie strap features may not be present.

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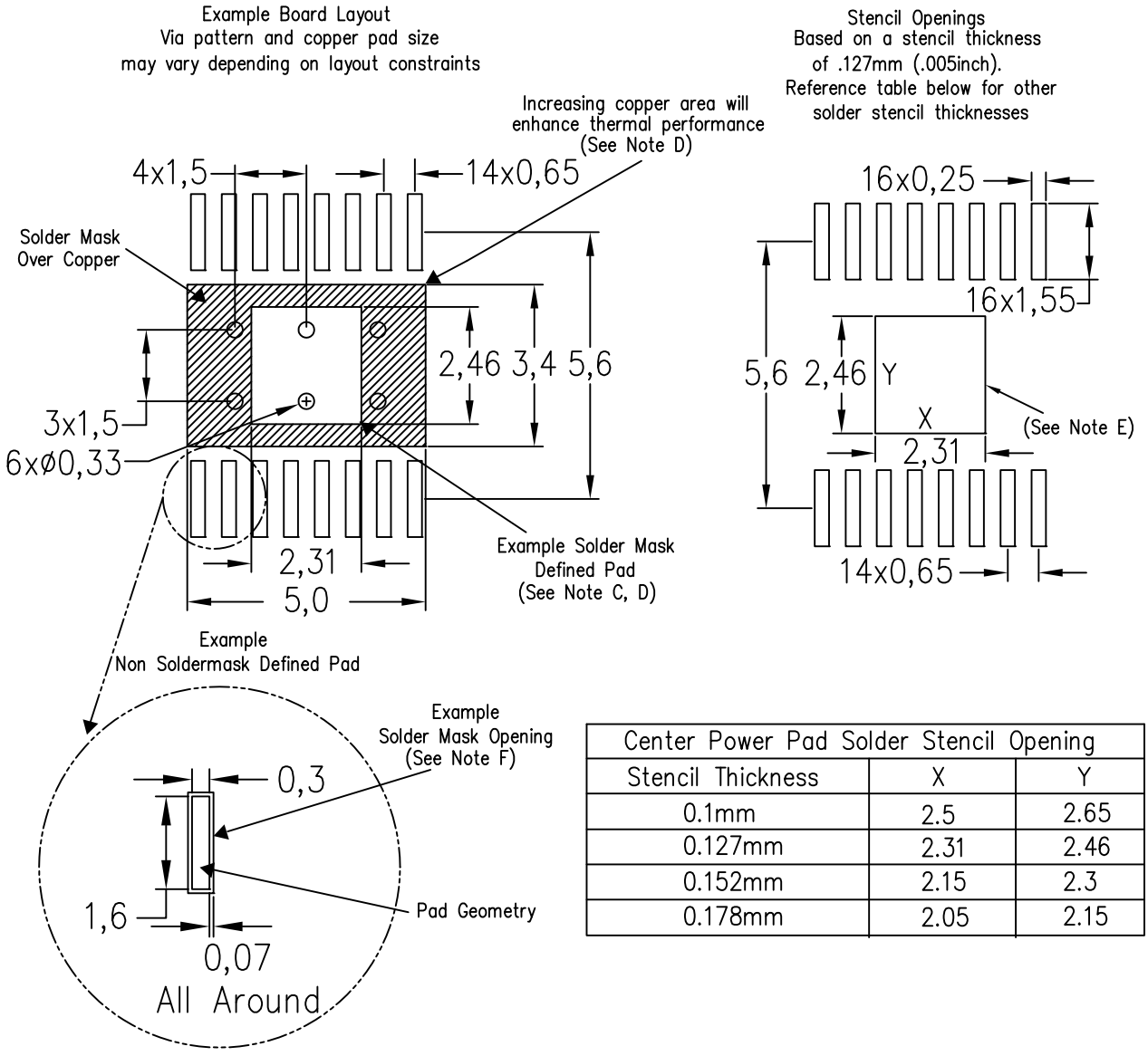
## PWP (R–PDSO–G16) PowerPAD™ PLASTIC SMALL OUTLINE

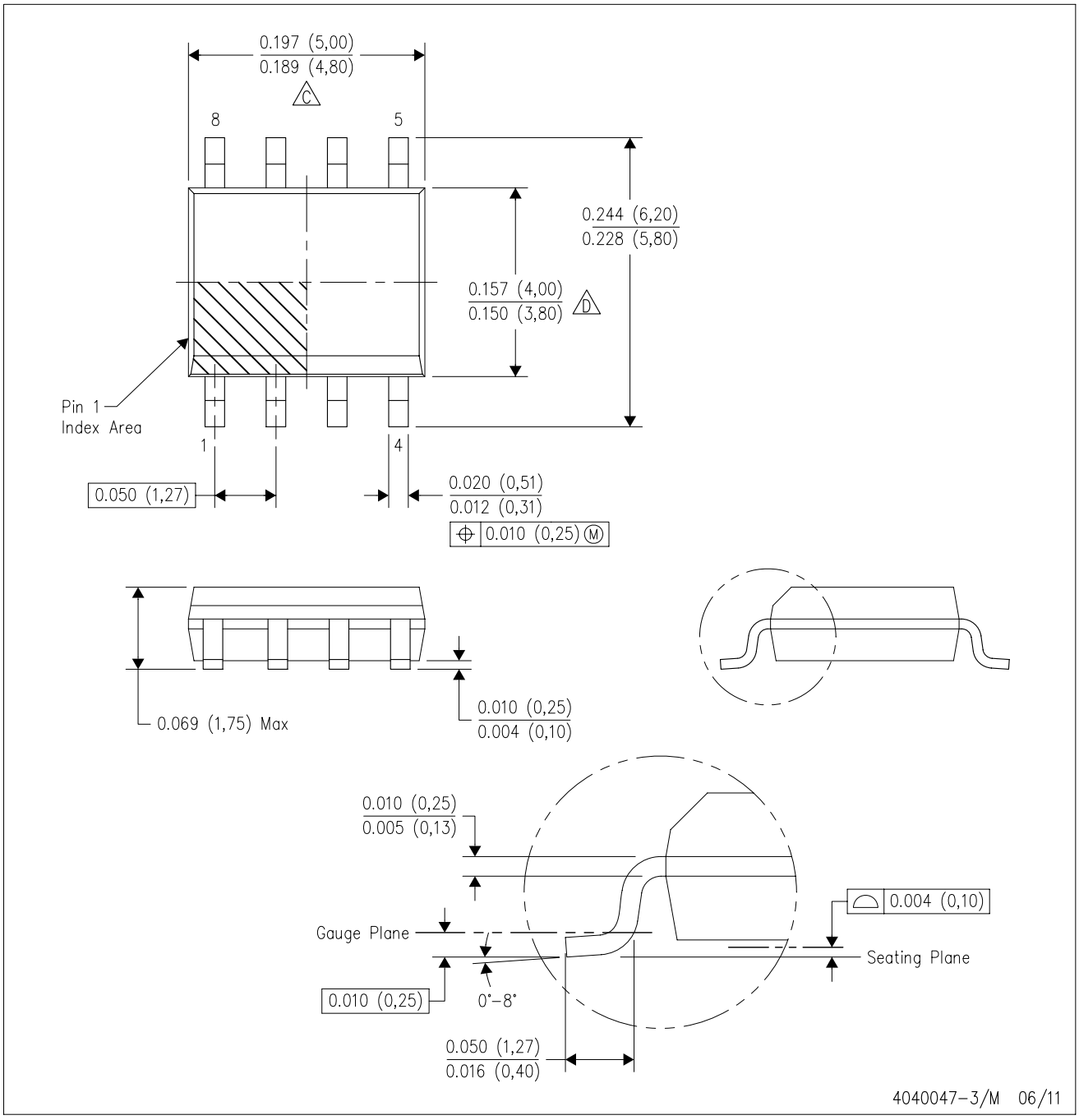



| Center Power Pad Solder Stencil Opening | | |
|---|---|---|
| Stencil Thickness | X | Y |
| 0.1mm | 2.5 | 2.65 |
| 0.127mm | 2.31 | 2.46 |
| 0.152mm | 2.15 | 2.3 |
| 0.178mm | 2.05 | 2.15 |

4207609–3/T 08/13

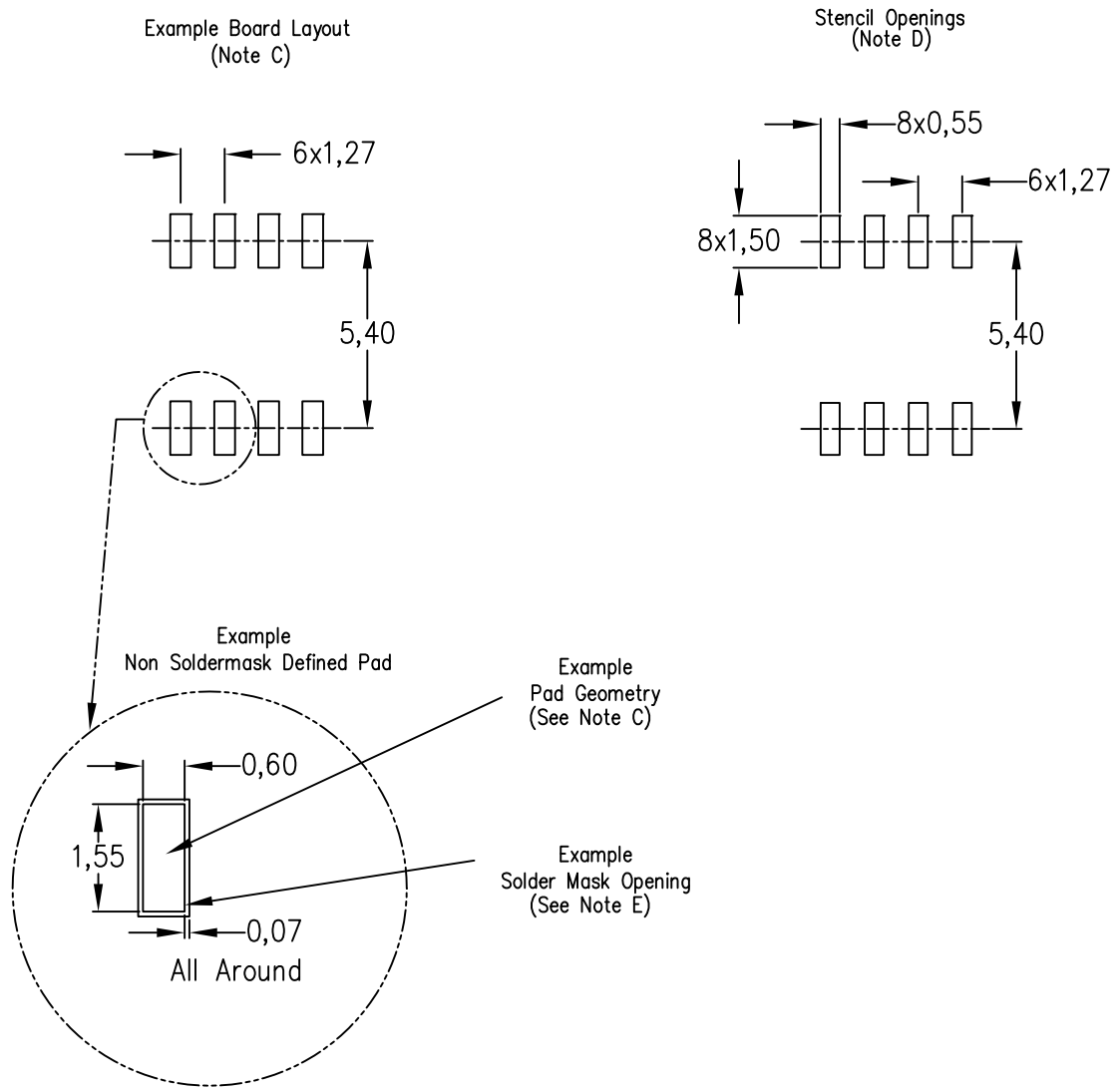
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE




NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AA.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE




NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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