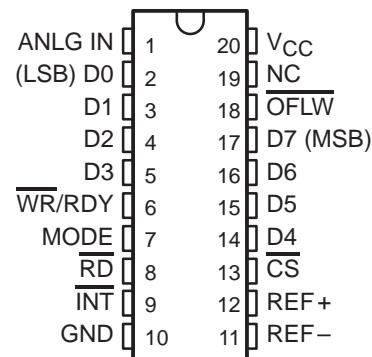


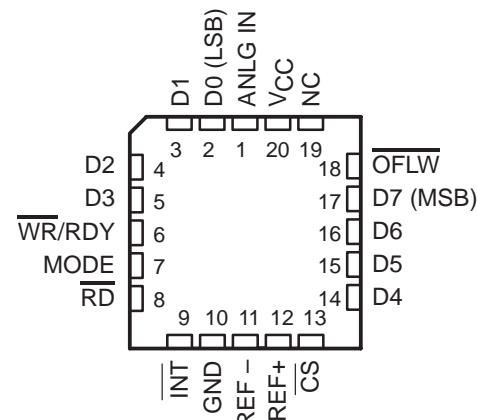
TLC0820AC, TLC0820AI
Advanced LinCMOS™ HIGH-SPEED 8-BIT ANALOG-TO-DIGITAL
CONVERTERS USING MODIFIED FLASH TECHNIQUES
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- Advanced LinCMOS™ Silicon-Gate Technology
- 8-Bit Resolution
- Differential Reference Inputs
- Parallel Microprocessor Interface
- Conversion and Access Time Over Temperature Range
- Read Mode . . . 2.5 μ s Max
- No External Clock or Oscillator Components Required
- On-Chip Track and Hold
- Single 5-V Supply
- TLC0820A Is Direct Replacement for National Semiconductor ADC0820C/CC and Analog Devices AD7820K/B/T

DB, DW, OR N PACKAGE
(TOP VIEW)



FN PACKAGE
(TOP VIEW)



NC – No internal connection

AVAILABLE OPTIONS

TA	TOTAL UNADJUSTED ERROR	PACKAGE			
		SSOP (DB)	PLASTIC SMALL OUTLINE (DW)	PLASTIC CHIP CARRIER (FN)	PLASTIC DIP (N)
0°C to 70°C	± 1 LSB	TLC0820ACDB	TLC0820ACDW	TLC0820ACFN	TLC0820ACN
-40°C to 85°C	± 1 LSB	—	TLC0820AIDW	TLC0820AIFN	TLC0820AIN

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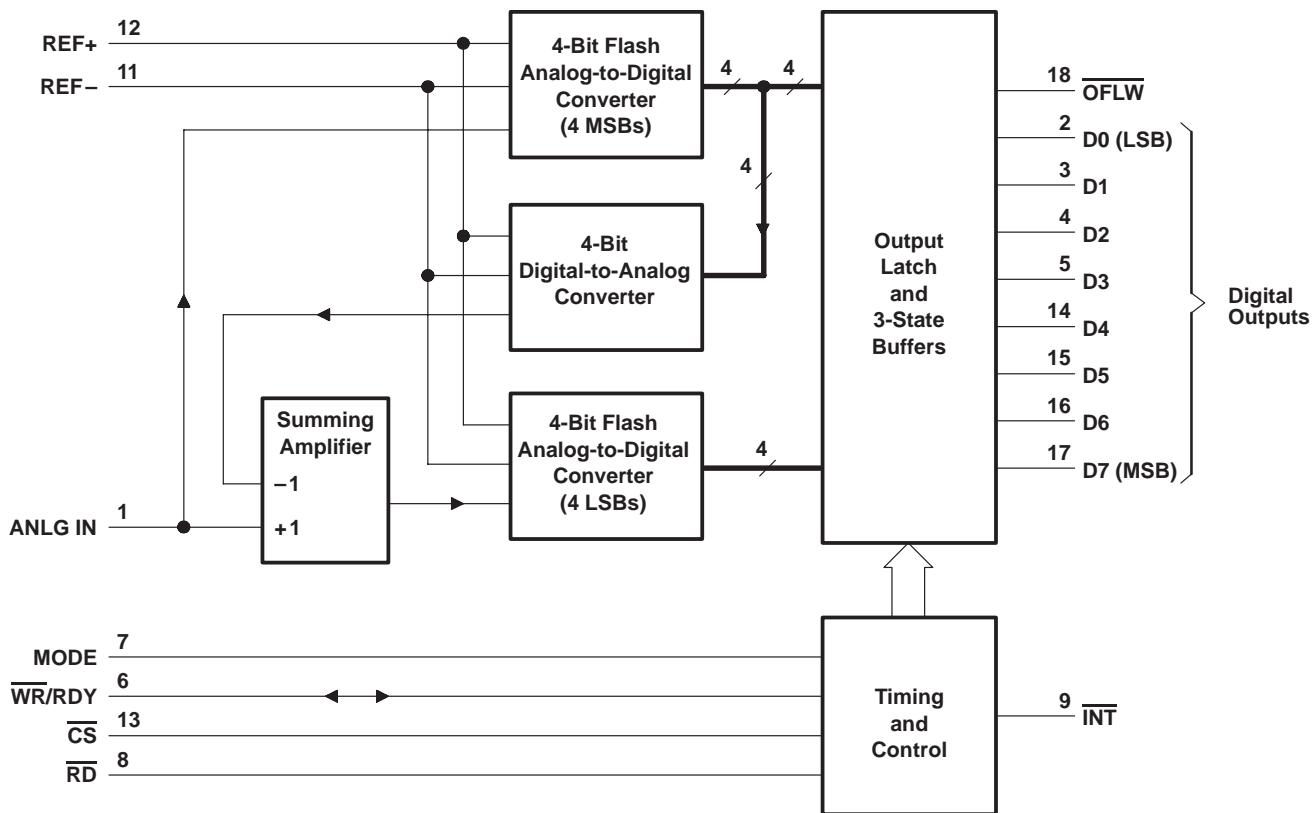
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functional block diagram



Terminal Functions

TERMINAL NAME	NO.	I/O	DESCRIPTION
ANLG IN	1	I	Analog input
CS	13	I	Chip select. CS must be low in order for RD or WR to be recognized by the ADC.
D0	2	O	Digital, 3-state output data, bit 1 (LSB)
D1	3	O	Digital, 3-state output data, bit 2
D2	4	O	Digital, 3-state output data, bit 3
D3	5	O	Digital, 3-state output data, bit 4
D4	14	O	Digital, 3-state output data, bit 5
D5	15	O	Digital, 3-state output data, bit 6
D6	16	O	Digital, 3-state output data, bit 7
D7	17	O	Digital, 3-state output data, bit 8 (MSB)
GND	10		Ground
INT	9	O	Interrupt. In the write-read mode, the interrupt output (INT) going low indicates that the internal count-down delay time, $t_{d(int)}$, is complete and the data result is in the output latch. The delay time $t_{d(int)}$ is typically 800 ns starting after the rising edge of WR (see operating characteristics and Figure 3). If RD goes low prior to the end of $t_{d(int)}$, INT goes low at the end of $t_{d(RD)}$ and the conversion results are available sooner (see Figure 2). INT is reset by the rising edge of either RD or CS.
MODE	7	I	Mode select. MODE is internally tied to GND through a 50- μ A current source, which acts like a pulldown resistor. When MODE is low, the read mode is selected. When MODE is high, the write-read mode is selected.
NC	19		No internal connection
OFLW	18	O	Overflow. Normally OFLW is a logical high. However, if the analog input is higher than V_{ref+} , OFLW will be low at the end of conversion. It can be used to cascade two or more devices to improve resolution (9 or 10 bits).
RD	8	I	Read. In the write-read mode with CS low, the 3-state data outputs D0 through D7 are activated when RD goes low. RD can also be used to increase the conversion speed by reading data prior to the end of the internal count-down delay time. As a result, the data transferred to the output latch is latched after the falling edge of RD. In the read mode with CS low, the conversion starts with RD going low. RD also enables the 3-state data outputs on completion of the conversion. RDY going into the high-impedance state and INT going low indicate completion of the conversion.
REF-	11	I	Reference voltage. REF – is placed on the bottom of the resistor ladder.
REF+	12	I	Reference voltage. REF + is placed on the top of the resistor ladder.
VCC	20		Power supply voltage
WR/RDY	6	I/O	Write ready. In the write-read mode with CS low, the conversion is started on the falling edge of the WR input signal. The result of the conversion is strobed into the output latch after the internal count-down delay time, $t_{d(int)}$, provided that the RD input does not go low prior to this time. The delay time $t_{d(int)}$ is approximately 800 ns. In the read mode, RDY (an open-drain output) goes low after the falling edge of CS and goes into the high-impedance state when the conversion is strobed into the output latch. It is used to simplify the interface to a microprocessor system.

TL-C0820AC, TL-C0820AI

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltages are with respect to network GND.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.5	5	8	V
Analog input voltage		-0.1		$V_{CC}+0.1$	V
Positive reference voltage, V_{ref+}		V_{ref-}		V_{CC}	V
Negative reference voltage, V_{ref-}		GND		V_{ref+}	V
High-level input voltage, V_{IH}	$V_{CC} = 4.75 \text{ V to } 5.25 \text{ V}$	\overline{CS} , $\overline{WR/RDY}$, \overline{RD}	2		V
		MODE	3.5		
Low-level input voltage, V_{IL}	$V_{CC} = 4.75 \text{ V to } 5.25 \text{ V}$	\overline{CS} , $\overline{WR/RDY}$, \overline{RD}		0.8	V
		MODE		1.5	
Pulse duration, write in write-read mode, $t_W(W)$ (see Figures 2, 3, and 4)			0.5	50	μs
Operating free-air temperature, T_A	TLC0820AC		0	70	$^{\circ}\text{C}$
	TLC0820AI		-40	85	

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electrical characteristics at specified operating free-air temperature, $V_{CC} = 5$ V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A^\dagger	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage D_0-D_7 , \overline{INT} , or \overline{OFLW}	$V_{CC} = 4.75$ V, $I_{OH} = -360$ μ A	Full range	2.4			V
		$V_{CC} = 4.75$ V, $I_{OH} = -10$ μ A	Full range	4.5			
			25°C	4.6			
V_{OL}	Low-level output voltage D_0-D_7 , \overline{OFLW} , \overline{INT} , or WR/RDY	$V_{CC} = 5.25$ V, $I_{OL} = 1.6$ mA	Full range		0.4		V
			25°C		0.34		
I_{IH}	High-level input current CS or \overline{RD} WR/RDY MODE	$V_{IH} = 5$ V	Full range	0.005	1		μ A
			Full range		3		
			25°C	0.1	0.3		
			Full range		200		
			25°C	50	170		
I_{IL}	Low-level input current CS , $\overline{WR/RDY}$, \overline{RD} , or MODE	$V_{IL} = 0$	Full range	-0.005	-1		μ A
I_{OZ}	Off-state (high-impedance-state) output current D_0-D_7 or $\overline{WR/RDY}$	$V_O = 5$ V	Full range		3		μ A
			25°C	0.1	0.3		
		$V_O = 0$	Full range		-3		
			25°C	-0.1	-0.3		
I_I	Analog input current CS at 5 V, $V_I = 5$ V CS at 5 V, $V_I = 0$	CS at 5 V, $V_I = 5$ V	Full range		3		μ A
			25°C		0.3		
		CS at 5 V, $V_I = 0$	Full range		-3		
			25°C		-0.3		
			25°C		-0.3		
I_{OS}	Short-circuit output current D_0-D_7 , \overline{OFLW} , \overline{INT}	$V_O = 5$ V	Full range	7			mA
			25°C	8.4	14		
		$V_O = 0$	Full range	-6			
			25°C	-7.2	-12		
			Full range	-4.5			
			25°C	-5.3	-9		
R_{ref}	Reference resistance		Full range	1.25	6		$k\Omega$
			25°C	1.4	2.3	5.3	
I_{CC}	Supply current	CS , $\overline{WR/RDY}$, and RD at 0 V	Full range		15		mA
			25°C		7.5	13	
C_i	Input capacitance D_0-D_7 ANLG IN		Full range	5			pF
				45			
C_o	Output capacitance D_0-D_7		Full range		5		pF

† Full range is as specified in recommended operating conditions.

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operating characteristics, $V_{CC} = 5$ V, $V_{ref+} = 5$ V, $V_{ref-} = 0$, $t_r = t_f = 20$ ns, $T_A = 25^\circ\text{C}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS [†]		MIN	TYP	MAX	UNIT
k_{SVS}	Supply-voltage sensitivity	$V_{CC} = 5$ V $\pm 5\%$, $T_A = \text{MIN to MAX}$		$\pm 1/16$	$\pm 1/4$	LSB
	Total unadjusted error [‡]	MODE at 0 V, $T_A = \text{MIN to MAX}$		1		LSB
$t_{conv(R)}$	Conversion time, read mode	MODE at 0 V, See Figure 1		1.6	2.5	μs
$t_a(R)$	Access time, $\overline{RD} \downarrow$ to data valid	MODE at 0 V, See Figure 1	$t_{conv(R)} + 20$	$t_{conv(R)} + 50$		ns
$t_a(R1)$	Access time, $\overline{RD} \downarrow$ to data valid	MODE at 5 V, $t_d(WR) < t_d(\text{int})$, See Figure 2	$C_L = 15$ pF	190	280	ns
			$C_L = 100$ pF	210	320	
$t_a(R2)$	Access time, $\overline{RD} \downarrow$ to data valid	MODE at 5 V, $t_d(WR) > t_d(\text{int})$, See Figure 3	$C_L = 15$ pF	70	120	ns
			$C_L = 100$ pF	90	150	
$t_a(\text{INT})$	Access time, $\overline{INT} \downarrow$ to data valid	MODE at 5 V, See Figure 4		20	50	ns
t_{dis}	Disable time, $\overline{RD} \uparrow$ to data valid	$R_L = 1$ k Ω , $C_L = 10$ pF, See Figures 1, 2, 3, and 5		70	95	ns
$t_d(\text{int})$	Delay time, WR/RDY \uparrow to INT \downarrow	MODE at 5 V, $C_L = 50$ pF, See Figures 2, 3, and 4		800	1300	ns
$t_d(\text{NC})$	Delay time, to next conversion	See Figures 1, 2, 3, and 4		500		ns
$t_d(WR)$	Delay time, WR/RDY \uparrow to $\overline{RD} \downarrow$ in write-read mode	See Figure 2		0.4		μs
$t_d(\text{RDY})$	Delay time, CS \downarrow to WR/RDY \downarrow	MODE at 0 V, $C_L = 50$ pF, See Figure 1		50	100	ns
$t_d(\text{RIH})$	Delay time, $\overline{RD} \uparrow$ to $\overline{INT} \uparrow$	$C_L = 50$ pF, See Figures 1, 2, and 3		125	225	ns
$t_d(\text{RIL})$	Delay time, RD \downarrow to INT \downarrow	MODE at 5 V, $t_d(WR) < t_d(\text{int})$, See Figure 2		200	290	ns
$t_d(\text{WIH})$	Delay time, WR/RDY \uparrow to $\overline{INT} \uparrow$	MODE at 5 V, $C_L = 50$ pF, See Figure 4		175	270	ns
Slew-rate tracking				0.1		V/ μs

[†] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.[‡] Total unadjusted error includes offset, full-scale, and linearity errors.

PARAMETER MEASUREMENT INFORMATION

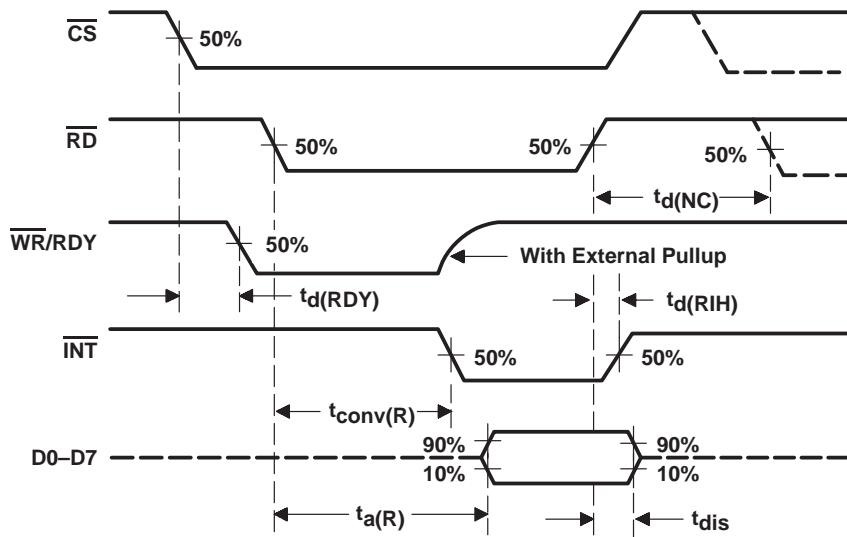
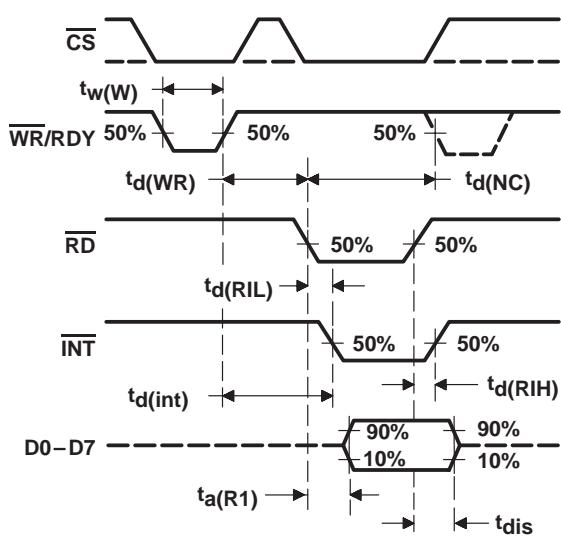
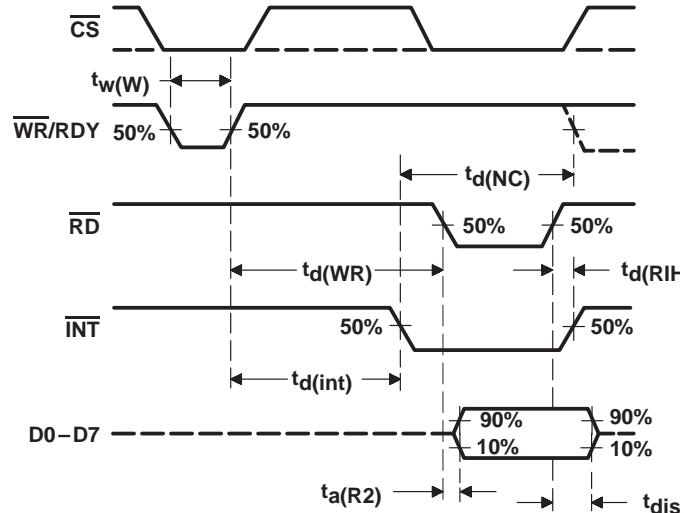


Figure 1. Read-Mode Waveforms (MODE Low)



**Figure 2. Write-Read-Mode Waveforms
 [MODE High and $t_d(WR) < t_d(int)$]**



**Figure 3. Write-Read-Mode Waveforms
 [MODE High and $t_d(WR) > t_d(int)$]**

PARAMETER MEASUREMENT INFORMATION

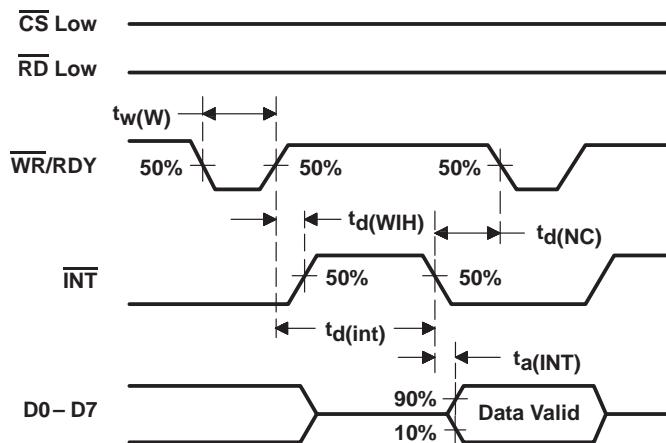


Figure 4. Write-Read-Mode Waveforms
(Stand-Alone Operation, MODE High, and \overline{RD} Low)

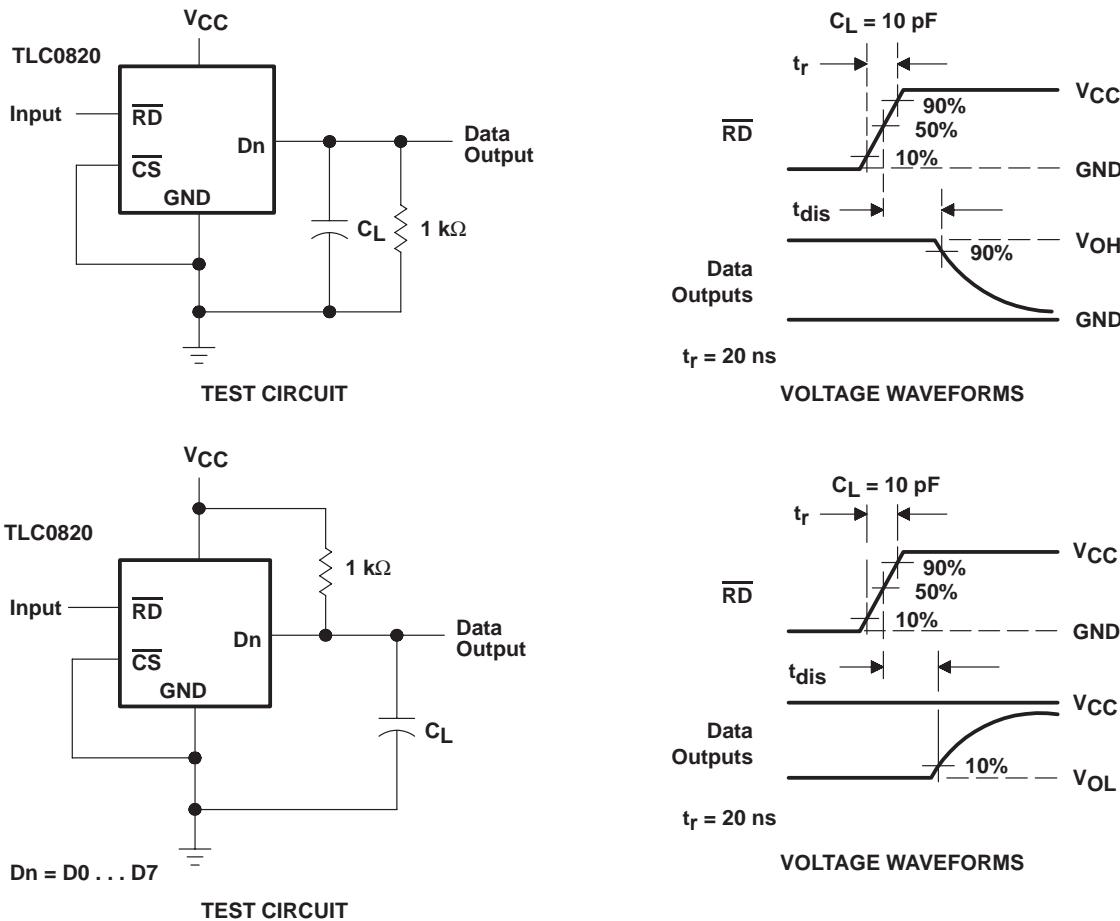


Figure 5. Test Circuit and Voltage Waveforms

PRINCIPLES OF OPERATION

The TLC0820AC and TLC0820AI each employ a combination of sampled-data comparator techniques and flash techniques common to many high-speed converters. Two 4-bit flash analog-to-digital conversions are used to give a full 8-bit output.

The recommended analog input voltage range for conversion is -0.1 V to $V_{CC} + 0.1\text{ V}$. Analog input signals that are less than $V_{ref-} + 1/2\text{ LSB}$ or greater than $V_{ref+} - 1/2\text{ LSB}$ convert to 00000000 or 11111111, respectively. The reference inputs are fully differential with common-mode limits defined by the supply rails. The reference input values define the full-scale range of the analog input. This allows the gain of the ADC to be varied for ratiometric conversion by changing the V_{ref+} and V_{ref-} voltages.

The device operates in two modes, read (only) and write-read, that are selected by MODE. The converter is set to the read (only) mode when MODE is low. In the read mode, $\overline{WR/RDY}$ is used as an output and is referred to as the ready terminal. In this mode, a low on $\overline{WR/RDY}$ while \overline{CS} is low indicates that the device is busy. Conversion starts on the falling edge of \overline{RD} and is completed no more than $2.5\text{ }\mu\text{s}$ later when \overline{INT} falls and $\overline{WR/RDY}$ returns to the high-impedance state. Data outputs also change from high-impedance to active states at this time. After the data is read, \overline{RD} is taken high, \overline{INT} returns high, and the data outputs return to their high-impedance states.

When MODE is high, the converter is set to the write-read mode and $\overline{WR/RDY}$ is referred to as the write terminal. Taking \overline{CS} and $\overline{WR/RDY}$ low selects the converter and initiates measurement of the input signal. Approximately 600 ns after $\overline{WR/RDY}$ returns high, the conversion is completed. Conversion starts on the rising edge of $\overline{WR/RDY}$ in the write-read mode.

The high-order 4-bit flash ADC measures the input by means of 16 comparators operating simultaneously. A high-precision 4-bit DAC then generates a discrete analog voltage from the result of that conversion. After a time delay, a second bank of comparators does a low-order conversion on the analog difference between the input level and the high-order DAC output. The results from each of these conversions enter an 8-bit latch and are output to the 3-state output buffers on the falling edge of \overline{RD} .

APPLICATION INFORMATION

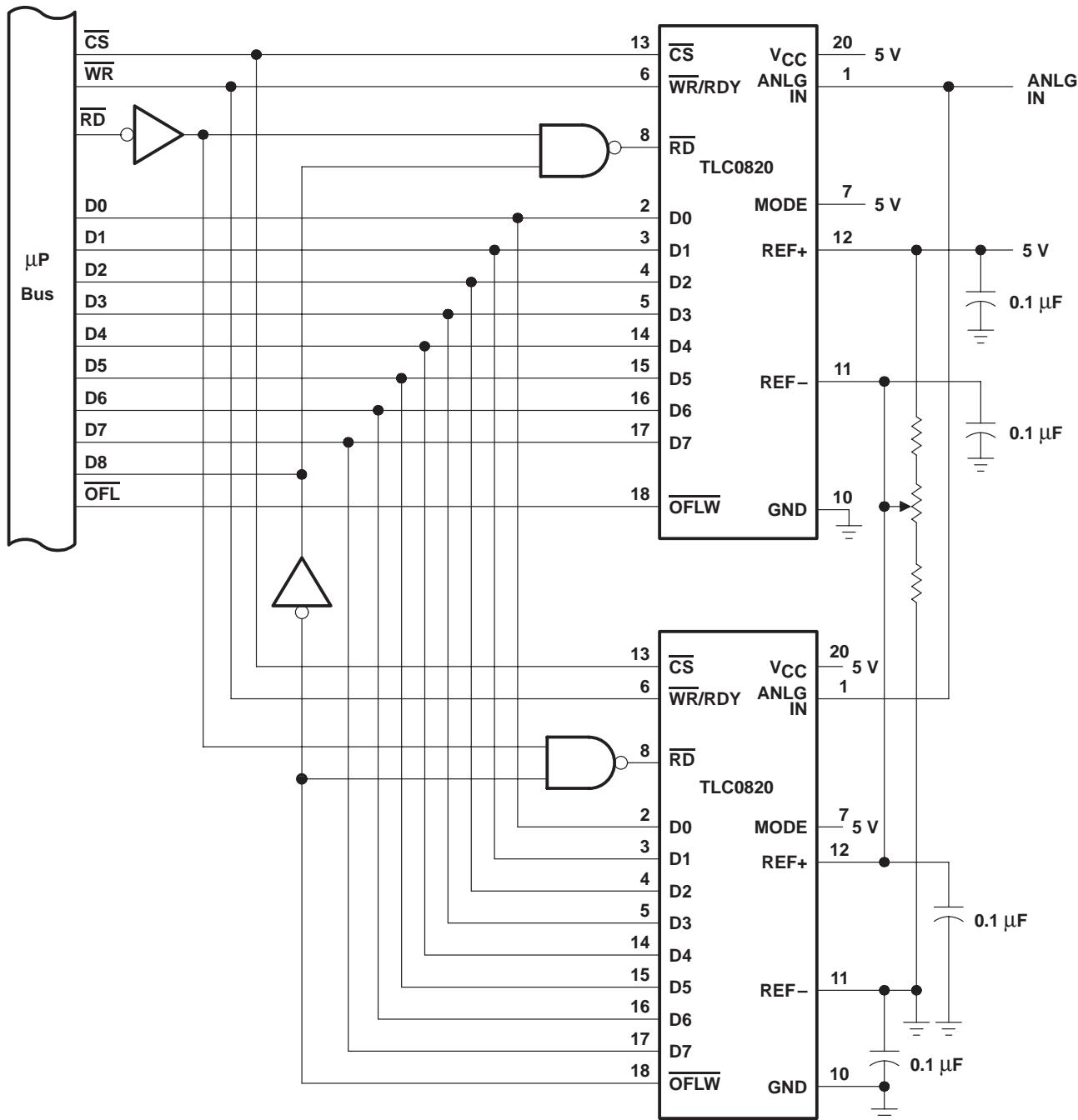


Figure 6. Configuration for 9-Bit Resolution

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
TLC0820ACDB	ACTIVE	SSOP	DB	20		Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLC0820ACDBG4	ACTIVE	SSOP	DB	20		Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLC0820ACDBR	ACTIVE	SSOP	DB	20		Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLC0820ACDW	ACTIVE	SOIC	DW	20		Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLC0820ACDWG4	ACTIVE	SOIC	DW	20		Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLC0820ACDWR	ACTIVE	SOIC	DW	20		Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLC0820ACDWG4	ACTIVE	SOIC	DW	20		Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLC0820ACFN	ACTIVE	PLCC	FN	20		Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM
TLC0820ACFNG3	ACTIVE	PLCC	FN	20		Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM
TLC0820ACFNR	ACTIVE	PLCC	FN	20		Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM
TLC0820ACFNRG3	ACTIVE	PLCC	FN	20		Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM
TLC0820ACN	ACTIVE	PDIP	N	20		Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
TLC0820ACNE4	ACTIVE	PDIP	N	20		Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
TLC0820AIDW	ACTIVE	SOIC	DW	20		Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLC0820AIDWG4	ACTIVE	SOIC	DW	20		Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLC0820AIDWR	ACTIVE	SOIC	DW	20		Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLC0820AIDWRG4	ACTIVE	SOIC	DW	20		Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLC0820AIFN	ACTIVE	PLCC	FN	20		Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM
TLC0820AIFNG3	ACTIVE	PLCC	FN	20		Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM
TLC0820AIN	ACTIVE	PDIP	N	20		Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
TLC0820AINE4	ACTIVE	PDIP	N	20		Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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