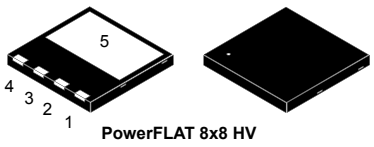
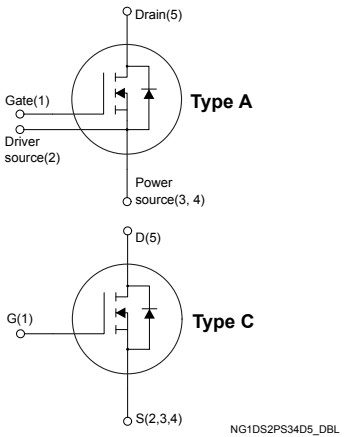
N-channel 650 V, 180 mΩ typ., 15 A, MDmesh M5 Power MOSFET in a PowerFLAT 8x8 HV package



PowerFLAT 8x8 HV



Features

Order code	V_{DS} @ T_{Jmax}	$R_{DS(on)}$ max.	I_D
STL22N65M5	710 V	210 mΩ	15 A

- Extremely low $R_{DS(on)}$
- Low gate charge and input capacitance
- Excellent switching performance
- 100% avalanche tested

Applications

- Switching applications

Description

This device is an N-channel Power MOSFET based on the MDmesh M5 innovative vertical process technology combined with the well-known PowerMESH horizontal layout. The resulting product offers extremely low on-resistance, making it particularly suitable for applications requiring high power and superior efficiency.

Product status link
STL22N65M5

Product summary	
Order code	STL22N65M5
Marking	22N65M5
Package	PowerFLAT 8x8 HV
Packing	Tape and reel

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{GS}	Gate-source voltage	±25	V
I_D	Drain current (continuous) at T_C = 25 °C	15	A
	Drain current (continuous) at T_C = 100 °C	9.5	
I_{DM}(1)	Drain current (pulsed)	60	A
P_{TOT}	Total power dissipation at T_C = 25 °C	110	W
dv/dt(2)	Peak diode recovery voltage slope	15	V/ns
T_{stg}	Storage temperature range	-55 to 150	°C
T_j	Operating junction temperature range		

1. *Pulse width is limited by safe operating area.*
2. *I_{SD} ≤ 15 A, di/dt ≤ 400 A/µs, $V_{DS(peak)}$ < $V_{(BR)DSS}$, V_{DD} = 400 V*

Table 2. Thermal data

Symbol	Parameter	Value	Unit
R_{thJA}	Thermal resistance, junction-to-case	1.14	°C/W
R_{thJB}(1)	Thermal resistance, junction-to-board	45	°C/W

1. *When mounted on an 1-inch² FR-4, 2oz Cu board*

Table 3. Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR}(1)	Avalanche current, repetitive or not repetitive	4	A
E_{AS}(2)	Single pulse avalanche energy	270	mJ

1. *Pulse width limited by T_{jmax}*
2. *Starting T_j = 25 °C, I_D = I_{AR}, V_{DD} = 50 V*

2 Electrical characteristics

(T_{case} = 25 °C unless otherwise specified)

Table 4. Static

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V, I_D = 1 mA	650			V
I_{DSS}	Zero gate voltage drain current	V_{GS} = 0 V, V_{DS} = 650 V			1	µA
		V_{GS} = 0 V, V_{DS} = 650 V, T_{case} = 125 °C(1)			100	
I_{GSS}	Gate-body leakage current	V_{DS} = 0 V, V_{GS} = ±25 V			±100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	3	4	5	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D = 8.5 A		180	210	mΩ

1. *Defined by design, not subject to production test.*

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS} = 100 V, f = 1 MHz, V_{GS} = 0 V	-	1434	-	pF
C_{oss}	Output capacitance		-	38	-	
C_{rss}	Reverse transfer capacitance		-	3.7	-	
$C_{o(er)}$(1)	Equivalent output capacitance energy related	V_{DS} = 0 to 520 V, V_{GS} = 0 V	-	35	-	pF
$C_{o(tr)}$(2)	Equivalent output capacitance time related		-	118	-	
R_G	Intrinsic gate resistance	f = 1 MHz open drain	-	3.5	-	Ω
Q_g	Total gate charge	V_{DD} = 520 V, I_D = 9 A, V_{GS} = 0 to 10 V (see Figure 15. Test circuit for gate charge behavior)	-	36	-	nC
Q_{gs}	Gate-source charge		-	7.5	-	
Q_{gd}	Gate-drain charge		-	18	-	

1. *$C_{o(er)}$ is a constant capacitance value that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS}.*
2. *$C_{o(tr)}$ is a constant capacitance value that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS}.*

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(v)}$	Voltage delay time	V_{DD} = 400 V, I_D = 12 A, R_G = 4.7 Ω, V_{GS} = 10 V (see Figure 16. Test circuit for inductive load switching and diode recovery times and Figure 19. Switching time waveform)	-	43	-	ns
$t_{r(v)}$	Voltage rise time		-	7.5	-	
$t_{f(i)}$	Current fall time		-	7.5	-	
$t_{c(off)}$	Crossing time		-	11.5	-	

Table 7. Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		15	A
I_{SDM}(1)	Source-drain current (pulsed)		-		60	A
V_{SD}(2)	Forward on voltage	V_{GS} = 0 V, I_{SD} = 15 A	-		1.5	V
t_{rr}	Reverse recovery time	I_{SD} = 15 A, di/dt = 100 A/µs,	-	272		ns
Q_{rr}	Reverse recovery charge	V_{DD} = 100 V	-	3.4		µC
I_{RRM}	Reverse recovery current	(see Figure 16. Test circuit for inductive load switching and diode recovery times)	-	25		A
t_{rr}	Reverse recovery time	I_{SD} = 15 A, di/dt = 100 A/µs,	-	336		ns
Q_{rr}	Reverse recovery charge	V_{DD} = 100 V, T_j = 150 °C	-	4.3		µC
I_{RRM}	Reverse recovery current	(see Figure 16. Test circuit for inductive load switching and diode recovery times)	-	25.6		A

1. *Pulse width is limited by safe operating area.*
2. *Pulse test: pulse duration = 300 µs, duty cycle 1.5%.*

2.1 Electrical characteristics curves

Figure 1. Safe operating area

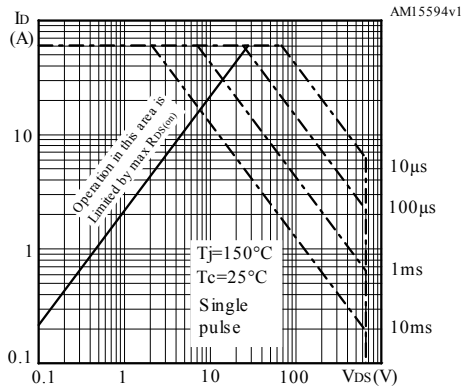


Figure 2. Thermal impedance

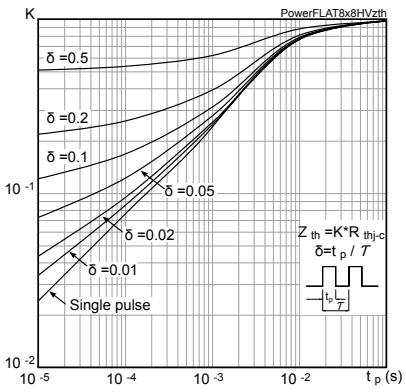


Figure 3. Output characterisics

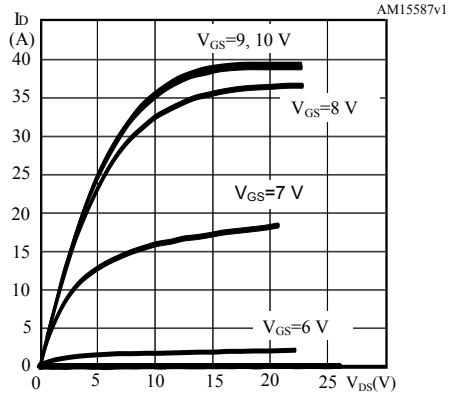


Figure 4. Transfer characteristics

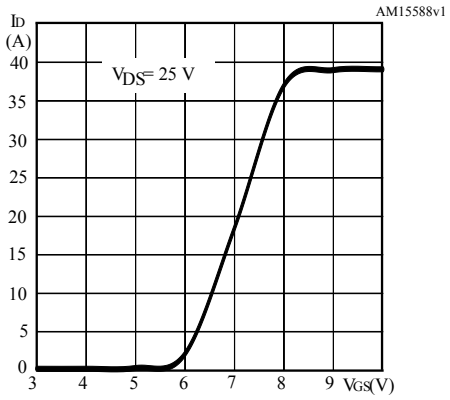


Figure 5. Gate charge vs gate-source voltage

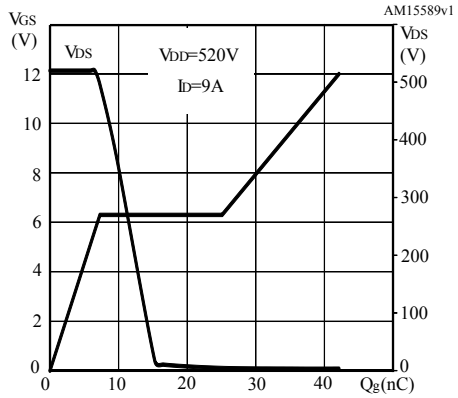


Figure 6. Static drain-source on-resistance

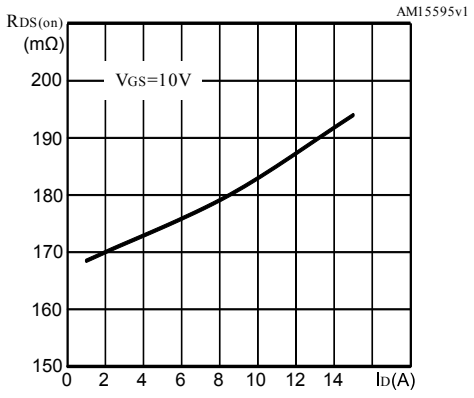


Figure 7. Capacitance variations

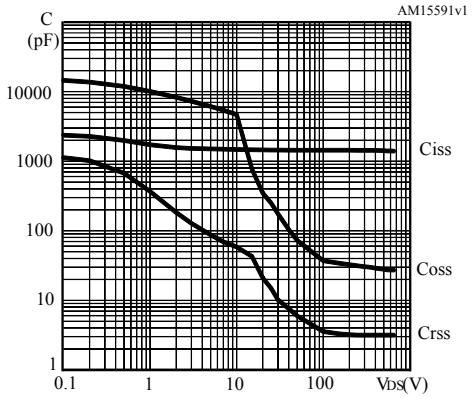


Figure 8. Output capacitance stored energy

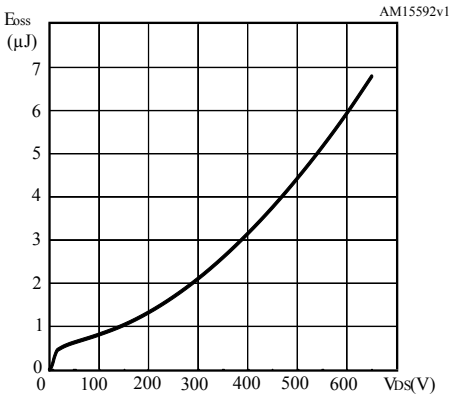


Figure 9. Normalized gate threshold voltage vs temperature

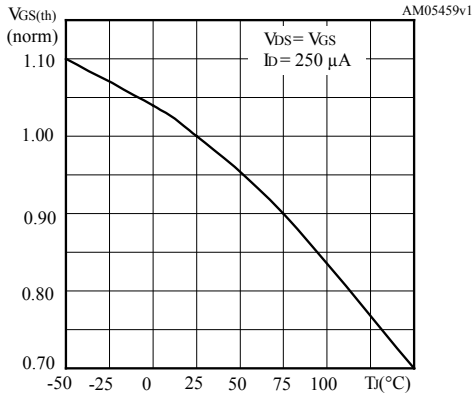


Figure 10. Normalized on-resistance vs temperature

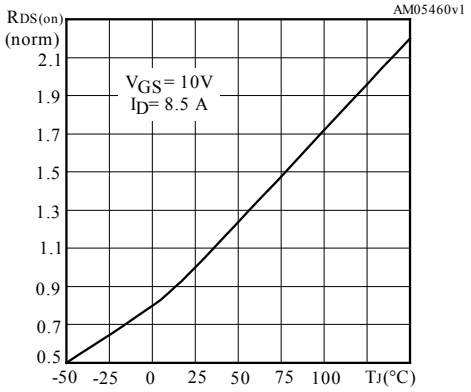


Figure 11. Normalized breakdown voltage vs temperature

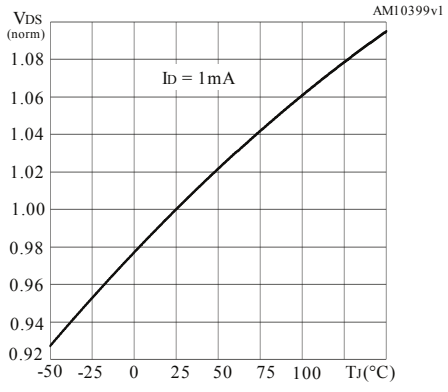


Figure 12. Drain-source diode forward characteristics

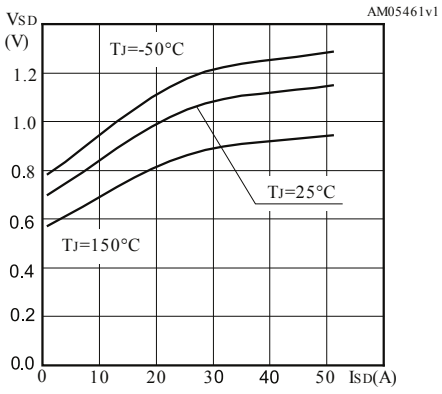
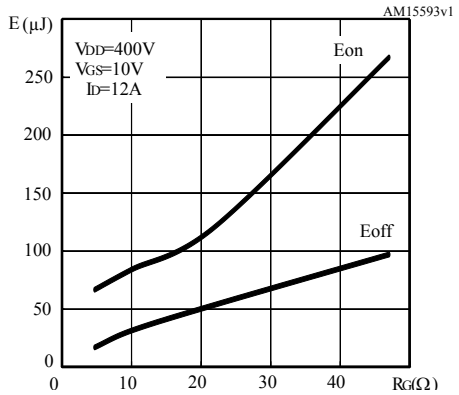


Figure 13. **Switching energy vs gate resistance**



3 Test circuits

Figure 14. Test circuit for resistive load switching times

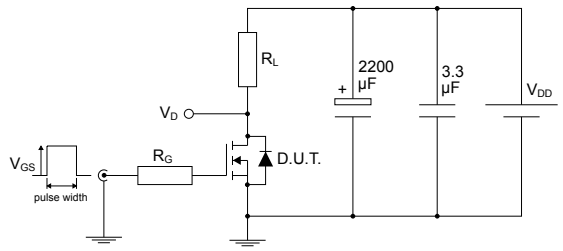


Figure 15. Test circuit for gate charge behavior

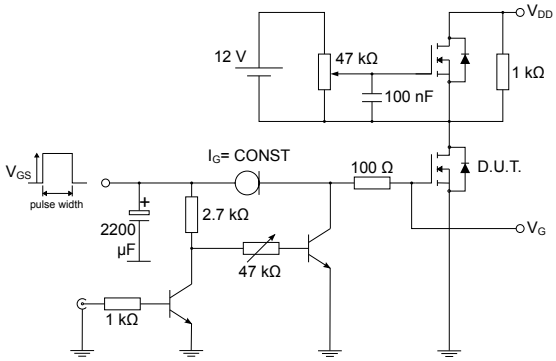


Figure 16. Test circuit for inductive load switching and diode recovery times

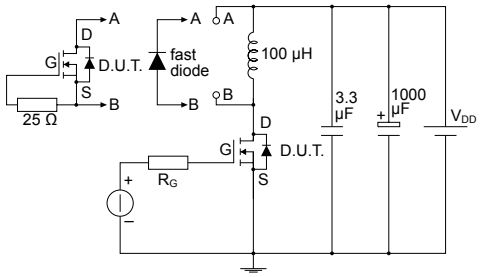


Figure 17. Unclamped inductive load test circuit

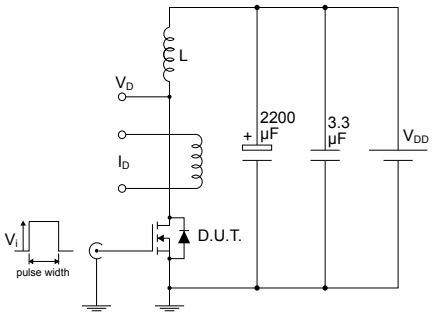


Figure 18. Unclamped inductive waveform

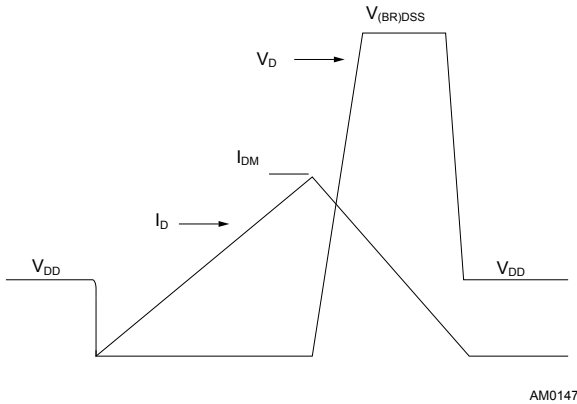
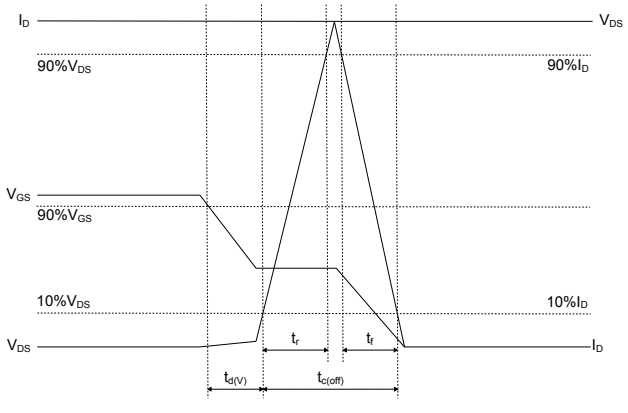


Figure 19. Switching time waveform



4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

4.1 PowerFLAT 8x8 HV type A package information

Figure 20. PowerFLAT 8x8 HV type A package outline

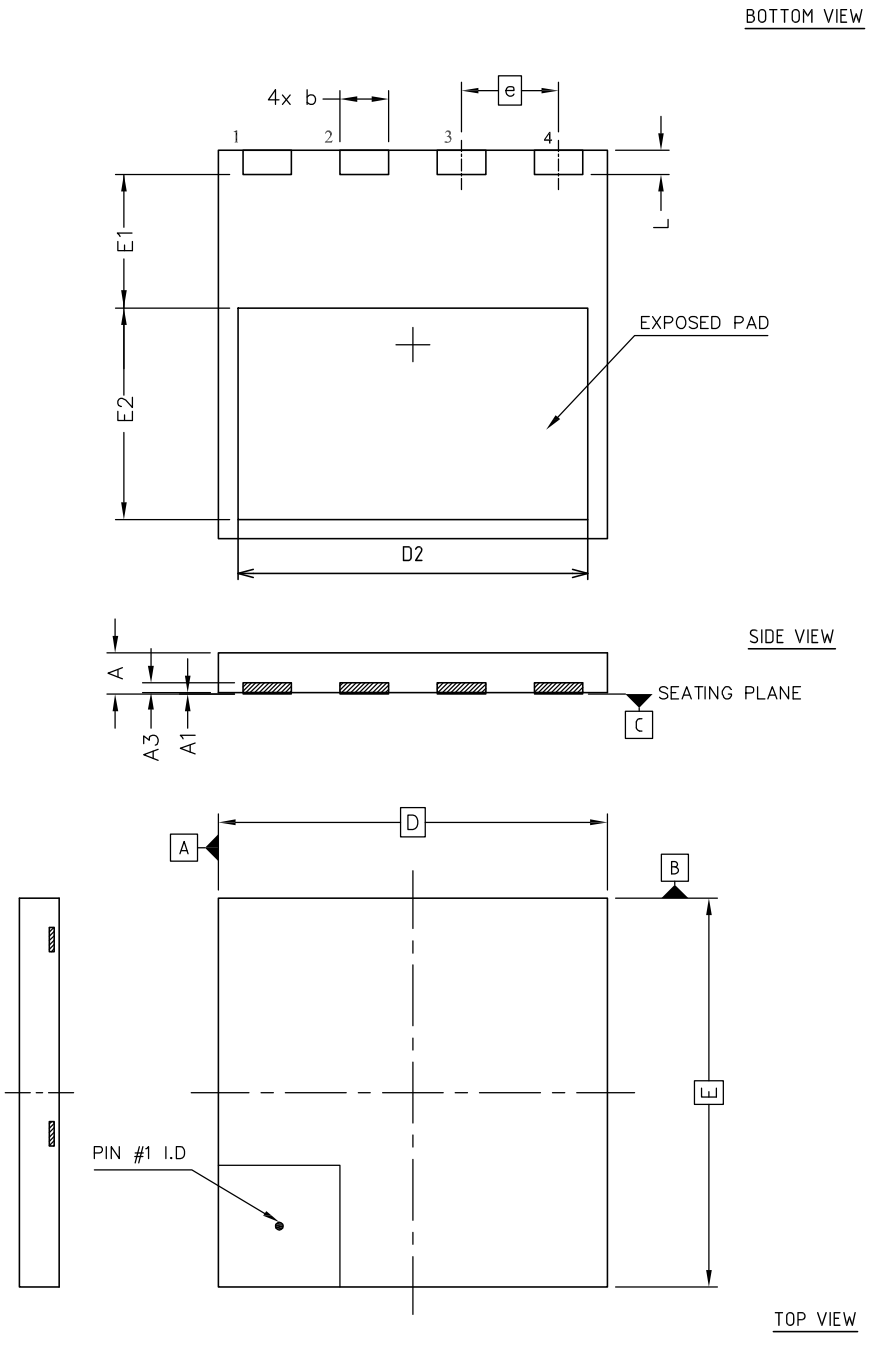
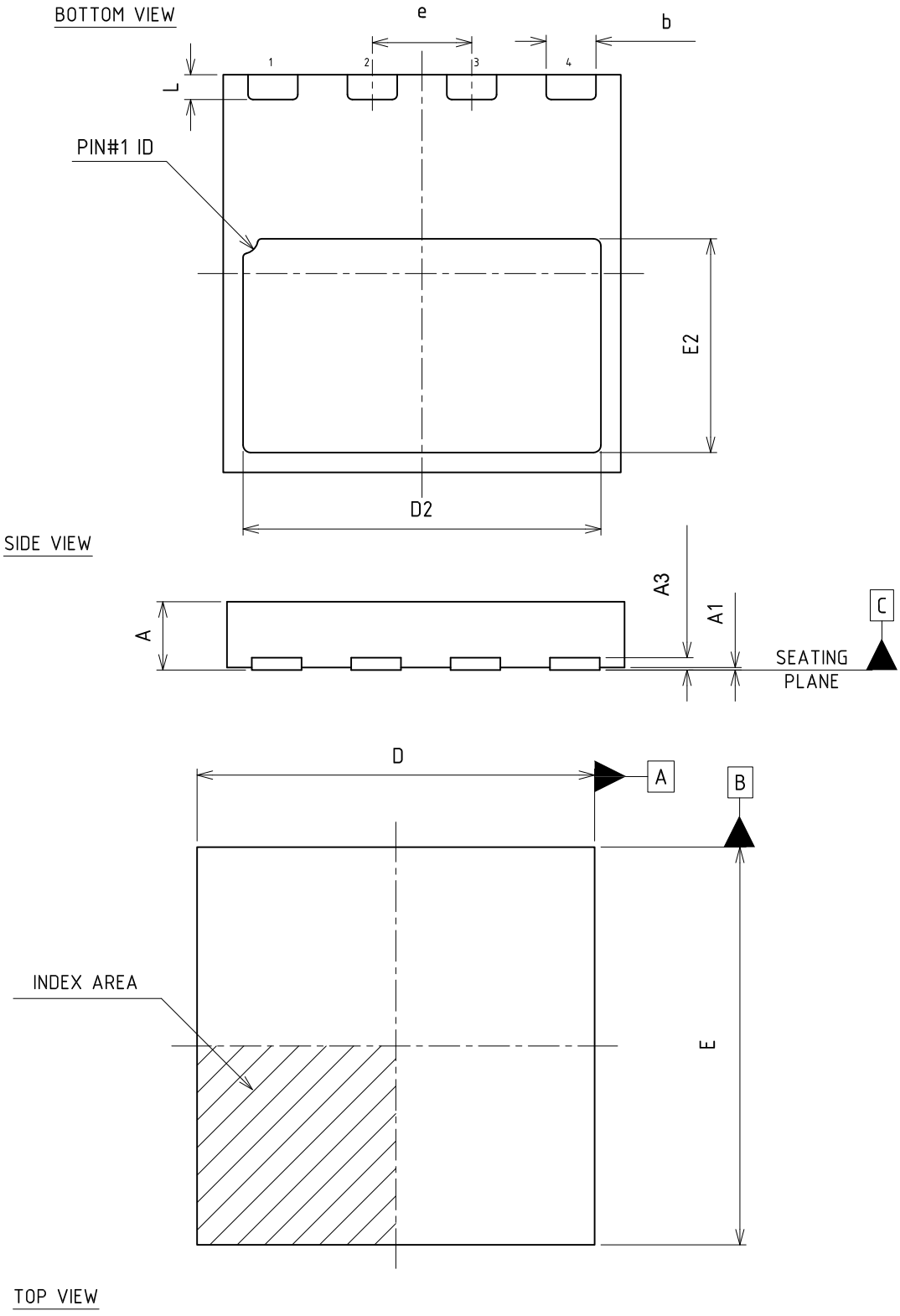


Table 8. **PowerFLAT 8x8 HV type A mechanical data**

Ref.	Dimensions (in mm)		
	Min.	Typ.	Max.
A	0.75	0.85	0.95
A1	0.00		0.05
A3	0.10	0.20	0.30
b	0.90	1.00	1.10
D	7.90	8.00	8.10
E	7.90	8.00	8.10
D2	7.10	7.20	7.30
E1	2.65	2.75	2.85
E2	4.25	4.35	4.45
e		2.00 BSC	
L	0.40	0.50	0.60

4.2 PowerFLAT 8x8 HV type C package information

Figure 21. **PowerFLAT 8x8 HV type C package outline**

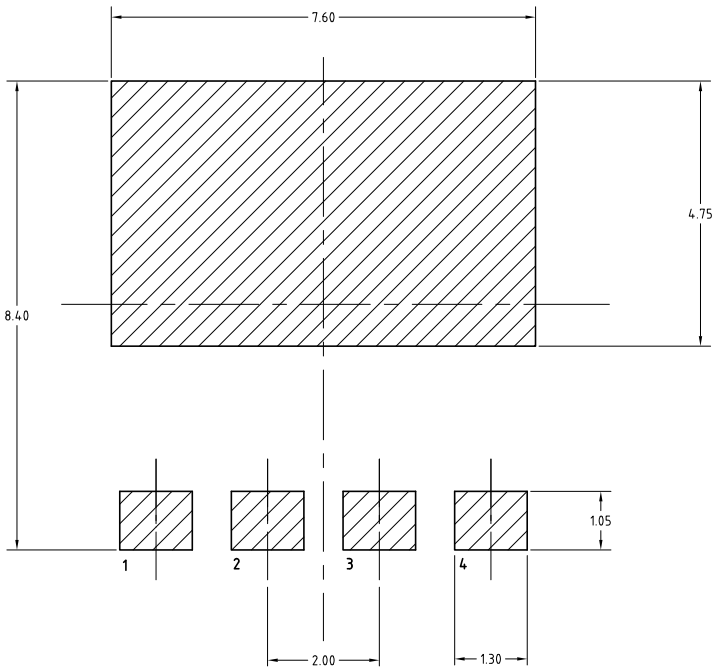


8222871_Rev4_typeC

Table 9. PowerFLAT 8x8 HV type C mechanical data

Ref.	Dimensions (in mm)		
	Min.	Typ.	Max.
A	0.80	0.90	1.00
A1	0.00	0.02	0.05
A3	0.10	0.20	0.30
b	0.95	1.00	1.05
D		8.00	
D2	7.05	7.20	7.30
E		8.00	
E2	4.15	4.30	4.40
e		2.00	
L	0.40	0.50	0.60

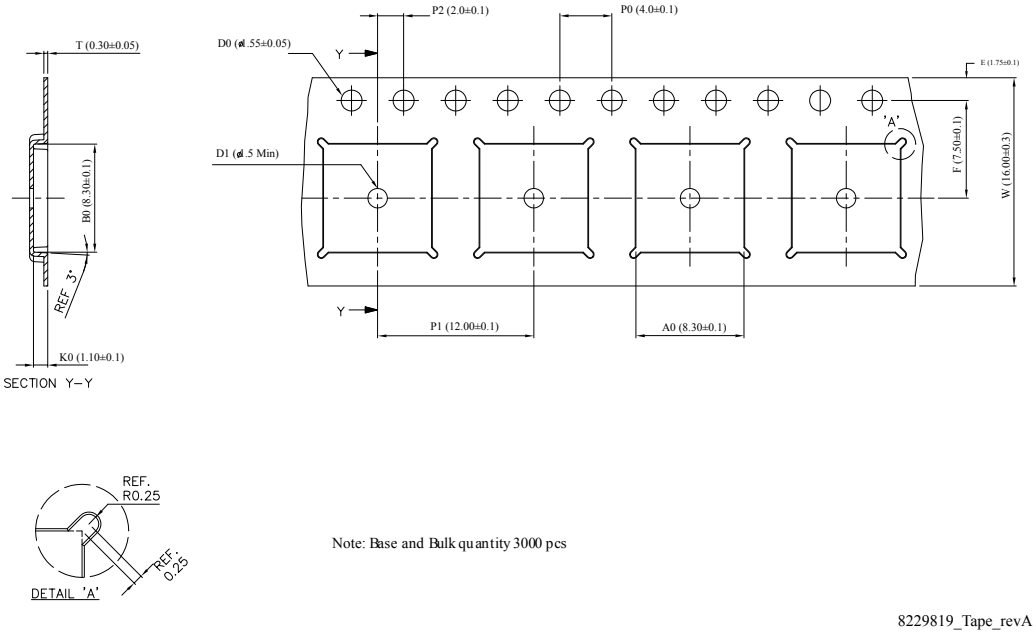
Figure 22. PowerFLAT 8x8 HV footprint



Note: All dimensions are in millimeters.

4.3 PowerFLAT 8x8 HV packing information

Figure 23. PowerFLAT 8x8 HV tape



Note: All dimensions are in millimeters.

Figure 24. PowerFLAT 8x8 HV package orientation in carrier tape

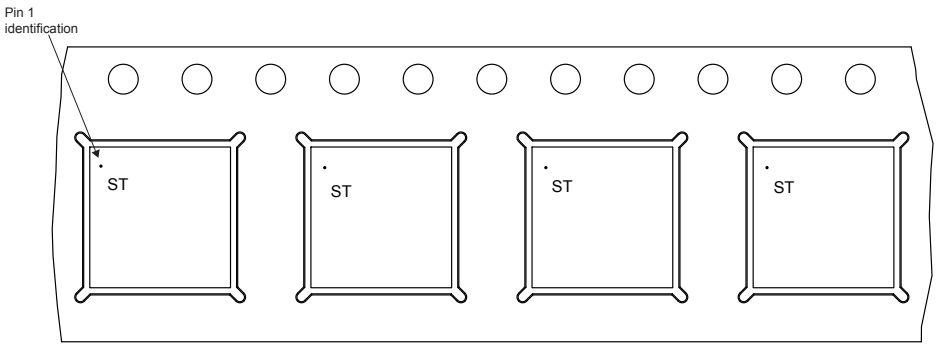
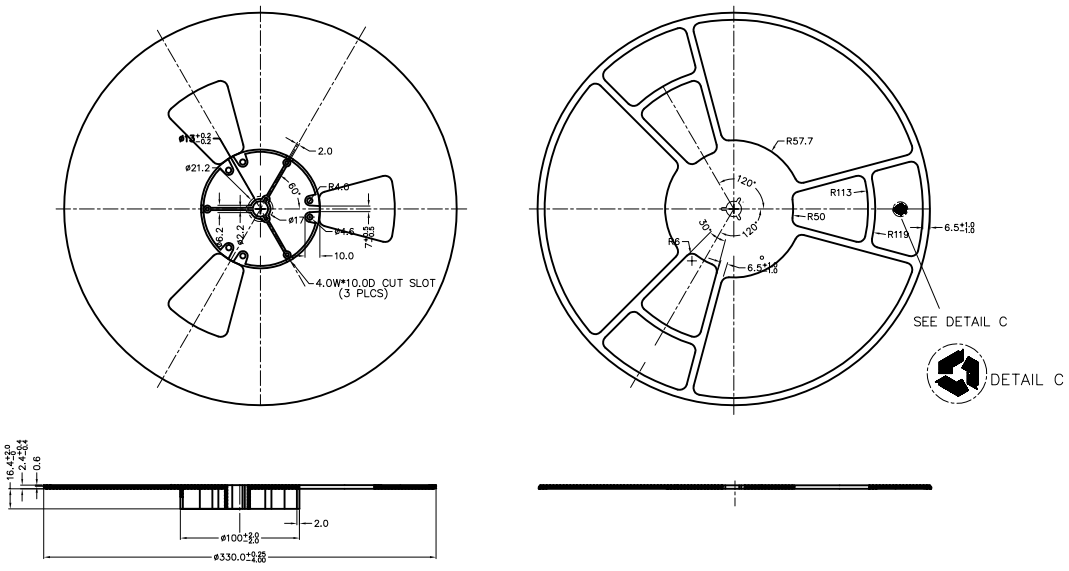


Figure 25. **PowerFLAT 8x8 HV reel**



Note: All dimensions are in millimeters.

Revision history

Table 10. **Document revision history**

Date	Version	Changes
06-Aug-2012	1	First release.
01-Feb-2013	2	– Document status promoted from preliminary data to production data – Modified: *Figure 1*, IDM, IAR, dv/dt values on *Table 2, note 4*, RDS(on) value on *Table 4*, tipical values on *Table 5, 6* and *7* and ISDM max value on *Table 7* – Inserted: *Section 2.1: Electrical characteristics (curves)* – Minor text changes
21-Oct-2020	3	Modified title, description and internal schematic diagram in cover page. Updated *Section 1 Electrical ratings* and *Section 2 Electrical characteristics*. Added *Section 4.2 PowerFLAT 8x8 HV type C package information*. Minor text changes.
16-Feb-2021	4	Modified Figure 24. PowerFLAT 8x8 HV package orientation in carrier tape. Minor text changes.

Contents