TC1303A/TC1303B/ TC1303C/TC1304

500 mA Synchronous Buck Regulator, + 300 mA LDO with Power-Good Output

Features

- Dual-Output Regulator (500 mA Buck Regulator and 300 mA Low-Dropout Regulator)
- Power-Good Output with 300 ms Delay
- Total Device Quiescent Current = 65 µA, Typical
- Independent Shutdown for Buck and LDO Outputs (**TC1303**)
- Both Outputs Internally Compensated
- Synchronous Buck Regulator:
  - Over 90% Typical Efficiency
  - 2.0 MHz Fixed-Frequency PWM (Heavy Load)
  - Low Output Noise
  - Automatic PWM to PFM mode transition
  - Adjustable (0.8V to 4.5V) and Standard Fixed-Output Voltages (0.8V, 1.2V, 1.5V, 1.8V, 2.5V, 3.3V)
- Low-Dropout Regulator:
  - Low-Dropout Voltage = 137 mV Typical @ 200 mA
  - Standard Fixed-Output Voltages (1.5V, 1.8V, 2.5V, 3.3V)
- Power-Good Function:
  - Monitors Buck Output Function (**TC1303A**)
  - Monitors LDO Output Function (**TC1303B**)
  - Monitors Both Buck and LDO Output Functions (**TC1303C and TC1304**)
  - 300 ms Delay Used for Processor Reset
- Sequenced Startup and Shutdown (**TC1304**)
- Small 10-pin 3x3 DFN or MSOP Package Options
- Operating Junction Temperature Range:
  - -40°C to +125°C
- Undervoltage Lockout (UVLO)
- Output Short Circuit Protection
- Overtemperature Protection

Applications

- Cellular Phones
- Portable Computers
- USB-Powered Devices
- Handheld Medical Instruments
- Organizers and PDAs

Description

The TC1303/TC1304 combines a 500 mA synchronous buck regulator and 300 mA Low-Dropout Regulator (LDO) with a power-good monitor to provide a highly integrated solution for devices that require multiple supply voltages. The unique combination of an integrated buck switching regulator and low-dropout linear regulator provides the lowest system cost for dual-output voltage applications that require one lower processor core voltage and one higher bias voltage.

The 500 mA synchronous buck regulator switches at a fixed frequency of 2.0 MHz when the load is heavy, providing a low noise, small-size solution. When the load on the buck output is reduced to light levels, it changes operation to a Pulse Frequency Modulation (PFM) mode to minimize quiescent current draw from the battery. No intervention is necessary for smooth transition from one mode to another.

The LDO provides a 300 mA auxiliary output that requires a single 1 µF ceramic output capacitor, minimizing board area and cost. The typical dropout voltage for the LDO output is 137 mV for a 200 mA load.

For the TC1303/TC1304, the power-good output is based on the regulation of the buck regulator output, the LDO output or the combination of both. The TC1304 features start-up and shutdown output sequencing.

The TC1303/TC1304 is available in either the 10-pin DFN or MSOP package.

Additional protection features include: UVLO, overtemperature and overcurrent protection on both outputs.

For a complete listing of TC1303/TC1304 standard parts, consult your Microchip representative.

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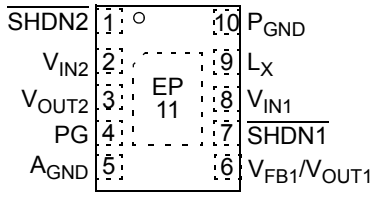
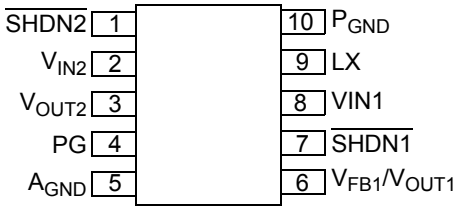
Package Types

TC1303A,B,C

10-Lead DFN

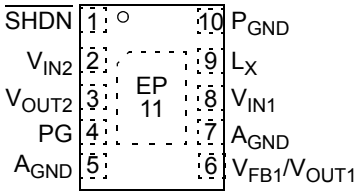


10-Lead MSOP

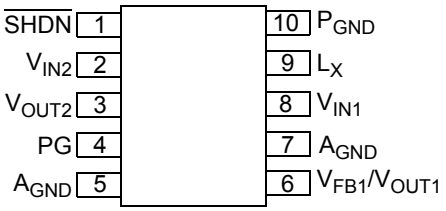


TC1304

10-Lead DFN



10-Lead MSOP



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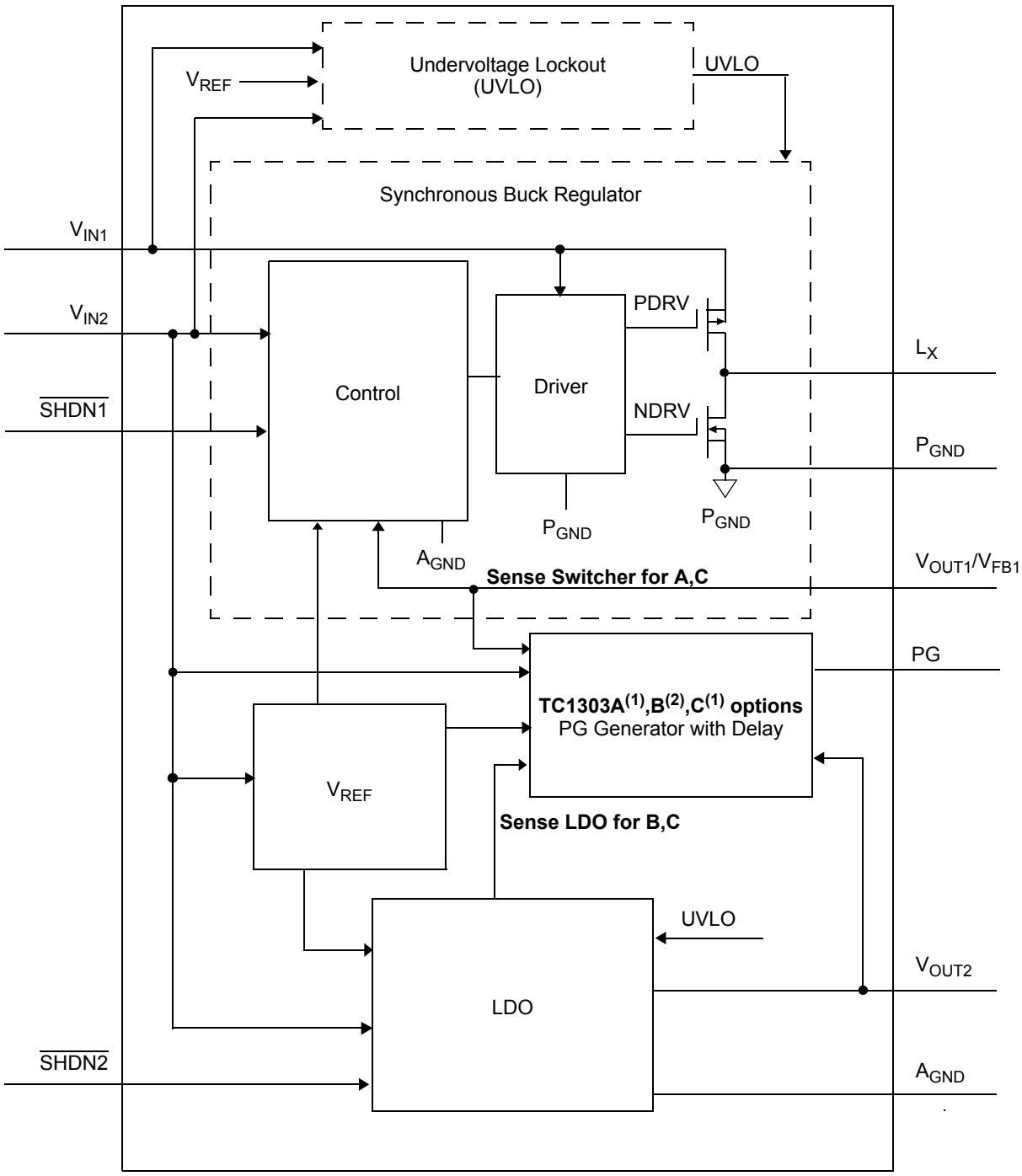
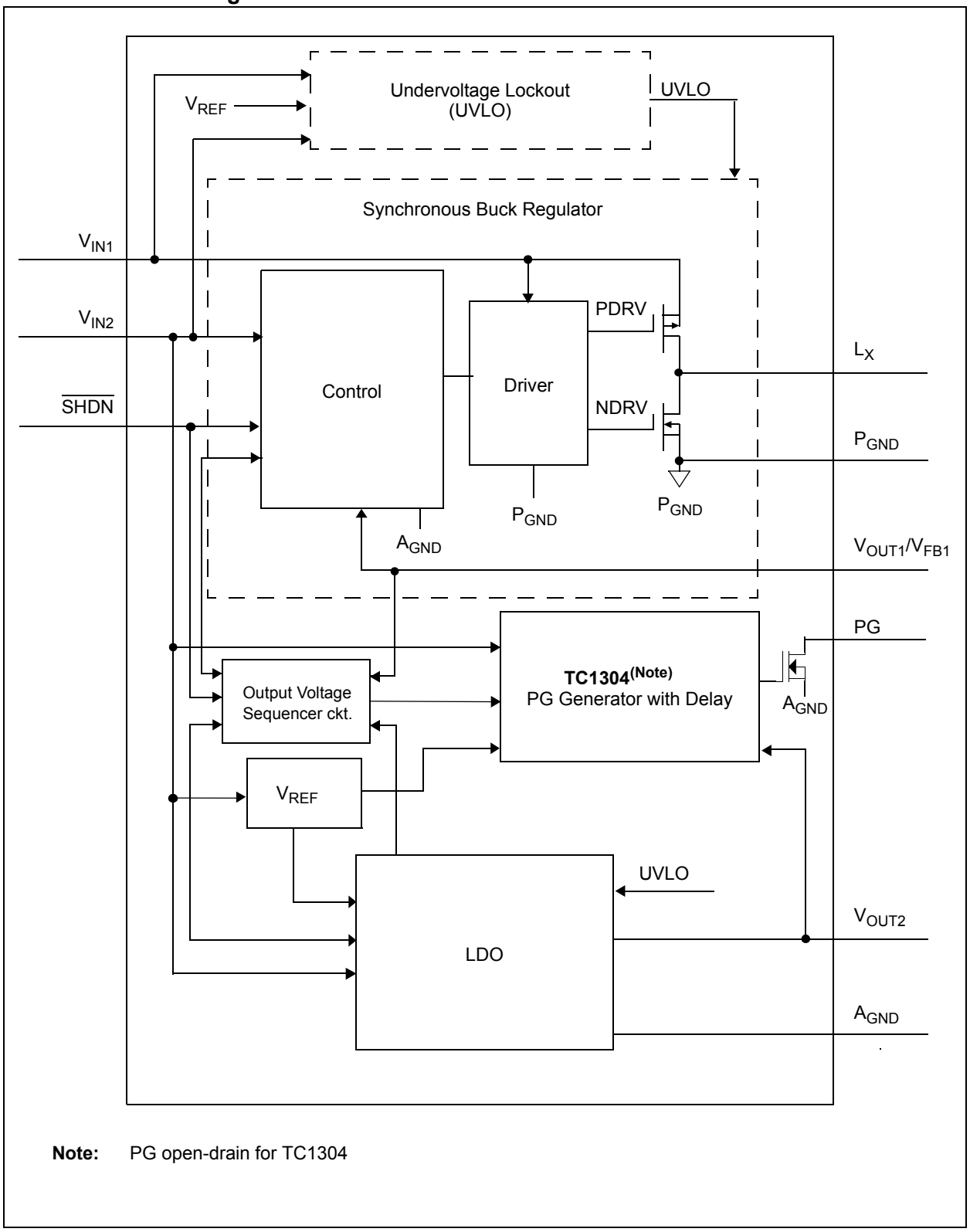
Functional Block Diagram – TC1303



Note 1: PG open-drain for A,C options

2: PG push-pull output for B option

Functional Block Diagram – TC1304



Note: PG open-drain for TC1304

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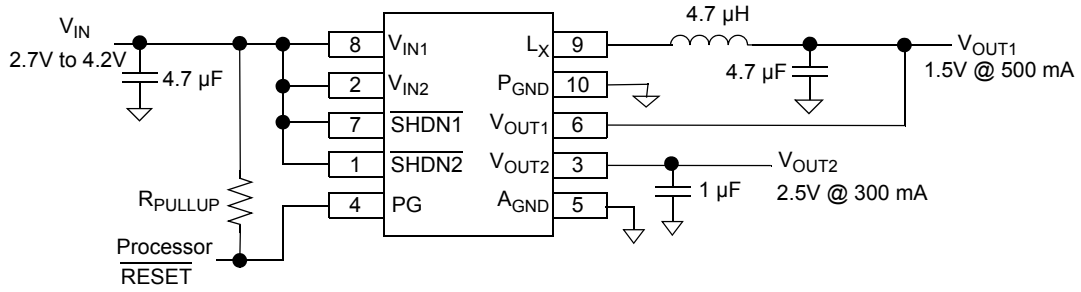
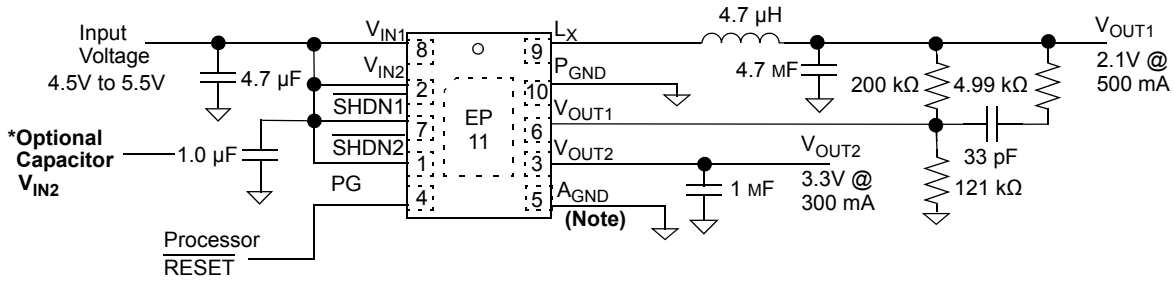
Typical Application Circuits

TC1303A
Fixed-Output Application
10-Lead MSOP

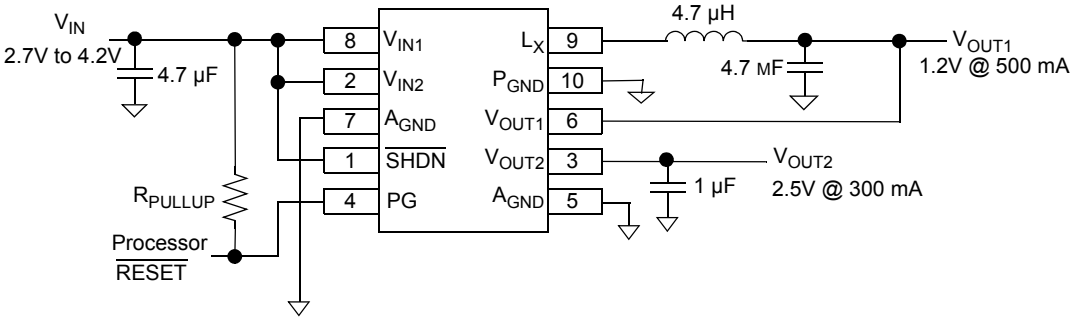


TC1303B
Adjustable-Output Application
10-Lead DFN



Note: Connect DFN package exposed pad to A_{GND}.

TC1304
Fixed-Output Application
10-Lead MSOP



NOTES:

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1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

V_{IN} - A_{GND}.....6.0V
All Other I/O .....(A_{GND} - 0.3V) to (V_{IN} + 0.3V)
L_X to P_{GND}.....-0.3V to (V_{IN} + 0.3V)
P_{GND} to A_{GND} ..... -0.3V to +0.3V
Output Short Circuit Current ..... Continuous
Power Dissipation (**Note 7**)..... Internally Limited
Storage temperature .....-65°C to +150°C
Ambient Temp. with Power Applied .....-40°C to +85°C
Operating Junction Temperature.....-40°C to +125°C
ESD protection on all pins (HBM) ..... 3 kV

† Notice: Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

Electrical Characteristics: V_{IN1} =V_{IN2} = $\overline{SHDN1,2}$ = 3.6V, C_{OUT1} = C_{IN} = 4.7 µF, C_{OUT2} = 1 µF, L = 4.7 µH, V_{OUT1} (ADJ) = 1.8V, I_{OUT1} = 100 mA, I_{OUT2} = 0.1 mA T_A = +25°C. **Boldface** specifications apply over the T_A range of **-40°C to +85°C**.

Parameters	Sym	Min	Typ	Max	Units	Conditions
Input/Output Characteristics						
Input Voltage	V_{IN}	**2.7**	—	**5.5**	V	**Note 1**, **Note 2, Note 8**
Maximum Output Current	I_{OUT1_MAX}	**500**	—	—	mA	**Note 1**
Maximum Output Current	I_{OUT2_MAX}	**300**	—	—	mA	**Note 1**
Shutdown Current Combined V_{IN1} and V_{IN2} Current	$I_{IN_\overline{SHDN}}$	—	0.05	1	µA	$\overline{SHDN1}$ = $\overline{SHDN2}$ = GND
TC1303A,B Operating I_Q **TC1303C**, **TC1304** Operating I_Q	I_Q I_Q	—	65.0 70.1	**110** **110**	µA	$\overline{SHDN1}$ = $\overline{SHDN2}$ = V_{IN2} I_{OUT1} = 0 mA, I_{OUT2} = 0 mA
Synchronous Buck I_Q		—	38	—	µA	$\overline{SHDN1}$ = V_{IN}, $\overline{SHDN2}$ = GND
LDO I_Q		—	46	—	µA	$\overline{SHDN1}$ = GND, $\overline{SHDN2}$ = V_{IN2}
Shutdown/UVLO/Thermal Shutdown Characteristics						
$\overline{SHDN1}$,$\overline{SHDN2}$, $\overline{SHDN}$ (**TC1304**) Logic Input Voltage Low	V_{IL}	—	—	**15**	%V_{IN}	V_{IN1} =V_{IN2} = 2.7V to 5.5V
$\overline{SHDN1}$,$\overline{SHDN2}$, $\overline{SHDN}$ (**TC1304**) Logic Input Voltage High	V_{IH}	**45**	—	—	%V_{IN}	V_{IN1} =V_{IN2} = 2.7V to 5.5V
$\overline{SHDN1}$,$\overline{SHDN2}$, $\overline{SHDN}$ (**TC1304**) Input Leakage Current	I_{IN}	**-1.0**	±0.01	**1.0**	µA	V_{IN1} =V_{IN2} = 2.7V to 5.5V $\overline{SHDNX}$ = GND $\overline{SHDNY}$ = V_{IN}
Thermal Shutdown	T_{SHD}	—	165	—	°C	**Note 6**, **Note 7**
Thermal Shutdown Hysteresis	$T_{SHD-HYS}$	—	10	—	°C	
Undervoltage Lockout (V_{OUT1} and V_{OUT2})	UVLO	**2.4**	2.55	**2.7**	V	V_{IN1} Falling
Undervoltage Lockout Hysteresis	UVLO-$_{HYS}$	—	200	—	mV	

Note 1: The Minimum V_{IN} has to meet two conditions: $V_{IN} \geq 2.7V$ and $V_{IN} \geq V_{RX} + V_{DROPOUT}$, V_{RX} = V_{R1} or V_{R2}.

2: V_{RX} is the regulator output voltage setting.

3: $TCV_{OUT2} = ((V_{OUT2max} – V_{OUT2min}) * 10^6)/(V_{OUT2} * D_T)$.

4: Regulation is measured at a constant junction temperature using low duty-cycle pulse testing. Load regulation is tested over a load range from 0.1 mA to the maximum specified output current.

5: Dropout voltage is defined as the input-to-output voltage differential at which the output voltage drops 2% below its nominal value measured at a 1V differential.

6: The maximum allowable power dissipation is a function of ambient temperature, the maximum allowable junction temperature and the thermal resistance from junction to air. (i.e. T_A, T_J, θ_{JA}). Exceeding the maximum allowable power dissipation causes the device to initiate thermal shutdown.

7: The integrated MOSFET switches have an integral diode from the L_X pin to V_{IN}, and from L_X to P_{GND}. In cases where these diodes are forward-biased, the package power dissipation limits must be adhered to. Thermal protection is not able to limit the junction temperature for these cases.

8: V_{IN1} and V_{IN2} are supplied by the same input source.

DC CHARACTERISTICS (CONTINUED)

Electrical Characteristics: V_{IN1} =V_{IN2} = $\overline{SHDN1,2}$ = 3.6V, C_{OUT1} = C_{IN} = 4.7 µF, C_{OUT2} = 1 µF, L = 4.7 µH, V_{OUT1} (ADJ) = 1.8V, I_{OUT1} = 100 mA, I_{OUT2} = 0.1 mA T_A = +25°C. **Boldface** specifications apply over the T_A range of **-40°C to +85°C**.

Parameters	Sym	Min	Typ	Max	Units	Conditions
Synchronous Buck Regulator (V_{OUT1})						
Adjustable Output Voltage Range	V_{OUT1}	**0.8**	—	**4.5**	V	
Adjustable Reference Feedback Voltage (V_{FB1})	V_{FB1}	**0.78**	0.8	**0.82**	V	
Feedback Input Bias Current (I_{FB1})	I_{VFB1}	—	-1.5	—	nA	
Output Voltage Tolerance Fixed (V_{OUT1})	V_{OUT1}	**-2.5**	±0.3	**+2.5**	%	**Note 2**
Line Regulation (V_{OUT1})	$V_{LINE-REG}$	—	0.2	—	%/V	V_{IN} =V_R+1V to 5.5V, I_{LOAD} = 100 mA
Load Regulation (V_{OUT1})	$V_{LOAD-REG}$	—	0.2	—	%	V_{IN} = V_R + 1.5V, I_{LOAD} = 100 mA to 500 mA (**Note 1**)
Dropout Voltage V_{OUT1}	$V_{IN} – V_{OUT1}$	—	280	—	mV	I_{OUT1} = 500 mA, V_{OUT1} = 3.3V (**Note 5**)
Internal Oscillator Frequency	F_{OSC}	**1.6**	2.0	**2.4**	MHz	
Start Up Time	T_{SS}	—	0.5	—	ms	T_R = 10% to 90%
R_{DSon} P-Channel	R_{DSon-P}	—	450	—	mΩ	I_P=100 mA
R_{DSon} N-Channel	R_{DSon-N}	—	450	—	mΩ	I_N=100 mA
L_X Pin Leakage Current	I_{LX}	**-1.0**	±0.01	**1.0**	µA	$\overline{SHDN}$ = 0V, V_{IN} = 5.5V, L_X = 0V, L_X = 5.5V
Positive Current Limit Threshold	$+I_{LX(MAX)}$	—	700	—	mA	
LDO Output (V_{OUT2})						
Output Voltage Tolerance (V_{OUT2})	V_{OUT2}	**-2.5**	±0.3	**+2.5**	%	**Note 2**
Temperature Coefficient	TCV_{OUT}	—	25	—	ppm/°C	**Note 3**
Line Regulation	$\Delta V_{OUT2}/\Delta V_{IN}$	**-0.2**	±0.02	**+0.2**	%/V	(V_R+1V) ≤ V_{IN} ≤ 5.5V
Load Regulation, $V_{OUT2} \geq$ 2.5V	$\Delta V_{OUT2}/I_{OUT2}$	**-0.75**	-0.08	**+0.75**	%	I_{OUT2} = 0.1 mA to 300 mA (**Note 4**)
Load Regulation, V_{OUT2} < 2.5V	$\Delta V_{OUT2}/I_{OUT2}$	**-0.9**	-0.18	**+0.9**	%	I_{OUT2} = 0.1 mA to 300 mA (**Note 4**)
Dropout Voltage V_{OUT2} > 2.5V	$V_{IN} – V_{OUT2}$	—	137 205	**300** **500**	mV	I_{OUT2} = 200 mA (**Note 5**) I_{OUT2} = 300 mA
Power Supply Rejection Ratio	PSRR	—	62	—	dB	f ≤ 100 Hz, I_{OUT1} = I_{OUT2} = 50 mA, C_{IN} = 0 µF
Output Noise	eN	—	1.8	—	µV/(Hz)^{½}	f ≤ 1 kHz, I_{OUT2} = 50 mA, $\overline{SHDN1}$ = GND

Note 1: The Minimum V_{IN} has to meet two conditions: $V_{IN} \geq 2.7V$ and $V_{IN} \geq V_{RX} + V_{DROPOUT}$, V_{RX} = V_{R1} or V_{R2}.

2: V_{RX} is the regulator output voltage setting.

3: $TCV_{OUT2} = ((V_{OUT2max} – V_{OUT2min}) * 10^6)/(V_{OUT2} * D_T)$.

4: Regulation is measured at a constant junction temperature using low duty-cycle pulse testing. Load regulation is tested over a load range from 0.1 mA to the maximum specified output current.

5: Dropout voltage is defined as the input-to-output voltage differential at which the output voltage drops 2% below its nominal value measured at a 1V differential.

6: The maximum allowable power dissipation is a function of ambient temperature, the maximum allowable junction temperature and the thermal resistance from junction to air. (i.e. T_A, T_J, θ_{JA}). Exceeding the maximum allowable power dissipation causes the device to initiate thermal shutdown.

7: The integrated MOSFET switches have an integral diode from the L_X pin to V_{IN}, and from L_X to P_{GND}. In cases where these diodes are forward-biased, the package power dissipation limits must be adhered to. Thermal protection is not able to limit the junction temperature for these cases.

8: V_{IN1} and V_{IN2} are supplied by the same input source.

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DC CHARACTERISTICS (CONTINUED)

Electrical Characteristics: V_{IN1} =V_{IN2} = $\overline{SHDN1,2}$ = 3.6V, C_{OUT1} = C_{IN} = 4.7 µF, C_{OUT2} = 1 µF, L = 4.7 µH, V_{OUT1} (ADJ) = 1.8V, I_{OUT1} = 100 mA, I_{OUT2} = 0.1 mA T_A = +25°C. **Boldface** specifications apply over the T_A range of **-40°C to +85°C**.

Parameters	Sym	Min	Typ	Max	Units	Conditions
Output Short Circuit Current (Average)	I_{OUTsc2}	—	240	—	mA	$R_{LOAD2} \leq 1\Omega$
Wake-Up Time (From $\overline{SHDN2}$ mode), (V_{OUT2})	t_{WK}	—	31	100	µs	I_{OUT1} = I_{OUT2} = 50 mA
Settling Time (From $\overline{SHDN2}$ mode), (V_{OUT2})	t_S	—	100	—	µs	I_{OUT1} = I_{OUT2} = 50 mA
Power-Good (PG)						
Voltage Range PG	V_{PG}	1.0 **1.2**	—	5.5 **5.5**	V	T_A = 0°C to +70°C T_A = -40°C to +85°C $V_{IN} \leq 2.7$ I_{SINK} = 100 µA
PG Threshold High (V_{OUT1} or V_{OUT2})	V_{TH_H}	—	94	**96**	% of V_{OUTX}	On Rising V_{OUT1} or V_{OUT2} V_{OUTX} = V_{OUT1} or V_{OUT2}
PG Threshold Low (V_{OUT1} or V_{OUT2})	V_{TH_L}	**89**	92	—	% of V_{OUTX}	On Falling V_{OUT1} or V_{OUT2} V_{OUTX} = V_{OUT1} or V_{OUT2}
PG Threshold Hysteresis (V_{OUT1} and V_{OUT2})	V_{TH_HYS}	—	2	—	% of V_{OUTX}	V_{OUTX} = V_{OUT1} or V_{OUT2}
PG Threshold Tempco	$\Delta V_{TH}/\Delta T$	—	30	—	ppm/°C	
PG Delay	t_{RPD}	—	165	—	µs	V_{OUT1} or V_{OUT2} = (V_{TH} + 100 mV) to (V_{TH} - 100 mV)
PG Active Time-out Period	t_{RPU}	**140**	262	**560**	ms	V_{OUT1} or V_{OUT2} = V_{TH} - 100 mV to V_{TH} + 100 mV, I_{SINK} = 1.2 mA
PG Output Voltage Low	PG_V_{OL}	—	—	**0.2**	V	V_{OUT1}orV_{OUT2} = V_{TH} - 100 mV, I_{PG}= 1.2 mA V_{IN2} > 2.7V I_{PG} = 100 µA, 1.0V < V_{IN2} < 2.7V
PG Output Voltage High (TC1303B only)	PG_V_{OH}	**0.9* V_{OUT2}**	—	—	V	V_{OUT1} or V_{OUT2} = V_{TH} + 100 mV $V_{OUT2} \geq$ 1.8V, I_{PG} = - 500 µA V_{OUT2} < 1.8V,I_{PG} = - 300 µA

Note 1: The Minimum V_{IN} has to meet two conditions: $V_{IN} \geq 2.7V$ and $V_{IN} \geq V_{RX} + V_{DROPOUT}$, V_{RX} = V_{R1} or V_{R2}.

2: V_{RX} is the regulator output voltage setting.

3: $TCV_{OUT2} = ((V_{OUT2max} - V_{OUT2min}) * 10^6)/(V_{OUT2} * D_T)$.

4: Regulation is measured at a constant junction temperature using low duty-cycle pulse testing. Load regulation is tested over a load range from 0.1 mA to the maximum specified output current.

5: Dropout voltage is defined as the input-to-output voltage differential at which the output voltage drops 2% below its nominal value measured at a 1V differential.

6: The maximum allowable power dissipation is a function of ambient temperature, the maximum allowable junction temperature and the thermal resistance from junction to air. (i.e. T_A, T_J, θ_{JA}). Exceeding the maximum allowable power dissipation causes the device to initiate thermal shutdown.

7: The integrated MOSFET switches have an integral diode from the L_X pin to V_{IN}, and from L_X to P_{GND}. In cases where these diodes are forward-biased, the package power dissipation limits must be adhered to. Thermal protection is not able to limit the junction temperature for these cases.

8: V_{IN1} and V_{IN2} are supplied by the same input source.

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TEMPERATURE SPECIFICATIONS

Electrical Specifications: Unless otherwise indicated, all limits are specified for: V_{IN} = +2.7V to +5.5V						
Parameters	**Sym**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
Temperature Ranges						
Operating Junction Temperature Range	T_J	-40	—	+125	°C	Steady state
Storage Temperature Range	T_A	-65	—	+150	°C	
Maximum Junction Temperature	T_J	—	—	+150	°C	Transient
Thermal Package Resistances						
Thermal Resistance, 10L-DFN	θ_{JA}	—	41	—	°C/W	Typical 4-layer Board with Internal Ground Plane and 2 Vias in Thermal Pad
Thermal Resistance, 10L-MSOP	θ_{JA}	—	113	—	°C/W	Typical 4-layer Board with Internal Ground Plane

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2.0 TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

Note: Unless otherwise indicated, $V_{IN1} = V_{IN2} = \overline{SHDN1,2} = 3.6V$, $C_{OUT1} = C_{IN} = 4.7\ \mu F$, $C_{OUT2} = 1\ \mu F$, $L = 4.7\ \mu H$, V_{OUT1} (ADJ) = 1.8V, T_A = +25°C. **Boldface** specifications apply over the T_A range of -40°C to +85°C. T_A = +25°C. Adjustable- or fixed-output voltage options can be used to generate the Typical Performance Characteristics.

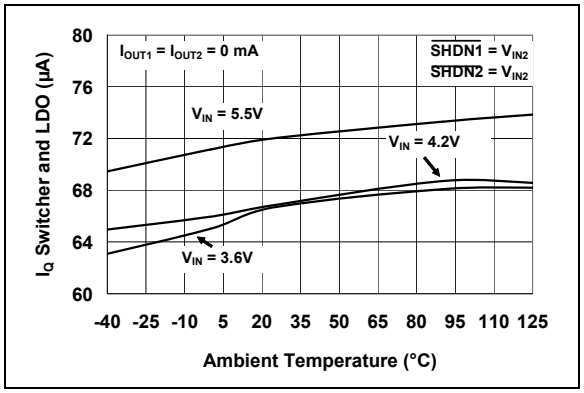

FIGURE 2-1: *I_Q Switcher and LDO Current vs. Ambient Temperature (TC1303A,B).*

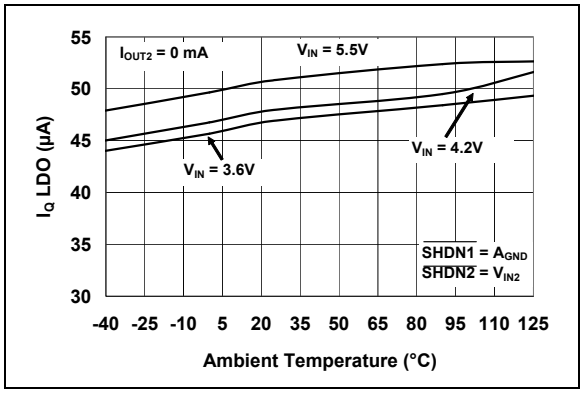

FIGURE 2-4: *I_Q LDO Current vs. Ambient Temperature.*

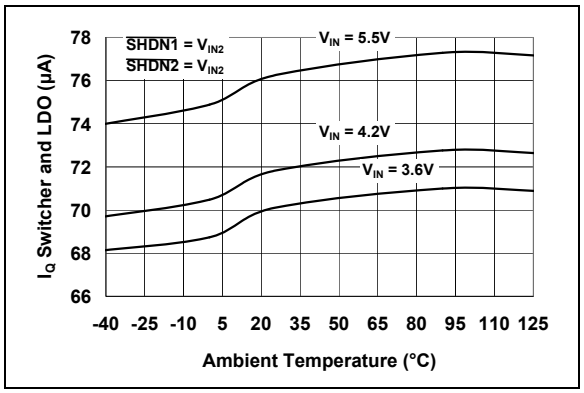

FIGURE 2-2: *I_Q Switcher and LDO Current vs. Ambient Temperature (TC1303C, TC1304).*

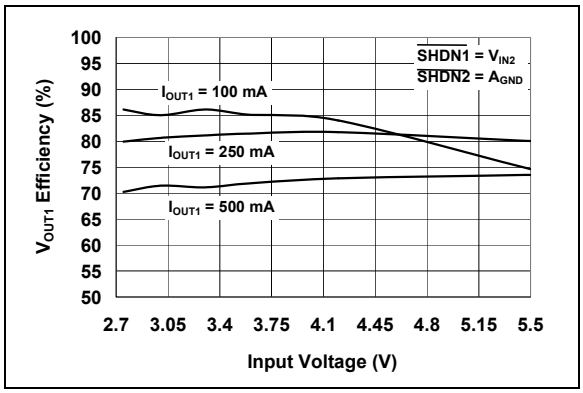

FIGURE 2-5: *V_{OUT1} Output Efficiency vs. Input Voltage (V_{OUT1} = 1.2V).*

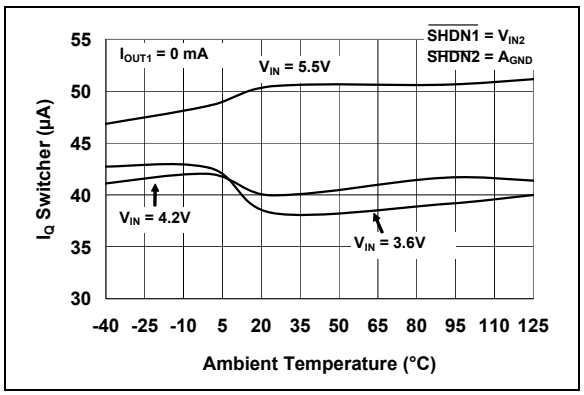

FIGURE 2-3: *I_Q Switcher Current vs. Ambient Temperature.*

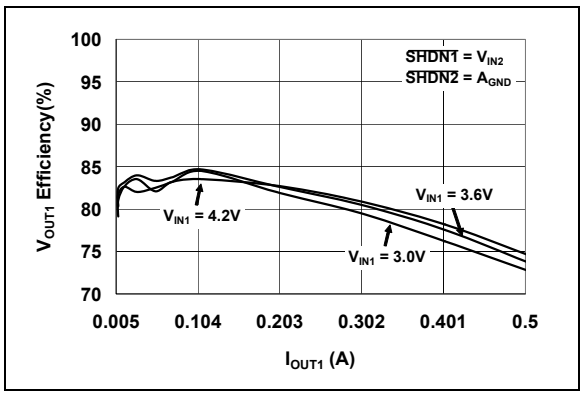

FIGURE 2-6: *V_{OUT1} Output Efficiency vs. I_{OUT1} (V_{OUT1} = 1.2V).*

Note: Unless otherwise indicated, $V_{IN1} = V_{IN2} = \overline{SHDN1,2} = 3.6V$, $C_{OUT1} = C_{IN} = 4.7\ \mu F$, $C_{OUT2} = 1\ \mu F$, $L = 4.7\ \mu H$, V_{OUT1} (ADJ) = 1.8V, T_A = +25°C. **Boldface** specifications apply over the T_A range of -40°C to +85°C. T_A = +25°C. Adjustable- or fixed-output voltage options can be used to generate the Typical Performance Characteristics.

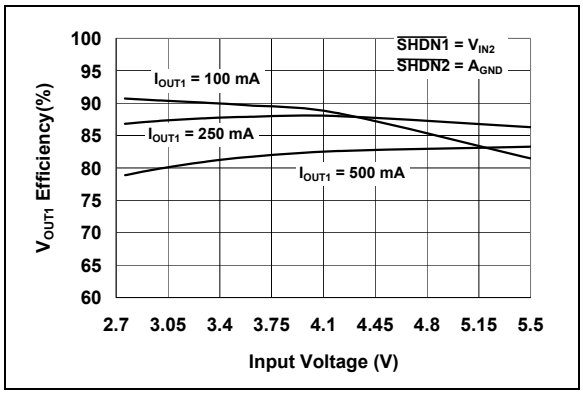

FIGURE 2-7: *V_{OUT1} Output Efficiency vs. Input Voltage (V_{OUT1} = 1.8V).*

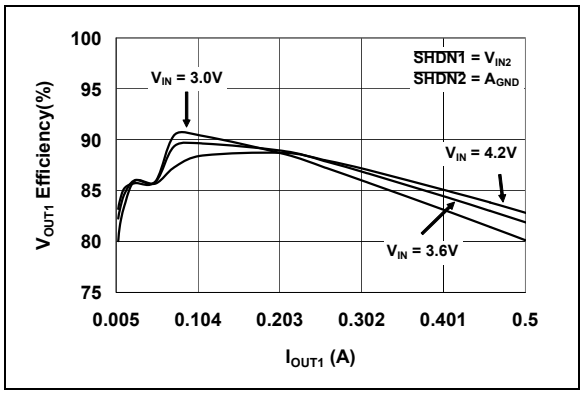

FIGURE 2-8: *V_{OUT1} Output Efficiency vs. I_{OUT1} (V_{OUT1} = 1.8V).*

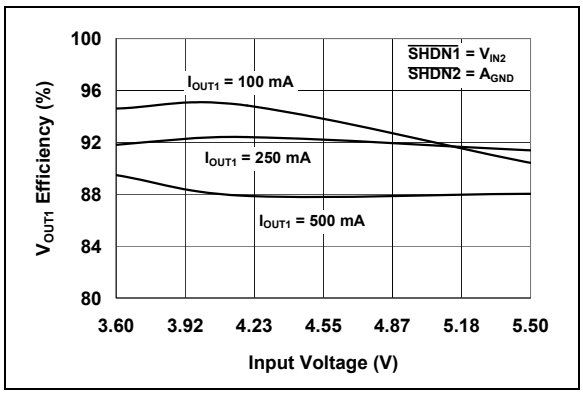

FIGURE 2-9: *V_{OUT1} Output Efficiency vs. Input Voltage (V_{OUT1} = 3.3V).*

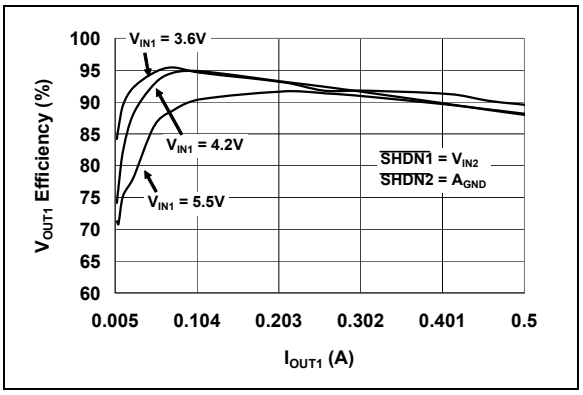

FIGURE 2-10: *V_{OUT1} Output Efficiency vs. I_{OUT1} (V_{OUT1} = 3.3V).*

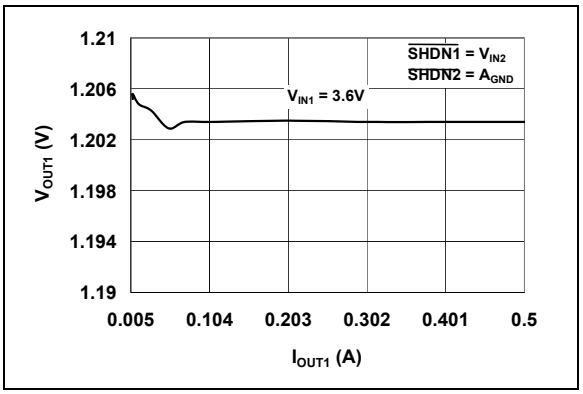

FIGURE 2-11: *V_{OUT1} vs. I_{OUT1} (V_{OUT1} = 1.2V).*

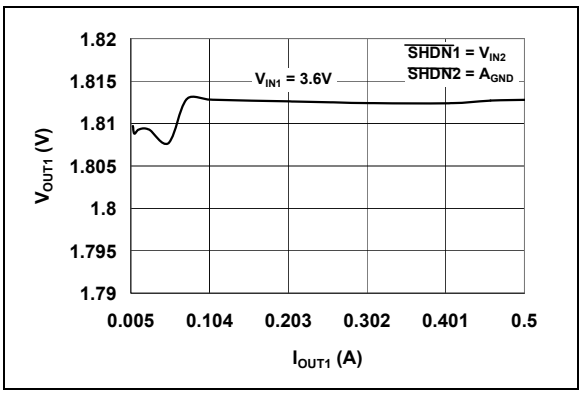

FIGURE 2-12: *V_{OUT1} vs. I_{OUT1} (V_{OUT1} = 1.8V).*

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Note: Unless otherwise indicated, $V_{IN1} = V_{IN2} = \overline{SHDN1,2} = 3.6V$, $C_{OUT1} = C_{IN} = 4.7\ \mu F$, $C_{OUT2} = 1\ \mu F$, $L = 4.7\ \mu H$, V_{OUT1} (ADJ) = 1.8V, T_A = +25°C. **Boldface** specifications apply over the T_A range of -40°C to +85°C. T_A = +25°C. Adjustable- or fixed-output voltage options can be used to generate the Typical Performance Characteristics.

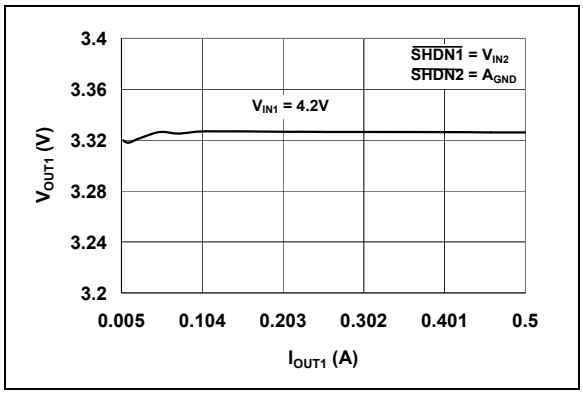

FIGURE 2-13: *V_{OUT1} vs. I_{OUT1} (V_{OUT1} = 3.3V).*

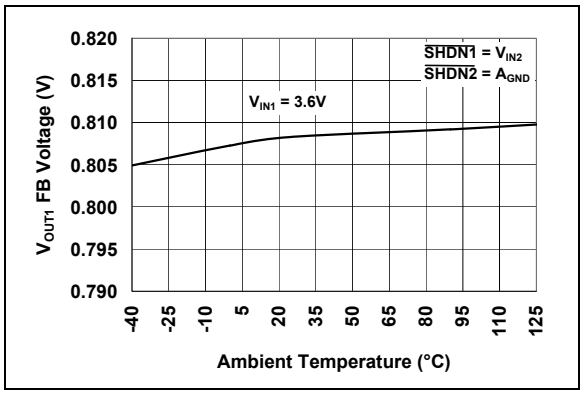

FIGURE 2-16: *V_{OUT1} Adjustable Feedback Voltage vs. Ambient Temperature.*

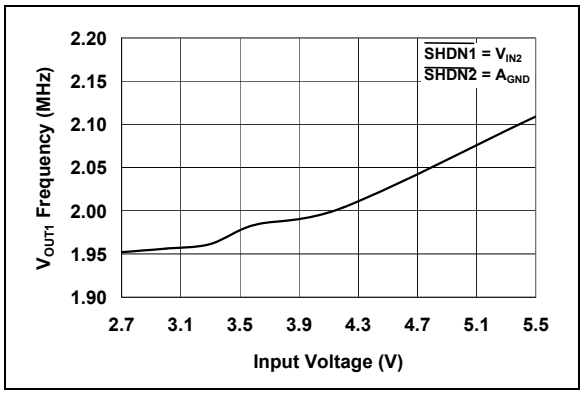

FIGURE 2-14: *V_{OUT1} Switching Frequency vs. Input Voltage.*

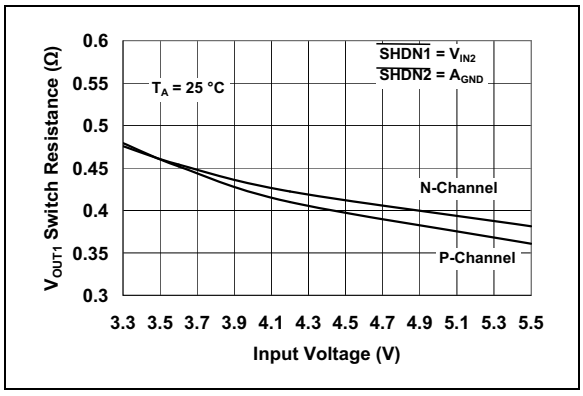

FIGURE 2-17: *V_{OUT1} Switch Resistance vs. Input Voltage.*

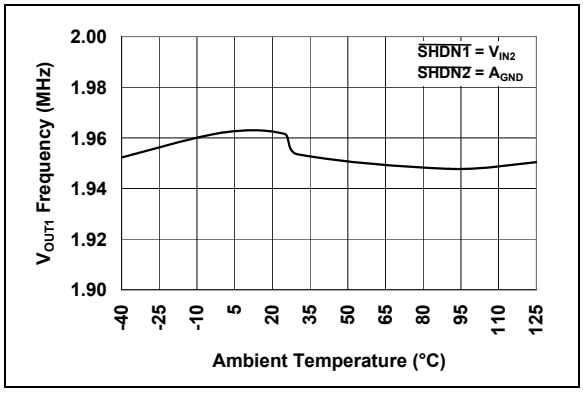

FIGURE 2-15: *V_{OUT1} Switching Frequency vs. Ambient Temperature.*

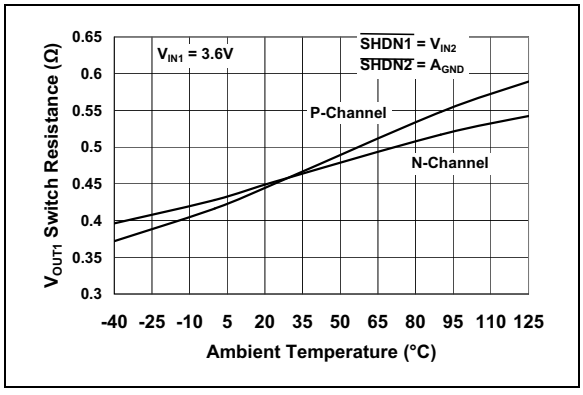

FIGURE 2-18: *V_{OUT1} Switch Resistance vs. Ambient Temperature.*

Note: Unless otherwise indicated, $V_{IN1} = V_{IN2} = \overline{SHDN1,2} = 3.6V$, $C_{OUT1} = C_{IN} = 4.7\ \mu F$, $C_{OUT2} = 1\ \mu F$, $L = 4.7\ \mu H$, V_{OUT1} (ADJ) = 1.8V, T_A = +25°C. **Boldface** specifications apply over the T_A range of -40°C to +85°C. T_A = +25°C. Adjustable- or fixed-output voltage options can be used to generate the Typical Performance Characteristics.

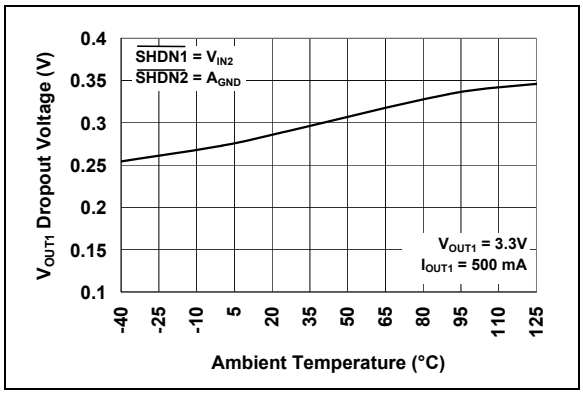

FIGURE 2-19: *V_{OUT1} Dropout Voltage vs. Ambient Temperature.*

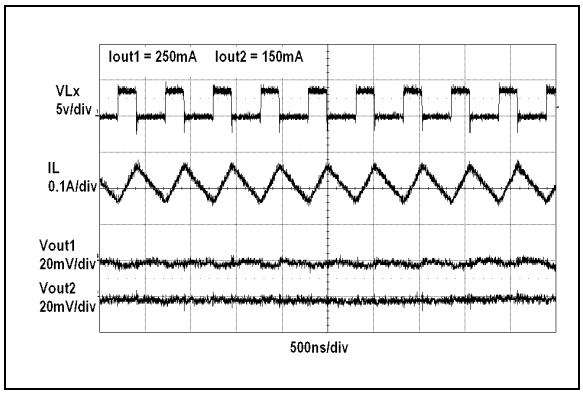

FIGURE 2-20: *V_{OUT1} and V_{OUT2} Heavy Load Switching Waveforms vs. Time.*

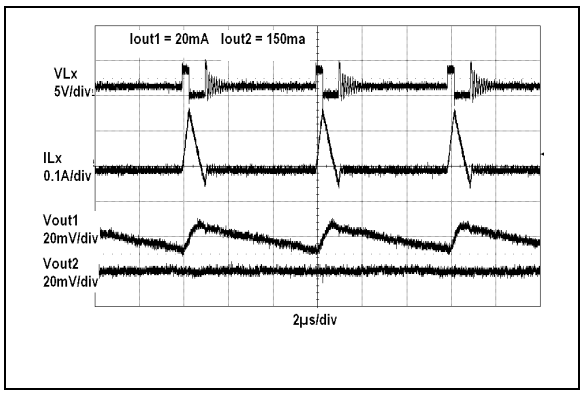

FIGURE 2-21: *V_{OUT1} and V_{OUT2} Light Load Switching Waveforms vs. Time.*

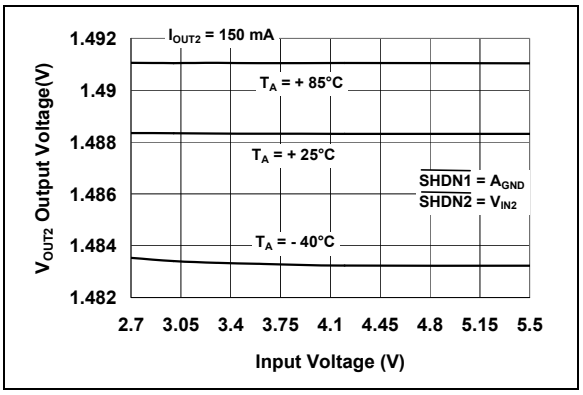

FIGURE 2-22: *V_{OUT2} Output Voltage vs. Input Voltage (V_{OUT2} = 1.5V).*

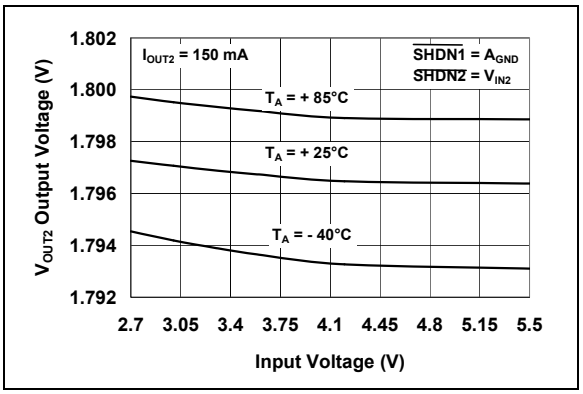

FIGURE 2-23: *V_{OUT2} Output Voltage vs. Input Voltage (V_{OUT2} = 1.8V).*

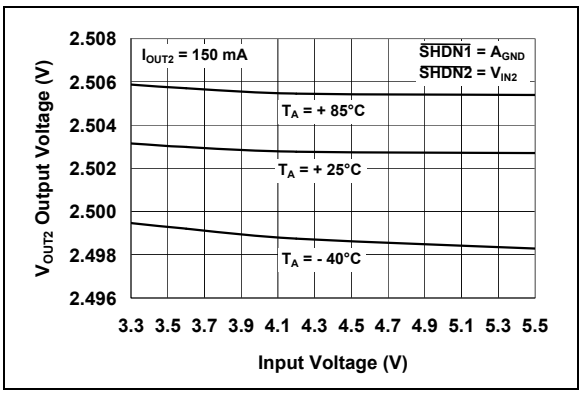

FIGURE 2-24: *V_{OUT2} Output Voltage vs. Input Voltage (V_{OUT2} = 2.5V).*

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Note: Unless otherwise indicated, $V_{IN1} = V_{IN2} = \overline{SHDN1,2} = 3.6V$, $C_{OUT1} = C_{IN} = 4.7\ \mu F$, $C_{OUT2} = 1\ \mu F$, $L = 4.7\ \mu H$, V_{OUT1} (ADJ) = 1.8V, T_A = +25°C. **Boldface** specifications apply over the T_A range of -40°C to +85°C. T_A = +25°C. Adjustable- or fixed-output voltage options can be used to generate the Typical Performance Characteristics.

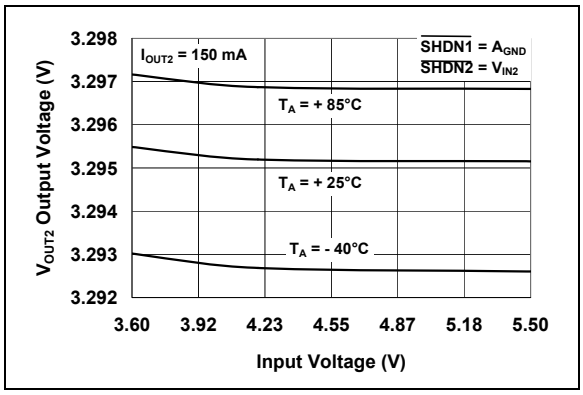

FIGURE 2-25: *V_{OUT2} Output Voltage vs. Input Voltage (V_{OUT2} = 3.3V).*

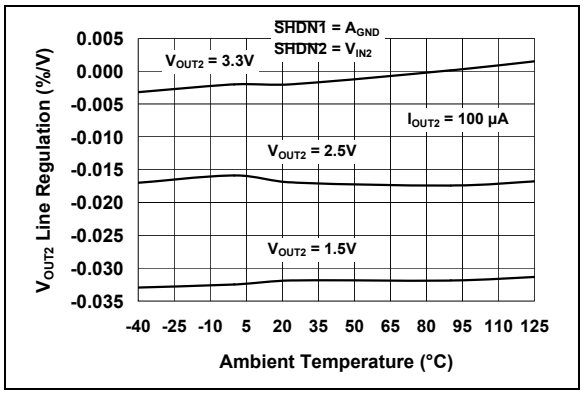

FIGURE 2-28: *V_{OUT2} Line Regulation vs. Ambient Temperature.*

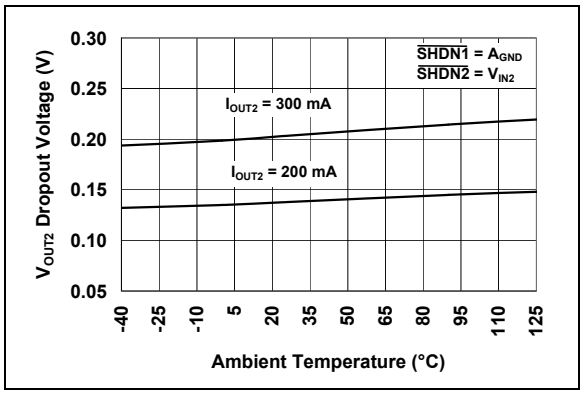

FIGURE 2-26: *V_{OUT2} Dropout Voltage vs. Ambient Temperature (V_{OUT2} = 2.5V).*

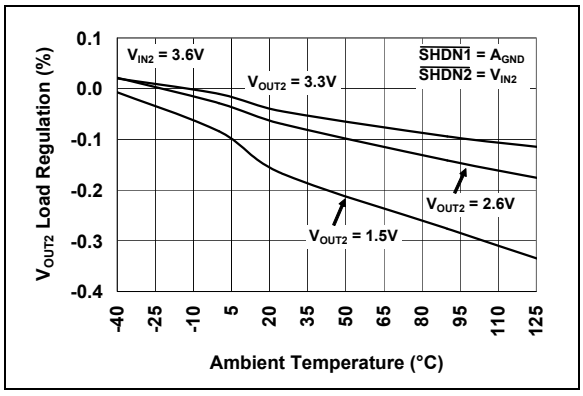

FIGURE 2-29: *V_{OUT2} Load Regulation vs. Ambient Temperature.*

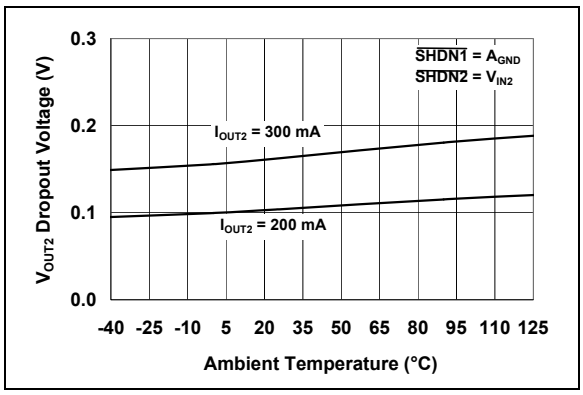

FIGURE 2-27: *V_{OUT2} Dropout Voltage vs. Ambient Temperature (V_{OUT2} = 3.3V).*

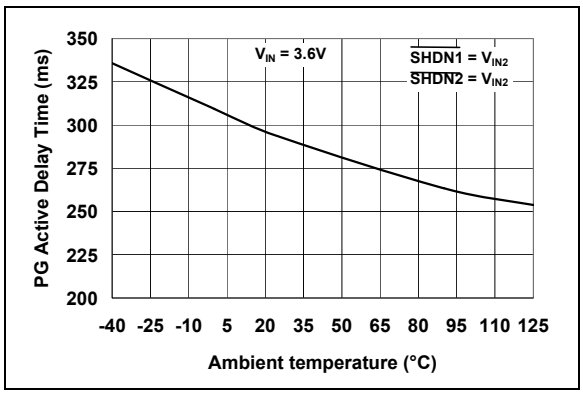

FIGURE 2-30: *PG Active Delay Time-out vs. Ambient Temperature.*

Note: Unless otherwise indicated, $V_{IN1} = V_{IN2} = \overline{SHDN1,2} = 3.6V$, $C_{OUT1} = C_{IN} = 4.7\ \mu F$, $C_{OUT2} = 1\ \mu F$, L = 4.7 µH, V_{OUT1} (ADJ) = 1.8V, T_A = +25°C. **Boldface** specifications apply over the T_A range of -40°C to +85°C. T_A = +25°C. Adjustable- or fixed-output voltage options can be used to generate the Typical Performance Characteristics.

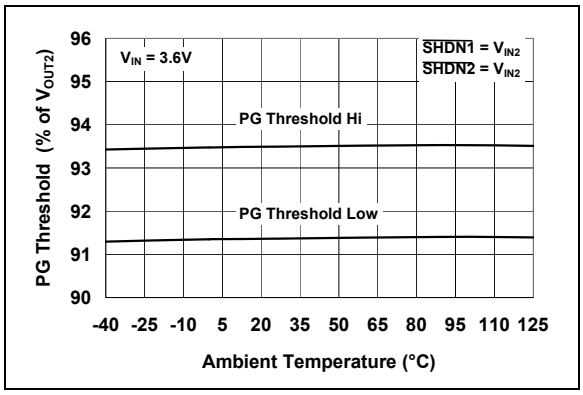

FIGURE 2-31: *PG Threshold Voltage vs. Ambient Temperature.*

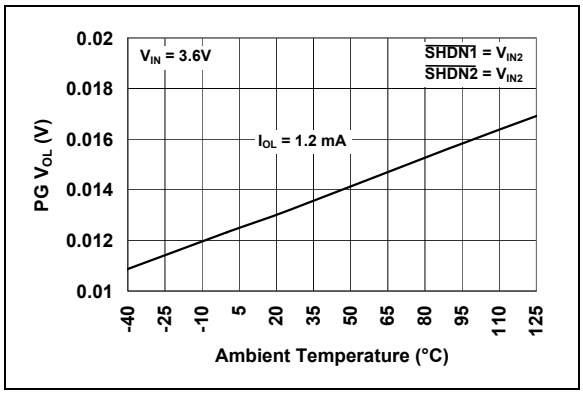

FIGURE 2-32: *PG Output Voltage Level Low vs. Ambient Temperature.*

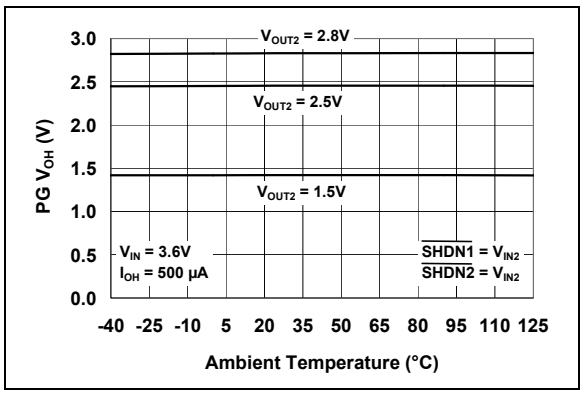

FIGURE 2-33: *PG Output Voltage Level High vs. Ambient Temperature.*

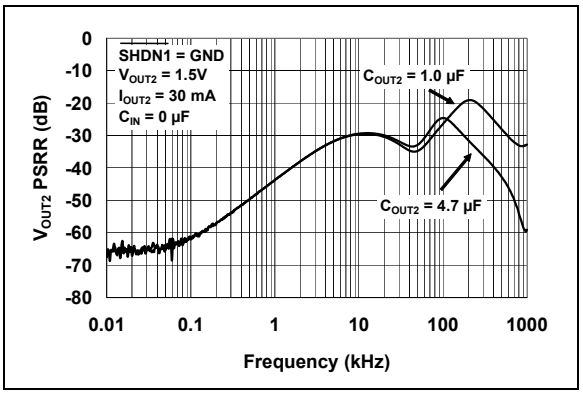

FIGURE 2-34: *V_{OUT2} Power Supply Ripple Rejection vs. Frequency.*

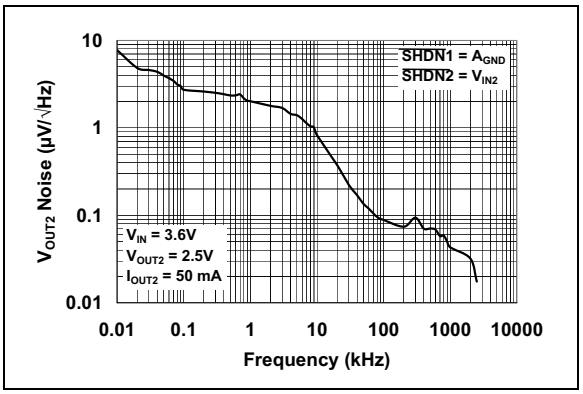

FIGURE 2-35: *V_{OUT2} Noise vs. Frequency.*

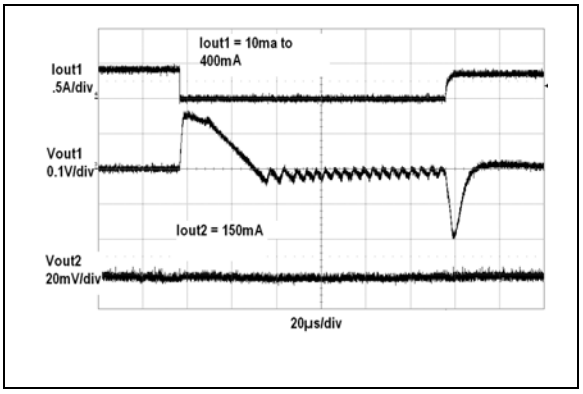

FIGURE 2-36: *V_{OUT1} Load Step Response vs. Time.*

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Note: Unless otherwise indicated, $V_{IN1} = V_{IN2} = \overline{SHDN1,2} = 3.6V$, $C_{OUT1} = C_{IN} = 4.7\ \mu F$, $C_{OUT2} = 1\ \mu F$, $L = 4.7\ \mu H$, V_{OUT1} (ADJ) = 1.8V, $T_A = +25°C$. **Boldface** specifications apply over the T_A range of -40°C to +85°C. $T_A = +25°C$. Adjustable- or fixed-output voltage options can be used to generate the Typical Performance Characteristics.

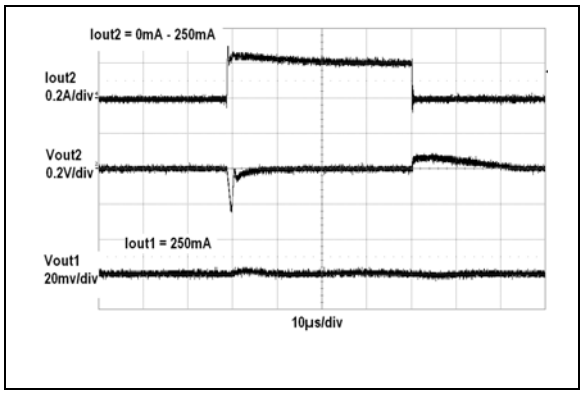

FIGURE 2-37: *V_{OUT2} Load Step Response vs. Time.*

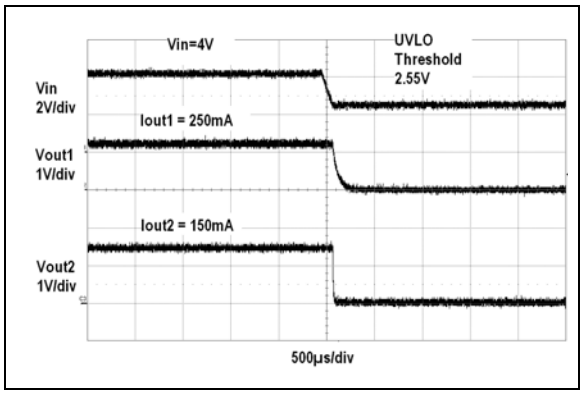

FIGURE 2-40: *V_{OUT1} and V_{OUT2} Shutdown Waveforms.*

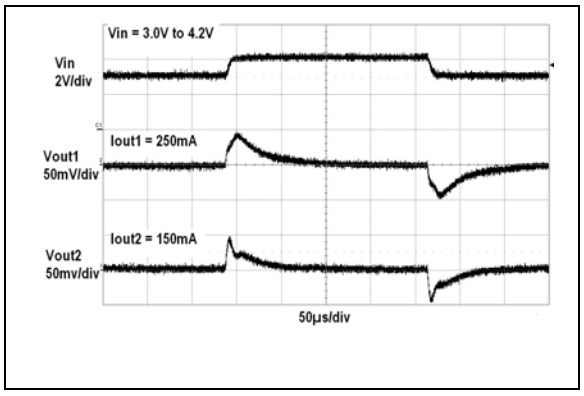

FIGURE 2-38: *V_{OUT1} and V_{OUT2} Line Step Response vs. Time.*

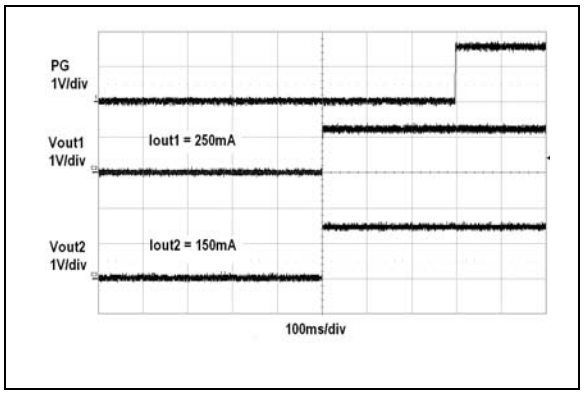

FIGURE 2-41: *Power-Good Output Timing.*

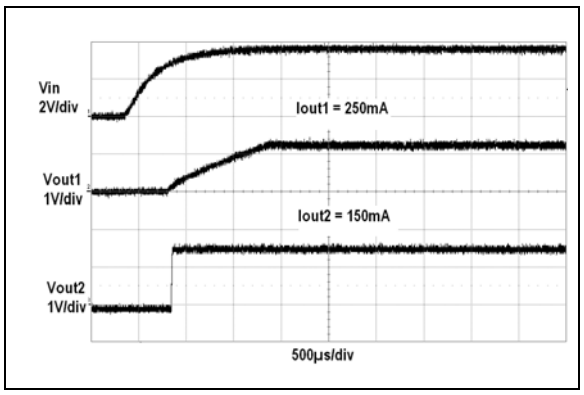

FIGURE 2-39: *V_{OUT1} and V_{OUT2} Start-up Waveforms.*

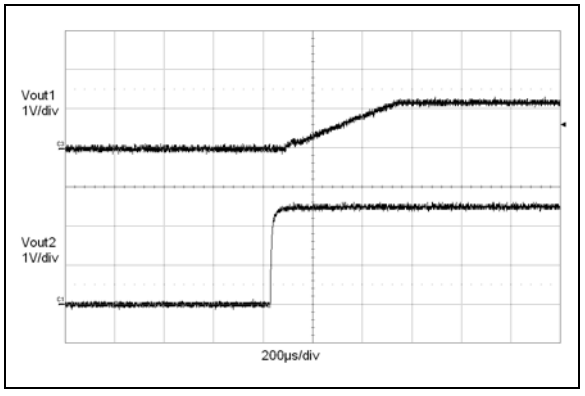

FIGURE 2-42: *Start-up Waveforms (TC1304).*

Note: Unless otherwise indicated, $V_{IN1} = V_{IN2} = \overline{SHDN1,2}$ = 3.6V, $C_{OUT1} = C_{IN}$ = 4.7 µF, C_{OUT2} = 1 µF, L = 4.7 µH, V_{OUT1} (ADJ) = 1.8V, T_A = +25°C. **Boldface** specifications apply over the T_A range of -40°C to +85°C. T_A = +25°C. Adjustable- or fixed-output voltage options can be used to generate the Typical Performance Characteristics.

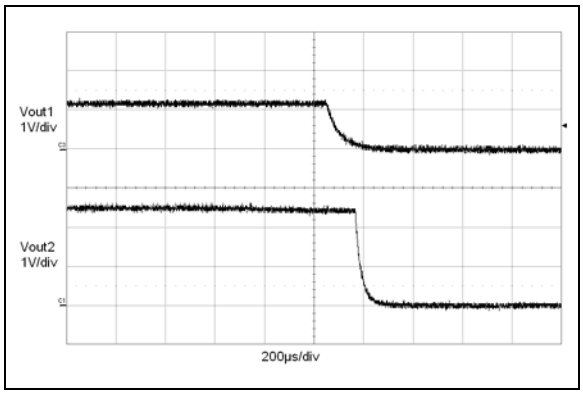

FIGURE 2-43: *Shutdown Waveforms (TC1304).*

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3.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 3-1.

TABLE 3-1: PIN FUNCTION TABLE

Pin No.	Symbol		Description
	TC1303	TC1304	
	MSOP, DFN	MSOP, DFN	
1	$\overline{SHDN2}$	—	Active Low Shutdown Input for LDO Output Pin
1	—	$\overline{SHDN}$	Active Low Shutdown Input both Buck Regulator Output and LDO Output. Initiates sequencing up and down
2	V_{IN2}	V_{IN2}	Analog Input Supply Voltage Pin
3	V_{OUT2}	V_{OUT2}	LDO Output Voltage Pin
4	PG	PG	Power-Good Output Pin
5	A_{GND}	A_{GND}	Analog Ground Pin
6	V_{FB}/V_{OUT1}	V_{FB}/V_{OUT1}	Buck Feedback Voltage (Adjustable Version) / Buck Output Voltage (Fixed Version) Pin
7	$\overline{SHDN1}$	—	Active Low Shutdown Input for Buck Regulator Output Pin
7	—	A_{GND}	Analog Ground Pin
8	V_{IN1}	V_{IN1}	Buck Regulator Input Voltage Pin
9	L_X	L_X	Buck Inductor Output Pin
10	P_{GND}	P_{GND}	Power Ground Pin
11	EP	EP	Exposed Pad - For the DFN package, the center exposed pad is a thermal path to remove heat from the device. Electrically this pad is at ground potential and should be connected to A_{GND}.

3.1 TC1303 LDO Shutdown Input Pin ($\overline{SHDN2}$)

$\overline{SHDN2}$ is a logic-level input used to turn the LDO Regulator on and off. A logic-high (> 45% of V_{IN}), will enable the regulator output. A logic-low (< 15% of V_{IN}) will ensure that the output is turned off.

3.2 TC1304 Shutdown Input Pin ($\overline{SHDN}$)

$\overline{SHDN}$ is a logic-level input used to initiate the sequencing of the LDO output, then the buck regulator output. A logic-high (> 45% of V_{IN}), will enable the regulator outputs. A logic-low (< 15% of V_{IN}) will ensure that the outputs are turned off.

3.3 LDO Input Voltage Pin (V_{IN2})

V_{IN2} is a LDO power input supply pin. Connect variable input voltage source to V_{IN2}. Connect V_{IN1} and V_{IN2} together with board traces as short as possible. V_{IN2} provides the input voltage for the LDO. An additional capacitor can be added to lower the LDO regulator input ripple voltage.

3.4 LDO Output Voltage Pin (V_{OUT2})

V_{OUT2} is a regulated LDO output voltage pin. Connect a 1 µF or larger capacitor to V_{OUT2} and A_{GND} for proper operation.

3.5 Power-Good Output Pin (PG)

PG is an output level indicating that V_{OUT2} (LDO) is within 94% of regulation. The PG output is configured as a push-pull for the TC1303B and open-drain output for the TC1303A, TC1303C and TC1304.

3.6 Analog Ground Pin (A_{GND})

A_{GND} is the analog ground connection. Tie A_{GND} to the analog portion of the ground plane (A_{GND}). See the physical layout information in **Section 5.0 "Application Circuits/Issues"** for grounding recommendations.

3.7 Buck Regulator Output Sense Pin (V_{FB}/V_{OUT1})

For V_{OUT1} adjustable-output voltage options, connect the center of the output voltage divider to the V_{FB} pin. For fixed-output voltage options, connect the output of the buck regulator to this pin (V_{OUT1}).

3.8 Buck Regulator Shutdown Input Pin (SHDN1)

$\overline{\text{SHDN1}}$ is a logic-level input used to turn the buck regulator on and off. A logic-high (> 45% of V_{IN}), will enable the regulator output. A logic-low (< 15% of V_{IN}) will ensure that the output is turned off.

3.9 Buck Regulator Input Voltage Pin (V_{IN1})

V_{IN1} is the buck regulator power input supply pin. Connect a variable input voltage source to V_{IN1}. Connect V_{IN1} and V_{IN2} together with board traces as short as possible.

3.10 Buck Inductor Output Pin (L_X)

Connect L_X directly to the buck inductor. This pin carries large signal-level current; all connections should be made as short as possible.

3.11 Power Ground Pin (P_{GND})

Connect all large-signal level ground returns to P_{GND}. These large-signal, level ground traces should have a small loop area and length to prevent coupling of switching noise to sensitive traces. Please see the physical layout information supplied in **Section 5.0 "Application Circuits/Issues"** for grounding recommendations.

3.12 Exposed Pad (EP)

For the DFN package, connect the EP to A_{GND}, with vias into the A_{GND} plane.

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4.0 DETAILED DESCRIPTION

4.1 Device Overview

The TC1303/TC1304 combines a 500 mA synchronous buck regulator with a 300 mA LDO and a power-good output. This unique combination provides a small, low-cost solution for applications that require two or more voltage rails. The buck regulator can deliver high-output current over a wide range of input-to-output voltage ratios while maintaining high efficiency. This is typically used for the lower-voltage, high-current processor core. The LDO is a minimal parts-count solution (single-output capacitor), providing a regulated voltage for an auxiliary rail. The typical LDO dropout voltage (137 mV @ 200 mA) allows the use of very low input-to-output LDO differential voltages, minimizing the power loss internal to the LDO pass transistor. A power-good output is provided, indicating that the buck regulator output, the LDO output or both outputs are in regulation. Additional features include independent shutdown inputs (TC1303), UVLO, output voltage sequencing (TC1304), overcurrent and overtemperature shutdown.

4.2 Synchronous Buck Regulator

The synchronous buck regulator is capable of supplying a 500 mA continuous output current over a wide range of input and output voltages. The output voltage range is from 0.8V (minimum) to 4.5V (maximum). The regulator operates in three different modes, automatically selecting the most efficient mode of operation. During heavy load conditions, the TC1303/TC1304 buck converter operates at a high, fixed frequency (2.0 MHz) using current mode control. This minimizes output ripple and noise (less than 8 mV peak-to-peak ripple) while maintaining high efficiency (typically > 90%). For standby or light load applications, the buck regulator will automatically switch to a power-saving Pulse Frequency Modulation (PFM) mode. This minimizes the quiescent current draw on the battery, while keeping the buck output voltage in regulation. The typical buck PFM mode current is 38 µA. The buck regulator is capable of operating at 100% duty cycle, minimizing the voltage drop from input-to-output for wide input, battery-powered applications. For fixed-output voltage applications, the feedback divider and control loop compensation components are integrated, eliminating the need for external components. The buck regulator output is protected against overcurrent, short circuit and overtemperature. While shut down, the synchronous buck N-channel and P-channel switches are off, so the L_X pin is in a high-impedance state (this allows for connecting a source on the output of the buck regulator as long as its voltage does not exceed the input voltage).

4.2.1 FIXED-FREQUENCY PWM MODE

While operating in Pulse Width Modulation (PWM) mode, the TC1303/TC1304 buck regulator switches at a fixed, 2.0 MHz frequency. The PWM mode is suited for higher load current operation, maintaining low output noise and high conversion efficiency. PFM-to-PWM mode transition is initiated for any of the following conditions:

- Continuous inductor current is sensed
- Inductor peak current exceeds 100 mA
- The buck regulator output voltage has dropped out of regulation (step load has occurred)

The typical PFM-to-PWM threshold is 80 mA.

4.2.2 PFM MODE

PFM mode is entered when the output load on the buck regulator is very light. Once detected, the converter enters the PFM mode automatically and begins to skip pulses to minimize unnecessary quiescent current draw by reducing the number of switching cycles per second. The typical quiescent current for the switching regulator is less than 35 µA. The transition from PWM to PFM mode occurs when discontinuous inductor current is sensed or the peak inductor current is less than 60 mA (typical). The typical PWM to PFM mode threshold is 30 mA. For low input-to-output differential voltages, the PWM-to-PFM mode threshold can be low due to the lack of ripple current. It is recommended that V_{IN1} be one volt greater than V_{OUT1} for PWM-to-PFM transitions.

4.3 Low Drop Out Regulator (LDO)

The LDO output is a 300 mA low-dropout linear regulator that provides a regulated output voltage with a single 1 µF external capacitor. The output voltage is available in fixed options only, ranging from 1.5V to 3.3V. The LDO is stable using ceramic output capacitors that inherently provide lower output noise and reduce the size and cost of the regulator solution. The quiescent current consumed by the LDO output is typically less than 40 µA, with a typical dropout voltage of 137 mV at 200 mA. While operating in Dropout mode, the LDO quiescent current will increase, minimizing the necessary voltage differential needed for the LDO output to maintain regulation. The LDO output is protected against overcurrent and overtemperature conditions.

4.4 Power-Good

A Power-Good (PG) output signal is generated based off of the buck regulator output voltage (V_{OUT1}), the LDO output voltage (V_{OUT2}) or the combination of both outputs. A fixed delay time of approximately 262 ms is generated once the monitored output voltage is above the power-good threshold (typically 94% of V_{OUTX}). As the monitored output voltage falls out of regulation, the falling PG threshold is typically 92% of the output voltage. The PG output signal is pulled up to the output voltage, indicating that power is good and pulled low, indicating that the output is out of regulation. The typical quiescent current draw for power-good circuitry is less than 10 µA.

If the monitored output voltage falls below the power-good threshold, the power-good output will transition to the Low state. The power-good circuitry has a 165 µs delay when detecting a falling output voltage. This helps to increase the noise immunity of the power-good output, avoiding false triggering of the PG signal during line and load transients.

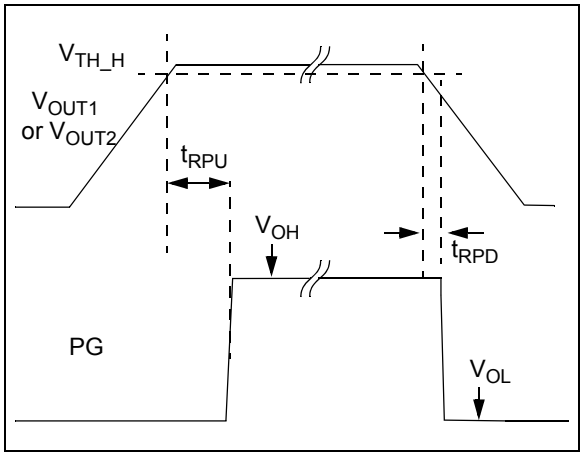

FIGURE 4-1: *Power-Good Timing.*

4.5 Power Good Output Options

There are three monitoring options for the TC1303 family.

For the TC1303A, only the buck regulator output voltage (V_{OUT1}) is monitored. The PG output signal depends only on V_{OUT1}.

For the TC1303B, only the LDO output voltage (V_{OUT2}) is monitored. The PG output signal depends only on V_{OUT2}.

For the TC1303C and TC1304, both the buck regulator output voltage and LDO output voltage are monitored. If either one of the outputs fall out of regulation, the PG will be low. Only if both V_{OUT1} and V_{OUT2} are within the PG voltage threshold limits will the PG output be high.

For the TC1303A,C and TC1304, the PG output pin is open drain and can be pulled up to any level within the given absolute maximum ratings (A_{GND} - 0.3V) to (V_{IN} + 0.3V).

TABLE 4-1: PG AVAILABLE OPTIONS

Part Number	PG Output Buck (V_{OUT1})	PG Output LDO (V_{OUT2})	PG Output Type
TC1303A	Yes	No	Open-Drain
TC1303B	No	Yes	Push-Pull (V_{OUT2})
TC1303C	Yes	Yes	Open-Drain
TC1304	Yes	Yes	Open-Drain

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4.6 TC1304 Sequencing

The TC1304 device features an integrated sequencing option. A sequencing circuit using only the SHDN input, (Pin1), will turn on the LDO output (V_{OUT2}) and delay the turn on of the Buck Regulator output (V_{OUT1}) until the LDO output is in regulation. During power-down, the sequencing circuit will turn off the Buck Regulator output prior to turning off LDO output.

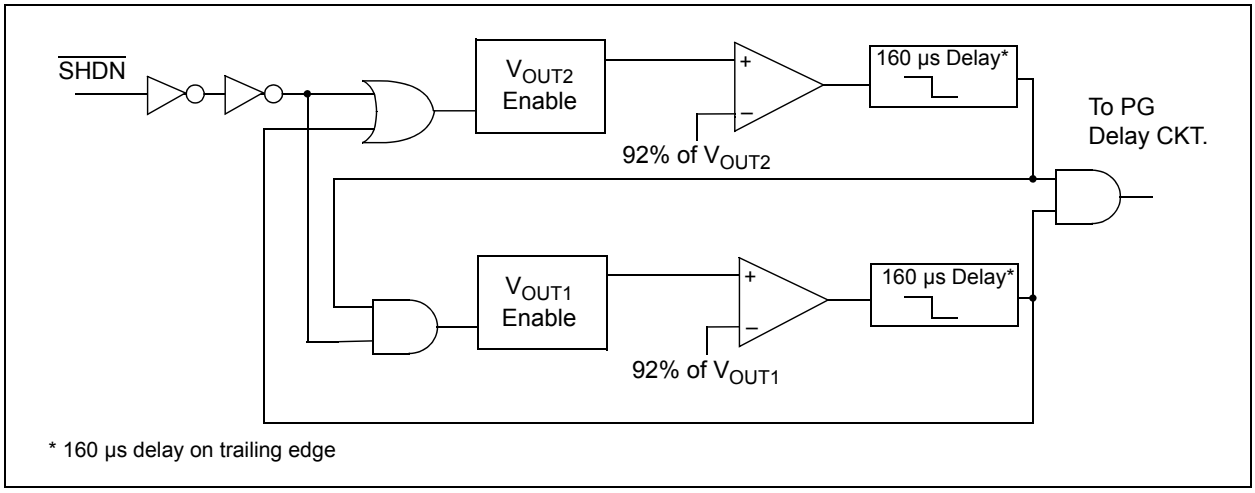

FIGURE 4-2: *TC1304 Sequencing Circuit.*

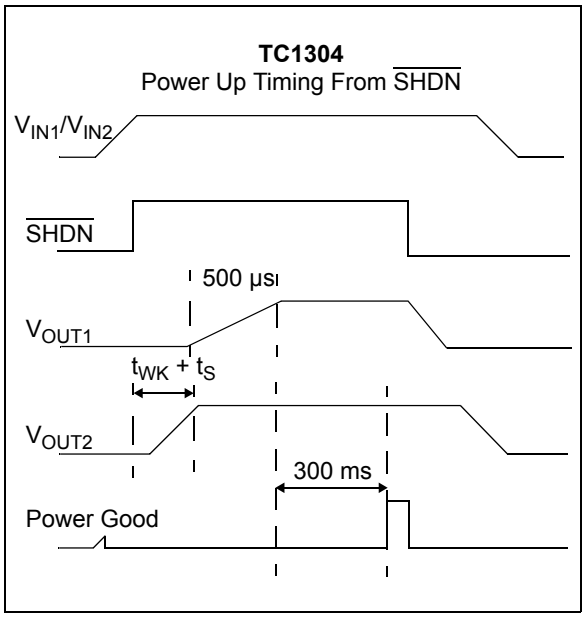

FIGURE 4-3: *TC1304 Power-up Timing from SHDN.*

4.7 Soft Start

Both outputs of the TC1303/TC1304 are controlled during start-up. Less than 1% of V_{OUT1} or V_{OUT2} overshoot is observed during start-up from V_{IN} rising above the UVLO voltage or either SHDN1 or SHDN2 being enabled.

4.8 Overtemperature Protection

The TC1303/TC1304 has an integrated overtemperature protection circuit that monitors the device junction temperature and shuts the device off if the junction temperature exceeds the typical 165°C threshold. If the overtemperature threshold is reached, the soft start is reset so that, once the junction temperature cools to approximately 155°C, the device will automatically restart.

NOTES:

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5.0 APPLICATION CIRCUITS/ ISSUES

5.1 Typical Applications

The TC1303/TC1304 500 mA buck regulator + 300 mA LDO with power-good operates over a wide input voltage range (2.7V to 5.5V) and is ideal for single-cell Li-Ion battery-powered applications, USB-powered applications, three-cell NiMH or NiCd applications and 3V to 5V regulated input applications. The 10-pin MSOP and 3x3 DFN packages provide a small footprint with minimal external components.

5.2 Fixed Output Application

A typical V_{OUT1} fixed-output voltage application is shown in "**Typical Application Circuits"**. A 4.7 µF V_{IN1} ceramic input capacitor, 4.7 µF V_{OUT1} ceramic capacitor, 1.0 µF ceramic V_{OUT2} capacitor and 4.7 µH inductor make up the entire external component solution for this dual-output application. No external dividers or compensation components are necessary. For this application, the input voltage range is 2.7V to 4.2V, V_{OUT1} = 1.5V at 500 mA, while V_{OUT2} = 2.5V at 300 mA.

5.3 Adjustable Output Application

A typical V_{OUT1} adjustable output application is also shown in "**Typical Application Circuits"**. For this application, the buck regulator output voltage is adjustable by using two external resistors as a voltage divider. For adjustable-output voltages, it is recommended that the top resistor divider value be 200 kΩ. The bottom resistor divider can be calculated using the following formula:

EQUATION 5-1:

$$R_{BOT} = R_{TOP} \times \left(\frac{V_{FB}}{V_{OUT1} - V_{FB}} \right)$$

Example:

R_{TOP} = 200 kΩ
V_{OUT1} = 2.1V
V_{FB} = 0.8V
R_{BOT} = 200 kΩ x (0.8V/(2.1V – 0.8V))
R_{BOT} = 123 kΩ (Standard Value = 121 kΩ)

For adjustable-output applications, an additional R-C compensation is necessary for the buck regulator control loop stability. Recommended values are:

R_{COMP} = 4.99 kΩ
C_{COMP} = 33 pF

An additional V_{IN2} capacitor can be added to reduce high-frequency noise on the LDO input voltage pin (V_{IN2}). This additional capacitor (1 µF on page 5) is not necessary for typical applications.

5.4 Input and Output Capacitor Selection

As with all buck-derived dc-dc switching regulators, the input current is pulled from the source in pulses. This places a burden on the TC1303/TC1304 input filter capacitor. In most applications, a minimum of 4.7 µF is recommended on V_{IN1} (buck regulator input voltage pin). In applications that have high source impedance, or have long leads, (10 inches) connecting to the input source, additional capacitance should be used. The capacitor type can be electrolytic (aluminum, tantalum, POSCAP, OSCON) or ceramic. For most portable electronic applications, ceramic capacitors are preferred due to their small size and low cost.

For applications that require very low noise on the LDO output, an additional capacitor (typically 1 µF) can be added to the V_{IN2} pin (LDO input voltage pin).

Low ESR electrolytic or ceramic can be used for the buck regulator output capacitor. Again, ceramic is recommended because of its physical attributes and cost. For most applications, a 4.7 µF is recommended. Refer to Table 5-1 for recommended values. Larger capacitors (up to 22 µF) can be used. There are some advantages in load step performance when using larger value capacitors. Ceramic materials X7R and X5R have low temperature coefficients and are well within the acceptable ESR range required.

TABLE 5-1: TC1303A, TC1303B, TC1303C, TC1304 RECOMMENDED CAPACITOR VALUES

	$C(V_{IN1})$	$C(V_{IN2})$	C_{OUT1}	C_{OUT2}
min	4.7 µF	none	4.7 µF	1 µF
max	none	none	22 µF	10 µF

5.5 Inductor Selection

For most applications, a 4.7 µH inductor is recommended to minimize noise. There are many different magnetic core materials and package options to select from. That decision is based on size, cost and acceptable radiated energy levels. Toroid and shielded ferrite pot cores will have low radiated energy, but tend to be larger and higher is cost. With a typical 2.0 MHz switching frequency, the inductor ripple current can be calculated based on the following formulas.

EQUATION 5-2:

$$DutyCycle = \frac{V_{OUT}}{V_{IN}}$$

Duty cycle represents the percentage of switch-on time.

EQUATION 5-3:

$$T_{ON} = DutyCycle \times \frac{1}{F_{SW}}$$

Where:

F_{SW} = Switching Frequency.

The inductor ac ripple current can be calculated using the following relationship:

EQUATION 5-4:

$$V_L = L \times \frac{\Delta I_L}{\Delta t}$$

Where:

V_L = voltage across the inductor ($V_{IN} – V_{OUT}$)

Δt = on-time of P-channel MOSFET

Solving for ΔI_L = yields:

EQUATION 5-5:

$$\Delta I_L = \frac{V_L}{L} \times \Delta t$$

When considering inductor ratings, the maximum DC current rating of the inductor should be at least equal to the maximum buck regulator load current (I_{OUT1}), plus one half of the peak-to-peak inductor ripple current (1/ 2 * ΔI_L). The inductor DC resistance can add to the buck converter I^2R losses. A rating of less than 200 mΩ is recommended. Overall efficiency will be improved by using lower DC resistance inductors.

TABLE 5-2: TC1303A, TC1303B, TC1303C, TC1304 RECOMMENDED INDUCTOR VALUES

Part Number	Value (µH)	DCR Ω (MAX)	MAX I_{DC} (A)	Size WxLxH (mm)
Coiltronics®				
SD10	2.2	0.091	1.35	5.2, 5.2, 1.0 max.
SD10	3.3	0.108	1.24	5.2, 5.2, 1.0 max.
SD10	4.7	0.154	1.04	5.2, 5.2, 1.0 max.
Coiltronics				
SD12	2.2	0.075	1.80	5.2, 5.2, 1.2 max.
SD12	3.3	0.104	1.42	5.2, 5.2, 1.2 max.
SD12	4.7	0.118	1.29	5.2, 5.2, 1.2 max.
Sumida Corporation®				
CMD411	2.2	0.116	0.950	4.4, 5.8, 1.2 max.
CMD411	3.3	0.174	0.770	4.4, 5.8, 1.2 max.
CMD411	4.7	0.216	0.750	4.4, 5.8, 1.2 max.
Coilcraft®				
1008PS	4.7	0.35	1.0	3.8, 3.8, 2.74 max.
1812PS	4.7	0.11	1.15	5.9, 5.0, 3.81 max

5.6 Thermal Calculations

5.6.1 BUCK REGULATOR OUTPUT (V_{OUT1})

The TC1303/TC1304 is available in two different 10-pin packages (MSOP and 3x3 DFN). By calculating the power dissipation and applying the package thermal resistance, (θ_{JA}), the junction temperature is estimated. The maximum continuous junction temperature rating for the TC1303/TC1304 is +125°C.

To quickly estimate the internal power dissipation for the switching buck regulator, an empirical calculation using measured efficiency can be used. Given the measured efficiency (**Section 2.0 "Typical Performance Curves"**), the internal power dissipation is estimated below:

EQUATION 5-6:

$$\left(\frac{V_{OUT1} \times I_{OUT1}}{Efficiency}\right) - (V_{OUT1} \times I_{OUT1}) = P_{Dissipation}$$

The first term is equal to the input power (definition of efficiency, P_{OUT}/P_{IN} = Efficiency). The second term is equal to the delivered power. The difference is internal power dissipation. This is an estimate assuming that most of the power lost is internal to the TC1303B. There is some percentage of power lost in the buck inductor, with very little loss in the input and output capacitors.

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As an example, for a 3.6V input, 1.8V output with a load of 400 mA, the efficiency taken from Figure 2-8 is approximately 84%. The internal power dissipation is approximately 137 mW.

5.6.2 LDO OUTPUT (V_{OUT2})

The internal power dissipation within the TC1303/TC1304 LDO is a function of input voltage, output voltage and output current. Equation 5-7 can be used to calculate the internal power dissipation for the LDO.

EQUATION 5-7:

$$P_{LDO} = (V_{IN(MAX))} - V_{OUT2(MIN)}) \times I_{OUT2(MAX))}$$

Where:

P_{LDO} = LDO Pass device internal power dissipation

$V_{IN(MAX)}$ = Maximum input voltage

$V_{OUT(MIN)}$ = LDO minimum output voltage

The maximum power dissipation capability for a package can be calculated given the junction-to-ambient thermal resistance and the maximum ambient temperature for the application. The following equation can be used to determine the package's maximum internal power dissipation.

5.6.3 LDO POWER DISSIPATION EXAMPLE

Input Voltage

V_{IN} = 5V±10%

LDO Output Voltage and Current

V_{OUT} = 3.3V

I_{OUT} = 300 mA

Internal Power Dissipation

$P_{LDO(MAX)} = (V_{IN(MAX)} - V_{OUT2(MIN)}) \times I_{OUT2(MAX)}$

P_{LDO} = (5.5V – 0.975 x 3.3V) x 300 mA

P_{LDO} = 684.8 mW

5.7 PCB Layout Information

Some basic design guidelines should be used when physically placing the TC1303/TC1304 on a Printed Circuit Board (PCB). The TC1303/TC1304 has two ground pins, identified as A_{GND} (analog ground) and P_{GND} (power ground). By separating grounds, it is possible to minimize the switching frequency noise on the LDO output. The first priority, while placing external components on the board, is the input capacitor (C_{IN1}). Wiring should be short and wide; the input current for the TC1303/TC1304 can be as high as 800 mA. The next priority would be the buck regulator output capacitor (C_{OUT1}) and inductor (L_1). All three of these components are placed near their respective pins to minimize trace length. The C_{IN1} and C_{OUT1} capacitor returns are connected closely together at the P_{GND} plane. The LDO optional input capacitor (C_{IN2}) and LDO output capacitor C_{OUT2} are returned to the A_{GND} plane. The analog ground plane and power ground plane are connected at one point (shown near L_1). All other signals ($\overline{SHDN1}$, $\overline{SHDN2}$, feedback in the adjustable-output case) should be referenced to A_{GND} and have the A_{GND} plane underneath them.

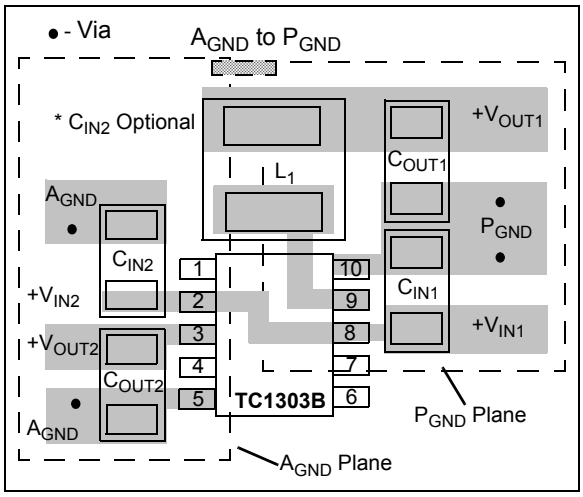

FIGURE 5-1: *Component Placement, Fixed 10-Pin MSOP.*

There will be some difference in layout for the 10-pin DFN package due to the thermal pad. A typical fixed-output DFN layout is shown below. For the DFN layout, the V_{IN1} to V_{IN2} connection is routed on the bottom of the board around the TC1303/TC1304 thermal pad.

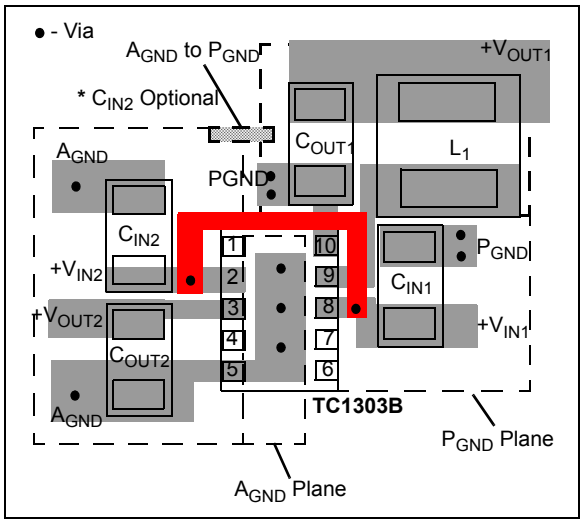

FIGURE 5-2: *Component Placement, Fixed 10-Pin DFN.*

5.8 Design Example

V_{OUT1} = 2.0V @ 500 mA
V_{OUT2} = 3.3V @ 300 mA
V_{IN} = 5V±10%
L = 4.7µH

Calculate PWM mode inductor ripple current

Nominal Duty Cycle = 2.0V/5.0V = 40%

P-channel Switch-on time = 0.40 x 1/(2 MHz) = 200 ns

V_L = (V_{IN}-V_{OUT1}) = 3V

ΔI_L = (V_L/L) x T_{ON} = 128 mA

Peak inductor current:

$I_{L(PK)}$ = I_{OUT1}+1/2ΔI_L = 564 mA

Switcher power loss:

Use efficiency estimate for 1.8V from Figure 2-8

Efficiency = 84%, P_{DISS1} = 190 mW

Resistor Divider:

R_{TOP} = 200 kΩ
R_{BOT} = 133 kΩ

LDO Output:

P_{DISS2} = ($V_{IN(MAX)}$ – $V_{OUT2(MIN)}$) x $I_{OUT2(MAX)}$

P_{DISS2} = (5.5V – (0.975) x 3.3V) x 300 mA

P_{DISS2} = 684.8 mW

Total Dissipation = 190 mW + 685 mW = 874 mW

Junction Temp Rise and Maximum Ambient Operating Temperature Calculations

10-Pin MSOP (4-Layer Board with internal Planes)

$R\theta_{JA}$ = 113° C/Watt

Junction Temp. Rise = 874 mW x 113° C/Watt = 98.8°C

Max. Ambient Temperature = 125°C - 98.8°C

Max. Ambient Temperature = 26.3°C

10-Pin DFN

$R\theta_{JA}$ = 41° C/Watt (4-Layer Board with internal planes and 2 vias)

Junction Temp. Rise = 874 mW x 41° C/Watt = 35.8°C

Max. Ambient Temperature = 125°C - 35.8°C

Max. Ambient Temperature = 89.2°C

This is above the +85°C max. ambient temperature.

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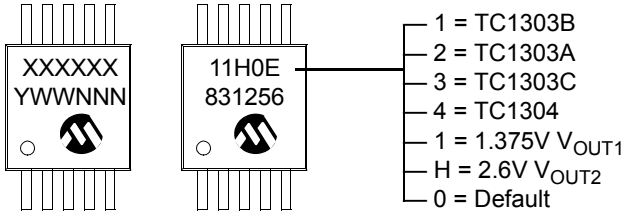
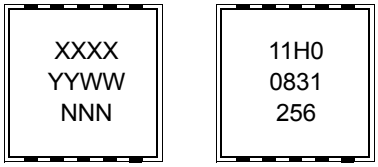
6.0 PACKAGING INFORMATION

6.1 Package Marking Information

10-Lead MSOP Example:



10-Lead DFN Example:



Second letter represents V_{OUT1} configuration:

Code	V_{OUT1}	Code	V_{OUT1}	Code	V_{OUT1}
A	3.3V	J	2.4V	S	1.5V
B	3.2V	K	2.3V	T	1.4V
C	3.1V	L	2.2V	U	1.3V
D	3.0V	M	2.1V	V	1.2V
E	2.9V	N	2.0V	W	1.1V
F	2.8V	O	1.9V	X	1.0V
G	2.7V	P	1.8V	Y	0.9V
H	2.6V	Q	1.7V	Z	Adj
I	2.5V	R	1.6V	1	1.375V

Third letter represents V_{OUT2} configuration:

Code	V_{OUT2}	Code	V_{OUT1}	Code	V_{OUT2}
A	3.3V	J	2.4V	S	1.5V
B	3.2V	K	2.3V	T	—
C	3.1V	L	2.2V	U	—
D	3.0V	M	2.1V	V	—
E	2.9V	N	2.0V	W	—
F	2.8V	O	1.9V	X	—
G	2.7V	P	1.8V	Y	—
H	2.6V	Q	1.7V	Z	—
I	2.5V	R	1.6V		

Fourth letter represents +50 mV Increments:

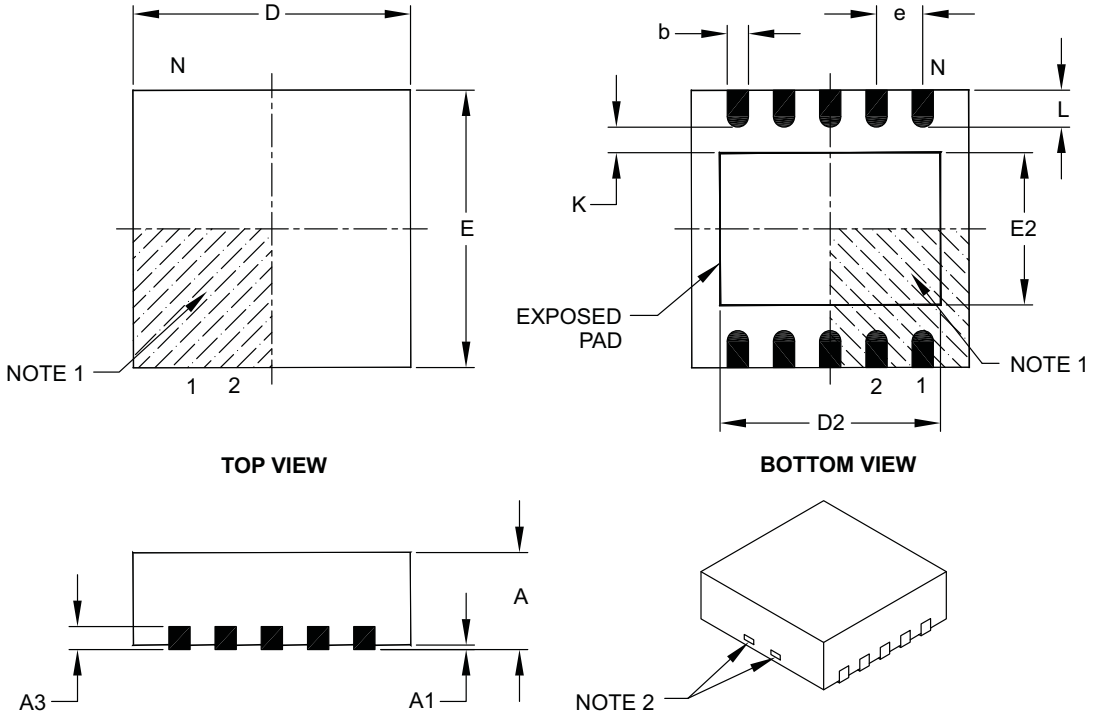
Code		Code	
0	Default	2	+50 mV to V2
1	+50 mV to V1	3	+50 mV to V1 and V2

Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

10-Lead Plastic Dual Flat, No Lead Package (MF) – 3x3x0.9 mm Body [DFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		10	
Pitch	e		0.50 BSC	
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.02	0.05
Contact Thickness	A3		0.20 REF	
Overall Length	D		3.00 BSC	
Exposed Pad Length	D2	2.20	2.35	2.48
Overall Width	E		3.00 BSC	
Exposed Pad Width	E2	1.40	1.58	1.75
Contact Width	b	0.18	0.25	0.30
Contact Length	L	0.30	0.40	0.50
Contact-to-Exposed Pad	K	0.20	–	–

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package may have one or more exposed tie bars at ends.
3. Package is saw singulated.
4. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-063B

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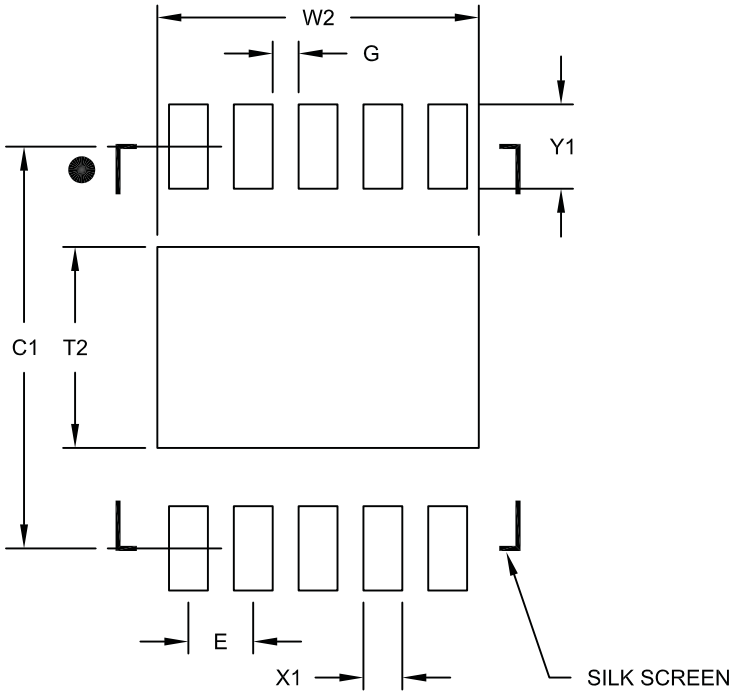
10-Lead Plastic Dual Flat, No Lead Package (MF) – 3x3x0.9 mm Body [DFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.50 BSC		
Optional Center Pad Width	W2			2.48
Optional Center Pad Length	T2			1.55
Contact Pad Spacing	C1		3.10	
Contact Pad Width (X8)	X1			0.30
Contact Pad Length (X8)	Y1			0.65
Distance Between Pads	G	0.20		

Notes:

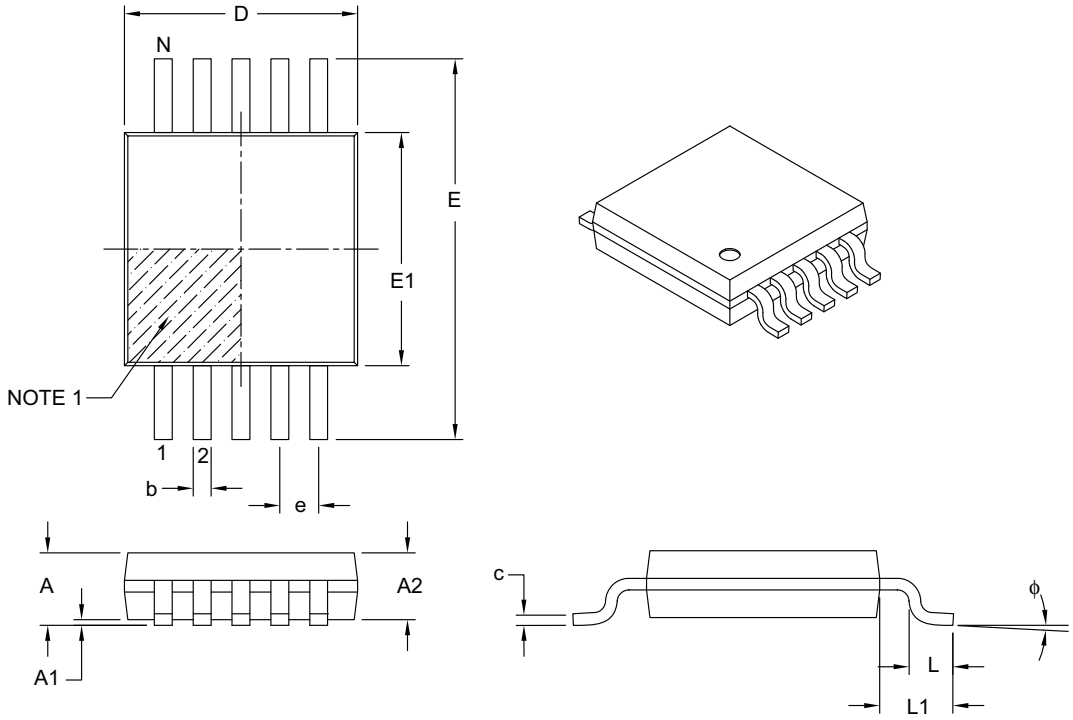
1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2063A

10-Lead Plastic Micro Small Outline Package (UN) [MSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		10	
Pitch	e		0.50 BSC	
Overall Height	A	–	–	1.10
Molded Package Thickness	A2	0.75	0.85	0.95
Standoff	A1	0.00	–	0.15
Overall Width	E		4.90 BSC	
Molded Package Width	E1		3.00 BSC	
Overall Length	D		3.00 BSC	
Foot Length	L	0.40	0.60	0.80
Footprint	L1		0.95 REF	
Foot Angle	ϕ	0°	–	8°
Lead Thickness	c	0.08	–	0.23
Lead Width	b	0.15	–	0.33

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15 mm per side.
3. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-021B

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APPENDIX A: REVISION HISTORY

Revision C (December 2008)

The following is the list of modifications:

1. Updated Package Types diagram and **Section 3.0 "Pin Descriptions"** to show the Exposed Thermal Pad (EP) information.
2. Updated **Section 6.0 "Packaging Information"**.

Revision B (July 2005)

The following is the list of modifications:

1. Added information on TC1303A, TC1303C and TC1304 throughout data sheet.

Revision A (June 2005)

- Original Release of this Document.

NOTES:

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PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	X-	X	X	X	X	XX	XX
TC1303	Type B	V_{OUT1}	V_{OUT2}	+50 mV Increments	Temp Range	Package	Tube or Tape & Reel

Device: TC1303A: PWM/LDO combo with Power-Good
TC1303B: PWM/LDO combo with Power-Good
TC1303C: PWM/LDO combo with Power-Good
TC1304: PWM/LDO combo with Power-Good

Options	Code	V_{OUT1}	Code	V_{OUT2}	Code	+50 mV
	A	3.3V	A	3.3V	0	Default
	B	3.2V	B	3.2V	1	+50 mV to V1
	C	3.1V	C	3.1V	2	+50 mV to V2
	D	3.0V	D	3.0V	3	+50 mV to V1 and V2
	E	2.9V	E	2.9V		
	F	2.8V	F	2.8V		
	G	2.7V	G	2.7V		
	H	2.6V	H	2.6V		
	I	2.5V	I	2.5V		
	J	2.4V	J	2.4V		
	K	2.3V	K	2.3V		
	L	2.2V	L	2.2V		
	M	2.1V	M	2.1V		
	N	2.0V	N	2.0V		
	O	1.9V	O	1.9V		
	P	1.8V	P	1.8V		
	Q	1.7V	Q	1.7V		
	R	1.6V	R	1.6V		
	S	1.5V	S	1.5V		
	T	1.4V	T			
	U	1.3V	U			
	V	1.2V	V			
	W	1.1V	W			
	X	1.0V	X			
	Y	0.9V	Y			
	Z	Adjustable	Z			
	1	1.375V	1			

* Contact Factory for Alternate Output Voltage and Reset Voltage Configurations.

Temperature Range: E = -40°C to +85°C

Package: MF = Dual Flat, No Lead (3x3 mm body), 10-lead
UN = Plastic Micro Small Outline (MSOP), 10-lead

Tube or Tape and Reel: Blank = Tube
TR = Tape and Reel

Examples:

a) TC1303A-SI0EMF: 1.5V, 2.5V, Default, 10LD DFN pkg.
b) TC1303A-ZA0EUN: Adj, 3.3V, Default, 10LD MSOP pkg.
c) TC1303A-PP3EMFTR: 1.8V, 1.8V, +50 mV, 10LD DFN pkg. Tape and Reel

a) TC1303B-1H0EMF: 1.375V, 2.6V, Default, 10LD DFN pkg.
b) TC1303B-AG0EUN: 3.3V, 2.7V, Default, 10LD MSOP pkg.
c) TC1303B-AD0EMF: 3.3V, 3.0V, Default, 10LD DFN pkg.
d) TC1303B-IA0EUN: 2.5V, 3.3V, Default, 10LD MSOP pkg.
e) TC1303B-IA0EMF: 2.5V, 3.3V, Default, 10LD DFN pkg.
f) TC1303B-PF0EUN: 1.8V, 2.8V, Default, 10LD MSOP pkg.
g) TC1303B-PF0EMF: 1.8V, 2.8V, Default, 10LD DFN pkg.
h) TC1303B-PG0EUN: 1.8V, 2.7V, Default, 10LD MSOP pkg.
i) TC1303B-DG0EMFTR: 3.0V, 2.7V, Default, 10LD DFN pkg. Tape and Reel

a) TC1303C-VP0EMF: 1.2V, 1.8V, Default, 10LD DFN pkg.
b) TC1303C-VP0EMFTR: 1.2V, 1.8V, Default, 10LD DFN pkg. Tape and Reel.

a) TC1304-VI0EMF: 1.2V, 2.5V, Default, 10LD DFN pkg.
b) TC1304-VP0EMF: 1.2V, 1.8V, Default, 10LD DFN pkg.
c) TC1304-VI0EUN: 1.2V, 2.5V, Default, 10LD MSOP pkg.
d) TC1304-VI0EMFTR: 1.2V, 2.5V, Default, 10LD DFN pkg. Tape and Reel.
e) TC1304-VP0EMFTR: 1.2V, 1.8V, Default 10LD DFN pkg. Tape and Reel.
f) TC1304-VI0EUNTR: 1.2V, 2.5V, Default, 10LD MSOP pkg. Tape and Reel.

NOTES:

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