DRAM

256K x 4 DRAM

STANDARD OR LOW POWER,
EXTENDED REFRESH

FEATURES

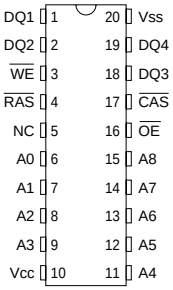
- 512-cycle refresh in 8ms (MT4C4256) or 64ms (MT4C4256 L)
- Industry-standard x4 pinout, timing, functions and packages
- High-performance CMOS silicon-gate process
- Single +5V ±10% power supply
- Low power, 0.8mW standby; 175mW active, typical
- All inputs, outputs and clocks are TTL-compatible
- FAST PAGE MODE access cycle
- Refresh modes: $\overline{RAS}$ ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$ (CBR), HIDDEN and Extended (MT4C4256L only)
- Low CMOS Standby Current, 200µA maximum (MT4C4256 L)

OPTIONS — MARKING

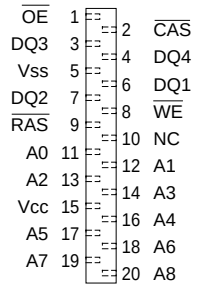
- Timing
  - 60ns access — -6
  - 70ns acces — -7
  - 80ns access — -8
- Packages
  - Plastic DIP (300 mil) — None
  - Plastic SOJ (300 mil) — DJ
  - Plastic ZIP (350 mil) — Z
- Version
  - 512-cycle refresh in 8 ms — None
  - 512-cycle refresh in 64 ms — L
- Part Number Example: MT4C4256DJ-7 L

PIN ASSIGNMENT (Top View)

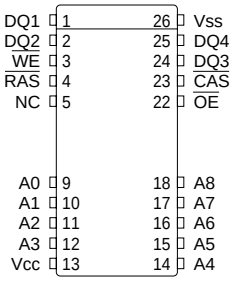
20-Pin DIP (DA-2)



20-Pin ZIP (DB-1)



20/26-Pin SOJ (DC-1)



GENERAL DESCRIPTION

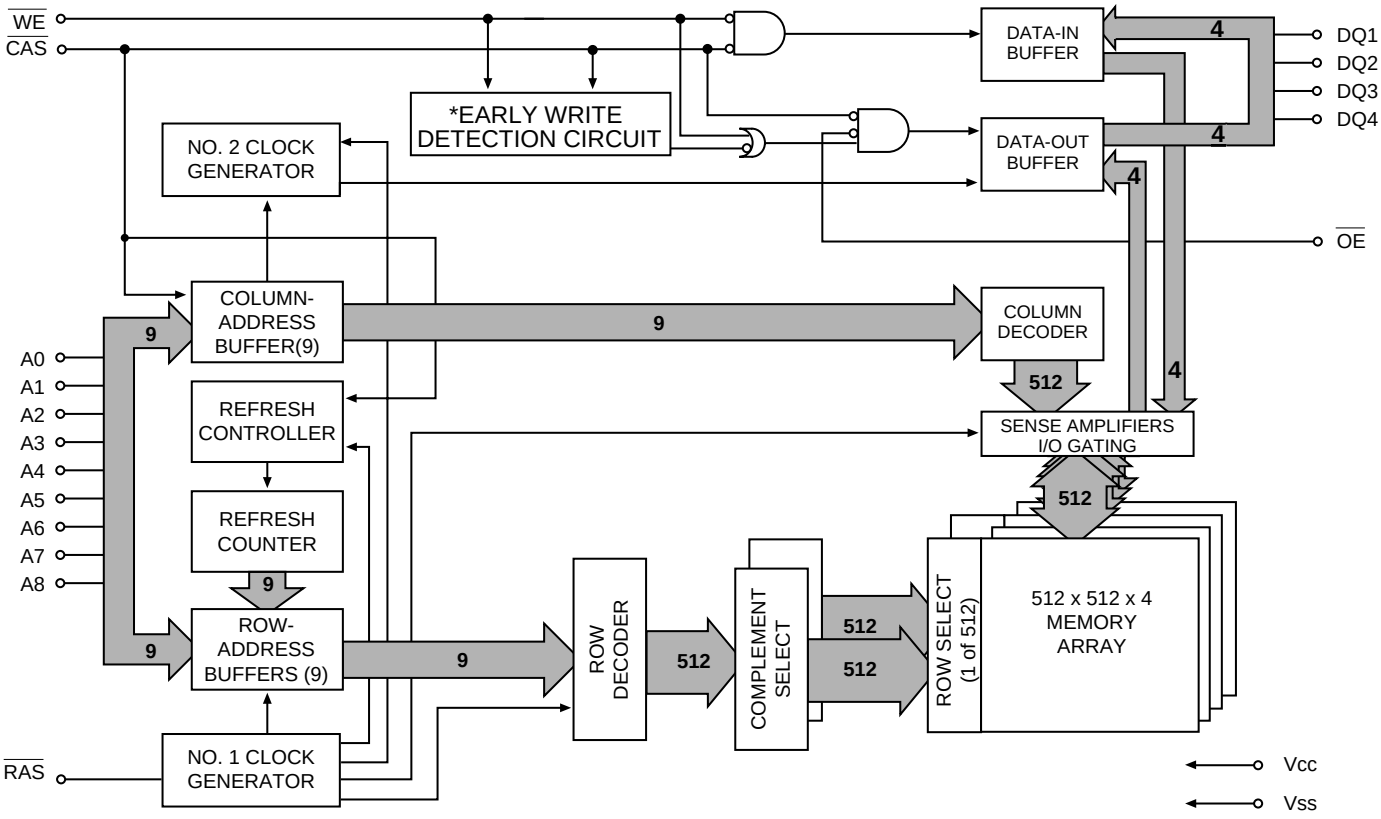
The MT4C4256(L) is a randomly accessed solid-state memory containing 1,048,576 bits organized in a x4 configuration. During READ or WRITE cycles, each bit is uniquely addressed through the 18 address bits, which are entered 9 bits (A0-A8) at a time. $\overline{RAS}$ is used to latch the first 9 bits and $\overline{CAS}$ the latter 9 bits. READ and WRITE cycles are selected with the $\overline{WE}$ input. A logic HIGH on $\overline{WE}$ dictates READ mode while a logic LOW on $\overline{WE}$ dictates WRITE mode. During a WRITE cycle, data-in (D) is latched by the falling edge of $\overline{WE}$ or $\overline{CAS}$, whichever occurs last. If $\overline{WE}$ goes LOW prior to $\overline{CAS}$ going LOW, the output pin(s) remain open (High-Z) until the next $\overline{CAS}$ cycle. If $\overline{WE}$ goes LOW after data reaches the output pin, data-out (Q) is activated and retains the selected cell data as long as $\overline{CAS}$ remains LOW (regardless of $\overline{WE}$ or $\overline{RAS}$). This late $\overline{WE}$ pulse results in a READ WRITE cycle. The four data inputs and four data outputs are routed through four pins using common I/O and pin direction is controlled by $\overline{WE}$ and $\overline{OE}$.

FAST PAGE MODE operations allow faster data operations (READ, WRITE or READ-MODIFY-WRITE) within a row-address-defined (A0-A8) page boundary. The FAST PAGE MODE cycle is always initiated with a row-address strobed-in by $\overline{RAS}$ followed by a column-address strobed-

in by $\overline{CAS}$. $\overline{CAS}$ may be toggled-in by holding $\overline{RAS}$ LOW and strobing-in different column-addresses, thus executing faster memory cycles. Returning $\overline{RAS}$ HIGH terminates the FAST PAGE MODE cycle.

Returning $\overline{RAS}$ and $\overline{CAS}$ HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the $\overline{RAS}$ HIGH time. Memory cell data is retained in its correct state by maintaining power and executing any $\overline{RAS}$ cycle (READ, WRITE) or $\overline{RAS}$ REFRESH cycle ($\overline{RAS}$ ONLY, CBR, or HIDDEN) so that all 512 combinations of $\overline{RAS}$ addresses (A0-A8) are executed at least every 8ms for the MT4C4256 and every 64ms for the MT4C4256L, regardless of sequence. The CBR REFRESH cycle will invoke the internal refresh counter for automatic $\overline{RAS}$ addressing.

FUNCTIONAL BLOCK DIAGRAM
FAST PAGE MODE



***NOTE:** 1. If $\overline{WE}$ goes LOW prior to $\overline{CAS}$ going LOW, EW detection circuit output is a HIGH (EARLY WRITE).
2. If $\overline{CAS}$ goes LOW prior to $\overline{WE}$ going LOW, EW detection circuit output is a LOW (LATE WRITE).

TRUTH TABLE

FUNCTION		RAS	CAS	WE	OE	ADDRESSES		DATA-IN/OUT
						^tR	^tC	DQ1-DQ4
Standby		H	H→X	X	X	X	X	High-Z
READ		L	L	H	L	ROW	COL	Data-Out
EARLY WRITE		L	L	L	X	ROW	COL	Data-In
READ WRITE		L	L	H→L	L→H	ROW	COL	Data-Out, Data-In
FAST-PAGE-MODE	1st Cycle	L	H→L	H	L	ROW	COL	Data-Out
READ	2nd Cycle	L	H→L	H	L	n/a	COL	Data-Out
FAST-PAGE-MODE	1st Cycle	L	H→L	L	X	ROW	COL	Data-In
EARLY-WRITE	2nd Cycle	L	H→L	L	X	n/a	COL	Data-In
FAST-PAGE-MODE	1st Cycle	L	H→L	H→L	L→H	ROW	COL	Data-Out, Data-In
READ-WRITE	2nd Cycle	L	H→L	H→L	L→H	n/a	COL	Data-Out, Data-In
RAS ONLY REFRESH		L	H	X	X	ROW	n/a	High-Z
HIDDEN	READ	L→H→L	L	H	L	ROW	COL	Data-Out
REFRESH	WRITE	L→H→L	L	L	X	ROW	COL	Data-In
CBR REFRESH		H→L	L	X	X	X	X	High-Z
Extended Refresh (MT4C4256 L only)		H→L	L	X	X	X	X	High-Z

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to V_{SS} ..... -1V to +7V
Operating Temperature, T_A (ambient) ..... 0°C to +70°C
Storage Temperature (plastic)..... -55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 6, 7) (V_{CC} = +5V ±10%)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.5	V	
Input High (Logic 1) Voltage, all inputs	V_{IH}	2.4	V_{CC}+1	V	
Input Low (Logic 0) Voltage, all inputs	V_{IL}	-1.0	0.8	V	
INPUT LEAKAGE CURRENT Any input 0V ≤ V_{IN} ≤ 6.5V (All other pins not under test = 0V)	I_I	-2	2	µA	
OUTPUT LEAKAGE CURRENT: (Q is disabled; 0V ≤ V_{OUT} ≤ 5.5V)	I_{OZ}	-10	10	µA	
OUTPUT LEVELS Output High Voltage (I_{OUT} = -5mA)	V_{OH}	2.4		V	
Output Low Voltage (I_{OUT} = 4.2mA)	V_{OL}		0.4	V	

			MAX				
PARAMETER/CONDITION	VERSION	SYMBOL	-6	-7	-8	UNITS	NOTES
STANDBY CURRENT: (TTL) ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})		I_{CC1}	2	2	2	mA	
STANDBY CURRENT: (CMOS)	MT4C4256	I_{CC2}	1	1	1	mA	
($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} -0.2V)	MT4C4256 L	I_{CC2}	200	200	200	µA	
OPERATING CURRENT: Random READ/WRITE Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Single Address Cycling: ^tRC = ^tRC [MIN])		I_{CC3}	90	80	70	mA	3, 4, 29
OPERATING CURRENT: FAST PAGE MODE Average power supply current ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: ^tPC = ^tPC [MIN])		I_{CC4}	70	60	50	mA	3, 4, 29
REFRESH CURRENT: $\overline{RAS}$ ONLY Average power supply current ($\overline{RAS}$ Cycling, $\overline{CAS}$ = V_{IH}: ^tRC = ^tRC [MIN])		I_{CC5}	90	80	70	mA	3, 29
REFRESH CURRENT: CBR Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC [MIN])		I_{CC6}	90	80	70	mA	3, 5
REFRESH CURRENT: Extended Average power supply current during Extended Refresh: $\overline{CAS}$ = 0.2V or CBR cycling; $\overline{RAS}$ = ^tRAS (MIN) to1µs; $\overline{WE}$, A0-A8 and D_{IN} = Vcc -0.2V or 0.2V (D_{IN} may be left open); ^tRC = 125µs (512 rows at 125µs = 64ms)	MT4C4256 L	I_{CC7}	200	200	200	µA	3, 5, 27

CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A0-A8	C_{I1}		5	pF	2
Input Capacitance: $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$	C_{I2}		7	pF	2
Input/Output Capacitance: DQ	C_{IO}		7	pF	2

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13, 23) (V_{CC} = +5V ±10%)

AC CHARACTERISTICS		-6		-7		-8			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	^tRC	110		130		150		ns	
READ WRITE cycle time	^tRWC	165		185		205		ns	
FAST-PAGE-MODE READ or WRITE cycle time	^tPC	35		40		45		ns	
FAST-PAGE-MODE READ-WRITE cycle time	^tPRWC	90		95		100		ns	
Access time from $\overline{RAS}$	^tRAC		60		70		80	ns	14
Access time from $\overline{CAS}$	^tCAC		20		20		20	ns	15
Output Enable	^tOE		20		20		20	ns	
Access time from column-address	^tAA		30		35		40	ns	
Access time from $\overline{CAS}$ precharge	^tCPA		35		40		45	ns	
$\overline{RAS}$ pulse width	^tRAS	60	100,000	70	100,000	80	100,000	ns	
$\overline{RAS}$ pulse width (FAST PAGE MODE)	^tRASP	60	100,000	70	100,000	80	100,000	ns	
$\overline{RAS}$ hold time	^tRSH	20		20		20		ns	
$\overline{RAS}$ precharge time	^tRP	40		50		60		ns	
$\overline{CAS}$ pulse width	^tCAS	20	100,000	20	100,000	20	100,000	ns	
$\overline{CAS}$ hold time	^tCSH	60		70		80		ns	
$\overline{CAS}$ precharge time	^tCPN	10		10		10		ns	16
$\overline{CAS}$ precharge time (FAST PAGE MODE)	^tCP	10		10		10		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	^tRCD	20	40	20	50	20	60	ns	17
$\overline{CAS}$ to $\overline{RAS}$ precharge time	^tCRP	5		5		5		ns	
Row-address setup time	^tASR	0		0		0		ns	
Row-address hold time	^tRAH	10		10		10		ns	
$\overline{RAS}$ to column-address delay time	^tRAD	15	30	15	35	15	40	ns	18
Column-address setup time	^tASC	0		0		0		ns	
Column-address hold time	^tCAH	15		15		15		ns	
Column-address hold time (referenced to $\overline{RAS}$)	^tAR	45		55		60		ns	
Column-address to $\overline{RAS}$ lead time	^tRAL	30		35		40		ns	
Read command setup time	^tRCS	0		0		0		ns	
Read command hold time (referenced to $\overline{CAS}$)	^tRCH	0		0		0		ns	19
Read command hold time (referenced to $\overline{RAS}$)	^tRRH	0		0		0		ns	19
$\overline{CAS}$ to output in Low-Z	^tCLZ	0		0		0		ns	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

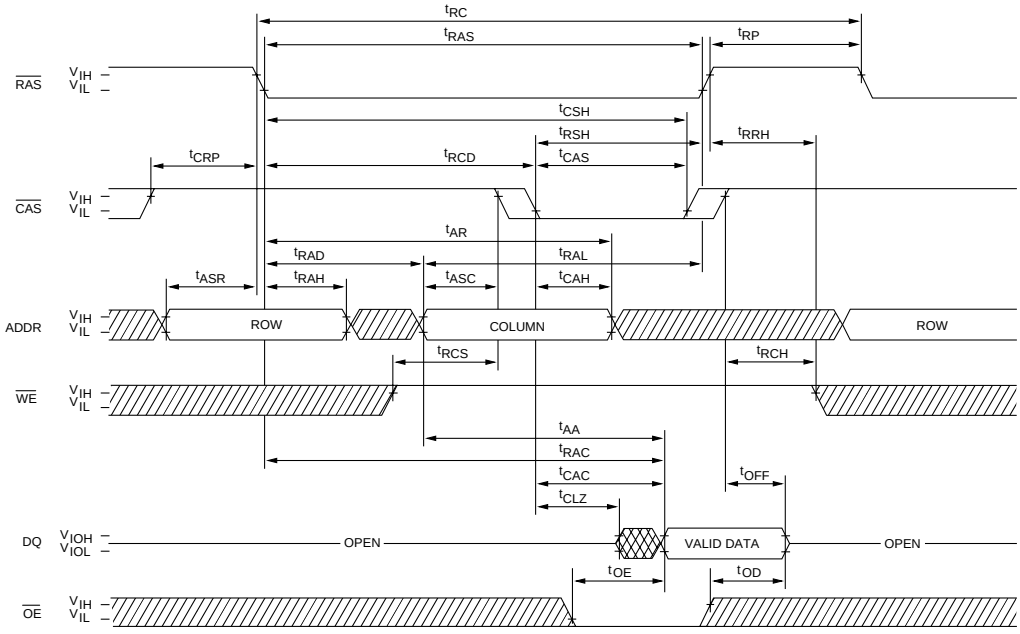
(Notes: 6, 7, 8, 9, 10, 11, 12, 13, 23) (Vcc = +5V ±10%)

AC CHARACTERISTICS		-6		-7		-8			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Output buffer turn-off delay	tOFF	3	20	3	20	3	20	ns	20, 26, 28
Output disable	tOD		15		20		20	ns	26
$\overline{WE}$ command setup time	tWCS	0		0		0		ns	21
Write command hold time	tWCH	10		15		15		ns	
Write command hold time (referenced to $\overline{RAS}$)	tWCR	45		55		60		ns	
Write command pulse width	tWP	10		15		15		ns	
Write command to $\overline{RAS}$ lead time	tRWL	20		20		20		ns	
Write command to $\overline{CAS}$ lead time	tCWL	20		20		20		ns	
Data-in setup time	tDS	0		0		0		ns	22
Data-in hold time	tDH	15		15		15		ns	22
Data-in hold time (referenced to $\overline{RAS}$)	tDHR	45		55		60		ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	tRWD	85		100		110		ns	21
Column-address to $\overline{WE}$ delay time	tAWD	60		65		70		ns	21
$\overline{CAS}$ to $\overline{WE}$ delay time	tCWD	40		50		55		ns	21
Transition time (rise or fall)	tT	3	50	3	50	3	50	ns	9, 10
Refresh period (512 cycles) MT4C4256 / MT4C4256 L	tREF		8 / 64		8 / 64		8 / 64	ms	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	tRPC	0		0		0		ns	
$\overline{CAS}$ setup time (CBR REFRESH)	tCSR	10		10		10		ns	5
$\overline{CAS}$ hold time (CBR REFRESH)	tCHR	10		15		15		ns	5
$\overline{OE}$ hold time from $\overline{WE}$ during READ-MODIFY-WRITE cycle	tOEH	15		20		20		ns	25
$\overline{OE}$ setup prior to $\overline{RAS}$ during HIDDEN REFRESH cycle	tORD	0		0		0		ns	24

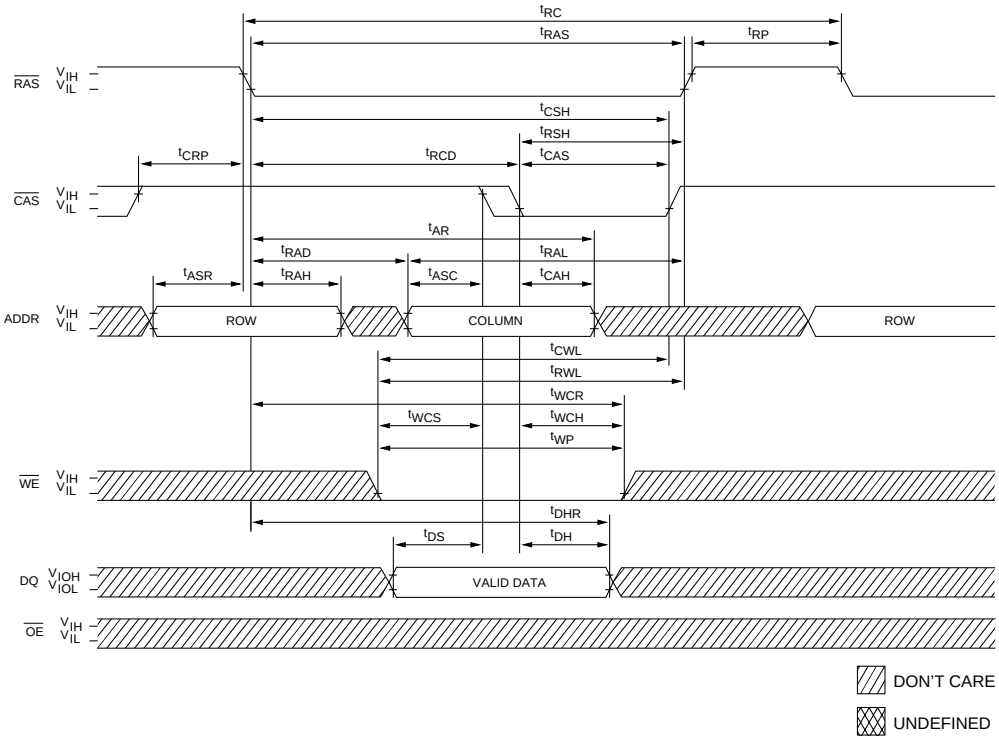
NOTES

1. All voltages referenced to V_{SS}.
2. This parameter is sampled. V_{CC} = 5V ±10%; f = 1 MHz.
3. I_{CC} is dependent on cycle rates.
4. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the outputs open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range is assured.
7. An initial pause of 100µs is required after power-up followed by any eight $\overline{RAS}$ cycles before proper device operation is assured. The eight $\overline{RAS}$ cycle wake-ups should be repeated any time the ^{t}REF refresh requirement is exceeded.
8. AC characteristics assume ^{t}T = 5ns.
9. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
10. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
11. If $\overline{CAS}$ = V_{IH}, data output is High-Z.
12. If $\overline{CAS}$ = V_{IL}, data output may contain data from the last valid READ cycle.
13. Measured with a load equivalent to two TTL gates and 100pF.
14. Assumes that $^{t}RCD < {}^{t}RCD$ (MAX). If ^{t}RCD is greater than the maximum recommended value shown in this table, ^{t}RAC will increase by the amount that ^{t}RCD exceeds the value shown.
15. Assumes that $^{t}RCD \geq {}^{t}RCD$ (MAX).
16. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, Q will be maintained from the previous cycle. To initiate a new cycle and clear the data-out buffer, $\overline{CAS}$ must be pulsed HIGH for ^{t}CPN.
17. Operation within the ^{t}RCD (MAX) limit ensures that ^{t}RAC (MAX) can be met. ^{t}RCD (MAX) is specified as a reference point only; if ^{t}RCD is greater than the specified ^{t}RCD (MAX) limit, then access time is controlled exclusively by ^{t}CAC.
18. Operation within the ^{t}RAD (MAX) limit ensures that ^{t}RAC (MIN) and ^{t}CAC (MIN) can be met. ^{t}RAD (MAX) is specified as a reference point only; if ^{t}RAD is greater than the specified ^{t}RAD (MAX) limit, then access time is controlled exclusively by ^{t}AA.
19. Either ^{t}RCH or ^{t}RRH must be satisfied for a READ cycle.
20. ^{t}OFF (MAX) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
21. ^{t}WCS, ^{t}RWD, ^{t}AWD and ^{t}CWD are not restrictive operating parameters. ^{t}WCS applies to EARLY WRITE cycles. ^{t}RWD, ^{t}AWD and ^{t}CWD apply to READ-MODIFY-WRITE cycles. If $^{t}WCS \geq {}^{t}WCS$ (MIN), the cycle is an EARLY WRITE cycle, and the data output will remain an open circuit throughout the entire cycle. If $^{t}RWD \geq {}^{t}RWD$ (MIN), $^{t}AWD \geq {}^{t}AWD$ (MIN) and $^{t}CWD \geq {}^{t}CWD$ (MIN), the cycle is a READ-MODIFY-WRITE cycle, and the data output will contain data read from the selected cell. If neither of the above conditions is met, the state of data-out is indeterminate. $\overline{OE}$ held HIGH and $\overline{WE}$ taken LOW after $\overline{CAS}$ goes LOW results in a LATE WRITE ($\overline{OE}$-controlled) cycle. ^{t}WCS, ^{t}RWD, ^{t}CWD and ^{t}AWD are not applicable in a LATE WRITE cycle.
22. These parameters are referenced to $\overline{CAS}$ leading edge in EARLY WRITE cycles and $\overline{WE}$ leading edge in LATE WRITE or READ-MODIFY-WRITE cycles.
23. If $\overline{OE}$ is tied permanently LOW, LATE WRITE or READ-MODIFY-WRITE operations are not possible.
24. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, $\overline{WE}$ = LOW and $\overline{OE}$ = HIGH.
25. LATE WRITE and READ-MODIFY-WRITE cycles must have both ^{t}OD and ^{t}OEH met ($\overline{OE}$ HIGH during WRITE cycle) in order to ensure that the output buffers will be open during the WRITE cycle. If $\overline{OE}$ is taken back LOW while $\overline{CAS}$ remains LOW, the DQs will remain open.
26. The DQs open during READ cycles once ^{t}OD or ^{t}OFF occur. If $\overline{CAS}$ goes HIGH before $\overline{OE}$, the DQs will open regardless of the state of $\overline{OE}$. If $\overline{CAS}$ stays LOW while $\overline{OE}$ is brought HIGH, the DQs will open. If $\overline{OE}$ is brought back LOW ($\overline{CAS}$ still LOW), the DQs will provide the previously read data.
27. Extended refresh current is reduced as ^{t}RAS is reduced from its maximum specification during the extended refresh cycle.
28. The 3ns minimum is a parameter guaranteed by design.
29. Column-address changed once each cycle.

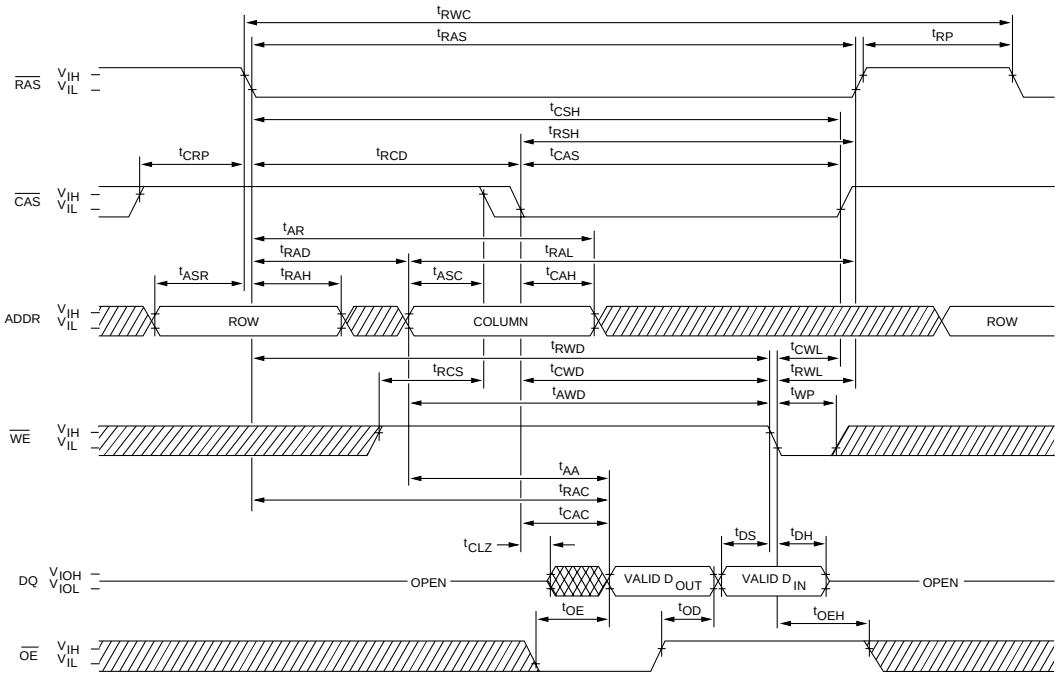
READ CYCLE



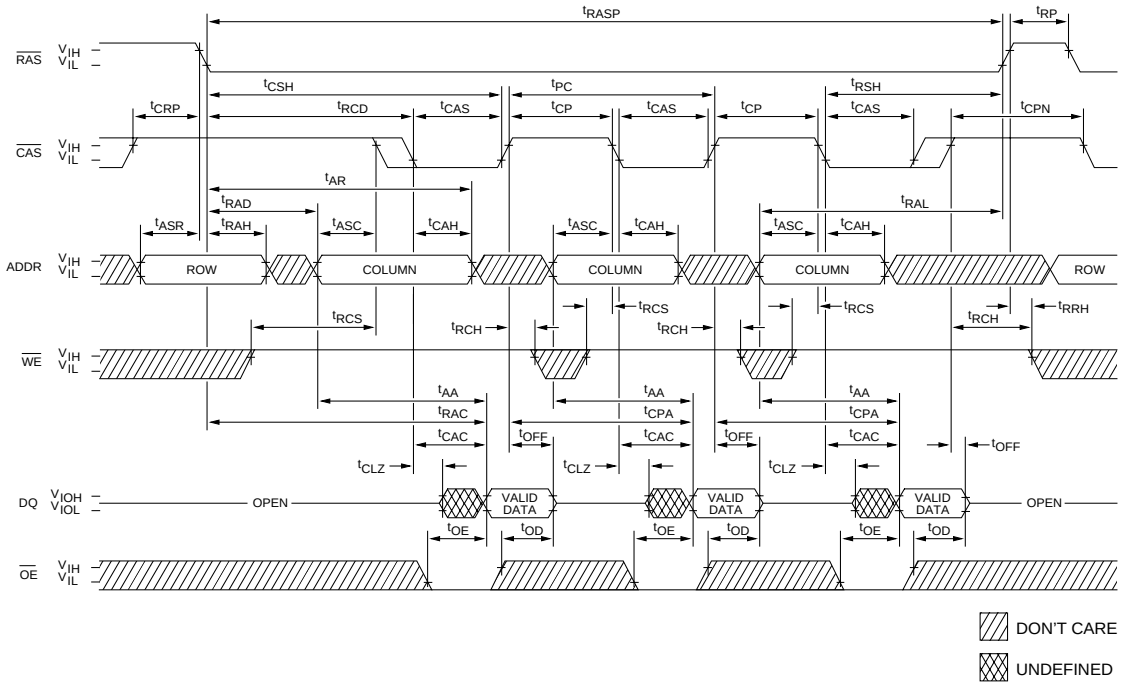
EARLY WRITE CYCLE



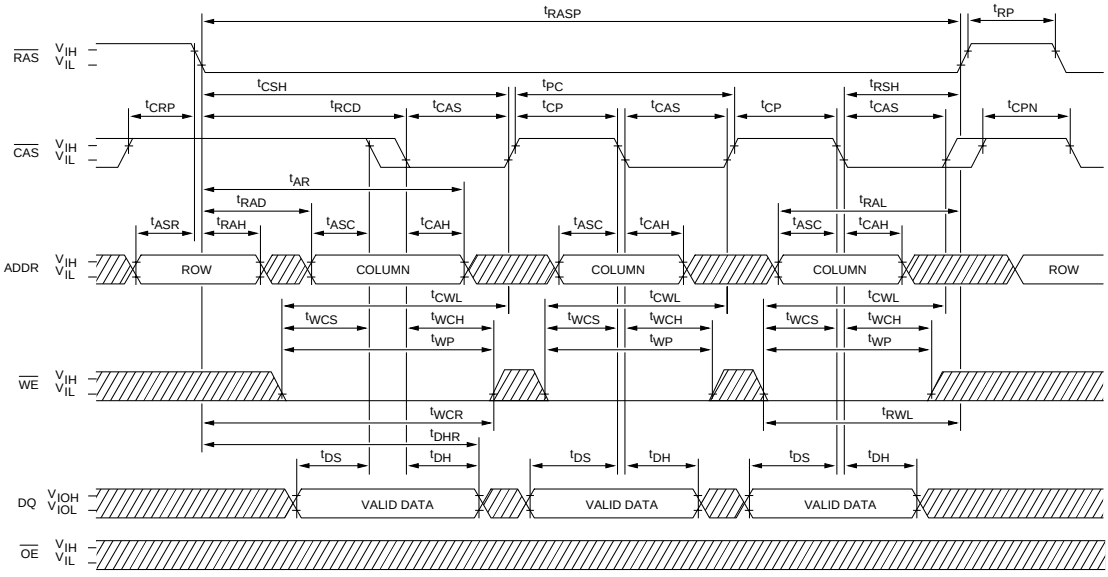
READ WRITE CYCLE
(LATE WRITE and READ-MODIFY-WRITE CYCLES)



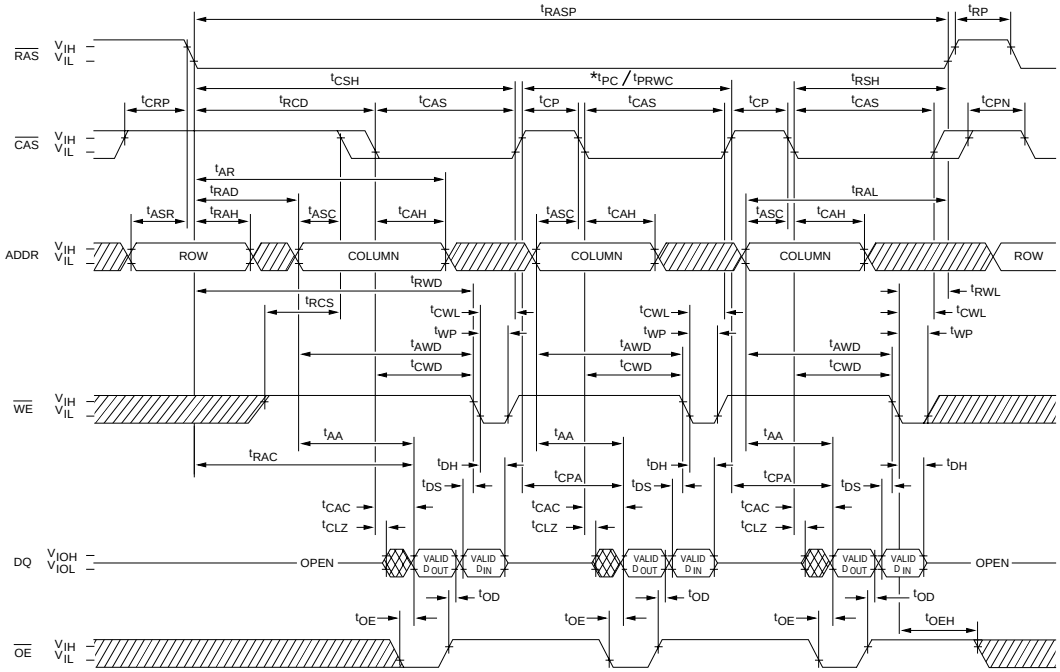
FAST-PAGE-MODE READ CYCLE



FAST-PAGE-MODE EARLY-WRITE CYCLE



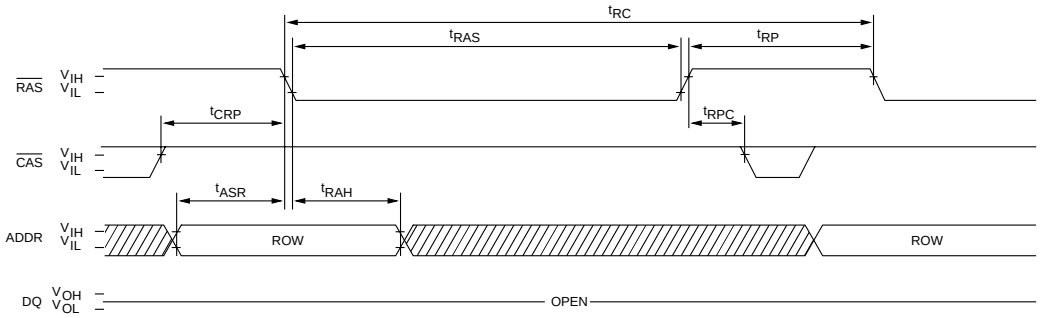
FAST-PAGE-MODE READ-WRITE CYCLE
(LATE WRITE and READ-MODIFY-WRITE CYCLES)



*tPC is for LATE WRITE only.

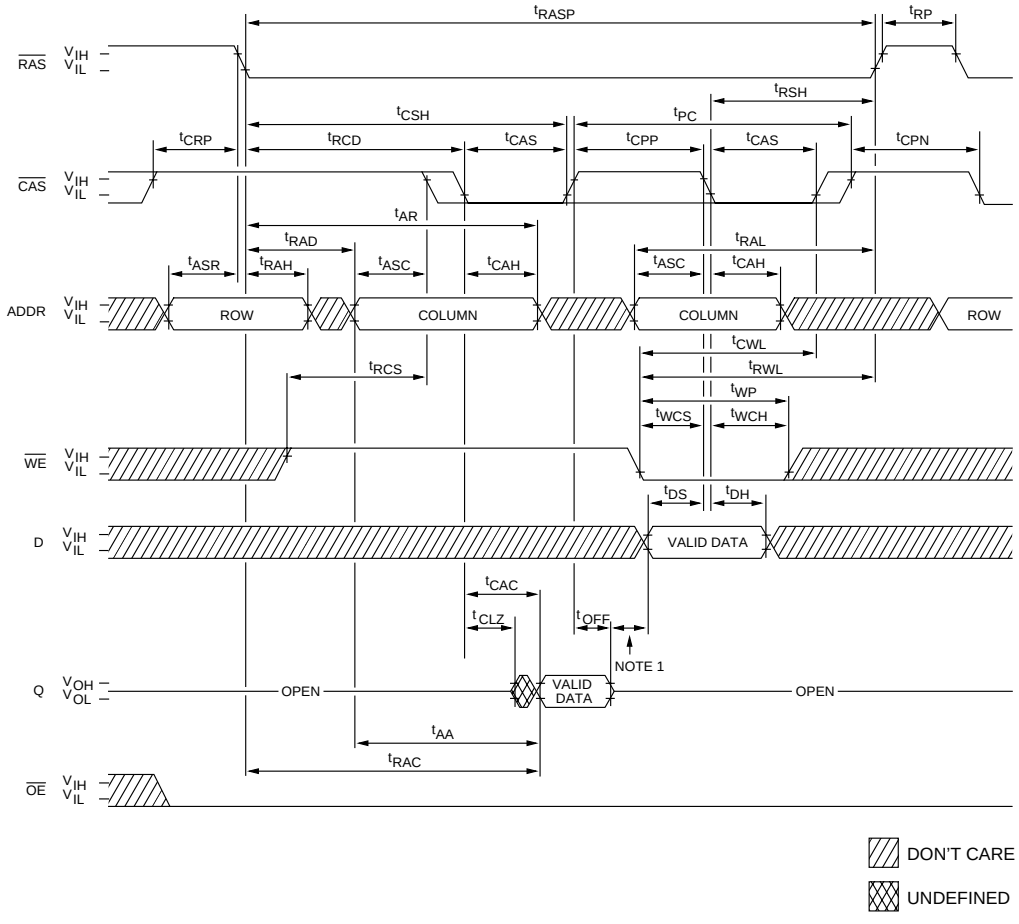
$\overline{RAS}$ ONLY REFRESH CYCLE

(ADDR = A0-A8; $\overline{WE}$ = DON'T CARE)



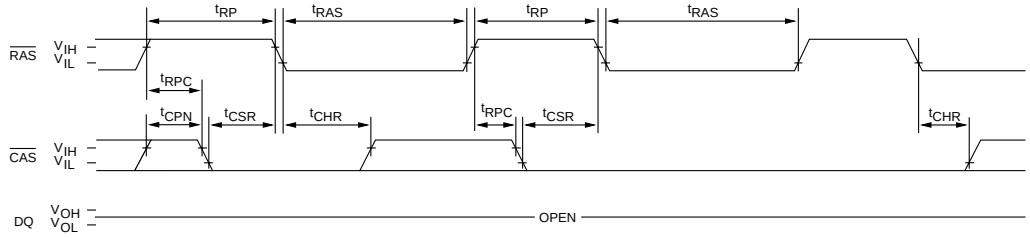
FAST-PAGE-MODE READ-EARLY-WRITE CYCLE

(Pseudo READ-MODIFY-WRITE)

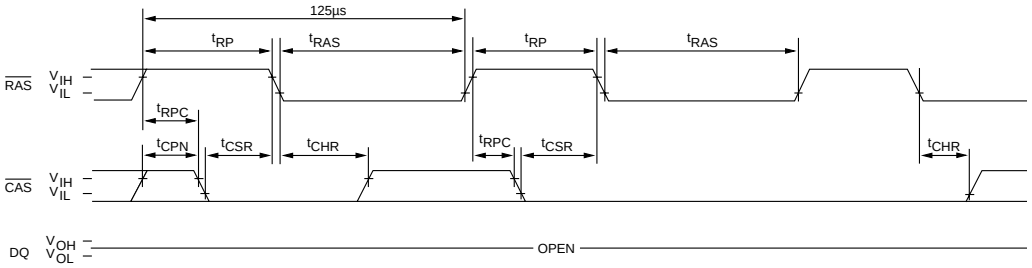


NOTE: 1. Do not drive data prior to tristate: ^{t}CPP(MIN) or ^{t}CP(whichever is greater) + ^{t}DS(MIN) + any guardband between data-out and driving the bus with the new data-in.

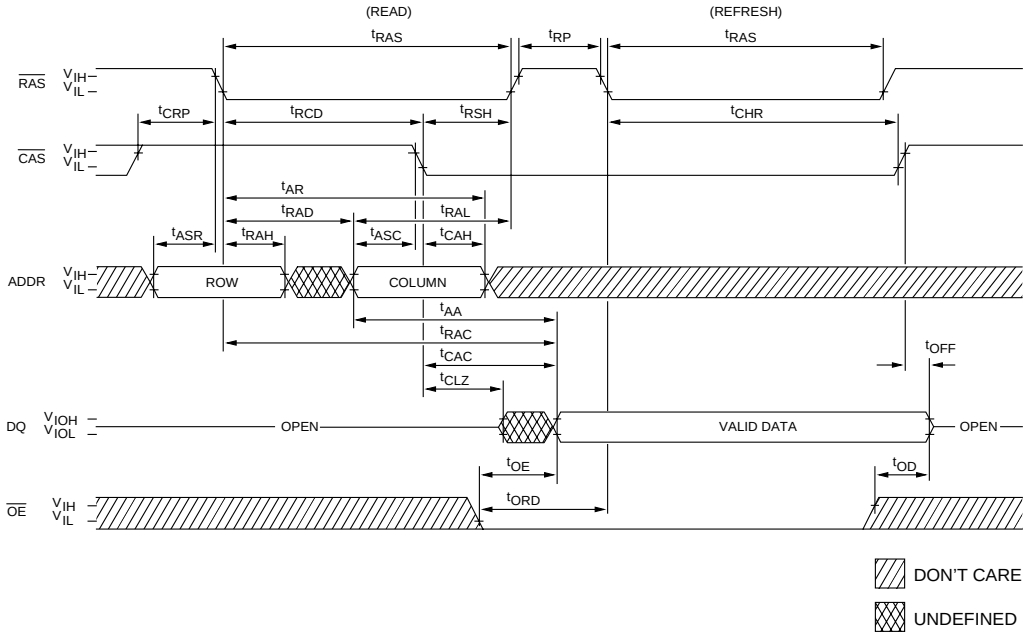
CBR REFRESH CYCLE
(A0-A8, $\overline{WE}$ and $\overline{OE}$ = DON'T CARE)



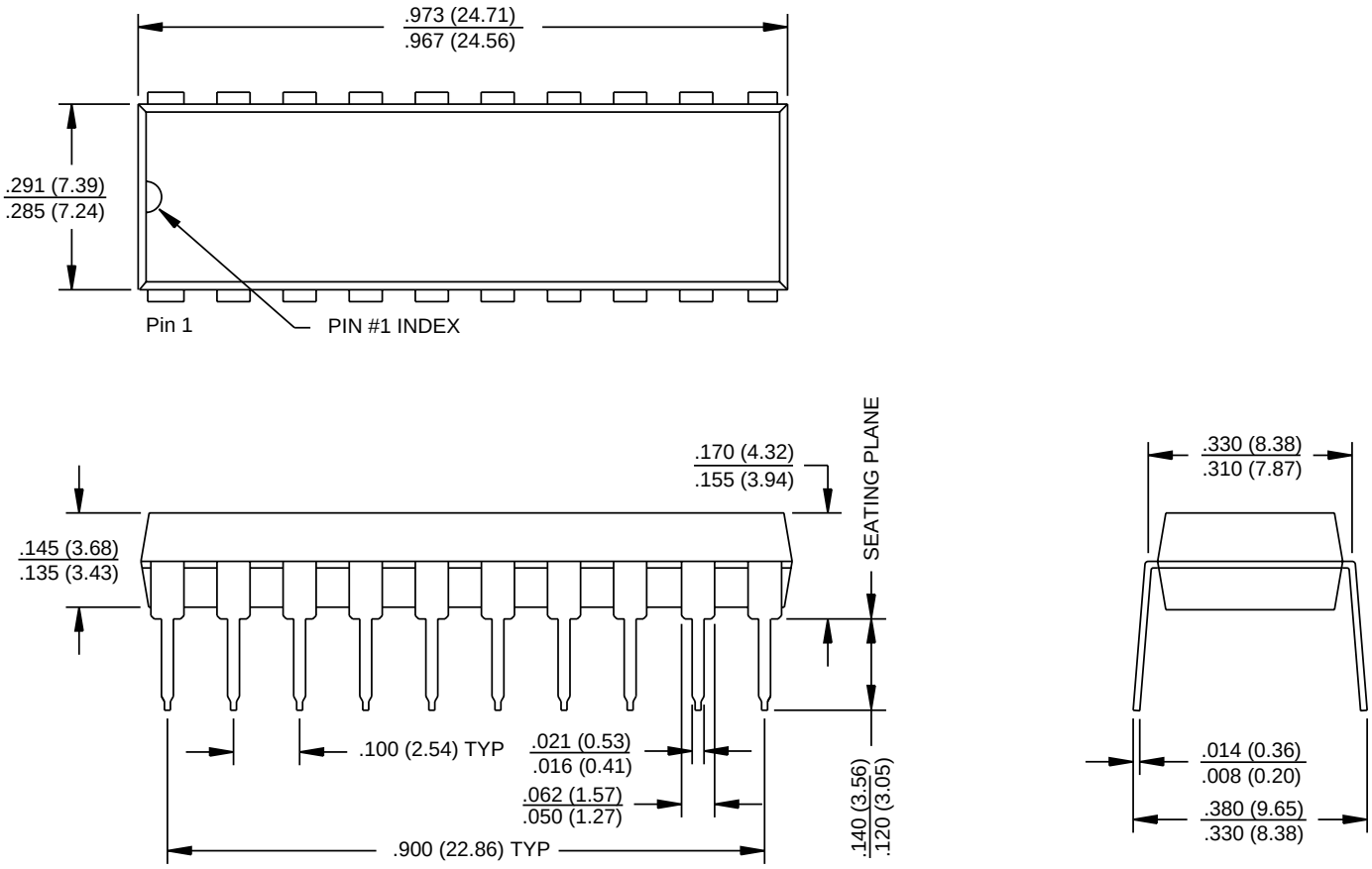
EXTENDED REFRESH CYCLE (MT4C4256 L ONLY)
(A0-A8, $\overline{WE}$ and $\overline{OE}$ = DON'T CARE)



HIDDEN REFRESH CYCLE [24]
($\overline{WE}$ = HIGH; $\overline{OE}$ = LOW)



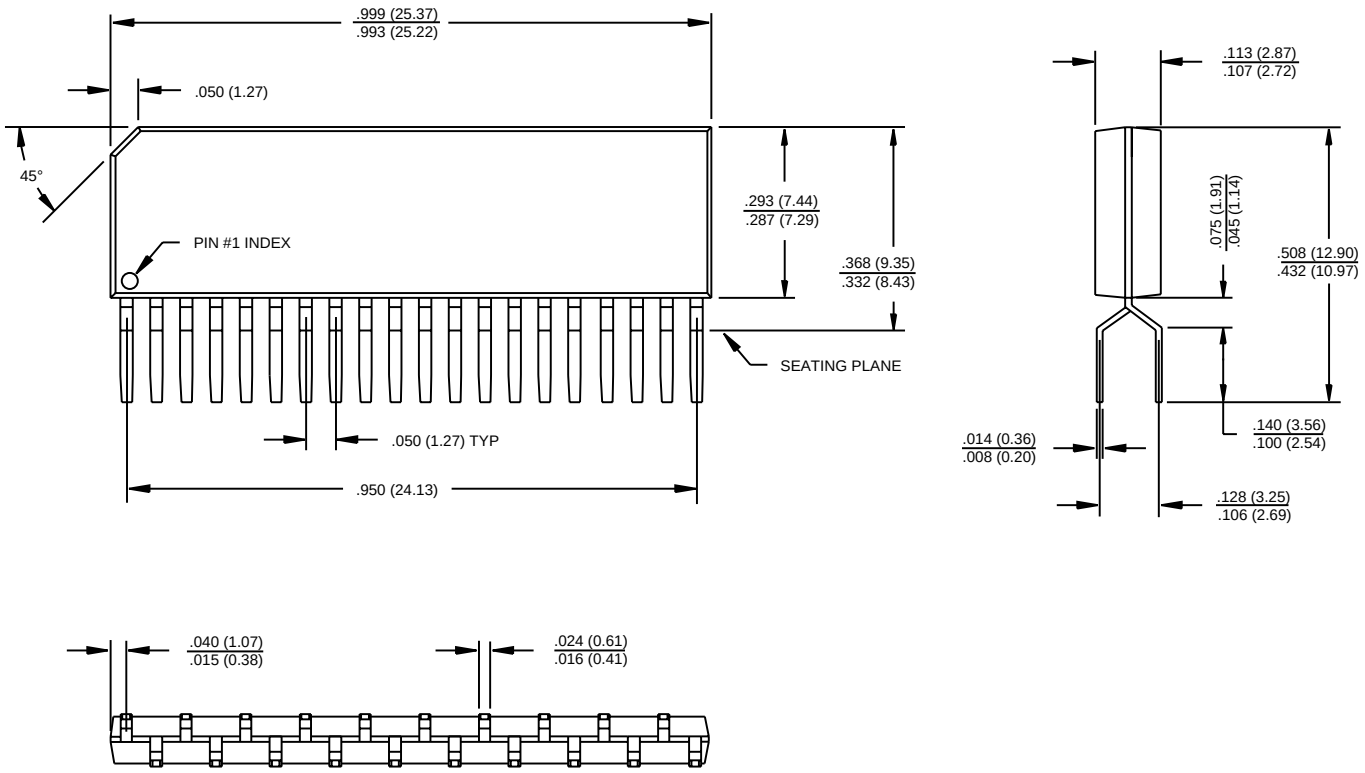
20-PIN PLASTIC DIP (300 mil)



NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

2. Package width and length do not include mold protrusion; allowable mold protrusion is .01" per side.

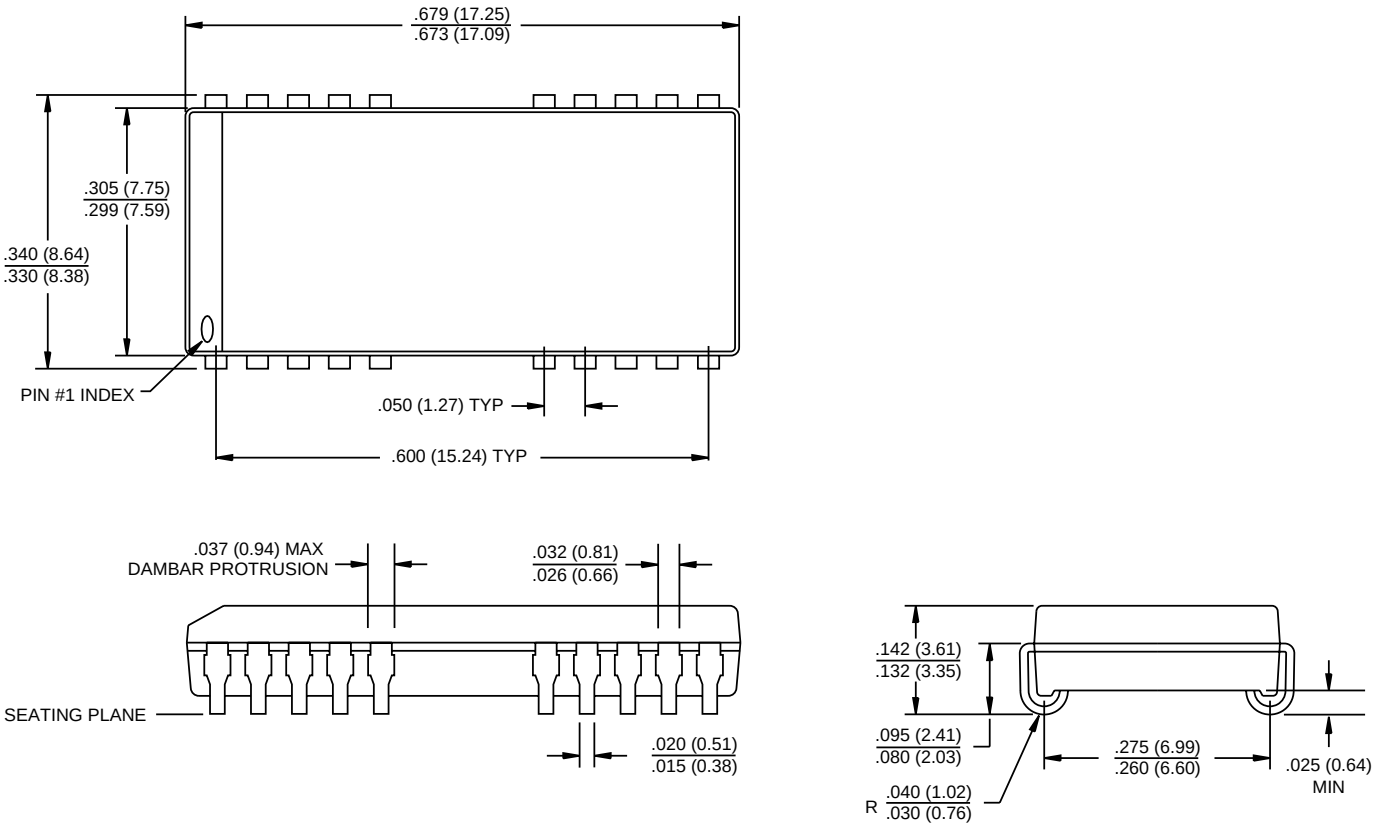
20-PIN PLASTIC ZIP (350 mil)



NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

2. Package width and length do not include mold protrusion; allowable mold protrusion is .01" per side.

20/26-PIN PLASTIC SOJ (300 mil)



NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

2. Package width and length do not include mold protrusion; allowable mold protrusion is .01" per side.

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