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Renesas Technology Corp.
Customer Support Dept.
April 1, 2003

Cautions

Keep safety first in your circuit designs!

1. Renesas Technology Corporation puts the maximum effort into making semiconductor products better and more reliable, but there is always the possibility that trouble may occur with them. Trouble with semiconductors may lead to personal injury, fire or property damage.

Remember to give due consideration to safety when making your circuit designs, with appropriate measures such as (i) placement of substitutive, auxiliary circuits, (ii) use of nonflammable material or (iii) prevention against any malfunction or mishap.

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2SK2225

Silicon N-Channel MOS FET

RENESAS

ADE-208-140 (Z)
1st. Edition
Aug. 1993

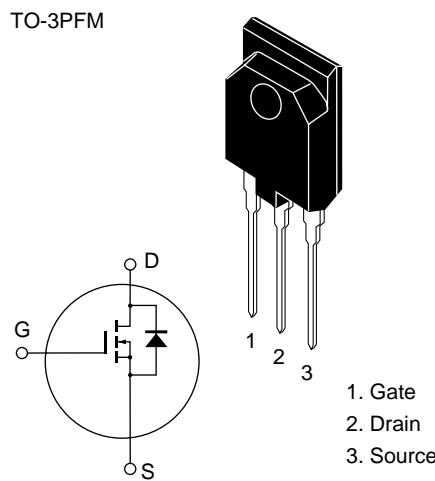
Application

High speed power switching

Features

- High breakdown voltage ($V_{DSS} = 1500$ V)
- High speed switching
- Low drive current
- No Secondary Breakdown
- Suitable for Switching regulator, DC-DC converter

Outline



Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	V _{DSS}	1500	V
Gate to source voltage	V _{GSS}	±20	V
Drain current	I _D	2	A
Drain peak current	I _{D(pulse)} ^{*1}	7	A
Body to drain diode reverse drain current	I _{DR}	2	A
Channel dissipation	Pch ^{*2}	50	W
Channel temperature	T _{ch}	150	°C
Storage temperature	T _{stg}	−55 to +150	°C

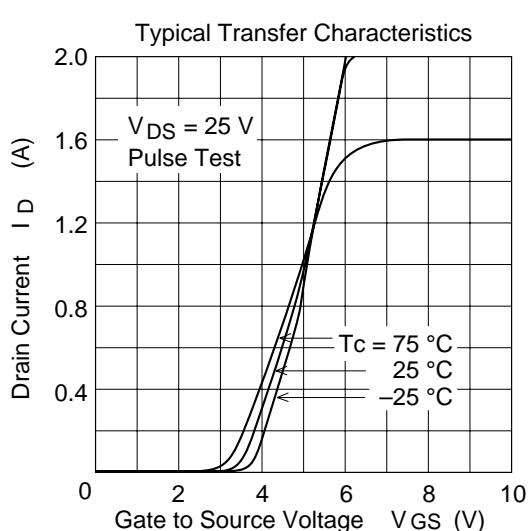
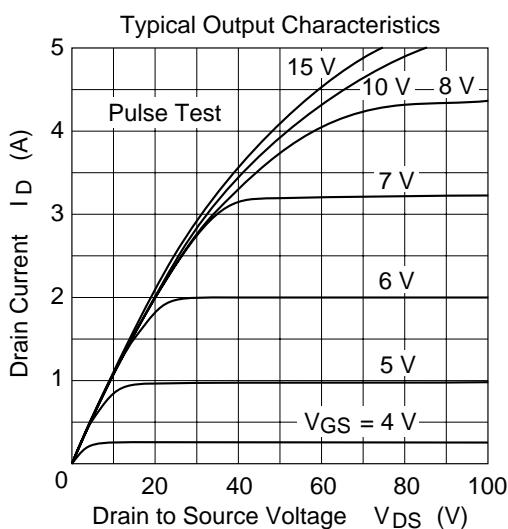
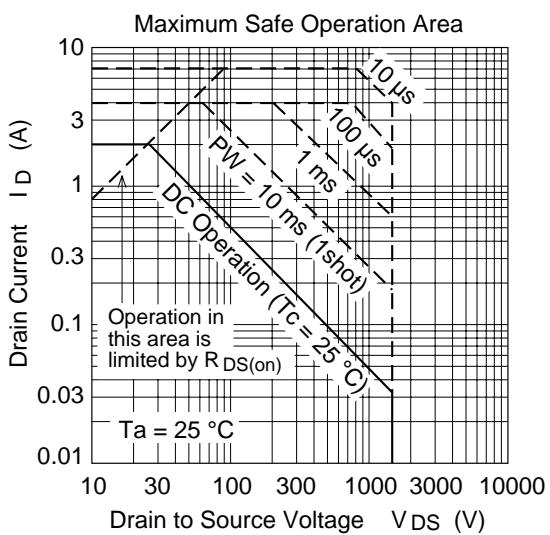
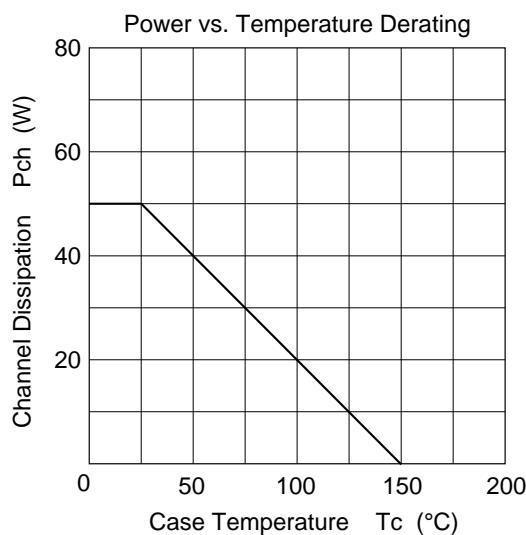
Notes 1. PW 10 µs, duty cycle 1 %

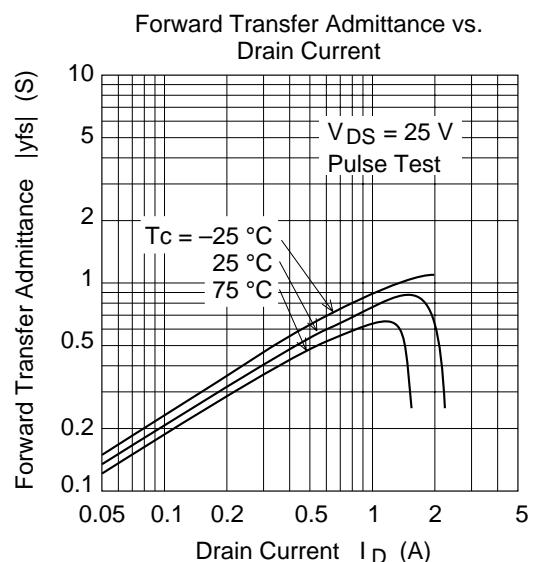
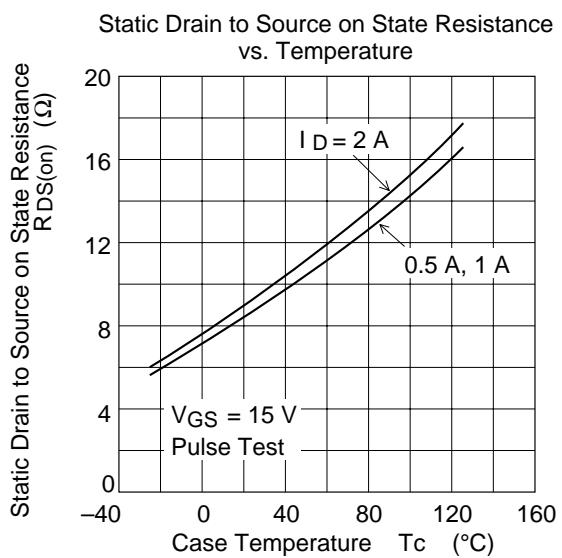
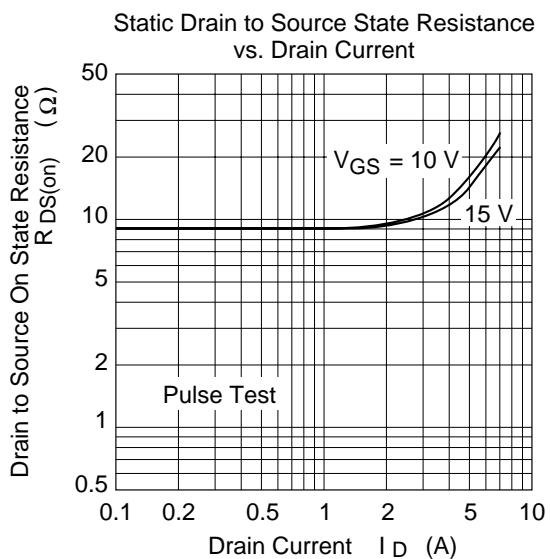
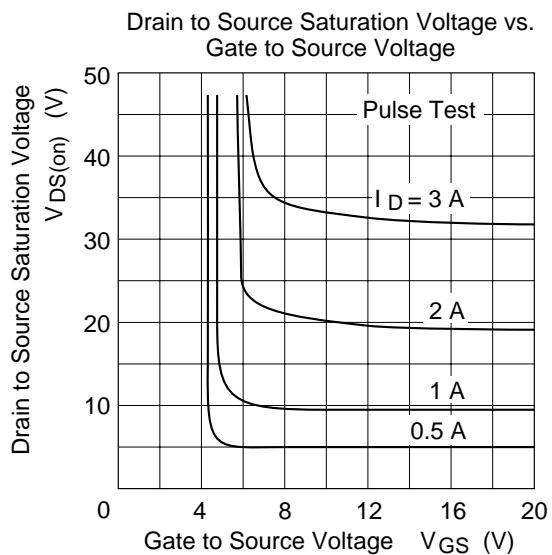
2. Value at T_c = 25 °C

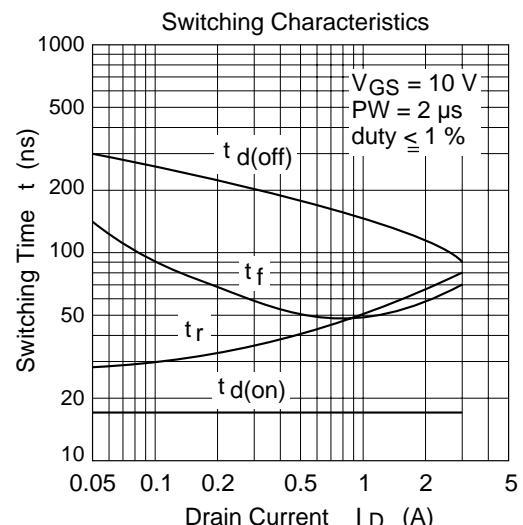
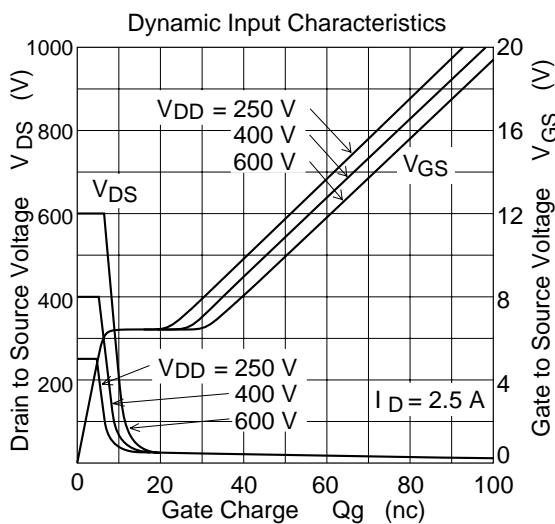
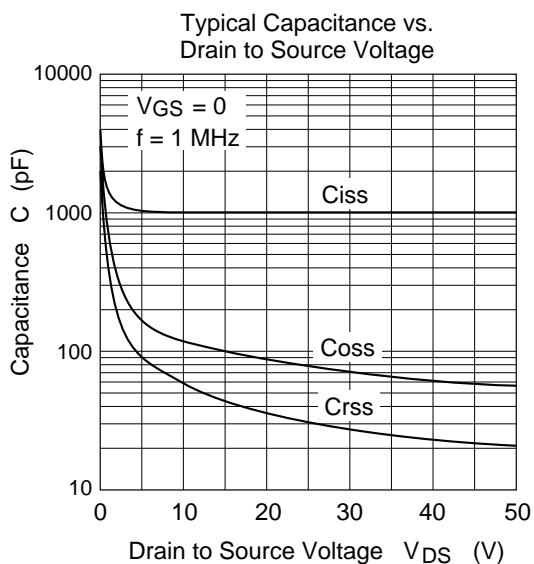
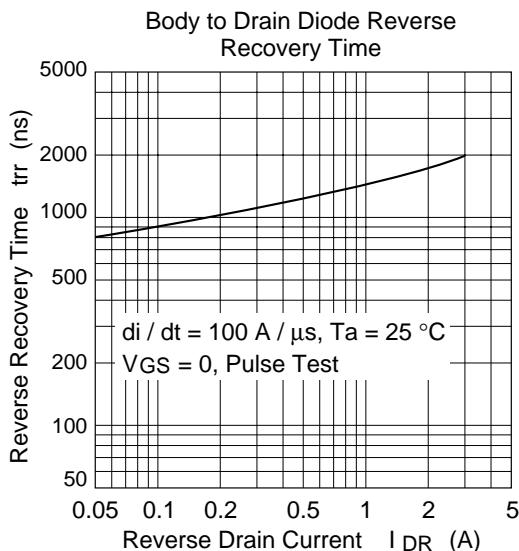
Electrical Characteristics (Ta = 25°C)

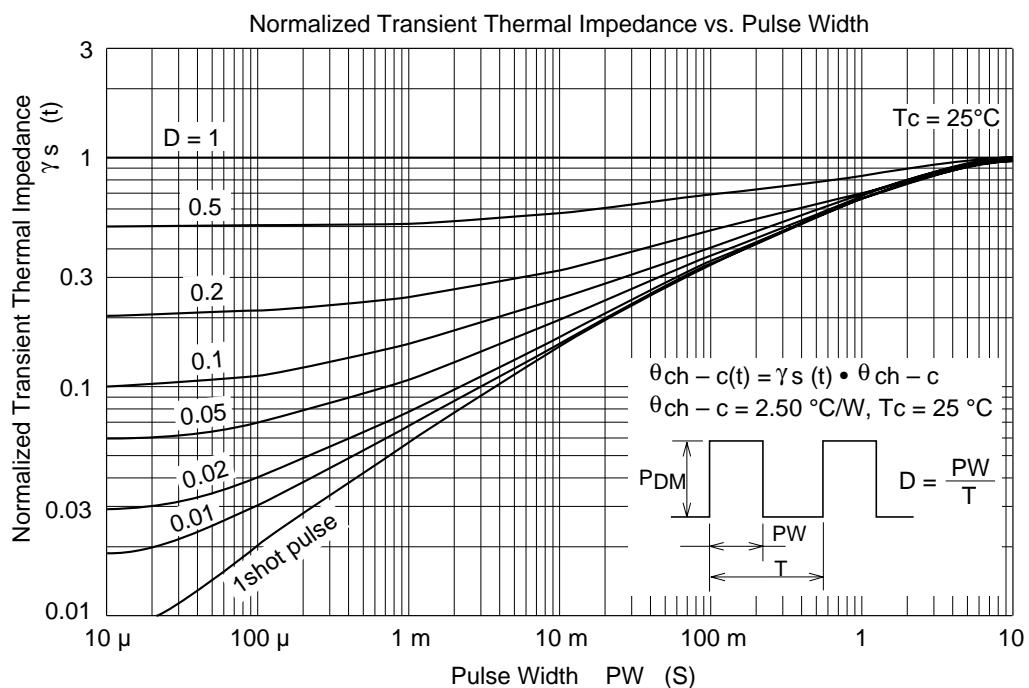
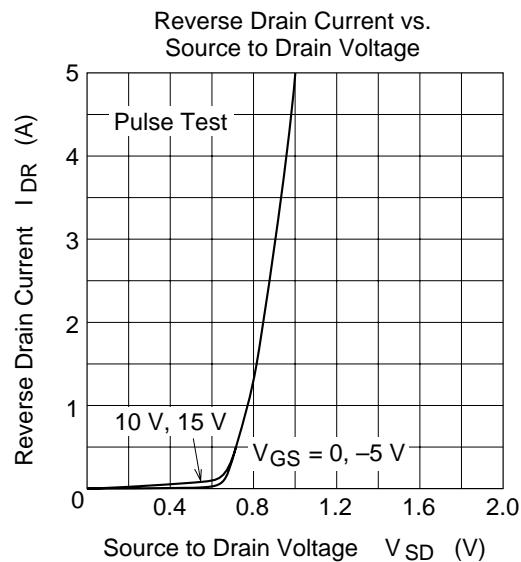
Item	Symbol	Min	Typ	Max	Unit	Test conditions
Drain to source breakdown voltage	V _{(BR)DSS}	1500	—	—	V	I _D = 10 mA, V _{GS} = 0
Gate to source leak current	I _{GSS}	—	—	±1	µA	V _{GS} = ±20 V, V _{DS} = 0
Zero gate voltage drain current	I _{DSS}	—	—	500	µA	V _{DS} = 1200 V, V _{GS} = 0
Gate to source cutoff voltage	V _{GS(off)}	2.0	—	4.0	V	I _D = 1 mA, V _{DS} = 10 V
Static drain to source on state resistance	R _{DS(on)}	—	9	12		I _D = 1 A V _{GS} = 15 V ^{*1}
Forward transfer admittance	y _{fs}	0.45	0.75	—	S	I _D = 1 A V _{DS} = 20 V ^{*1}
Input capacitance	C _{iss}	—	990	—	pF	V _{DS} = 10 V
Output capacitance	C _{oss}	—	125	—	pF	V _{GS} = 0
Reverse transfer capacitance	C _{rss}	—	60	—	pF	f = 1 MHz
Turn-on delay time	t _{d(on)}	—	17	—	ns	I _D = 1 A
Rise time	t _r	—	50	—	ns	V _{GS} = 10 V
Turn-off delay time	t _{d(off)}	—	150	—	ns	R _L = 30
Fall time	t _f	—	50	—	ns	
Body to drain diode forward voltage	V _{DF}	—	0.9	—	V	I _F = 2 A, V _{GS} = 0
Body to drain diode reverse recovery time	t _{rr}	—	1750	—	ns	I _F = 20 A, V _{GS} = 0, dI _F / dt = 100 A / µs

Note 1. Pulse Test

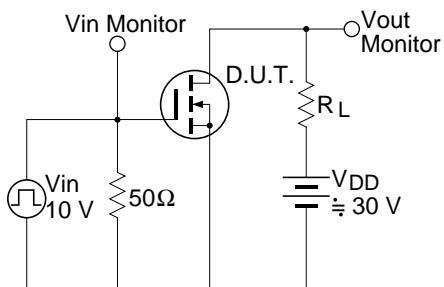




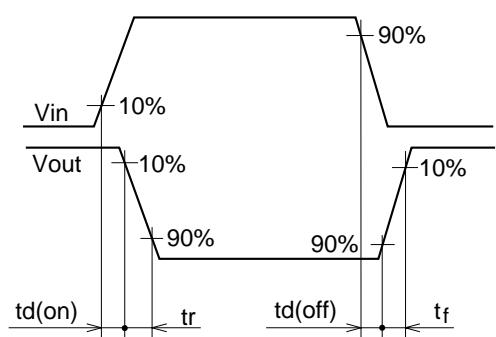




Switching Time Test Circuit

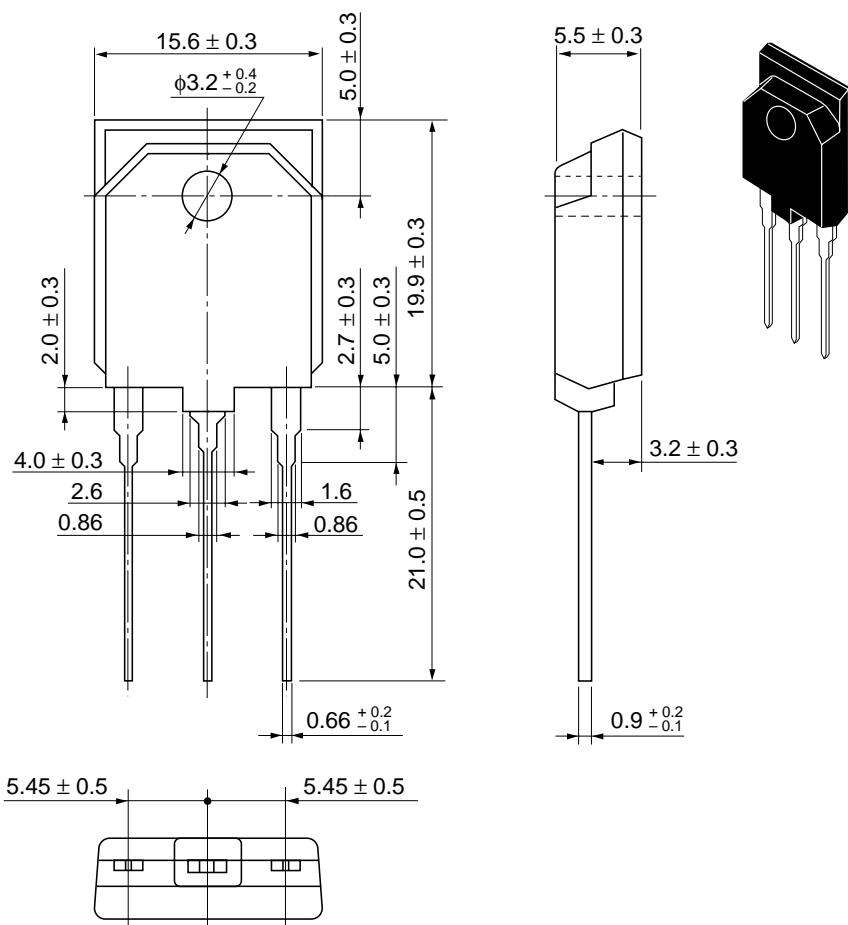


Waveform



Package Dimensions

As of January, 2001
Unit: mm



Hitachi Code	TO-3PFM
JEDEC	—
EIAJ	—
Mass (reference value)	5.2 g

Cautions

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HITACHI

Hitachi, Ltd.

Semiconductor & Integrated Circuits.

Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100-0004, Japan

Tel: Tokyo (03) 3270-2111 Fax: (03) 3270-5109

URL	NorthAmerica	:	http://semiconductor.hitachi.com/
	Europe	:	http://www.hitachi-eu.com/hel/ecg
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For further information write to:

Hitachi Semiconductor (America) Inc.	Hitachi Europe GmbH
179 East Tasman Drive, San Jose, CA 95134	Electronic Components Group
Tel: <1> (408) 433-1990	Dornacher Straße 3
Fax: <1>(408) 433-0223	D-85622 Feldkirchen, Munich
	Germany
	Tel: <49> (89) 9 9180-0
	Fax: <49> (89) 9 29 30 00

Hitachi Europe Ltd.
Electronic Components Group.
Whitebrook Park
Lower Cookham Road
Maidenhead
Berkshire SL6 8YA, United Kingdom
Tel: <44> (1628) 585000
Fax: <44> (1628) 585160

Hitachi Asia Ltd.
Hitachi Tower
16 Collyer Quay #20-00,
Singapore 049318
Tel : <65>-538-6533/538-8577
Fax : <65>-538-6933/538-3877
URL : http://www.hitachi.com.sg

Hitachi Asia Ltd.
(Taipei Branch Office)
4/F, No. 167, Tun Hwa North Road,
Hung-Kuo Building,
Taipei (105), Taiwan
Tel : <886>-(2)-2718-3666
Fax : <886>-(2)-2718-8180
Telex : 23222 HAS-TP
URL : http://www.hitachi.com.tw

Hitachi Asia (Hong Kong) Ltd.
Group III (Electronic Components)
7/F., North Tower,
World Finance Centre,
Harbour City, Canton Road
Tsim Sha Tsui, Kowloon,
Hong Kong
Tel : <852>-(2)-735-9218
Fax : <852>-(2)-730-0281
URL : http://www.hitachi.com.hk

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