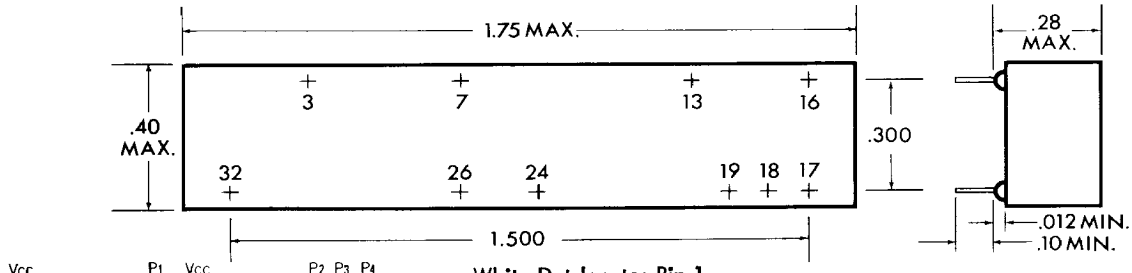
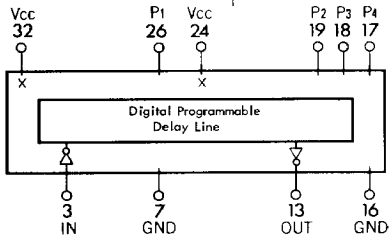
TTL DIGITAL PROGRAMMABLE DELAY LINES

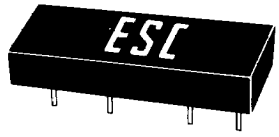
32 PIN PACKAGE

4 BIT

SERIES PTT4







Model No.	Zero Step Delay (ns)	Maximum Delay (ns) (nom)	Delay per step (ns)
PTT4-1	15 ± 2	30	1 ± .5
PTT4-2		45	2 ± .5
PTT4-3		60	3 ± .6
PTT4-4		75	4 ± .8
PTT4-5		90	5 ± 1
PTT4-6		105	6 ± 1
PTT4-7		120	7 ± 1
PTT4-8		135	8 ± 1
PTT4-9		150	9 ± 1
PTT4-10		165	10 ± 1

TYPICAL TRUTH TABLE EXAMPLE

Data Select Pins / Model Number																	
	P4-17	L	L	L	L	L	L	L	L	H	H	H	H	H	H	H	H
	P3-18	L	L	L	L	H	H	H	H	L	L	L	L	H	H	H	H
	P2-19	L	L	H	H	L	L	H	H	L	L	H	H	L	L	H	H
	P1-26	L	H	L	H	L	H	L	H	L	H	L	H	L	H	L	H
PTT4-1	—	15	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15

SPECIFICATIONS:

- Zero step delay is measured from the input pin #3
- All programmable delays after step zero are referenced to step zero
- Programmable delay tolerances: ± 2ns or 5% whichever is greater
- Rise Time: 4ns max
- Minimum Pulse Width: 40% of Total Delay
- Maximum Duty Cycle: 50%
- * Operating temp. range: 0°C to + 70°C
- Temp. coeff. of delay: 1.0ns + 500ppm/°C
- Vol: .4V max
- Voh: 2.4Vmin
- Vcc: 5VDC ± 0.25V
- Icc: 170mA max
- Terminals: Electro tin plated alloy 42 .020w x .010th

*Available for -55°C to + 125°C operation, specify PTTC4 series. The height will change to .360.

TEST CONDITIONS:

- Vcc=5.0VDC, Temp. 25°C
- Time delay measured at the 1.5 volt level of the leading edge
- Rise time measured from .75V to 2.4 volts
- Output loaded with 15pf
- Input pulse width: 3 x max time delay
- Pulse amplitude: 3.0 volts
- Pulse spacing: 1000ns

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