EFM32 Leopard Gecko
EFM32LG Errata

This document contains information on the errata of EFM32LG. The latest available revision of this device is revision E.

For errata on older revisions, please refer to the errata history section for the device. The device revision is typically the first letter on the line immediately under the part number on the package marking. This is typically the second or third line.

Errata effective date: April 10th, 2017.

1. Active Errata Summary

These tables lists all known errata for the EFM32LG and all unresolved errata in revision E of the EFM32LG.

Table 1.1. Errata History Overview

Designator	Title/Problem	Exists on Revision:			
		B	C	D	E
ADC_E116	Offset in ADC Temperature Sensor Calibration Data	—	—	X	—
ADC_E117	TIMEBASE not wide enough	X	X	X	—
AES_E101	BYTEORDER Does Not Work in Combination with DATA-START/XORSTART	X	X	X	—
AES_E102	AES_STATUS_RUNNING Set One Cycle Late With BYTEORDER Set	X	X	X	—
BU_E101	Backup Power Increased Power Consumtion	X	—	—	—
BU_E102	EM4 GPIO Retention in Backup Mode	X	—	—	—
BU_E104	EM4 with Backup BODs	X	—	—	—
BU_E105	LFXO Missing Cycles During IOVDD Ramping	X	X	X	X
BU_E106	Current Leakage in Backup Mode	—	—	X	—
BURTC_E101	BURTC LPMODE Entry	X	X	X	—
BURTC_E102	BURTC_CNT Read Error	X	X	X	—
CMU_E108	LFxCLKEN Write	X	—	—	—
CMU_E110	LFXO Phase Shift	X	—	—	—
CMU_E111	LFXO Configuration Incorrect	X	X	—	—
CMU_E112	LFXO Boost Buffer Current Setting	—	—	X	—
CMU_E113	LFXO Startup at High Temperature	—	—	X	—
CMU_E114	Device Not Waking Up From EM2 When Using Prescaled Non-HFRCO Oscillator as HFCLK	X	X	X	X
CUR_E103	Increased EM2 Current	—	X	—	—
CUR_E104	Increased Current on AVDD2 (USB)	X	X	—	—
CUR_E105	Increased Current on AVDD2 (No USB)	X	X	—	—
DAC_E109	DAC Output Drift Over Lifetime	X	X	X	X
DI_E101	Flash Page Size	X	X	X	—
DMA_E101	EM2 with WFE and DMA	X	X	X	—
EBI_E101	EBI Masking Functionality	X	—	—	—
EBI_E102	EBI Access Fails	X	—	—	—
EBI_E103	Page Mode Read in D16A16ALE Mode	X	X	X	—
EMU_E105	Debug Unavailable During DMA Processing from EM2	X	—	—	—
EMU_E107	Interrupts During EM2 Entry	X	X	X	X
EMU_E110	Potential Hard Fault when Exiting EM2	—	—	—	X
ETM_E101	ETM Trace Clock	X	—	—	—

Designator	Title/Problem	Exists on Revision:			
		B	C	D	E
GPIO_E101	GPIO Wakeup from EM4	X	—	—	—
LES_E101	LESENSE and Schmitt Trigger	X	—	—	—
LES_E102	LESENSE and DAC CH1 Configuration	X	—	—	—
LES_E103	AUXHFRCO and LESENSE	—	—	X	—
OPA_E101	OPAMP 2 Startup Rampup	X	—	—	—
PCNT_E102	PCNT Pulse Width Filtering Does Not Work	X	X	X	X
PRS_E101	Edge Detect on GPIO/ACMP	X	X	X	—
RMU_E101	POR Calibration Initialization Issue	—	—	—	X
TIMER_E103	Capture/Compare Output is Unreliable with RSSCOIST Enabled	X	X	X	X
USART_E112	USART AUTOTX Continues to Transmit Even With Full RX Buffer	X	X	X	—
USB_E101	USB DMA Transfers with Prescaled HFCLK	X	—	—	—
USB_E102	USB Datalines	X	—	—	—
USB_E103	HNP Sequence Fails if A-Device Connects After 3.4 ms	X	X	X	X
USB_E104	USB A-Device Delays the HNP Switch Back Process	X	X	X	X
USB_E105	B-Device as Host Driving K-J Pairs During Reset	X	X	X	X
USB_E106	USB Interrupts	X	—	—	—
USB_E107	Entry to EM4 Causes Temporary Leakage from VREGO	X	X	—	—
USB_E108	Floating DM/DP Pins Cause Leakage when USB is Disabled	X	X	—	—
USB_E109	Missing USB_GINTSTS.SESSREQINT Interrupt with USB_PCGCCTL.STOPPCLK = 1	X	X	X	X
USB_E110	Unexpected USB_HCx_INT.CHHLTD Interrupt	X	X	X	X

Table 1.2. Active Errata Status Summary

Errata #	Designator	Title/Problem	Workaround Exists	Affected Revision	Resolution
1	BU_E105	LFXO Missing Cycles During IOVDD Ramping	Yes	E	—
2	CMU_E114	Device Not Waking Up From EM2 When Using Prescaled Non-HFRCO Oscillator as HFCLK	Yes	E	—
3	DAC_E109	DAC Output Drift Over Lifetime	Yes	E	—
4	EMU_E107	Interrupts During EM2 Entry	Yes	E	—
5	EMU_E110	Potential Hard Fault when Exiting EM2	Yes	E	E, targeted for Q4 2017
6	PCNT_E102	PCNT Pulse Width Filtering Does Not Work	No	E	—

Errata #	Designator	Title/Problem	Workaround Exists	Affected Revision	Resolution
7	RMU_E101	POR Calibration Initialization Issue	Yes	E	E devices (date code ≥ 1539 and PROD_REV ≥ 0x96)
8	TIMER_E103	Capture/Compare Output is Unreliable with RSSCO-IST Enabled	No	E	—
9	USB_E103	HNP Sequence Fails if A-Device Connects After 3.4 ms	No	E	—
10	USB_E104	USB A-Device Delays the HNP Switch Back Process	No	E	—
11	USB_E105	B-Device as Host Driving K-J Pairs During Reset	No	E	—
12	USB_E109	Missing USB_GINTSTS.SESSREQINT Interrupt with USB_PCGCCTL.STOPPCLK = 1	Yes	E	—
13	USB_E110	Unexpected USB_HCx_INT.CHHLTD Interrupt	Yes	E	—

2. Detailed Errata Descriptions

2.1 BU_E105 — LFXO Missing Cycles During IOVDD Ramping

Description of Errata
LFXO missing cycles during IOVDD ramping when used in combination with Backup mode.
Affected Conditions / Impacts
When IOVDD is ramped, the dc-level of the XTAL signal changes, resulting in missed LFXO cycles and possible glitches on the LFXO clock.
Workaround
Set PRESC in BURTC_CTRL to greater then 0 when ramping IOVDD in combination with Backup mode to avoid glitches on the LFXO clock.
Resolution
There is currently no resolution for this issue.

2.2 CMU_E114 — Device Not Waking Up From EM2 When Using Prescaled Non-HFRCO Oscillator as HFCLK

Description of Errata
Device not waking up from EM2 when using prescaled non-HFRCO oscillator as HFCLK.
Affected Conditions / Impacts
If the device is running from any prescaled oscillator other than HFRCO as HFCLK and HFRCO is disabled, the device will not wake up from EM2.
Workaround
Before entering EM2, clear CMU_CTRL_HFCLKDIV. Alternatively, enable HFRCO by setting CMU_OSCENCMD_HFRCOEN and wait until CMU_STATUS_HFRCORDY is set.
Resolution
There is currently no resolution for this issue.

2.3 DAC_E109 — DAC Output Drift Over Lifetime

Description of Errata
The voltage output of the DAC might drift over time.
Affected Conditions / Impacts
When the device is powered and the DAC is disabled, stress on an internal circuit node can cause the output voltage of the DAC to drift over time, and in some cases may violate the $V_{DACOFFSET}$ specification. If the DAC is always enabled while the device is powered, this condition cannot occur.
Workaround
Both in the startup initialization code and prior to disabling the DAC in application code, set the OPAnSHORT bit in DACn_OPACTRL to a '1' for the corresponding DAC(s) used by the application. This will prevent the output voltage drift over time effect.
Resolution
There is currently no resolution for this issue.

2.4 EMU_E107 — Interrupts During EM2 Entry

Description of Errata
An interrupt from a peripheral running from the high frequency clock that is received during EM2 entry will cause the EMU to ignore the SLEEPDEEP flag.
Affected Conditions / Impacts
During EM2 entry, the high frequency clocks that are disabled during EM2 will run for some clock cycles after WFI isissued to allow safe shutdown of the peripherals. If an enabled interrupt is requested from one of these non-EM2 peripherals during this shutdown period, the attempt to enter EM2 will fail, and the device will enter EM1 instead. As a result, the pending interrupt will immediately wake the device to EM0.
Workaround
Before entering EM2, disable all high frequency peripheral interrupts in the core.
Resolution
There is currently no resolution for this issue.

2.5 EMU_E110 — Potential Hard Fault when Exiting EM2

Description of Errata
The flash is powered down in EM2 to save power. Some control registers in the flash can rarely enter an invalid state upon power-on, causing the first read of flash to be incorrect. If this occurs after exiting EM2, the core attempts to fetch the interrupt address, but the value will be incorrect and may be invalid. In the case of an invalid value, the core will then jump to the hard fault handler for attempting to execute code from an invalid address. All subsequent reads from the flash are unaffected, and it is only the first flash read after exit from EM2 that is potentially erroneous.
Affected Conditions / Impacts
When exiting EM2, some devices may intermittently execute code incorrectly or enter the hard fault handler instead of entering the expected ISR associated with the wake source.
Workaround
To workaround this issue, move the interrupt vector table and interrupt service routines for EM2 wake sources to RAM and perform a dummy read of the flash in the ISR. Additional information on the workaround and examples provided is available from the following Knowledge Base article URL: http://community.silabs.com/t5/32-bit-MCU-Knowledge-Base/EMU-E110-Potential-Hard-Fault-when-Exiting-EM2/ta-p/192479 This workaround will be included in v5.3.0 or later of the Gecko SDK, which will be included in the v1.1.0 Gecko SDK Suite.
Resolution
This issue will be resolved in future devices, but the date code of the fixed devices is not yet available. These devices are currently targeted to be available in Q4 2017. The Knowledge Base article will be updated as soon as the specific date code information is available.

2.6 PCNT_E102 — PCNT Pulse Width Filtering Does Not Work

Description of Errata
PCNT pulse width filtering does not work.
Affected Conditions / Impacts
The PCNT pulse width filter does not work as intended.
Workaround
Do not use the pulse width filter, i.e. ensure FILT = 0 in PCNTn_CTRL.
Resolution
There is currently no resolution for this issue.

2.7 RMU_E101 — POR Calibration Initialization Issue

Description of Errata
Upon initial power-on, some devices may not be able to access flash memory above the 4 kB boundary, or some calibration registers on some devices may not be set to their factory calibration values.
Affected Conditions / Impacts
The list of affected devices can be found in the Knowledge Base (KB) article listed under Fix/Workaround. Some devices are sensitive to the power supply ramp during initial power-on. Specific ramp profiles on these devices can cause an intermittent issue resulting in one of two failure modes (A) or (B): A. Flash memory above the 4 kB boundary is inaccessible. Reads of the flash will return zeros. Write attempts will return an invalid address error code in the MSC_STATUS register. Code execution will behave as though the memory above 4 kB was filled with zeros until the device resets itself. B. Some parts of the calibration initialization process do not complete successfully. On USB devices, the USB voltage regulator does not get calibrated. Specific peripheral registers that may not be calibrated are as follows (not all registers apply to all devices): ADC0_CAL, IDAC_CAL, DAC0_CAL, DAC0_BIASPROG, DAC0_OPACTRL, and DAC0_OPAOFFSET. A SYSRESETREQ reset will clear either failure mode, and the device will behave normally until the next power-on event.
Workaround
Additional information including a software workaround is available from the following KB article URL: http://community.silabs.com/t5/32-bit-MCU-Knowledge-Base/POR-calibration-initialization-issue/ta-p/154716
Resolution
Devices with a date code and PROD_REV greater than or equal to 1539 and 0x96 respectively will not have this issue.

2.8 TIMER_E103 — Capture/Compare Output is Unreliable with RSSCOIST Enabled

Description of Errata
The TIMER capture/compare output is unreliable when RSSCOIST is enabled and the clock is prescaled.
Affected Conditions / Impacts
When RSSCOIST is set and PRESC > 0 in TIMERn_CTRL, the capture/compare output value is not reliable.
Workaround
Do not use a prescaled clock, i.e. ensure PRESC = 0 in TIMERn_CTRL when RSSCOIST is enabled.
Resolution
There is currently no resolution for this issue.

2.9 USB_E103 — HNP Sequence Fails if A-Device Connects After 3.4 ms

Description of Errata
HNP Sequence fails if A-Device connects after 3.4 ms.
Affected Conditions / Impacts
The B-Device core only waits for up to 3.4 ms before signalling HNP fail and reverting back to Peripheral mode. Therefore, the HNP sequence fails if the A-Device connects after 3.4 ms.
Workaround
No known workaround.
Resolution
There is currently no resolution for this issue.

2.10 USB_E104 — USB A-Device Delays the HNP Switch Back Process

Description of Errata
The D+ line disconnects after 200 ms, delaying the HNP switch back process.
Affected Conditions / Impacts
The A-Device core delays the HNP switch back process. As per the USB-OTG 2.0 specification, the B-Device on the otherside of the USB pipe either should wait for disconnect from the A-Device or should switch to Peripheral mode and wait for the A-Device to issue a USB reset. Hence, there is no significant impact on actual operation.
Workaround
No known workaround.
Resolution
There is currently no resolution for this issue.

2.11 USB_E105 — B-Device as Host Driving K-J Pairs During Reset

Description of Errata
The A-Device misinterprets the K-J pairs as Suspend after switching to High Speed mode.
Affected Conditions / Impacts
If the B-Device as Host on the other side of the USB pipe drives K-J pairs for more than 200 ms during USB reset, the A-Device core exits peripheral state, causing the HNP process to fail. There is no significant impact since normally the host drives USB reset for a shorter time than 200 ms.
Workaround
No known workaround.
Resolution
There is currently no resolution for this issue.

2.12 USB_E109 — Missing USB_GINTSTS.SESSREQINT Interrupt with USB_PCGCCTL.STOPPCLK = 1

Description of Errata
A Host-initiated Suspend, followed by a Host Disconnect and Host Connect will not result in a SessReq interrupt.
Affected Conditions / Impacts
When USB_PCGCCTL.STOPPCLK is set and the device is acting as a B-peripheral, a Host-initated Suspend, followed by a Host Disconnect and Host Connect will not result in a SessReq interrupt.
Workaround
If this is an expected use-case, USB_PCGCCTL.STOPPCLK should not be set. USB_PCGCCTL.GATEHCLK can still be used to save power.
Resolution
There is currently no resolution for this issue.

2.13 USB_E110 — Unexpected USB_HCx_INT.CHHLTD Interrupt

Description of Errata
In some cases the USB_HCx_INT.CHHLTD interrupt might be incorrectly set.
Affected Conditions / Impacts
In some cases, an unexpected USB_HCx_INT.CHHLTD interrupt might be received from another endpoint that does not have the USB_HCx_CHAR.CHDIS, USB_HCx_INT.XACTERR, USB_HCx_INT.BBLERR, USB_HCx_INT.DATATGLERR, or USB_HCx_INT.XFERCOMPL interrupts enabled.
Workaround
If such an interrupt is received, the application must re-enable the channel for which it received the unexpected USB_HCx_INT.CHHLTD interrupt.
Resolution
There is currently no resolution for this issue.

3. Errata History

This section contains the errata history for EFM32LG devices.

For errata on latest revision, please refer to the beginning of this document. The device data sheet explains how to identify chip revision, either from package marking or electronically.

3.1 Errata History Summary

This tables lists all resolved errata for the EFM32LG.

Table 3.1. Errata History Status Summary

Errata #	Designator	Title/Problem	Workaround Exists	Affected Revision	Resolution
1	ADC_E116	Offset in ADC Temperature Sensor Calibration Data	Yes	D	E
2	ADC_E117	TIMEBASE not wide enough	Yes	D	E
3	AES_E101	BYTEORDER Does Not Work in Combination with DATASTART/XORSTART	Yes	D	E
4	AES_E102	AES_STATUS_RUNNING Set One Cycle Late With BYTEORDER Set	Yes	D	E
5	BURTC_E101	BURTC LPMODE Entry	No	D	E
6	BURTC_E102	BURTC_CNT Read Error	Yes	D	E
7	BU_E101	Backup Power Increased Power Consumtion	Yes	B	C
8	BU_E102	EM4 GPIO Retention in Backup Mode	No	B	C
9	BU_E104	EM4 with Backup BODs	No	B	C
10	BU_E106	Current Leakage in Backup Mode	Yes	D	E
11	CMU_E108	LFxCLKEN Write	Yes	B	C
12	CMU_E110	LFXO Phase Shift	No	B	C
13	CMU_E111	LFXO Configuration Incorrect	Yes	C	D
14	CMU_E112	LFXO Boost Buffer Current Setting	Yes	D	E
15	CMU_E113	LFXO Startup at High Temperature	Yes	D	E
16	CUR_E103	Increased EM2 Current	No	C	D
17	CUR_E104	Increased Current on AVDD2 (USB)	Yes	C	D
18	CUR_E105	Increased Current on AVDD2 (No USB)	Yes	C	D
19	DI_E101	Flash Page Size	Yes	D	E
20	DMA_E101	EM2 with WFE and DMA	Yes	D	E
21	EBI_E101	EBI Masking Functionality	Yes	B	C
22	EBI_E102	EBI Access Fails	Yes	B	C
23	EBI_E103	Page Mode Read in D16A16ALE Mode	Yes	D	E
24	EMU_E105	Debug Unavailable During DMA Processing from EM2	Yes	B	C
25	ETM_E101	ETM Trace Clock	Yes	B	C
26	GPIO_E101	GPIO Wakeup from EM4	Yes	B	C
27	LES_E101	LESENSE and Schmitt Trigger	Yes	B	C
28	LES_E102	LESENSE and DAC CH1 Configuration	Yes	B	C
29	LES_E103	AUXHFRCO and LESENSE	Yes	D	E
30	OPA_E101	OPAMP 2 Startup Rampup	No	B	C

Errata #	Designator	Title/Problem	Workaround Exists	Affected Revision	Resolution
31	PRS_E101	Edge Detect on GPIO/ACMP	No	D	E
32	USART_E112	USART AUTOTX Continues to Transmit Even With Full RX Buffer	No	D	E
33	USB_E101	USB DMA Transfers with Prescaled HFCLK	Yes	B	C
34	USB_E102	USB Datalines	No	B	C
35	USB_E106	USB Interrupts	Yes	B	C
36	USB_E107	Entry to EM4 Causes Temporary Leakage from VREGO	No	C	D
37	USB_E108	Floating DM/DP Pins Cause Leakage when USB is Disabled	Yes	C	D

3.2 Detailed Errata Descriptions

3.2.1 ADC_E116 — Offset in ADC Temperature Sensor Calibration Data

Description of Errata
The ADC temperature sensor calibration value stored in the Device Information (DI) Page has an offset.
Affected Conditions / Impacts
For devices with PROD_REV values of 16 or 17, the ADC0_TEMP_0_READ_1V25 register of the Device Information Page has an offset of 112. Using this value for calculating the absolute temperature gives an approximately 18 degrees too high value. Relative temperature measurements (temperature changes) are not affected by this offset.
Workaround
For devices with PROD_REV values of 16 or 17, use ADC0_TEMP_0_READ_1V25 - 112 instead of ADC0_TEMP_0_READ_1V25 when calculating the temperature.
Resolution
This issue is resolved in revision E devices.

3.2.2 ADC_E117 — TIMEBASE not wide enough

Description of Errata
For 48 MHz ADC clock, the ADC_CTRL_TIMEBASE is not wide enough.
Affected Conditions / Impacts
For ADC warm-up, the user is required to set the ADC_CTRL_TIMEBASE to the number of ADC clock cycles in 1 µs. As this register is only 5 bits wide, it does not support frequencies above 32 MHz.
Workaround
If an ADC clock above 32 MHz is required, the acquistion time should be increased to also account for too short warmup-time.
Resolution
This issue is resolved in revision E devices.

3.2.3 AES_E101 — BYTEORDER Does Not Work in Combination with DATASTART/XORSTART

Description of Errata
When the BYTEORDER bit in AES_CTRL is set, an encryption or decryption should not be started through DATASTART or XOR-START.
Affected Conditions / Impacts
If BYTEORDER is used in combination with DATASTART or XORSTART, the AES data and key are interpreted in the wrong order.
Workaround
Do not use BYTEORDER in combination with DATASTART or XORSTART.
Resolution
This issue is resolved in revision E devices.

3.2.4 AES_E102 — AES_STATUS_RUNNING Set One Cycle Late With BYTEORDER Set

Description of Errata
When the BYTEORDER bit in AES_CTRL is set, AES_STATUS_RUNNING is set one cycle late.
Affected Conditions / Impacts
If BYTEORDER is used, it will take one cycle for the AES_STATUS_RUNNING flag to be set. This means that polling this status flag should be postponed at least one cycle after starting encryption/decryption.
Workaround
If polling the AES_STATUS_RUNNING is preferred, insert a No Operation assembly instruction (NOP()) before starting to poll the status flag.
Resolution
This issue is resolved in revision E devices.

3.2.5 BURTC_E101 — BURTC LPMODE Entry

Description of Errata
Entering LPMODE with LPCOMP=7 causes counter error.
Affected Conditions / Impacts
A counting error occurs if overflow on 7 LSBs happens when entering LPMODE with LPCOMP=7. This results in the counter value being 256 less than it should be after the error. The error accumulates.
Workaround
Avoid using LPMODE with LPCOMP=7.
Resolution
This issue is resolved in revision E devices.

3.2.6 BURTC_E102 — BURTC_CNT Read Error

Description of Errata
Software reads from BURTC_CNT might fail when LPMODE is activated.
Affected Conditions / Impacts
When LPMODE is active (i.e. BURTC_STATUS_LPMODEACT is high), software reads might result in the wrong value being read from BURTC_CNT.
Workaround
Before reading BURTC_CNT, disable LPMODE and wait for BURTC_STATUS_LPMODEACT to be cleared before reading BURTC_CNT.
Resolution
This issue is resolved in revision D devices.

3.2.7 BU_E101 — Backup Power Increased Power Consumtion

Description of Errata
Additional current consumption on BU_VIN approximately 100uA when VDD_DREG is between 0.3 BU_VIN to 0.7 BU_VIN.
Affected Conditions / Impacts
Additional current consumption on BU_VIN approximately 100uA when VDD_DREG is between 0.3 BU_VIN to 0.7 BU_VIN.
Workaround
Avoid having VDD_DREG in between 0.3 BU_VIN to 0.7 BU_VIN.
Resolution
This issue is resolved in revision C devices.

3.2.8 BU_E102 — EM4 GPIO Retention in Backup Mode

Description of Errata
EM4 GPIO retention not shut off in backup mode.
Affected Conditions / Impacts
With GPIO retention enabled, GPIO pins will still drive in backup mode.
Workaround
Do not use EM4 GPIO retention in combination with backup mode.
Resolution
This issue is resolved in revision C devices.

3.2.9 BU_E104 — EM4 with Backup BODs

Description of Errata
EM4 with backup BODs does not trigger reset.
Affected Conditions / Impacts
EM4 with backup BODs does not trigger reset.
Workaround
Avoid using backup BODs when entering EM4.
Resolution
This issue is resolved in revision C devices.

3.2.10 BU_E106 — Current Leakage in Backup Mode

Description of Errata
In Backup mode, when VDD > BU_VIN + 0.7, current will leak from VDD.
Affected Conditions / Impacts
In Backup mode, when VDD > BU_VIN + 0.7, current will leak from VDD.
Workaround
To avoid leakage, exit Backup mode before VDD exceeds the voltage where the leakage start by configuring the threshold in EMU_BUACT.
Resolution
This issue is resolved in revision E devices.

3.2.11 CMU_E108 — LFxCLKEN Write

Description of Errata
First write to LFxCLKEN can be missed.
Affected Conditions / Impacts
For devices with PROD_REV < 15, enabling the clock for LFA/LFB after reset and then immediately writing LFACLKEN/LFBCLKEN may cause the write to miss its effect.
Workaround
For devices with PROD_REV < 15, make sure CMU_SYNCBUSY is not set before writing LFACLKEN/LFBCLKEN. Can temporarily switch to HFCORECLKLEDIV2 to speed up clearing synchbusy.
Resolution
This issue is resolved in revision C devices.

3.2.12 CMU_E110 — LFXO Phase Shift

Description of Errata
Transients on pin D8 cause LFXO phase shift.
Affected Conditions / Impacts
Transients on pin D8 can give a temporary phase shift on LFXO. Frequency is unchanged.
Workaround
No known workaround.
Resolution
This issue is resolved in revision C devices.

3.2.13 CMU_E111 — LFXO Configuration Incorrect

Description of Errata
For devices with PROD_REV < 15, LFXOBUFCUR in CMU_CTRL is default 0 and LFXOBOOST in CMU_CTRL is default 1. However, these values are incorrect.
Affected Conditions / Impacts
For devices with PROD_REV < 15, LFXOBUFCUR in CMU_CTRL is default 0 and LFXOBOOST in CMU_CTRL is default 1. However, these values are incorrect.
Workaround
On devices with PROD_REV < 15, change LFXOBUFCUR to 1 and LFXOBOOST to 0.
Resolution
This issue is resolved in revision D devices.

3.2.14 CMU_E112 — LFXO Boost Buffer Current Setting

Description of Errata
LFXO boost buffer current must be disabled.
Affected Conditions / Impacts
LFXO will not work properly with LFXOBUFCUR in CMU_CTRL set.
Workaround
Do not set LFXOBUFCUR in CMU_CTRL.
Resolution
This issue is resolved in revision E devices.

3.2.15 CMU_E113 — LFXO Startup at High Temperature

Description of Errata
LFXO does not start at high temperature with default configuration.
Affected Conditions / Impacts
For devices with PROD_REV ≥ 16, the LFXO may have startup issues with low capacitance crystals when using the default LFXO configuration.
Workaround
Make this line of code part of your startup code, typically in the start of `main()`: `*((volatile uint32_t*) 0x400c80C0) = (*((volatile uint32_t*) 0x400c80C0) & ~(1<<6)) | (1<<4);` Version v5.1.1 of the Gecko SDK will include this workaround for all affected device revisions.
Resolution
This issue is resolved in revision E devices.

3.2.16 CUR_E103 — Increased EM2 Current

Description of Errata
Increased consumption in EM2.
Affected Conditions / Impacts
Current consumption in EM2 and EM3 has two stable states, the normal state (1200 nA and 900 nA for EM2 and EM3 respectively) and an error state. In the error state, the current consumption in EM2 and EM3 is typically 4.5 µA at 25C (manufacturing test limits is set to 7 µA) but will increase with increased temperature. At 85C, the error state EM2 and EM3 current consumption is typically 25 µA. It is unpredictable which state the device will go into on EM2/EM3 entry and it can also change state during operation.
Workaround
No known workaround.
Resolution
This issue is resolved in revision D devices.

3.2.17 CUR_E104 — Increased Current on AVDD2 (USB)

Description of Errata
On devices with USB, there can be increased current on AVDD2 related to VREGO.
Affected Conditions / Impacts
When VREGO is floating or 0 V, a leakage can appear on AVDD2. This leakage is typically less than 10 µA, but can also rise to around 300 µA.
Workaround
Make sure VREGO is always defined high when there is power on AVDD2. For bus-powered devices this is always the case, but for devices where the power on VREGO can be lost during operation, e.g. a USB device where the USB phy is powered from VBUS when a master is attached, a 5 MΩ to VDD can help keep VREGO defined.
Resolution
This issue is resolved in revision D devices.

3.2.18 CUR_E105 — Increased Current on AVDD2 (No USB)

Description of Errata
On devices without USB, an increased current on AVDD2 can appear due to a floating internal node. This leakage is typically less than 10 µA, but can also rise to around 300 µA. The leakage is present in all energy modes.
Affected Conditions / Impacts
An increased current on AVDD2 can appear due to a floating internal node. This leakage is typically less than 10 µA, but can also rise to around 300 µA. The leakage is present in all energy modes.
Workaround
To reduce this leakage to a few hundred nanoamps, set MODE10 and MODE11 in GPIO->P[5].MODEH to GPIO_P_MODEH_MODE10_PUSHPULL and GPIO_P_MODEH_MODE11_PUSHPULL respectively, and make sure bits 10 and 11 in GPIO->P[5].DOUT are set. To ensure GPIO->P[5] bits 10 and 11 stay set in EM4, set EM4RET in GPIO_CTRL to turn on GPIO retention before entering EM4.
Resolution
This issue is resolved in revision D devices.

3.2.19 DI_E101 — Flash Page Size

Description of Errata
The MEM_INFO_PAGE_SIZE value stored in the Device Information (DI) Page is incorrect.
Affected Conditions / Impacts
For devices with PROD_REV values lower than 18, the MEM_INFO_PAGE_SIZE register value in the Device Information Page is incorrect.
Workaround
Use fixed flash page size of 4 kB.
Resolution
This issue is resolved in revision D devices.

3.2.20 DMA_E101 — EM2 with WFE and DMA

Description of Errata
WFE does not work for the DMA in EM2.
Affected Conditions / Impacts
In EM2, when sleeping with WFE (Wait for Event), an interrupt from the DMA will not wake up the system.
Workaround
Use WFI (Wait for Interrupt) or EM1 instead.
Resolution
This issue is resolved in revision D devices.

3.2.21 EBI_E101 — EBI Masking Functionality

Description of Errata
EBI masking functionality is not limited to bank selected for TFT.
Affected Conditions / Impacts
EBI masking functionality is not limited to the bank selected for TFT (by BANKSEL field in EBI_TFTCTRL). When masking is enabled, a mask match can be generated and suppress writes to any bank.
Workaround
Disable masking when doing writes that should not be affected.
Resolution
This issue is resolved in revision C devices.

3.2.22 EBI_E102 — EBI Access Fails

Description of Errata
Certain EBI accesses via the Cortex and Debug interface do not work.
Affected Conditions / Impacts
Any access from the Cortex to the EBI not aligned to its size does not work. Also, only word accesses from the debug interface works.
Workaround
Make sure all accesses via the Cortex are aligned to its size, and that all debug accesses are word accesses.
Resolution
This issue is resolved in revision C devices.

3.2.23 EBI_E103 — Page Mode Read in D16A16ALE Mode

Description of Errata
Page mode read in D16A16ALE mode skips RDSETUP stage for page mode accesses.
Affected Conditions / Impacts
Page mode read in D16A16ALE mode skips RDSETUP stage for page mode accesses, making the read process go directly from ADDRSETUP to RDPA.
Workaround
To compensate for the missing hold time related to the ALE address latch, the HALFALE field in EBI_ADDRTIMING can be enabled providing a 1/2 cycle hold time.
Resolution
This issue is resolved in revision E devices.

3.2.24 EMU_E105 — Debug Unavailable During DMA Processing from EM2

Description of Errata
The debugger cannot access the system processing DMA request from EM2.
Affected Conditions / Impacts
DMA requests from the LEUART can trigger a DMA operation from EM2. While waiting for the DMA to fetch data from the respective peripheral, the debugger cannot access the system. If such a DMA request is not handled by the DMA controller, the system will keep waiting for it while denying debug access.
Workaround
Make sure DMA requests triggered from EM2 are handled.
Resolution
This issue is resolved in revision C devices.

3.2.25 ETM_E101 — ETM Trace Clock

Description of Errata
ETM Trace Clock needs to be delayed.
Affected Conditions / Impacts
ETM trace clock is out of phase making the data transition occur at the same time as the ETM trace clock transitions.
Workaround
ETM trace clock needs to be delayed between 10 ns and 1/4 of the trace clock period.
Resolution
This issue is resolved in revision C devices.

3.2.26 GPIO_E101 — GPIO Wakeup from EM4

Description of Errata
On GPIO wakeup from EM4, all cause bits for high-polarity wakeup pins are set.
Affected Conditions / Impacts
All EM4 wakeup cause bits for EM4 wakeup pins with high polarity are set on wakeup.
Workaround
Use low polarity if possible. For active high, slow changing inputs, a solution is to sample the inputs on wakeup.
Resolution
This issue is resolved in revision C devices.

3.2.27 LES_E101 — LESENSE and Schmitt Trigger

Description of Errata
Schmitt trigger cannot be disabled on pins used for sensor excitation
Affected Conditions / Impacts
When using LESENSE to excite a pin, the pin has to be configured in push-pull mode, which also enables the Schmitt trigger. If this pin has an input voltage somewhere in between 0.3*VDD and 0.7*VDD, the Schmitt trigger will consume a considerable ammount of current.
Workaround
Keep the input voltage to pins configured as push-pull outside the range 0.3*VDD to 0.7*VDD when LESENSE is not interacting with the connected sensor.
Resolution
This issue is resolved in revision C devices.

3.2.28 LES_E102 — LESENSE and DAC CH1 Configuration

Description of Errata
LESENSE cannot control DAC CH1 if DACCH0CONV in LESENSE_PERCTRL is set to DISABLE.
Affected Conditions / Impacts
LESENSE control of DAC CH1 cannot be enabled if DACCH0CONV in LESENSE_PERCTRL is set to DISABLE.
Workaround
Configure DACCH0CONV in LESENSE_PERCTRL to anything but DISABLE, this enables DAC CH1 to be controlled properly. If DAC CH0 is not to be used, set DACCH0OUT in LESENSE_PERCTRL to DISABLE. This will disable LESENSE control of DAC CH0, but still allow LESENSE to control DAC CH1.
Resolution
This issue is resolved in revision C devices.

3.2.29 LES_E103 — AUXHFRCO and LESENSE

Description of Errata
LESENSE will not work properly at low AUXHFRCO frequencies.
Affected Conditions / Impacts
LESENSE will not work properly when used with the AUXHFRCO running at the 1 or 7 MHz band.
Workaround
Do not use a AUXHFRCO frequency band of 1 or 7 MHz when used in combination with LESENSE.
Resolution
This issue is resolved in revision E devices.

3.2.30 OPA_E101 — OPAMP 2 Startup Rampup

Description of Errata
When OPA2 is started, the output rampup is constant independent of bias setting.
Affected Conditions / Impacts
When OPA2 is started the output rampup is constant independent of bias setting.
Workaround
No known workaround.
Resolution
This issue is resolved in revision C devices.

3.2.31 PRS_E101 — Edge Detect on GPIO/ACMP

Description of Errata
Edge detect on peripherals with asynchronous edges might be missed.
Affected Conditions / Impacts
When using edge detect in PRS on signals from ACMP, GPIO, RTC, LETIMER, LESENSE, VCMP, and BURTC, edges can be missed.
Workaround
Do not use edge detect on ACMP, GPIO, RTC, LETIMER, LESENSE, VCMP, and BURTC.
Resolution
This issue is resolved in revision E devices.

3.2.32 USART_E112 — USART AUTOTX Continues to Transmit Even With Full RX Buffer

Description of Errata
USART AUTOTX continues to transmit even with full RX buffer.
Affected Conditions / Impacts
When AUTOTX in USARTn_CTRL or AUTOTXEN in USARTn_TRIGCTRL is set, the USART will continue to transmit data even after the RX buffer is full. This may cause the RX buffer to overflow if the data is not read out in time.
Workaround
No known workaround.
Resolution
This issue is resolved in revision E devices.

3.2.33 USB_E101 — USB DMA Transfers with Prescaled HFCLK

Description of Errata
USB DMA transfers to flash fail when prescaling HFCLK.
Affected Conditions / Impacts
USB DMA transfers to flash may fail when prescaling HFCLK.
Workaround
Do not prescale HFCLK when using USB-DMA transfers to read from flash.
Resolution
This issue is resolved in revision C devices.

3.2.34 USB_E102 — USB Datalines

Description of Errata
USB datalines rise and fall time are slightly outside specification.
Affected Conditions / Impacts
USB datalines rise and fall time are slightly outside specification under worst case conditions. They may fail USB certification eye test depending on PCB layout.
Workaround
No known workaround.
Resolution
This issue is resolved in revision C devices.

3.2.35 USB_E106 — USB Interrupts

Description of Errata
USB interrupts have changed from being level triggered to edge triggered.
Affected Conditions / Impacts
USB inteerrupts are now trigggered by signal edge rather then signal level.
Workaround
Make sure to handle edge triggered interrupts, rather then signal level interrupts.
Resolution
This issue is resolved in revision C devices.

3.2.36 USB_E107 — Entry to EM4 Causes Temporary Leakage from VREGO

Description of Errata
Entry to EM4 causes temporary leakage from VREGO.
Affected Conditions / Impacts
On transition from EM0 to EM4, a current leakage from VREGO of up to 1 mA lasting a few seconds can occur.
Workaround
No known workaround.
Resolution
This issue is resolved in revision D devices.

3.2.37 USB_E108 — Floating DM/DP Pins Cause Leakage when USB is Disabled

Description of Errata
Floating DM/DP pins cause leakage when USB is disabled.
Affected Conditions / Impacts
When the USB_DM or USB_DP pins are floating while the USB PHY is disabled, a current in the order of a couple hundred µA may leak from USB_VREGO to VSS. This will not be an issue if there is no voltage applied to USB_VREGO, either externally or through the USB regulator.
Workaround
If there is no intention to use the USB module, e.g. the USB PHY is disabled, but there is still a voltage on USB_VREGO, make sure the USB_DM and USB_DP pins are defined. This can be done using GPIO or by defining them externally.
Resolution
This issue is resolved in revision D devices.

4. Revision History

4.1 Revision 1.20

April 10th, 2017

Added EMU_E110.

Updated errata formatting.

Merged all errata documents for EFM32LG devices into one document.

Merged errata history and errata into one document.

4.2 Revision 1.10

October 5th, 2015

Added DAC_E109, EMU_E107, TIMER_E103, RMU_E101, and PCNT_E102.

4.3 Revision 1.00

October 15th, 2014

Initial release for EFM32LG360 and EFM32LG900 devices.

4.4 Revision 0.70

June 13th, 2014

Updated to product revision E.

Removed erratas that are not applicable to revision E.

4.5 Revision 0.60

August 21st, 2013

Added ADC_E117, AES_E102, USB_E109, and USB_E110.

Updated disclaimer, trademark and contact information.

4.6 Revision 0.50

July 30th, 2013

Added AES_E101, BURTC_E102, CMU_E114, and DMA_E101.

Updated errata naming convention.

4.7 Revision 0.40

June 5th, 2012

Added ADC_E101 and DI_E101.

4.8 Revision 0.30

April 24th, 2012

Added BU_E106, CMU_E104, CMU_E105, LES_E103, and USART_E101.

Removed Erratas not valid for chip revision.

4.9 Revision 0.20

January 6th, 2012

Added CMU_E103, CUR_E103, CUR_E105, CUR_E104, USB_E107, USB_E108, and MSC_E101.

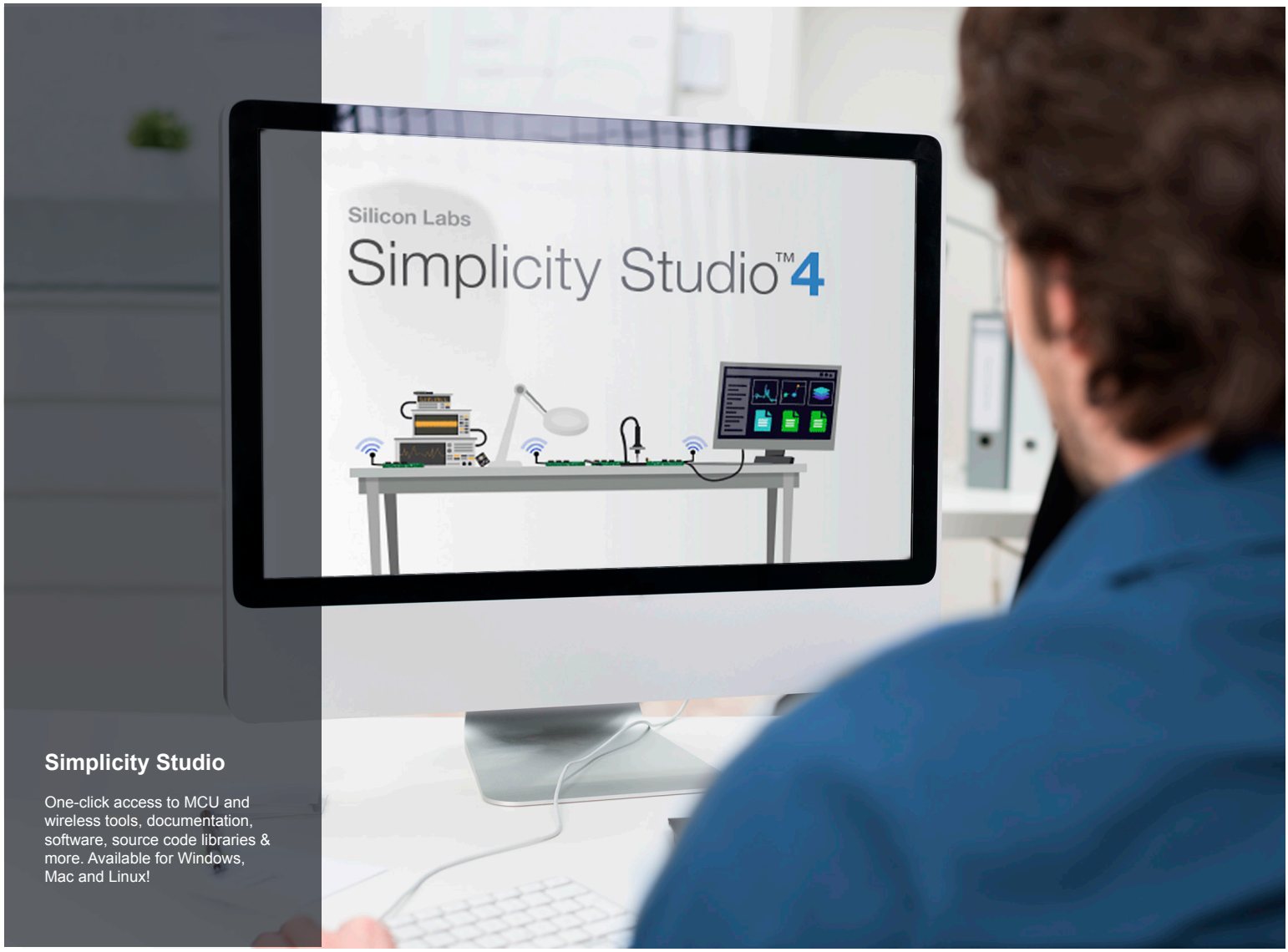
Updated PRS_E101.

Removed Erratas not valid for chip revision.

4.10 Revision 0.10

November 4th, 2011

Initial preliminary release.



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