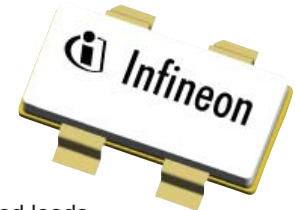


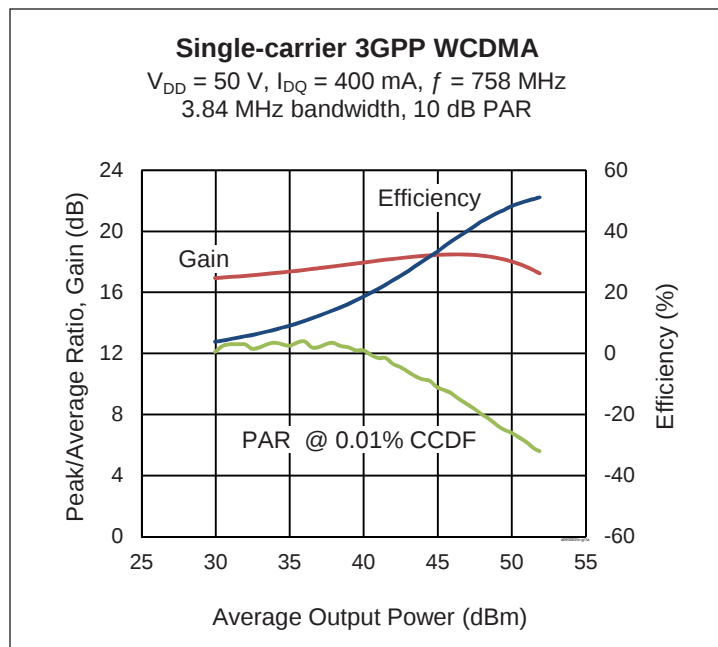
Thermally-Enhanced High Power RF LDMOS FET 300 W, 50 V, 703 – 960 MHz

Description

The PTVA093002TC is a 300-watt LDMOS FET. Designed for use in multi-standard cellular power amplifier applications, it can be used as single-ended or in a Doherty configuration. It features dual-path design, input matching, and a thermally-enhanced surface-mount package. Manufactured with Infineon's advanced LDMOS process, this device provides excellent thermal performance and superior reliability.



PTVA093002TC
Package H-49248H-4, formed leads



Features

- Typical CW performance in a combined-lead 50-ohm single-ended fixture, 780 MHz, 50 V
 - Output power at P_{1dB} = 158 W
 - Gain = 18.2 dB
 - Efficiency = 52%
- Typical pulsed CW performance in a combined-lead 50-ohm single-ended fixture, 870 MHz, 50 V
 - Output power at P_{3dB} = 280 W
 - Gain = 16.2 dB
 - Efficiency = 50%
- Integrated ESD protection, Human Body Model class 2 (per JESD22-A114)
- Capable of withstanding a 10:1 load mismatch at 50 V, 63 W (CW) output power
- Low thermal resistance
- Pb-free and RoHS compliant

RF Specifications

Single-carrier WCDMA Characteristics (device with flat leads tested in an Infineon Doherty production test fixture)

$V_{DD} = 50\text{ V}$, $I_{DQ} = 400\text{ mA}$, $V_{GSpeak} = 1.9\text{ V}$, $P_{OUT} = 63\text{ W}$ average, $f = 803\text{ MHz}$.

3GPP WCDMA signal: 3.84 MHz bandwidth, 10 dB PAR @0.01% CCDF.

Characteristic	Symbol	Min	Typ	Max	Unit
Gain	G_{ps}	17.5	18.5	—	dB
Drain Efficiency	η_D	40	45	—	%
Adjacent Channel Power Ratio	ACPR	—	-34	-32	dBc

All published data at $T_{CASE} = 25^\circ\text{C}$ unless otherwise indicated

ESD: Electrostatic discharge sensitive device—observe handling precautions!

DC Characteristics

Characteristic	Conditions	Symbol	Min	Typ	Max	Unit
Drain-source Breakdown Voltage	$V_{GS} = 0\text{ V}$, $I_{DS} = 10\text{ mA}$	$V_{(BR)DSS}$	105	—	—	V
Drain Leakage Current	$V_{DS} = 50\text{ V}$, $V_{GS} = 0\text{ V}$	I_{DSS}	—	—	1.0	μA
	$V_{DS} = 105\text{ V}$, $V_{GS} = 0\text{ V}$	I_{DSS}	—	—	10.0	μA
Gate Leakage Current	$V_{GS} = 10\text{ V}$, $V_{DS} = 0\text{ V}$	I_{GSS}	—	—	1.0	μA
On-state Resistance	$V_{GS} = 10\text{ V}$, $V_{DS} = 0.1\text{ V}$	$R_{DS(on)}$	—	0.265	—	Ω
Operating Gate Voltage	(main) $V_{DS} = 50\text{ V}$, $I_{DQ} = 400\text{ mA}$	V_{GS}	—	3.8	—	V
	(peak) $V_{DS} = 50\text{ V}$, $I_{DQ} = 0\text{ A}$	V_{GS}	—	1.9	—	V

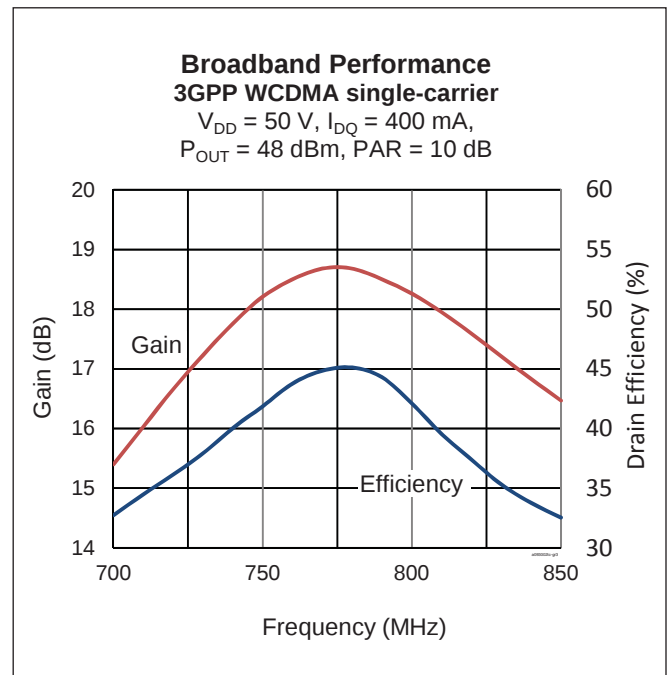
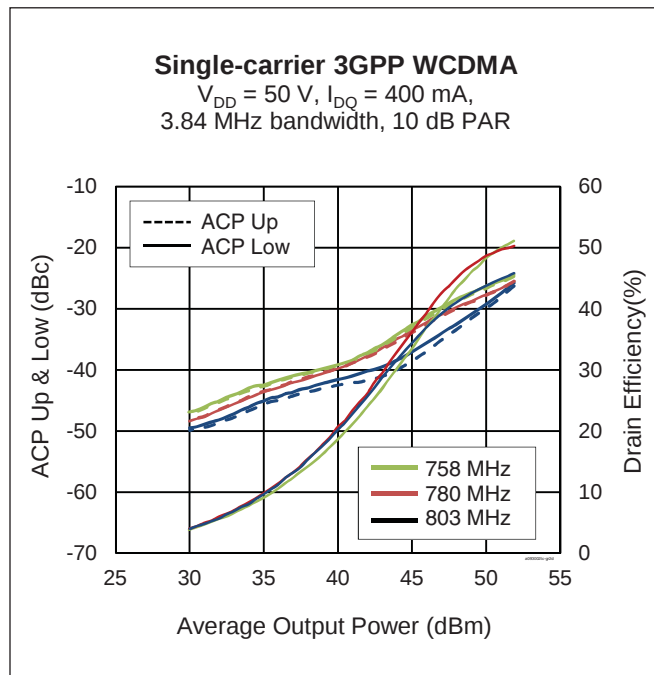
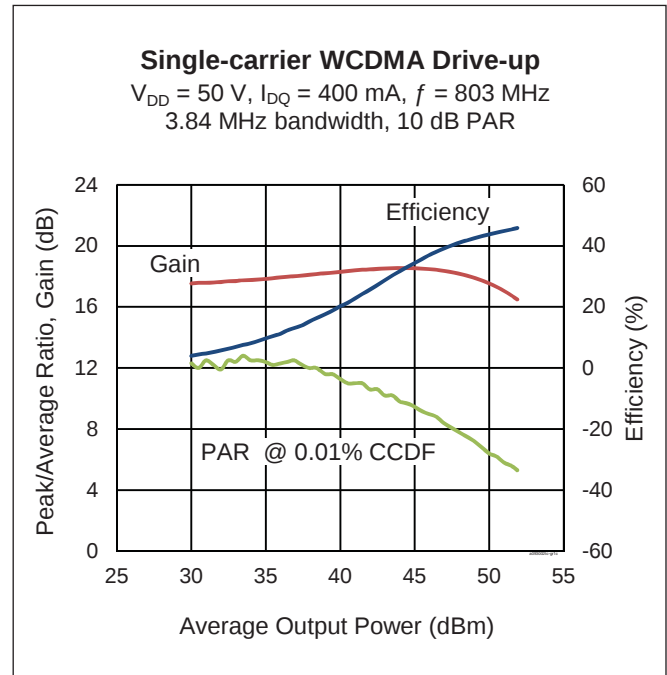
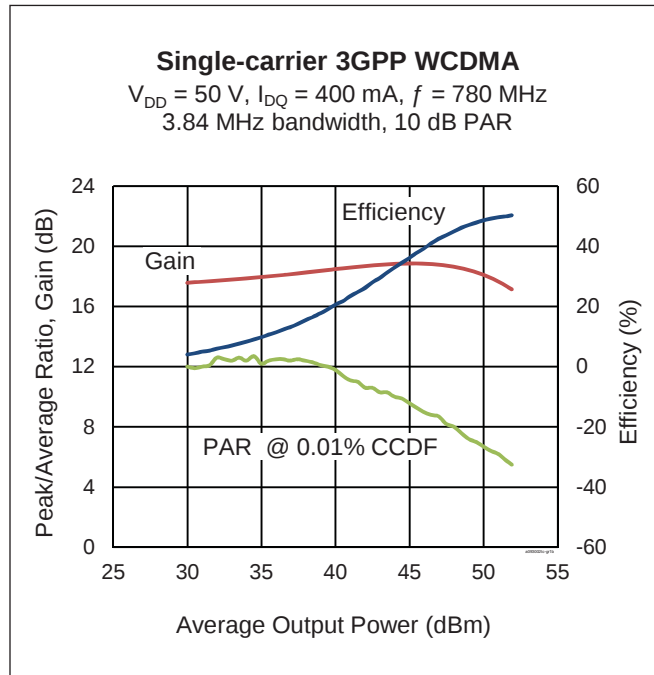
Maximum Ratings

Parameter	Symbol	Value	Unit
Drain-source Voltage	V_{DSS}	105	V
Gate-source Voltage	V_{GS}	−6 to +12	V
Junction Temperature	T_J	200	$^{\circ}\text{C}$
Storage Temperature Range	T_{STG}	−65 to +150	$^{\circ}\text{C}$
Thermal Resistance ($T_{CASE} = 70^{\circ}\text{C}$, 200 W CW)	$R_{\theta JC}$	0.44	$^{\circ}\text{C/W}$

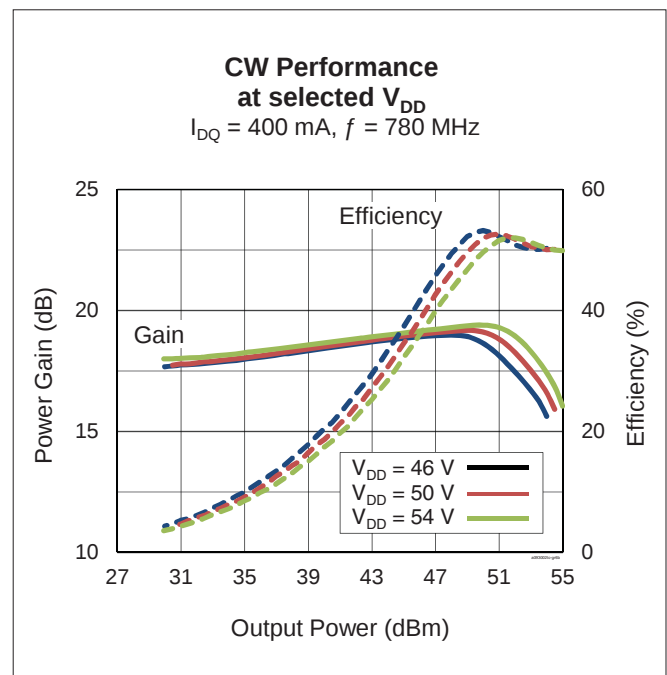
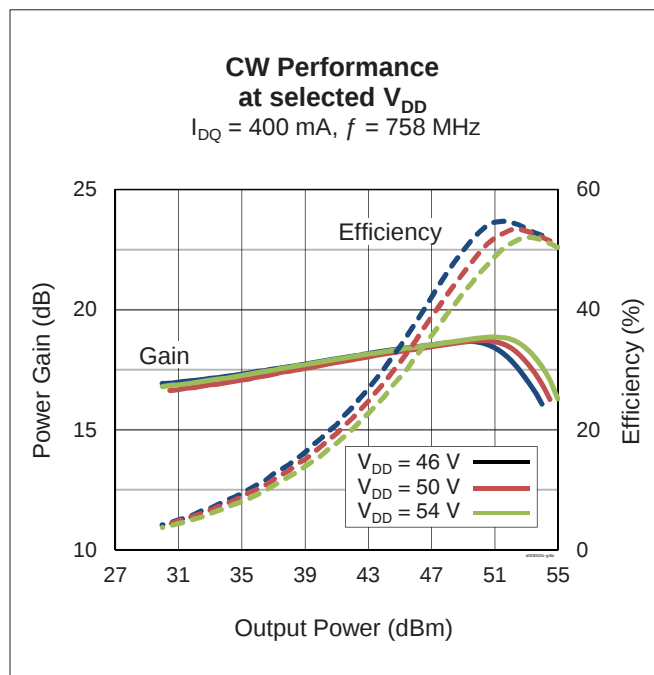
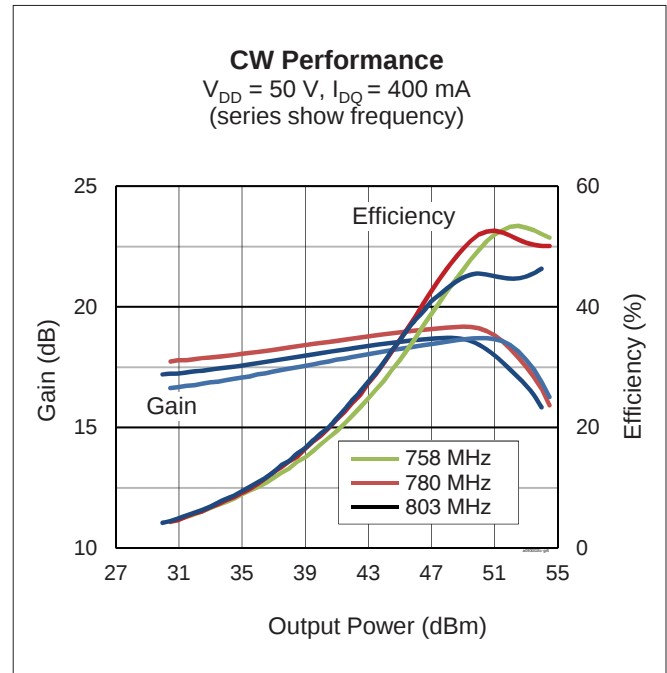
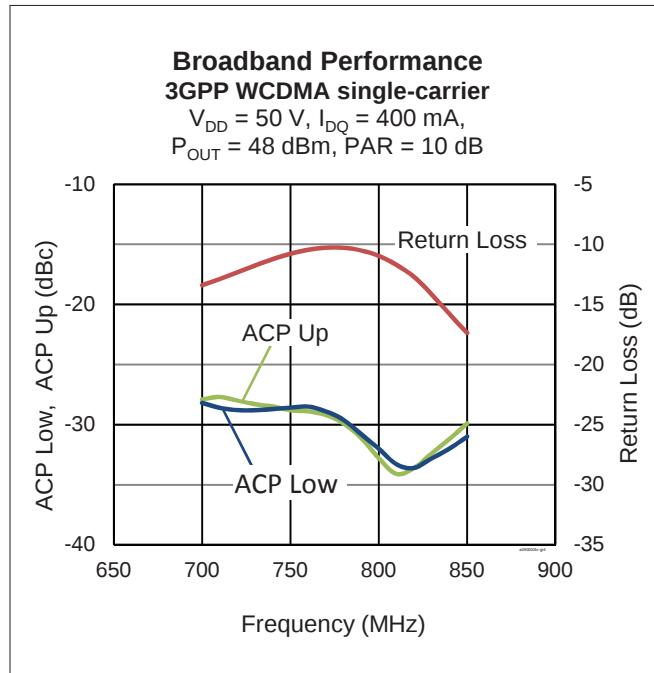
Ordering Information

Type and Version	Order Code	Package and Description	Shipping
PTVA093002TC V1 R250	PTVA093002TCV1R250XTMA1	H-49248H-4, earless, ceramic open-cavity, formed leads, surface mount	Tape & Reel, 250 pcs

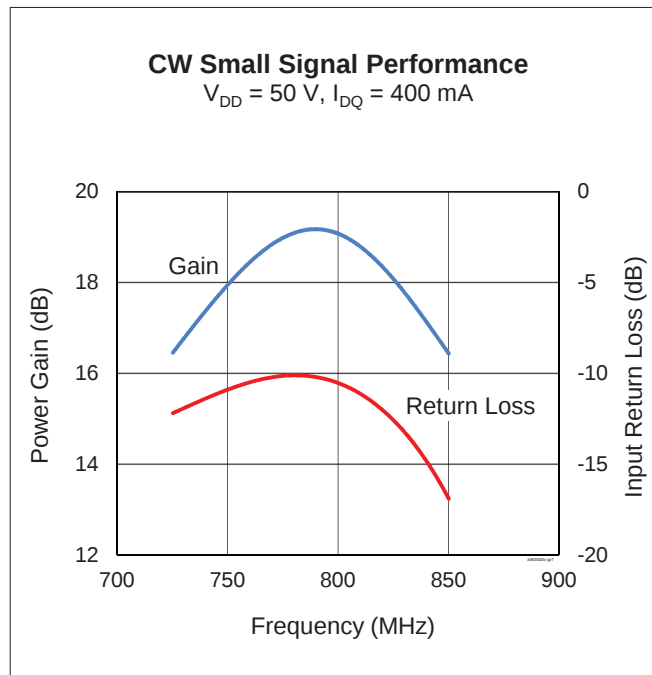
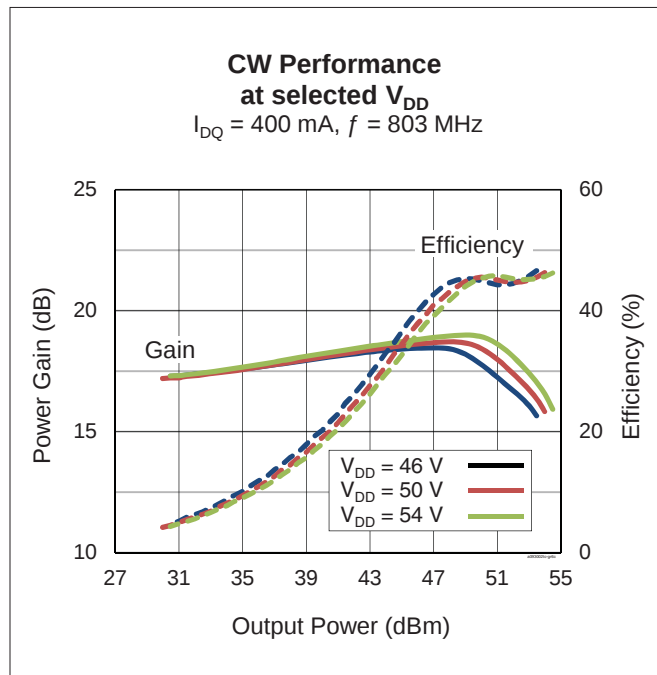
Typical Performance (data taken in a reference test fixture)



Typical Performance (cont.)

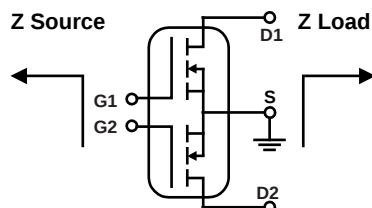


Typical Performance (cont.)



See next page for Load Pull

Load Pull Performance



Main side pulsed CW signal: 160 μ sec, 10% duty cycle; 50 V, $V_{GS} = 3.8$ V, $I_{DQ} = 350$ mA

Class AB		P _{1dB}									
		Max Output Power					Max PAE				
Freq [MHz]	Z _s [Ω]	Z _L [Ω]	Gain [dB]	P _{OUT} [dBm]	P _{OUT} [W]	PAE [%]	Z _L [Ω]	Gain [dB]	P _{OUT} [dBm]	P _{OUT} [W]	PAE [%]
758	1.62 – j4.90	2.53 – j2.78	21.16	53.39	218	59.8	2.25 – j0.37	23.46	51.01	126	71.9
791	2.16 – j5.30	2.59 – j2.99	21.12	53.32	215	60.7	1.78 – j0.51	23.61	50.31	107	73.2
803	2.54 – j5.29	2.16 – j2.82	21.08	53.39	218	61.4	1.81 – j0.56	23.59	50.38	109	74.1

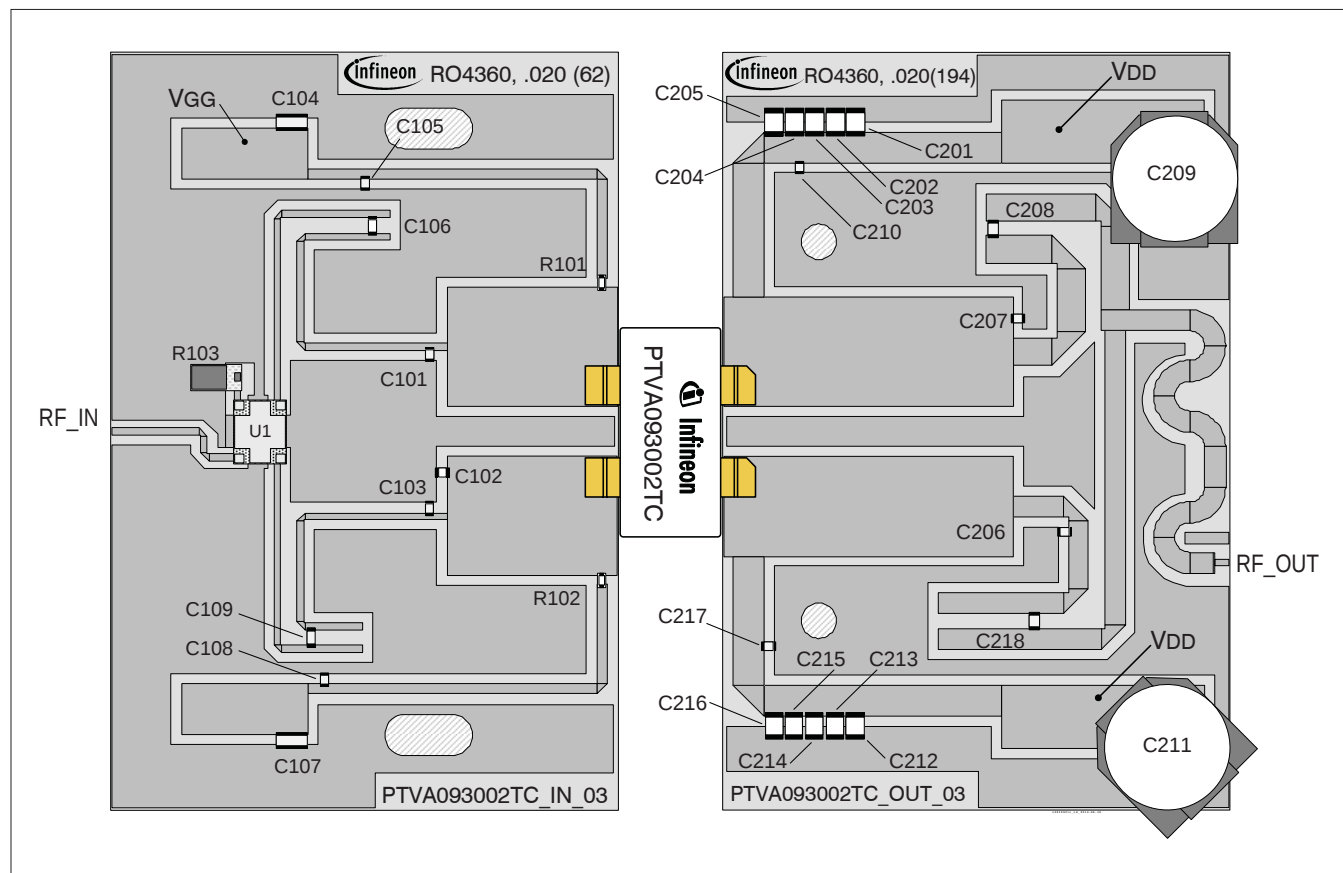
Peak side pulsed CW signal: 160 μ sec, 10% duty cycle; 28 V, $I_{DQ} = 75$ mA

Class C		P _{1dB}									
		Max Output Power					Max PAE				
Freq [MHz]	Z _s [Ω]	Z _L [Ω]	Gain [dB]	P _{OUT} [dBm]	P _{OUT} [W]	PAE [%]	Z _L [Ω]	Gain [dB]	P _{OUT} [dBm]	P _{OUT} [W]	PAE [%]
MHz	Ohm	Ohm	dB	dBm	W	%	Ohm	dB	dBm	W	%
758	1.62 – j4.90	2.47 – j2.74	20.43	53.46	222	63.9	2.14 – j0.55	22.20	51.32	135	75.0
791	2.16 – j5.30	2.15 – j2.66	20.46	53.38	218	66.1	1.92 – j0.99	22.02	51.41	138	76.3
803	2.54 – j5.29	2.14 – j2.82	20.30	53.49	224	65.7	1.91 – j0.89	22.08	51.19	131	77.4

Reference Circuit, tuned for 758 – 803 MHz

DUT	PTVA093002TC
Test Fixture Part No.	LTD/PTVA093002TC V1
PCB	Rogers RO4360, 0.508 mm [.020"] thick, 2 oz. copper, $\epsilon_r = 6.4$
Find Gerber files for this reference fixture on the Infineon Web site at (www.infineon.com/rfpower)	

Reference Circuit, tuned for 758 – 803 MHz (cont.)



Reference circuit assembly diagram (not to scale)

Component Information

Component	Description	Manufacturer	P/N
Input			
C101	Chip capacitor, 3.6 pF	ATC	ATC100A3R6CW150XB
C102	Chip capacitor, 3.9 pF	ATC	ATC800A3R9CW150XB
C104, C107	Capacitor, 10 μ F	Murata Electronics North America	LLL31BC70G106MA01L
C105, C106, C108, C109	Chip capacitor, 6 pF	ATC	ATC100A6R0CW150XB
R101, R102	Resistor, 10 Ohm	Panasonic – ECG	ERJ-3GEYJ100V
R103	Resistor, 50 Ohm	Anaren	RFP-060120A15Z50
U1	Hybrid Coupler, 4 dB, 90°	Anaren	X3C07P-04S

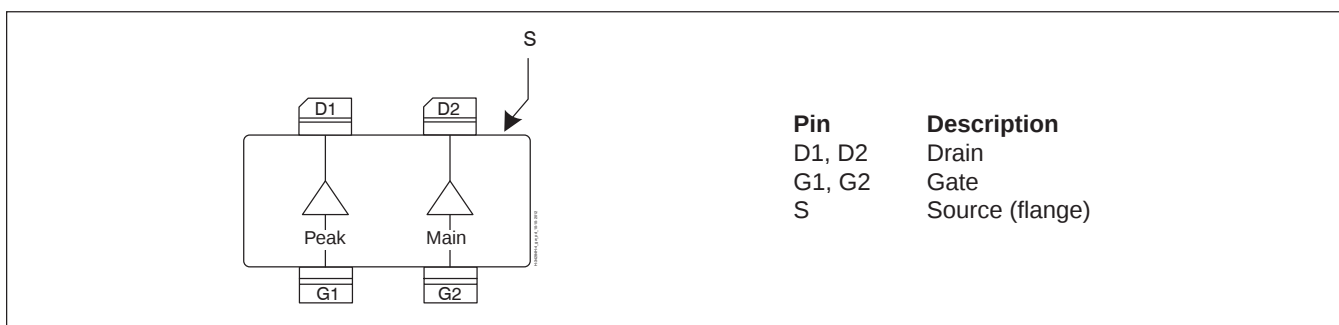
(table continued on page 8)

Reference Circuit (cont.)

Component Information (cont.)

Component	Description	Manufacturer	P/N
Output			
C206	Chip capacitor, 3.3 pF	ATC	ATC100A3R3CW150XB
C207	Chip capacitor, 5.6 pF	ATC	ATC800A5R6CW150XB
C208, C210, C217, C218	Chip capacitor, 6 pF	ATC	ATC100A6R0CW150XB
C207, C209	Capacitor, 10 μ F	Taiyo Yuden	UMK325C7106MM-T
C209, C211	Capacitor, 100 μ F, 100 V	United Chemi-Con	EMVE101ARA101MKE0S

Pinout Diagram (top view)



Lead connections for PTVA093002TC

Package Outline Specifications

Package H-49248H-4, formed leads

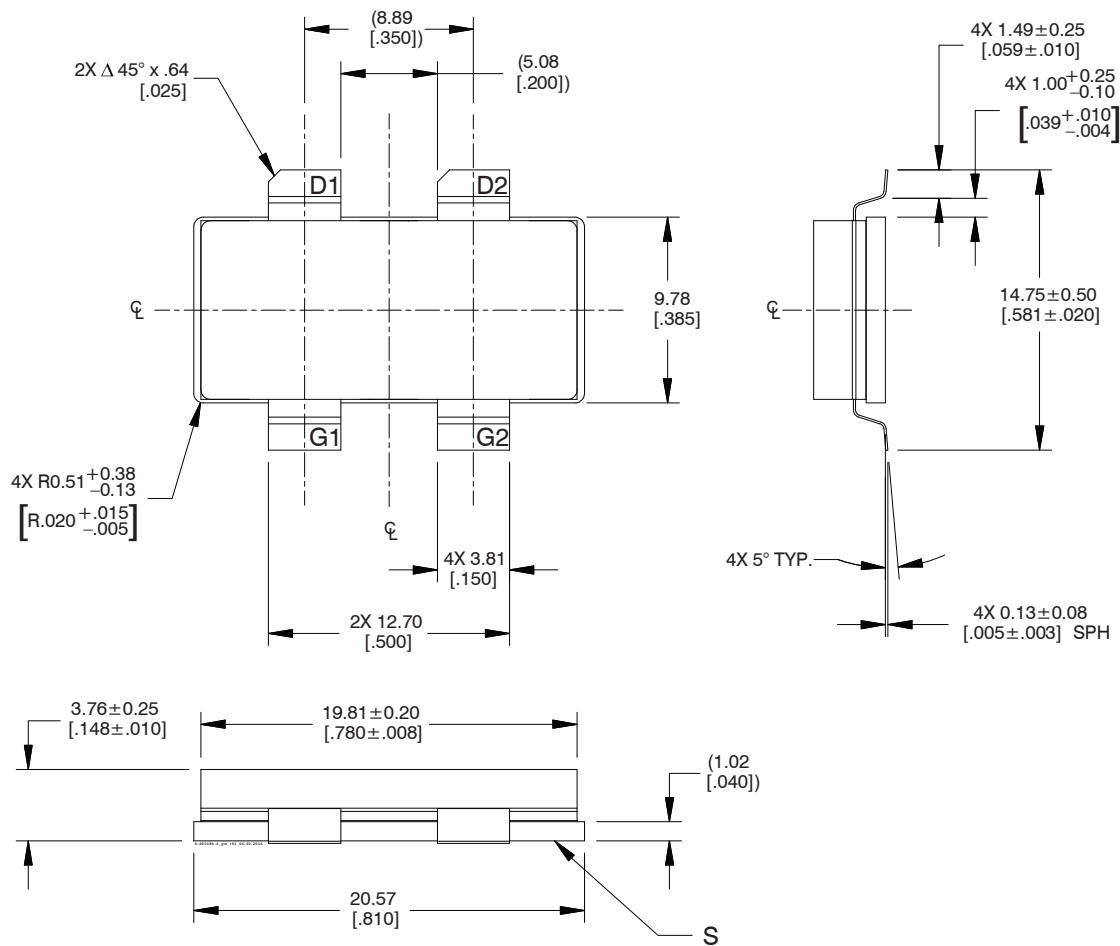


Diagram Notes—unless otherwise specified:

1. Interpret dimensions and tolerances per ASME Y14.5M-1994.
2. Primary dimensions are mm. Alternate dimensions are inches.
3. All tolerances ± 0.127 [.005].
4. Pins: D1, D2 – drain; G1, G2 – gate; S – source (flange).
5. Lead thickness: $0.10 + 0.051/-0.025$ [.004⁺_{-.001}].
6. Gold plating thickness:
flange – 0.25 micron [10 microinch] max;
leads – 1.14 ± 0.38 micron [45 $\pm$ 15 microinch] max.

Find the latest and most complete information about products and packaging at the Infineon Internet page (www.infineon.com/rfpower)

Revision History

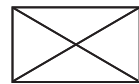
Revision	Date	Data Sheet	Page	Subjects (major changes since last revision)
01	2014-01-08	Advance	All	New product, proposed only.
02	2014-01-29	Advance	All	Package type number and configuration revised.
03	2014-05-02	Advance	All	Package type number revised.
04	2014-06-16	Production	All	Data Sheet now represents released product specifications, including reference circuit and performance information

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To request other information, contact us at:
+1 877 465 3667 (1-877-GO-LDMOS) USA
or +1 408 776 0600 International



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