

SN54ALS874B, SN74ALS874B, SN74ALS876A SN74AS874, SN74AS876 DUAL 4-BIT D-TYPE EDGE-TRIGGERED FLIP-FLOPS

SDAS061C – APRIL 1982 – REVISED JANUARY 1995

- 3-State Buffer-Type Outputs Drive Bus Lines Directly
- Bus-Structured Pinout
- Choice of True or Inverting Logic
 - SN54ALS874B, SN74ALS874B, SN74AS874 Have True Outputs
 - SN74ALS876A, SN74AS876 Have Inverting Outputs
- Asynchronous Clear
- Package Options Include Plastic Small-Outline (DW) Packages, Plastic (FN) and Ceramic (FK) Chip Carriers, and Standard Plastic (NT) and Ceramic (JT) 300-mil DIPs

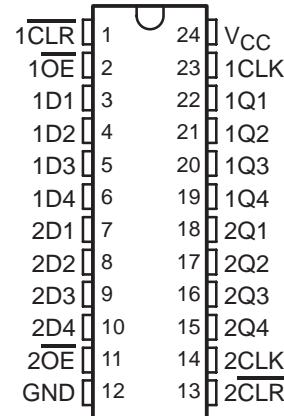
description

These dual 4-bit D-type edge-triggered flip-flops feature 3-state outputs designed specifically as bus drivers. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

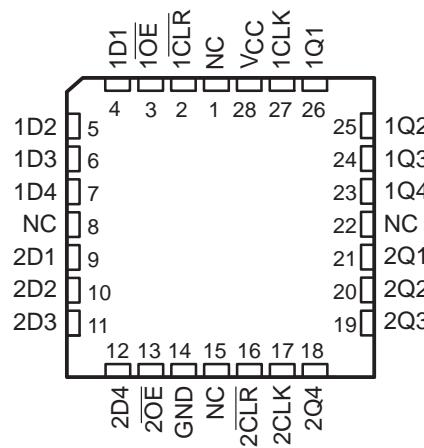
The edge-triggered flip-flops enter data on the low-to-high transition of the clock (CLK) input. The SN54ALS874B, SN74ALS874B, and SN74AS874 have clear (CLR) inputs and noninverting Q outputs. The SN74ALS876A and SN74AS876 have preset (PRE) inputs and inverting \bar{Q} outputs; taking PRE low causes the four Q or \bar{Q} outputs to go low independently of the clock.

The SN54ALS874B is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74ALS874B, SN74ALS876A, SN74AS874, and SN74AS876 devices are characterized for operation from 0°C to 70°C .

SN54ALS874B . . . JT PACKAGE
SN74ALS874B, SN74AS874 . . . DW OR NT PACKAGE
(TOP VIEW)

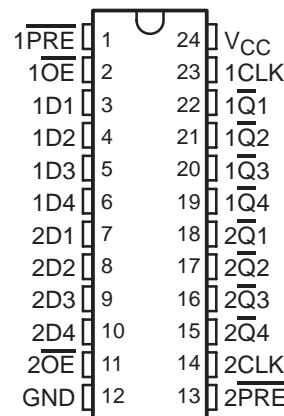


SN54ALS874B . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

SN74ALS876A, SN74AS876 . . . DW OR NT PACKAGE
(TOP VIEW)



**SN54ALS874B, SN74ALS874B, SN74ALS876A
SN74AS874, SN74AS876
DUAL 4-BIT D-TYPE EDGE-TRIGGERED FLIP-FLOPS**

SDAS061C – APRIL 1982 – REVISED JANUARY 1995

Function Tables

**SN54ALS874B, SN74ALS874B, SN74AS876
(each flip-flop)**

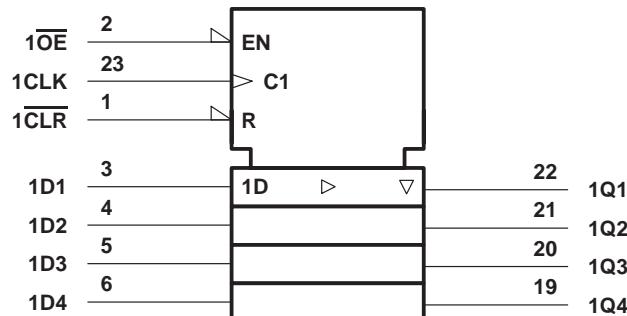
INPUTS				OUTPUT Q
\overline{OE}	\overline{CLR}	CLK	D	
L	L	X	X	L
L	H	\uparrow	H	H
L	H	\uparrow	L	L
L	H	L	X	Q_0
H	X	X	X	Z

**SN74ALS876A, SN74AS876
(each flip-flop)**

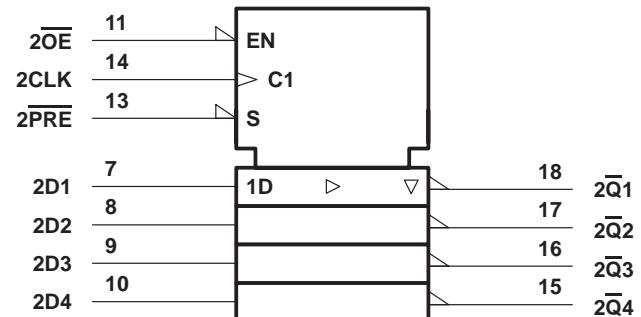
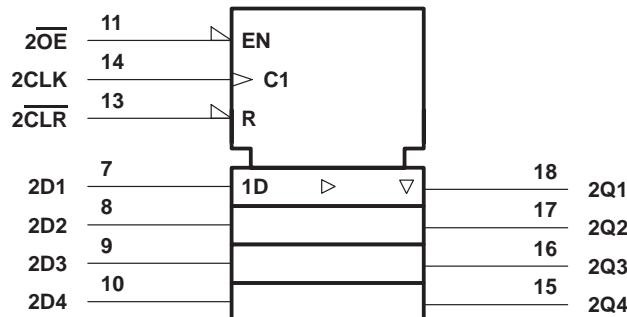
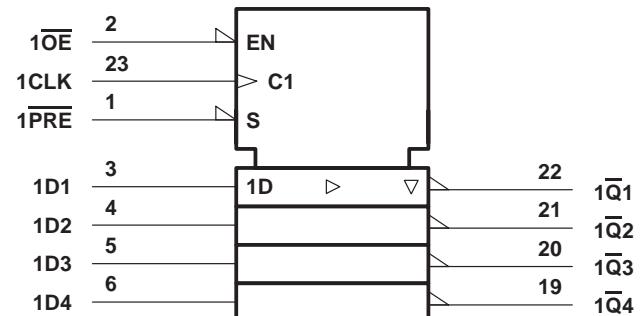
INPUTS				OUTPUT \overline{Q}
\overline{OE}	\overline{PRE}	CLK	D	
L	L	X	X	L
L	H	\uparrow	H	L
L	H	\uparrow	L	H
L	H	L	X	\overline{Q}_0
H	X	X	X	Z

logic symbols[†]

SN54ALS874B, SN74ALS874B, SN74AS876

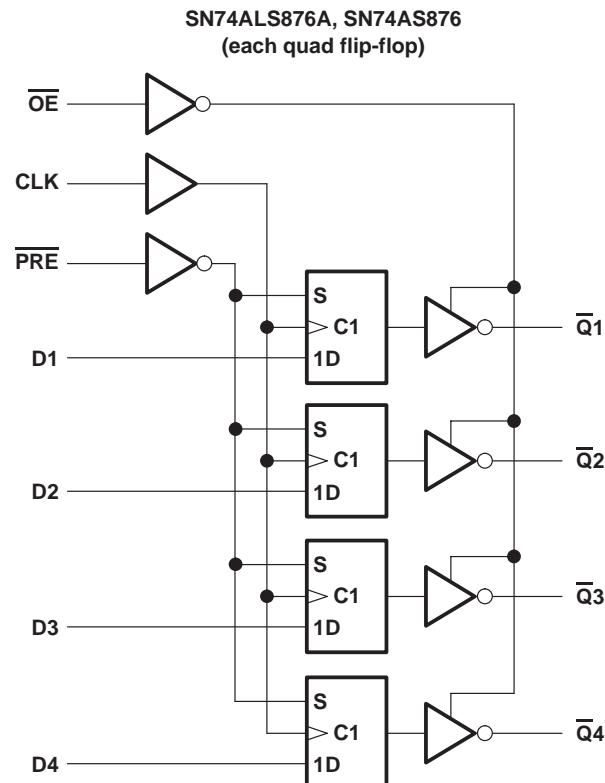
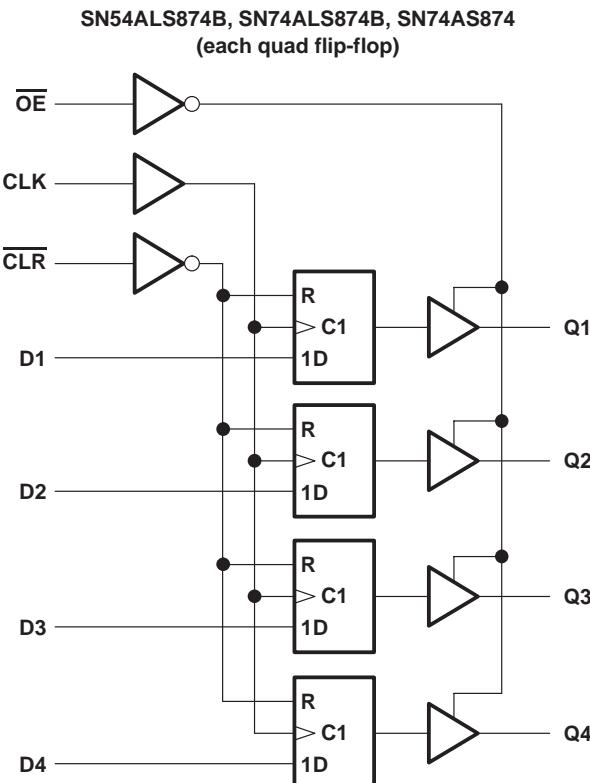


SN74ALS876A, SN74AS876



[†] These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for the DW, JT, and NT packages.

logic diagrams (positive logic)



Pin numbers shown are for the DW, JT, and NT packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage, V_{CC}	7 V
Input voltage, V_I	7 V
Voltage applied to a disabled 3-state output	5.5 V
Operating free-air temperature range, T_A : SN54ALS874B	-55°C to 125°C
SN74ALS874B, SN74ALS876A	0°C to 70°C
Storage temperature range	-65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

**SN54ALS874B, SN74ALS874B, SN74ALS876A
 SN74AS874, SN74AS876
 DUAL 4-BIT D-TYPE EDGE-TRIGGERED FLIP-FLOPS**

SDAS061C – APRIL 1982 – REVISED JANUARY 1995

recommended operating conditions

		SN54ALS874B			SN74ALS874B SN74ALS876A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V _{IH}	High-level input voltage	2			2			V
V _{IL}	Low-level input voltage			0.7			0.8	V
I _{OH}	High-level output current			-1			-2.6	mA
I _{OL}	Low-level output current			12			24	mA
f _{clock}	Clock frequency	0	25	0	0	25	30	MHz
t _w	Pulse duration	PRE or CLR low	15		10			ns
		CLK high	20		16.5			
		CLK low	20		16.5			
t _{su}	Setup time before CLK↑	Data	15		15			ns
		PRE or CLR inactive	15		10			
t _h	Hold time, data after CLK↑	4			0			ns
T _A	Operating free-air temperature	-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	SN54ALS874B			SN74ALS874B SN74ALS876A			UNIT
		MIN	TYP†	MAX	MIN	TYP†	MAX	
V _{IK}	V _{CC} = 4.5 V, I _I = -18 mA			-1.2			-1.2	V
V _{OH}	V _{CC} = 4.5 V to 5.5 V, I _{OH} = -0.4 mA	V _{CC} - 2			V _{CC} - 2			V
	V _{CC} = 4.5 V	I _{OH} = -1 mA	2.4	3.3				
		I _{OH} = -2.6 mA			2.4	3.2		
V _{OL}	V _{CC} = 4.5 V	I _{OL} = 12 mA	0.25	0.4	0.25	0.4		V
		I _{OL} = 24 mA			0.35	0.5		
I _{OZH}	V _{CC} = 5.5 V, V _O = 2.7 V		20		20		20	µA
I _{OZL}	V _{CC} = 5.5 V, V _O = 0.4 V		-20		-20		-20	µA
I _I	V _{CC} = 5.5 V, V _I = 7 V		0.1		0.1		0.1	mA
I _{IH}	V _{CC} = 5.5 V, V _I = 2.7 V		20		20		20	µA
I _{IL}	V _{CC} = 5.5 V, V _I = 0.4 V		-0.2		-0.2		-0.2	mA
I _{O‡}	V _{CC} = 5.5 V, V _O = 2.25 V	-20	-112	-30	-112	-30	-112	mA
I _{CC}	'ALS874B	Outputs high	14	21	14	21		mA
		Outputs low	19	30	19	30		
		Outputs disabled	20	32	20	32		
	SN74ALS876A	Outputs high			14	21		mA
		Outputs low			18	29		
		Outputs disabled			20	31		

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.



POST OFFICE BOX 655303 • DALLAS, TEXAS 75265
 POST OFFICE BOX 1443 • HOUSTON, TEXAS 77251-1443

**SN54ALS874B, SN74ALS874B, SN74ALS876A
SN74AS874, SN74AS876**
DUAL 4-BIT D-TYPE EDGE-TRIGGERED FLIP-FLOPS

SDAS061C – APRIL 1982 – REVISED JANUARY 1995

switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$, $C_L = 50 \text{ pF}$, $R1 = 500 \Omega$, $R2 = 500 \Omega$, $T_A = \text{MIN to MAX}^{\dagger}$				UNIT	
			SN54ALS874B		SN74ALS874B			
			MIN	MAX	MIN	MAX		
f_{max}			25	30			MHz	
t_{PLH}	CLK	Any Q	4	18	4	14	ns	
t_{PHL}			4	16	4	14		
t_{PHL}	\overline{CLR}	Any Q	5	23	5	17	ns	
t_{PZH}	\overline{OE}	Any Q	4	24	4	18	ns	
t_{PZL}			4	21	4	18		
t_{PHZ}	\overline{OE}	Any Q	2	15	2	10	ns	
t_{PLZ}			3	22	3	12		

[†] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$, $C_L = 50 \text{ pF}$, $R1 = 500 \Omega$, $R2 = 500 \Omega$, $T_A = \text{MIN to MAX}^{\dagger}$				UNIT	
			SN74ALS876A					
			MIN	MAX				
f_{max}			30				MHz	
t_{PLH}	CLK	Any \overline{Q}	4	14			ns	
t_{PHL}			4	14				
t_{PHL}	\overline{PRE}	Any \overline{Q}	6	19			ns	
t_{PZH}	\overline{OE}	Any \overline{Q}	4	18			ns	
t_{PZL}			4	18				
t_{PHZ}	\overline{OE}	Any \overline{Q}	2	10			ns	
t_{PLZ}			3	13				

[†] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[‡]

Supply voltage, V_{CC}	7 V
Input voltage, V_I	7 V
Operating free-air temperature range, T_A : SN74AS874, SN74AS876	0°C to 70°C
Storage temperature range	-65°C to 150°C

[‡] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

**SN54ALS874B, SN74ALS874B, SN74ALS876A
 SN74AS874, SN74AS876
 DUAL 4-BIT D-TYPE EDGE-TRIGGERED FLIP-FLOPS**

SDAS061C – APRIL 1982 – REVISED JANUARY 1995

recommended operating conditions

			SN74AS874			SN74AS876			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V _{IH}	High-level input voltage		2			2			V
V _{IL}	Low-level input voltage				0.8			0.8	V
I _{OH}	High-level output current				-15			-15	mA
I _{OL}	Low-level output current				48			48	mA
f _{clock}	Clock frequency		0	125		0	80		MHz
t _w	Pulse duration	PRE or CLR low		2		4.5			ns
		CLK high		3		6.2			
		CLK low		4		6.2			
t _{su}	Setup time before CLK↑	Data		2		4.5			ns
		PRE or CLR inactive		4		5			
t _h	Hold time, data after CLK↑		1			2			ns
T _A	Operating free-air temperature		0	70		0	70		°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS			SN74AS874 SN74AS876			UNIT
	MIN	TYP†	MAX	MIN	TYP†	MAX	
V _{IK}	V _{CC} = 4.5 V,	I _I = -18 mA				-1.2	V
V _{OH}	V _{CC} = 4.5 V to 5.5 V,	I _{OH} = -2 mA		V _{CC} – 2			V
	V _{CC} = 4.5 V,	I _{OH} = -15 mA		2.4	3.3		
V _{OL}	V _{CC} = 4.5 V,	I _{OL} = 48 mA		0.35	0.5		V
I _{OZH}	V _{CC} = 5.5 V,	V _O = 2.7 V		50			µA
I _{OZL}	V _{CC} = 5.5 V,	V _O = 0.4 V		-50			µA
I _I	V _{CC} = 5.5 V,	V _I = 7 V		0.1			mA
I _{IH}	V _{CC} = 5.5 V,	V _I = 2.7 V		20			µA
I _{IL}	D	V _{CC} = 5.5 V,			V _I = 0.4 V	-2	mA
	All others					-0.5	
I _O ‡		V _{CC} = 5.5 V,	V _O = 2.25 V	-30	-112		mA
I _{CC}	SN74AS874	V _{CC} = 5.5 V	Outputs high	82	133		mA
			Outputs low	92	149		
			Outputs disabled	100	160		
	SN74AS876	V _{CC} = 5.5 V	Outputs high	88	142		
			Outputs low	94	150		
			Outputs disabled	100	160		

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.



POST OFFICE BOX 655303 • DALLAS, TEXAS 75265
 POST OFFICE BOX 1443 • HOUSTON, TEXAS 77251-1443

**SN54ALS874B, SN74ALS874B, SN74ALS876A
SN74AS874, SN74AS876
DUAL 4-BIT D-TYPE EDGE-TRIGGERED FLIP-FLOPS**

SDAS061C – APRIL 1982 – REVISED JANUARY 1995

switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V},$ $C_L = 50 \text{ pF},$ $R1 = 500 \Omega,$ $R2 = 500 \Omega,$ $T_A = \text{MIN to MAX}^\dagger$		UNIT	
			SN74AS874			
			MIN	MAX		
f_{max}			125		MHz	
t_{PLH}	CLK	Any Q	3	8.5	ns	
t_{PHL}			4	10.5		
t_{PHL}	\overline{CLR}	Any Q	4	9.5	ns	
t_{PZH}	\overline{OE}	Any Q	2	7	ns	
t_{PZL}			3	10.5		
t_{PHZ}	\overline{OE}	Any Q	2	6	ns	
t_{PLZ}			2	7.5		

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

switching characteristics (see Figure 1)

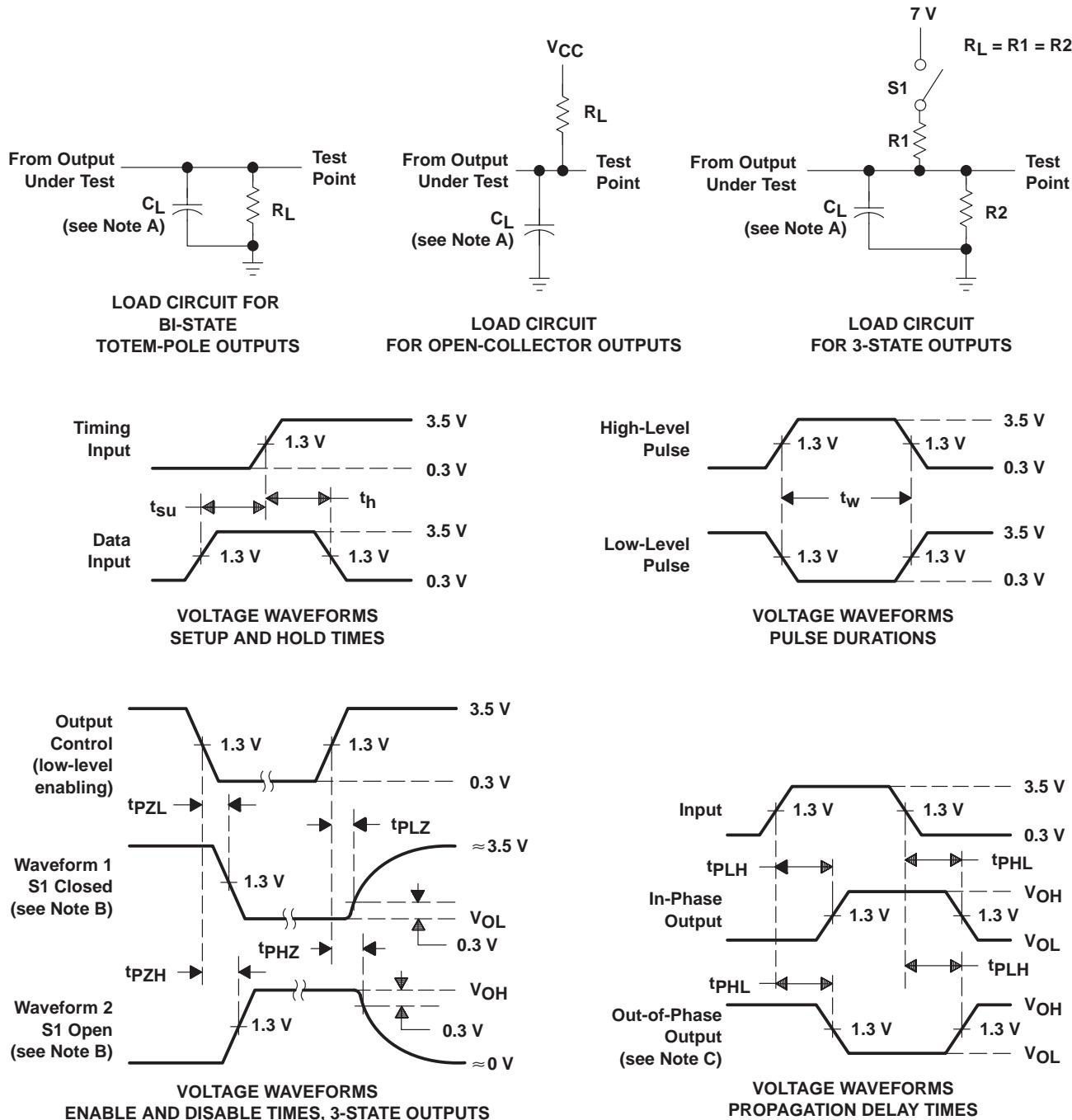
PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V},$ $C_L = 50 \text{ pF},$ $R1 = 500 \Omega,$ $R2 = 500 \Omega,$ $T_A = \text{MIN to MAX}^\dagger$		UNIT	
			SN74AS876			
			MIN	MAX		
f_{max}			80		MHz	
t_{PLH}	CLK	Any \overline{Q}	3	8.5	ns	
t_{PHL}			4	10.5		
t_{PHL}	\overline{PRE}	Any \overline{Q}	4	9.5	ns	
t_{PZH}	\overline{OE}	Any \overline{Q}	2	7	ns	
t_{PZL}			3	11		
t_{PHZ}	\overline{OE}	Any \overline{Q}	2	7	ns	
t_{PLZ}			2	7		

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

**SN54ALS874B, SN74ALS874B, SN74ALS876A
SN74AS874, SN74AS876
DUAL 4-BIT D-TYPE EDGE-TRIGGERED FLIP-FLOPS**

SDAS061C - APRIL 1982 - REVISED JANUARY 1995

**PARAMETER MEASUREMENT INFORMATION
SERIES 54ALS/74ALS AND 54AS/74AS DEVICES**



NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. When measuring propagation delay items of 3-state outputs, switch S1 is open.
 D. All input pulses have the following characteristics: $PRR \leq 1 \text{ MHz}$, $t_r = t_f = 2 \text{ ns}$, duty cycle = 50%.
 E. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
84010013A	ACTIVE	LCCC	FK	28	1	TBD	POST-PLATE	N / A for Pkg Type
8401001KA	OBsolete	CFP	W	24		TBD	Call TI	Call TI
8401001LA	ACTIVE	CDIP	JT	24	1	TBD	A42	N / A for Pkg Type
SN54ALS874BJT	ACTIVE	CDIP	JT	24	1	TBD	A42	N / A for Pkg Type
SN74ALS874BDW	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALS874BDWE4	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALS874BDWG4	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALS874BDWR	ACTIVE	SOIC	DW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALS874BDWRE4	ACTIVE	SOIC	DW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALS874BDWRG4	ACTIVE	SOIC	DW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALS874BNSRE4	ACTIVE	SO	NS	24		TBD	Call TI	Call TI
SN74ALS874BNSRG4	ACTIVE	SO	NS	24		TBD	Call TI	Call TI
SN74ALS874BNT	ACTIVE	PDIP	NT	24	15	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74ALS874BNTE4	ACTIVE	PDIP	NT	24	15	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74ALS876ADW	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALS876ADWE4	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALS876ADWG4	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALS876ADWRE4	ACTIVE	SOIC	DW	24		TBD	Call TI	Call TI
SN74ALS876ADWRG4	ACTIVE	SOIC	DW	24		TBD	Call TI	Call TI
SN74ALS876ANT	ACTIVE	PDIP	NT	24	15	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74ALS876ANTE4	ACTIVE	PDIP	NT	24	15	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74AS874DW	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AS874DWE4	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AS874DWG4	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AS874DWRE4	ACTIVE	SOIC	DW	24		TBD	Call TI	Call TI
SN74AS874DWRG4	ACTIVE	SOIC	DW	24		TBD	Call TI	Call TI
SN74AS874NT	ACTIVE	PDIP	NT	24	15	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74AS874NTE4	ACTIVE	PDIP	NT	24	15	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74AS876DW	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
SN74AS876DWE4	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AS876DWG4	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AS876DWRE4	ACTIVE	SOIC	DW	24		TBD	Call TI	Call TI
SN74AS876DWRG4	ACTIVE	SOIC	DW	24		TBD	Call TI	Call TI
SN74AS876NT	ACTIVE	PDIP	NT	24	15	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74AS876NTE4	ACTIVE	PDIP	NT	24	15	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SNJ54ALS874BFK	ACTIVE	LCCC	FK	28	1	TBD	POST-PLATE	N / A for Pkg Type
SNJ54ALS874BJT	ACTIVE	CDIP	JT	24	1	TBD	A42	N / A for Pkg Type

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

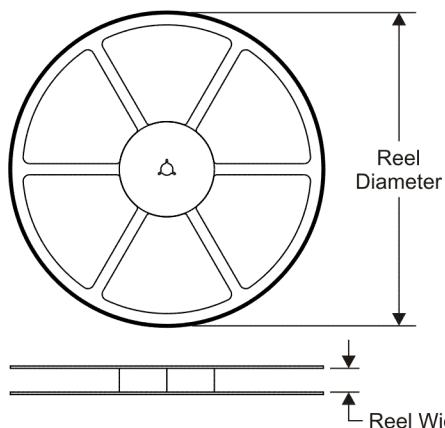
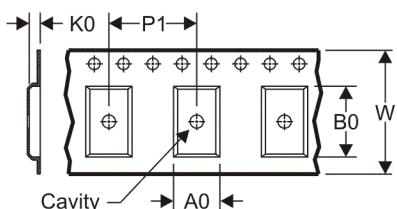
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

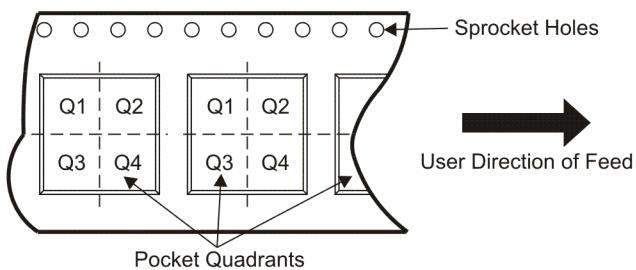
⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

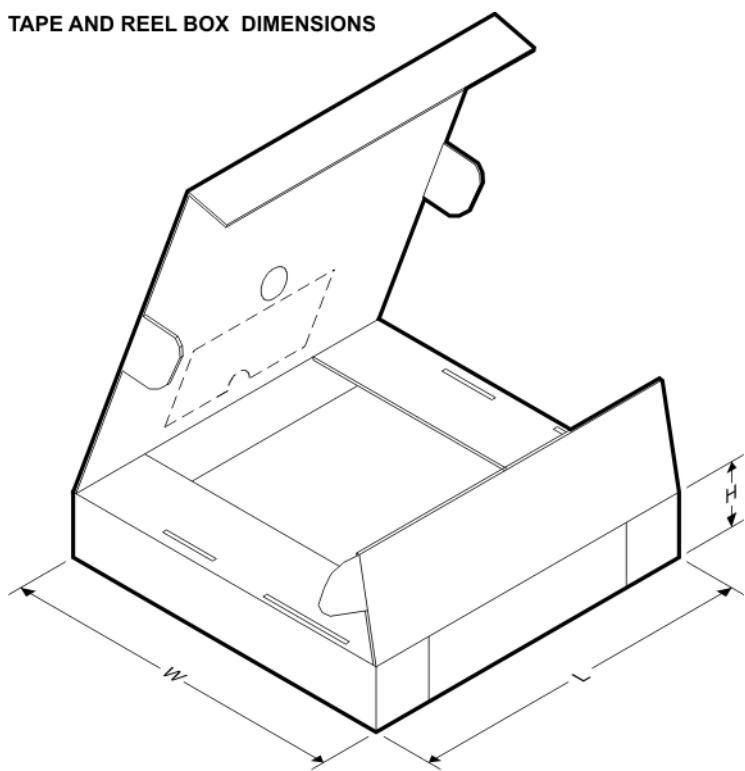
TAPE AND REEL INFORMATION
REEL DIMENSIONS

TAPE DIMENSIONS


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74ALS874BDWR	SOIC	DW	24	2000	330.0	24.4	10.75	15.7	2.7	12.0	24.0	Q1

TAPE AND REEL BOX DIMENSIONS

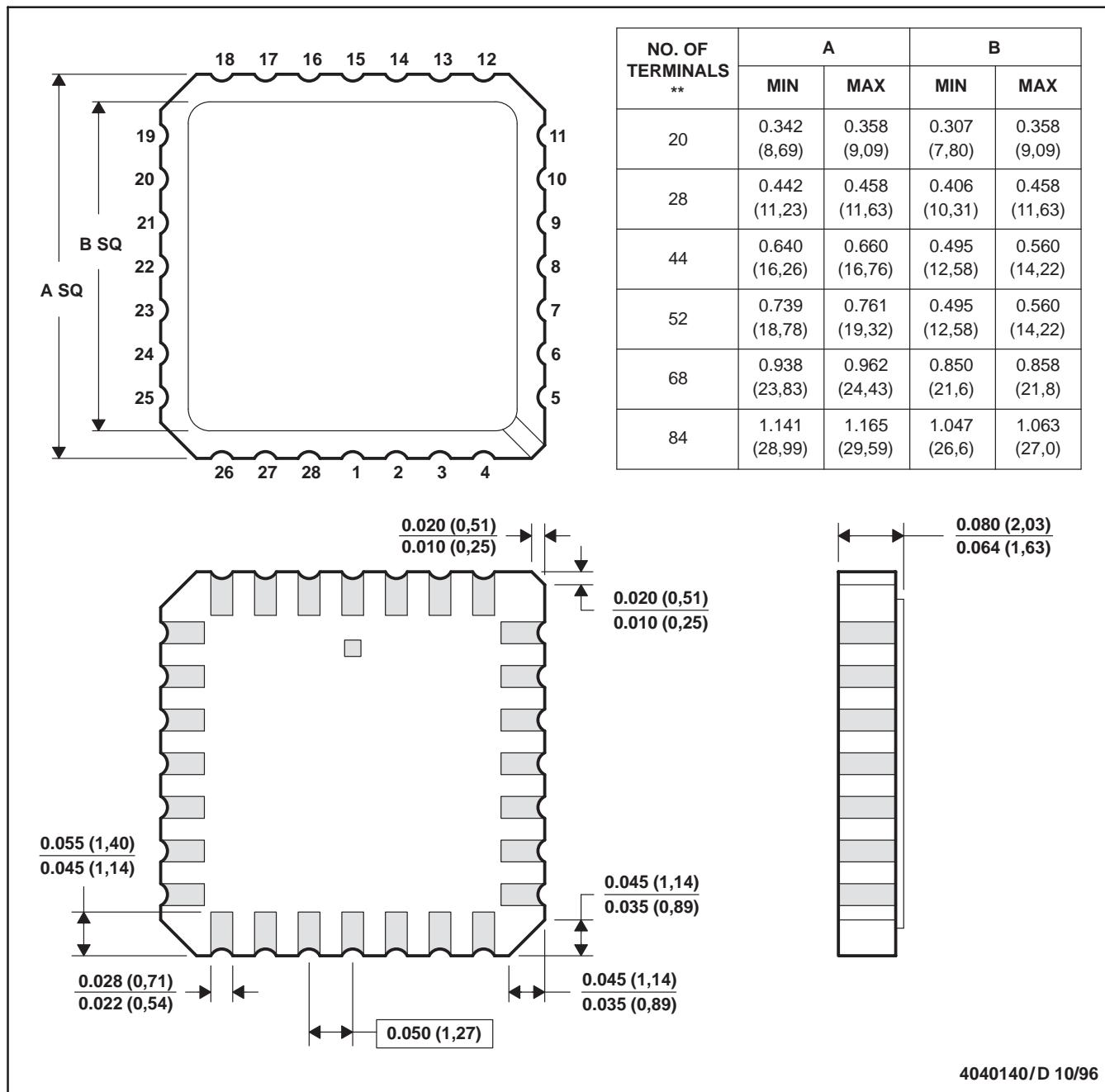
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74ALS874BDWR	SOIC	DW	24	2000	346.0	346.0	41.0

FK (S-CQCC-N**)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



NOTES:

- All linear dimensions are in inches (millimeters).
- This drawing is subject to change without notice.
- This package can be hermetically sealed with a metal lid.
- The terminals are gold plated.
- Falls within JEDEC MS-004

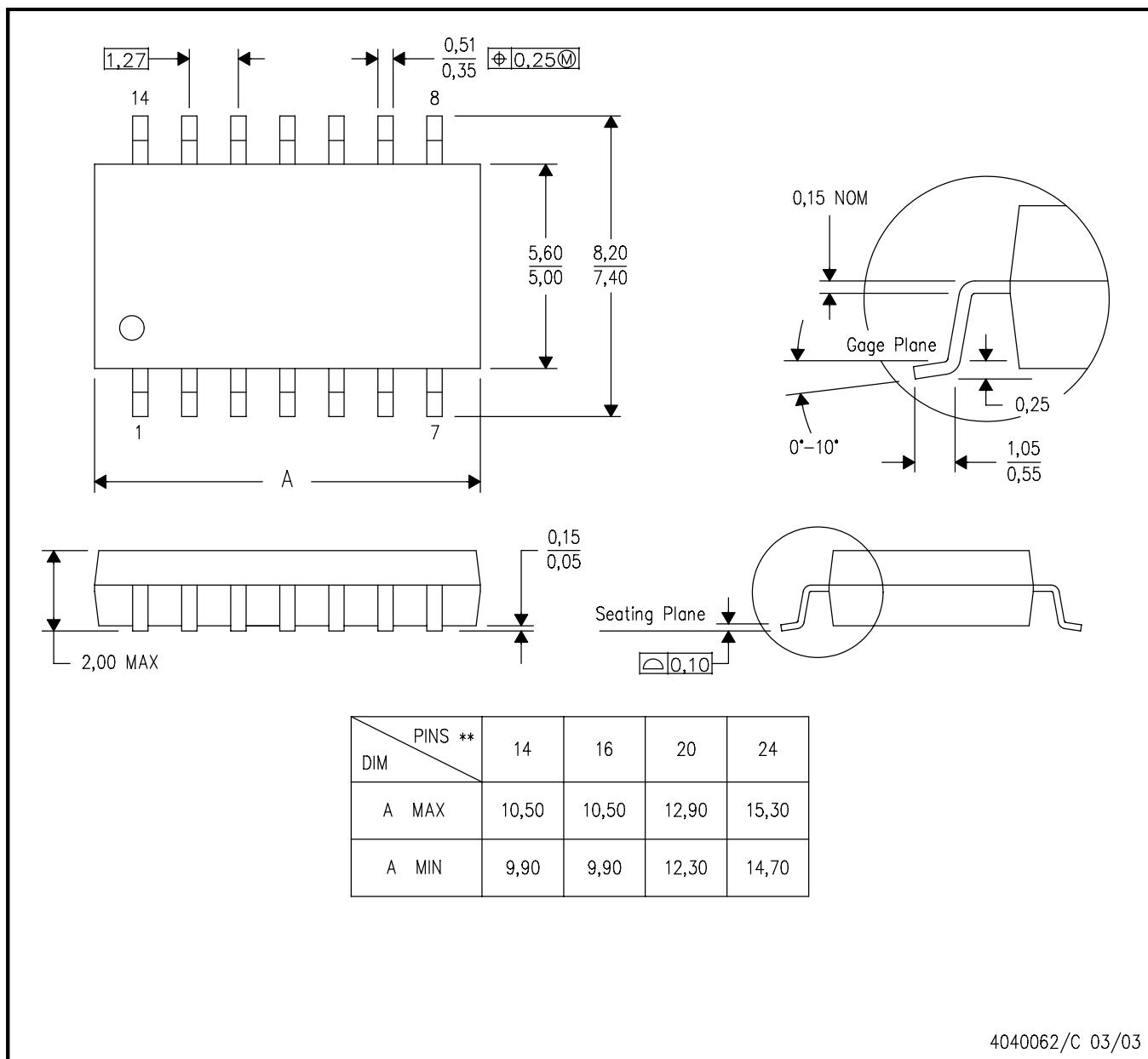
4040140/D 10/96

MECHANICAL DATA

NS (R-PDSO-G**)

14-PINS SHOWN

PLASTIC SMALL-OUTLINE PACKAGE



4040062/C 03/03

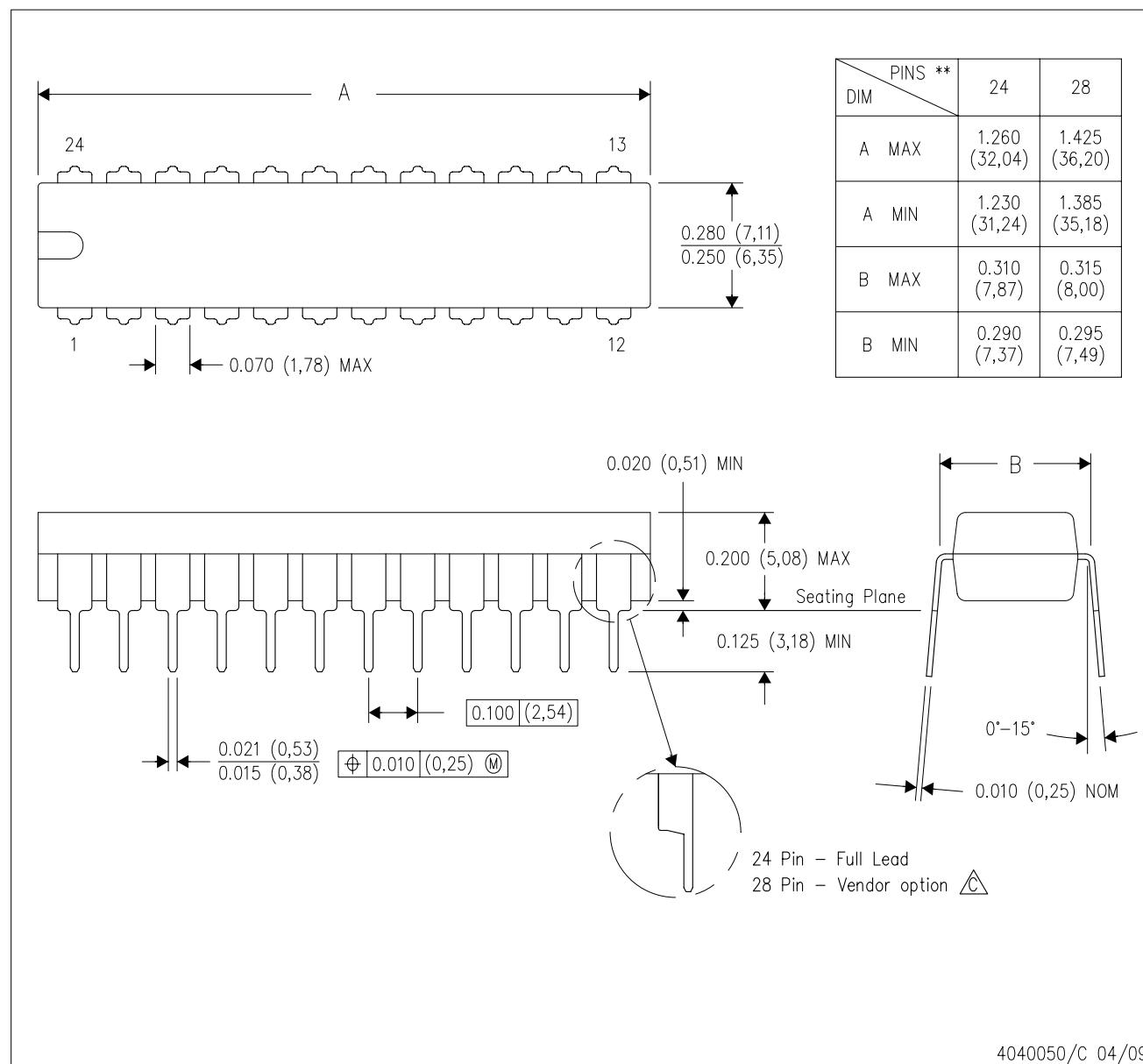
NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

MECHANICAL DATA

NT (R-PDIP-T**)

24 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



4040050/C 04/09

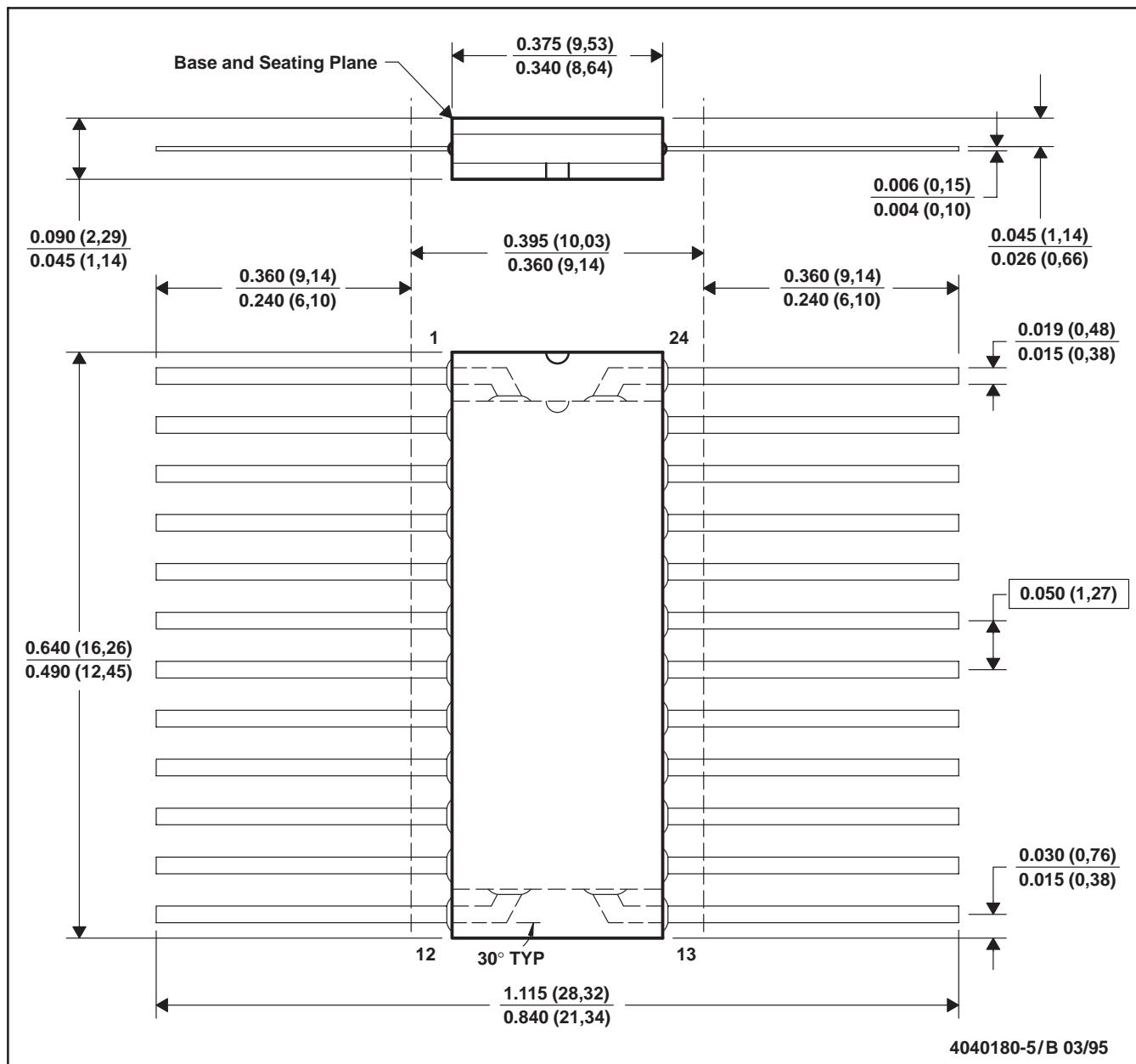
NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.

B. This drawing is subject to change without notice.

\triangle The 28 pin end lead shoulder width is a vendor option, either half or full width.

W (R-GDFP-F24)

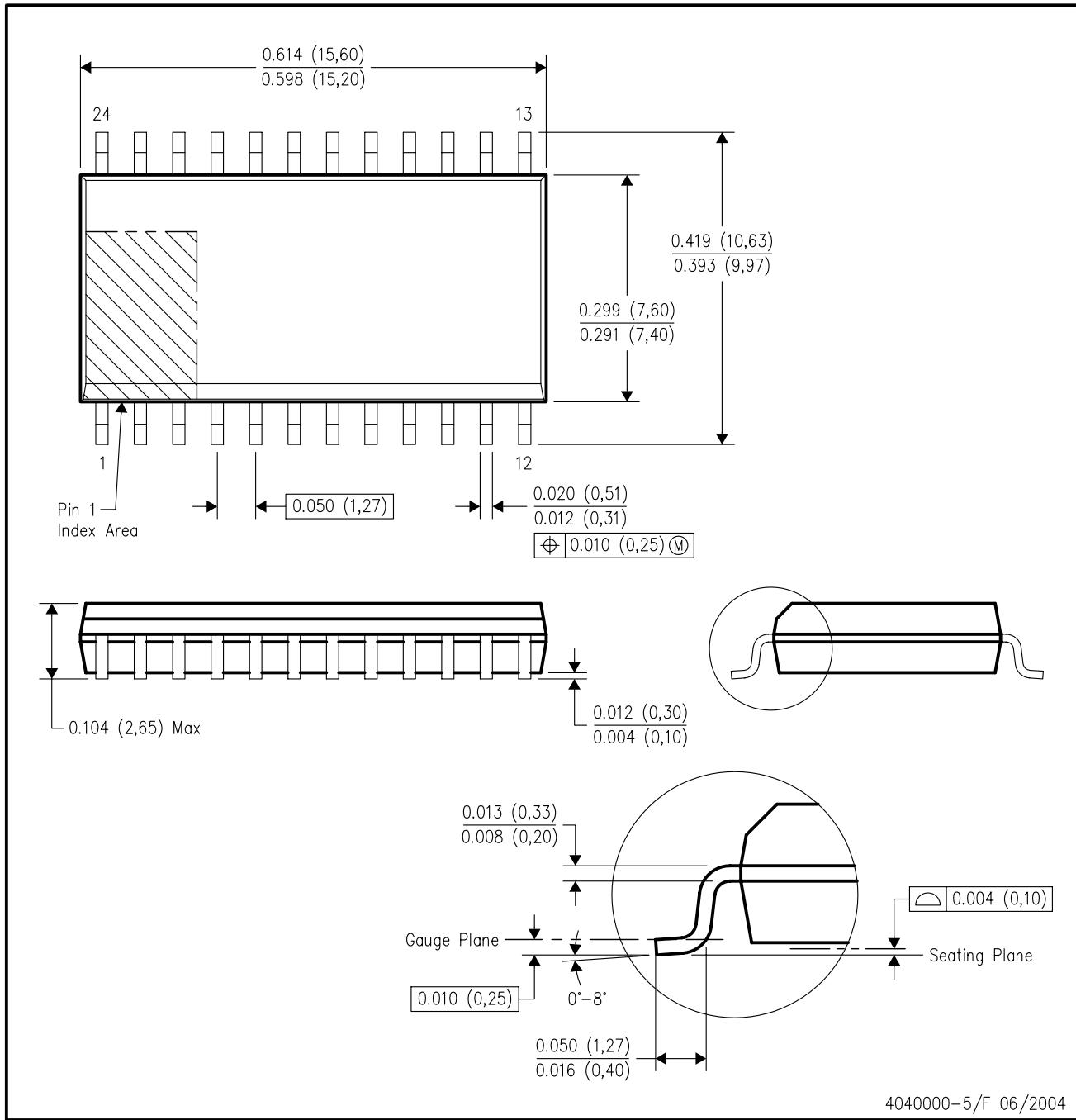
CERAMIC DUAL FLATPACK



NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. This package can be hermetically sealed with a ceramic lid using glass frit.
 D. Falls within MIL-STD-1835 GDFP2-F24 and JEDEC MO-070AD
 E. Index point is provided on cap for terminal identification only.

DW (R-PDSO-G24)

PLASTIC SMALL-OUTLINE PACKAGE



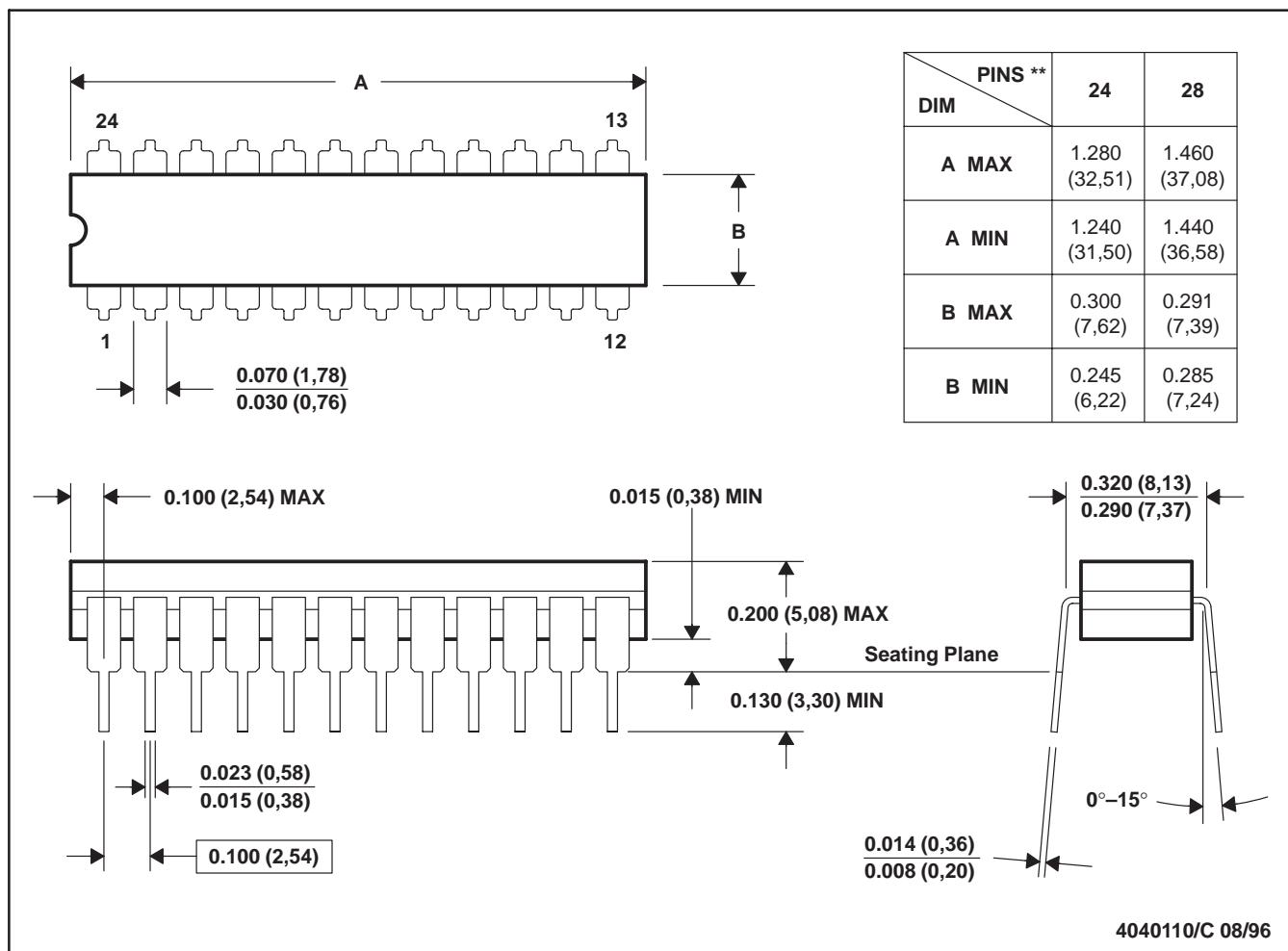
NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
- D. Falls within JEDEC MS-013 variation AD.

JT (R-GDIP-T**)

24 LEADS SHOWN

CERAMIC DUAL-IN-LINE



NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. This package can be hermetically sealed with a ceramic lid using glass frit.
 D. Index point is provided on cap for terminal identification.
 E. Falls within MIL STD 1835 GDIP3-T24, GDIP4-T28, and JEDEC MO-058 AA, MO-058 AB

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

TI products are not authorized for use in safety-critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, unless officers of the parties have executed an agreement specifically governing such use. Buyers represent that they have all necessary expertise in the safety and regulatory ramifications of their applications, and acknowledge and agree that they are solely responsible for all legal, regulatory and safety-related requirements concerning their products and any use of TI products in such safety-critical applications, notwithstanding any applications-related information or support that may be provided by TI. Further, Buyers must fully indemnify TI and its representatives against any damages arising out of the use of TI products in such safety-critical applications.

TI products are neither designed nor intended for use in military/aerospace applications or environments unless the TI products are specifically designated by TI as military-grade or "enhanced plastic." Only products designated by TI as military-grade meet military specifications. Buyers acknowledge and agree that any such use of TI products which TI has not designated as military-grade is solely at the Buyer's risk, and that they are solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI products are neither designed nor intended for use in automotive applications or environments unless the specific TI products are designated by TI as compliant with ISO/TS 16949 requirements. Buyers acknowledge and agree that, if they use any non-designated products in automotive applications, TI will not be responsible for any failure to meet such requirements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products

Amplifiers	amplifier.ti.com
Data Converters	dataconverter.ti.com
DLP® Products	www.dlp.com
DSP	dsp.ti.com
Clocks and Timers	www.ti.com/clocks
Interface	interface.ti.com
Logic	logic.ti.com
Power Mgmt	power.ti.com
Microcontrollers	microcontroller.ti.com
RFID	www.ti-rfid.com
RF/IF and ZigBee® Solutions	www.ti.com/lprf

Applications

Audio	www.ti.com/audio
Automotive	www.ti.com/automotive
Broadband	www.ti.com/broadband
Digital Control	www.ti.com/digitalcontrol
Medical	www.ti.com/medical
Military	www.ti.com/military
Optical Networking	www.ti.com/opticalnetwork
Security	www.ti.com/security
Telephony	www.ti.com/telephony
Video & Imaging	www.ti.com/video
Wireless	www.ti.com/wireless

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

Copyright © 2009, Texas Instruments Incorporated