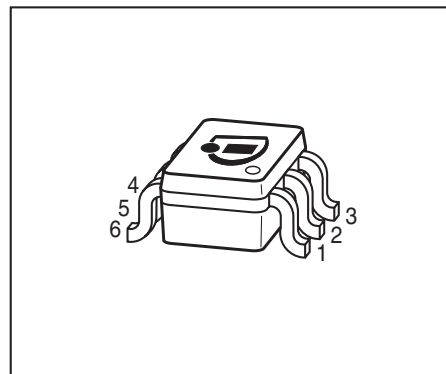


DUAL N-Channel MOSFET Tetrode

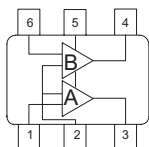
- Designed for input stages of 2 band tuners
- Two AGC amplifiers in one single package with on-chip internal switch
- Only one switching line to control both FETs
- Integrated gate protection diodes
- High gain, low noise figure, high AGC-range
- Good cross modulation at gain reduction
- Pb-free (RoHS compliant) package
- Qualified according AEC Q101



Detailed functional diagram on page 4



BG3430R



ESD (Electrostatic discharge) sensitive device, observe handling precaution!

Type	Package	Pin Configuration						Marking
BG3430R	SOT363	1=G1*	2=S	3=D*	4=D**	5=G2	6=G1**	KNs

* For amp. A; ** for amp. B

180° rotated tape loading orientation available

Maximum Ratings

Parameter	Symbol	Value	Unit
Drain-source voltage	V_{DS}	8	V
Continuous drain current	I_D	25	mA
Gate 1/ gate 2-source current	$\pm I_{G1/2SM}$	1	
Gate 1/ gate 2-source voltage	$\pm V_{G1/G2S}$	6	V
Total power dissipation	P_{tot}	200	mW
Storage temperature	T_{stg}	-55 ... 150	°C
Channel temperature	T_{ch}	150	

Thermal Resistance

Parameter	Symbol	Value	Unit
Channel - soldering point ¹⁾	R_{thchs}	≤ 280	K/W

¹⁾For calculation of R_{thJA} please refer to Application Note Thermal Resistance

Electrical Characteristics at $T_A = 25^\circ\text{C}$, unless otherwise specified

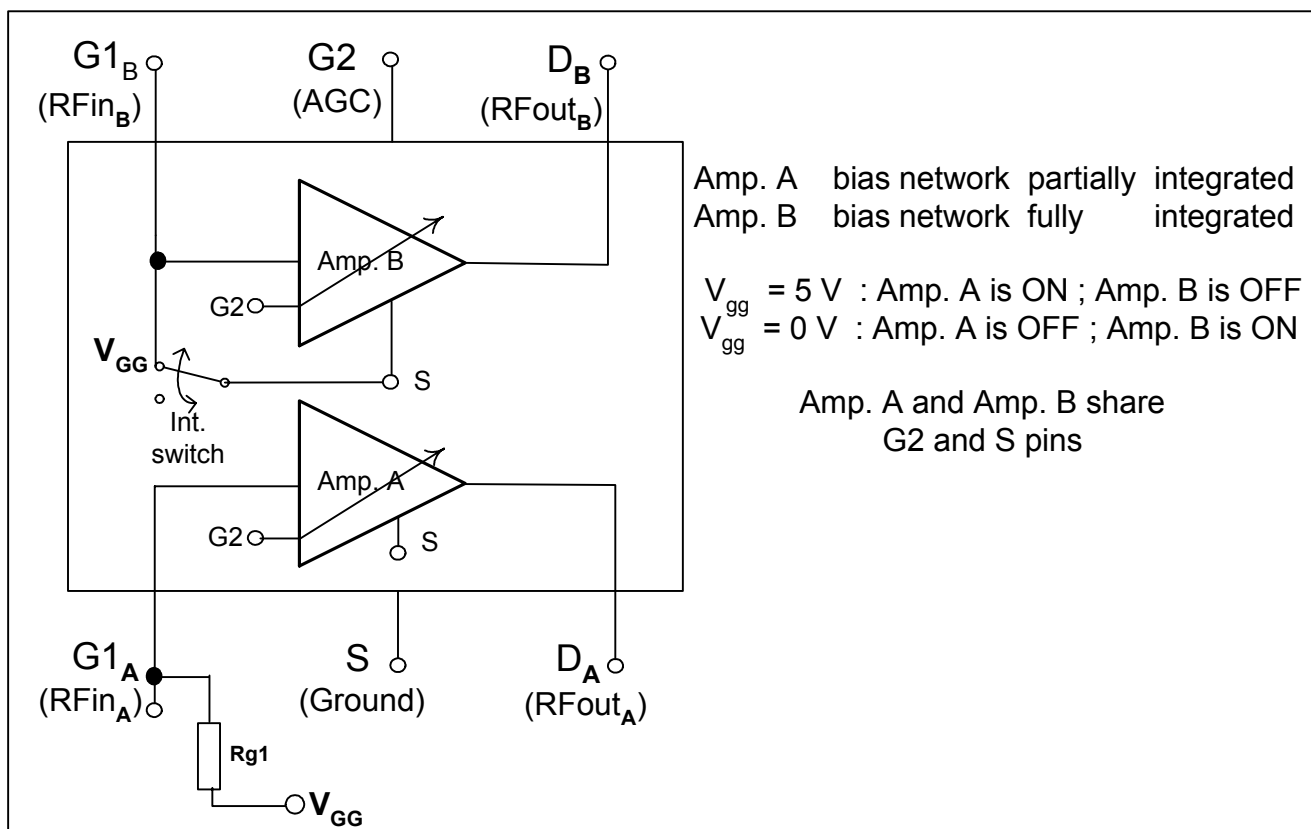
Parameter	Symbol	Values			Unit
		min.	typ.	max.	
DC Characteristics					
Drain-source breakdown voltage $I_D = 100\ \mu\text{A}$, $V_{G1S} = 0\ \text{V}$, $V_{G2S} = 0\ \text{V}$	$V_{(\text{BR})\text{DS}}$	12	-	-	V
Gate1-source breakdown voltage $+I_{G1S} = 10\ \text{mA}$, $V_{G2S} = 0\ \text{V}$, $V_{\text{DS}} = 0\ \text{V}$	$+V_{(\text{BR})\text{G1SS}}$	6	-	15	
Gate2-source breakdown voltage $+I_{G2S} = 10\ \text{mA}$, $V_{G1S} = 0\ \text{V}$, $V_{\text{DS}} = 0\ \text{V}$	$+V_{(\text{BR})\text{G2SS}}$	6	-	15	
Gate1-source leakage current $V_{G1S} = 6\ \text{V}$, $V_{G2S} = 0\ \text{V}$	$+I_{\text{G1SS}}$	-	-	5	μA
Gate2-source leakage current $V_{G2S} = 6\ \text{V}$, $V_{G1S} = 0\ \text{V}$, $V_{\text{DS}} = 0\ \text{V}$	$+I_{\text{G2SS}}$	-	-	50	nA
Drain current $V_{\text{DS}} = 5\ \text{V}$, $V_{G1S} = 0\ \text{V}$, $V_{G2S} = 4\ \text{V}$	I_{DSS}	-	-	100	μA
Operating current (selfbiased) $V_{\text{DS}} = 5\ \text{V}$, $V_{G2S} = 4\ \text{V}$, amp.B	I_{DSO}	-	13	-	mA
Drain-source current $V_{\text{DS}} = 5\ \text{V}$, $V_{G2S} = 4\ \text{V}$, $R_{G1} = 100\ \text{k}\Omega$, amp. A	I_{DSX}	-	13	-	
Gate1-source pinch-off voltage $V_{\text{DS}} = 5\ \text{V}$, $V_{G2S} = 4\ \text{V}$, $I_D = 100\ \mu\text{A}$	$V_{\text{G1S(p)}}$	-	0.5	-	V
Gate2-source pinch-off voltage $V_{\text{DS}} = 5\ \text{V}$, $I_D = 100\ \mu\text{A}$	$V_{\text{G2S(p)}}$	-	0.6	-	

Electrical Characteristics at $T_A = 25^\circ\text{C}$, unless otherwise specified

Parameter	Symbol	Values			Unit
		min.	typ.	max.	
AC Characteristics $V_{DS} = 5V$, $V_{G2S} = 4V$, ($I_D = 14\text{ mA}$) (verified by random sampling)					
Forward transconductance	g_{fs}	-	33	-	mS
Gate1 input capacitance $f = 10\text{ MHz}$	C_{g1ss}	-	1.9	-	pF
Output capacitance $f = 10\text{ MHz}$	C_{dss}	-	1.3	-	
Power gain $f = 800\text{ MHz}$ $f = 45\text{ MHz}$	G_p	- -	25 33	- -	dB
Noise figure $f = 800\text{ MHz}$ $f = 45\text{ MHz}$	F	- -	1.3 1	- -	
Gain control range $V_{G2S} = 4 \dots 0\text{ V}$, $f = 800\text{ MHz}$	ΔG_p	45	-	-	
Cross-modulation $k=1\%$, $f_w=50\text{MHz}$, $f_{unw}=60\text{MHz}$ AGC = 0 dB AGC = 10 dB AGC = 40 dB	X_{mod}	90 - -	- 93 105	- - -	-

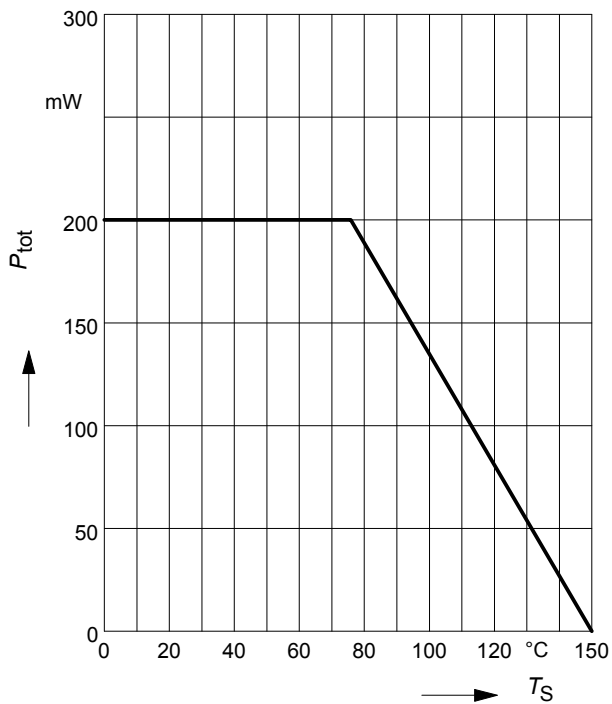
Functional diagram

a) shows pinning of BG3430R.



Total power dissipation $P_{\text{tot}} = f(T_S)$

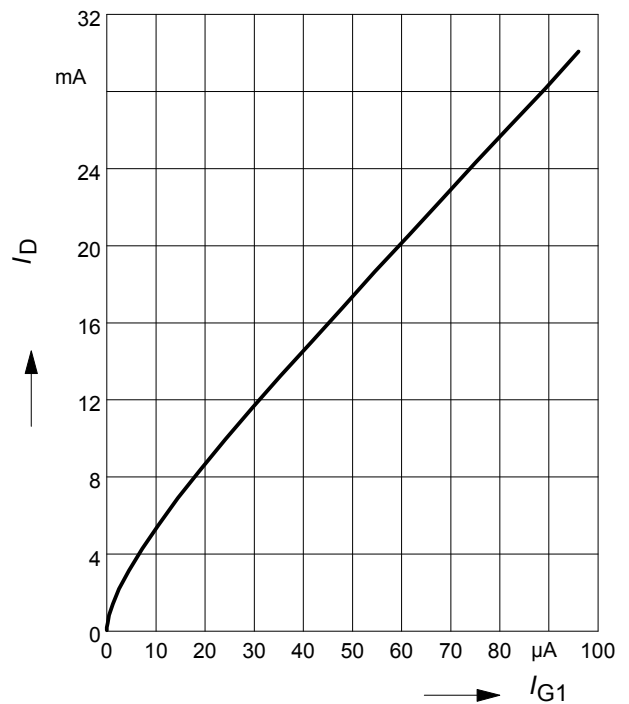
amp. A = amp. B



Drain current $I_D = f(I_{G1})$

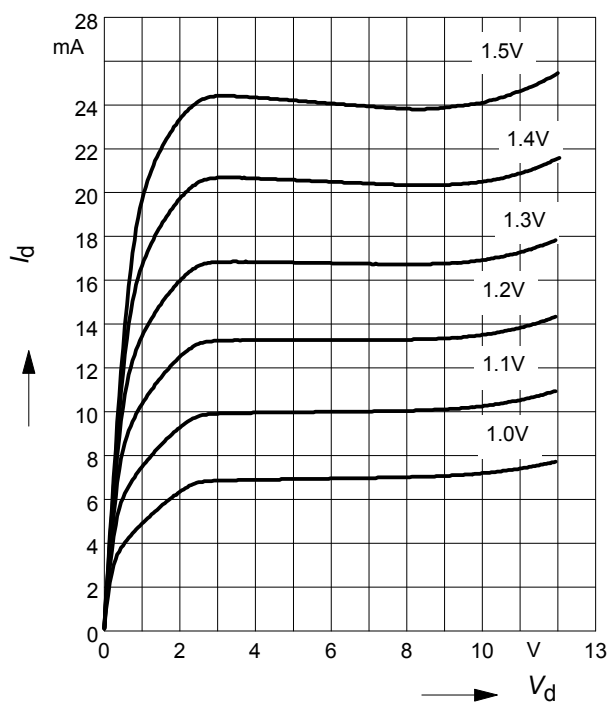
$V_{G2S} = 4V$

amp. A



Output characteristics $I_D = f(V_{DS})$

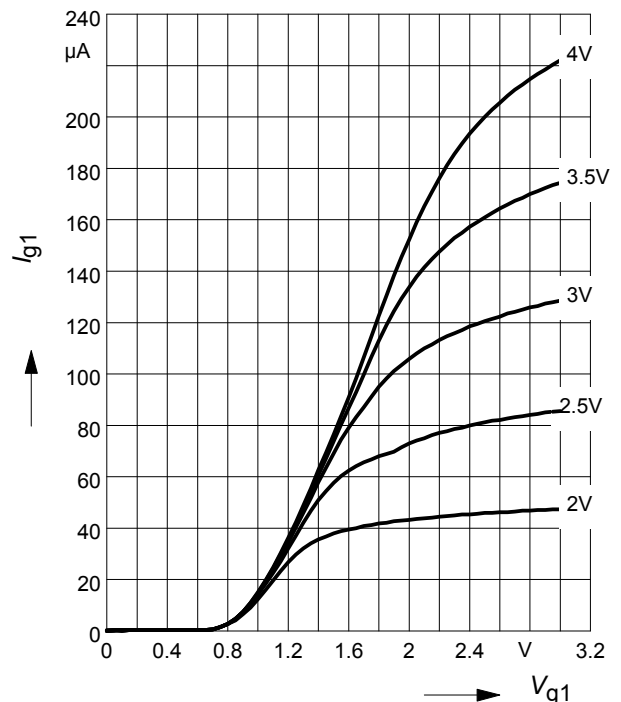
amp. A = amp. B



Gate 1 current $I_{G1} = f(V_{G1S})$

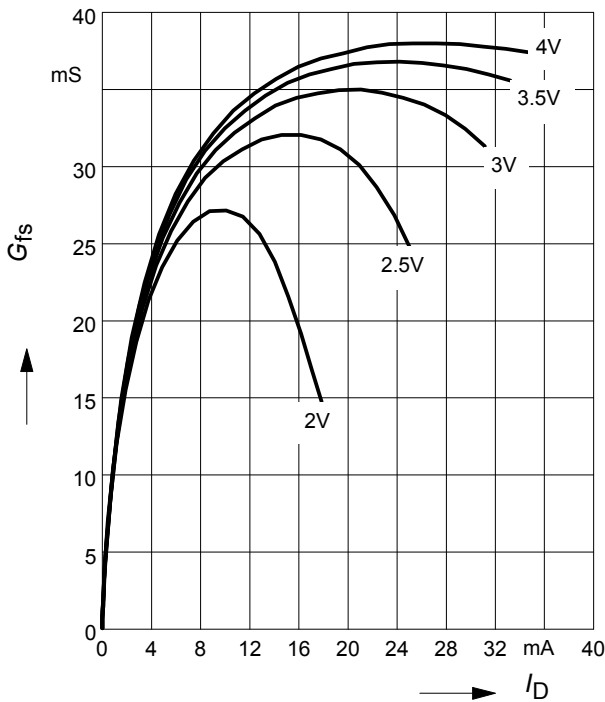
$V_{DS} = 5V$, $V_{G2S} = \text{Parameter}$

amp. A

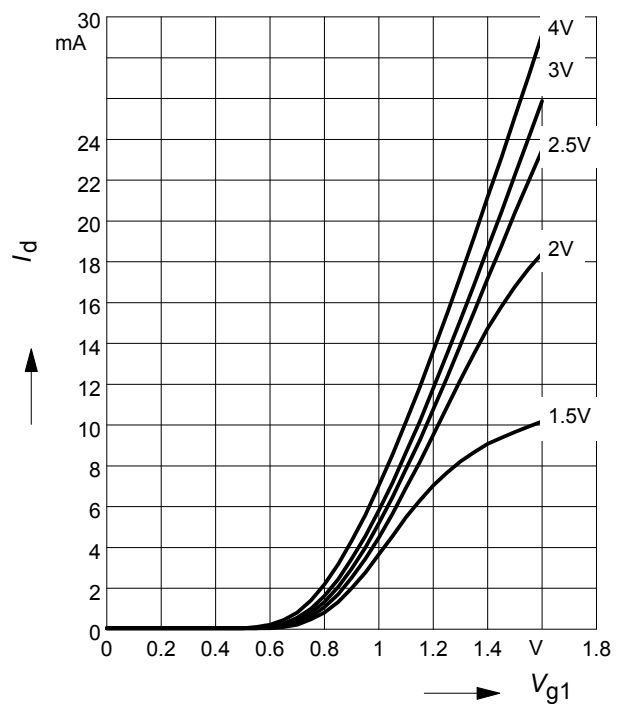


Gate 1 forward transconductance

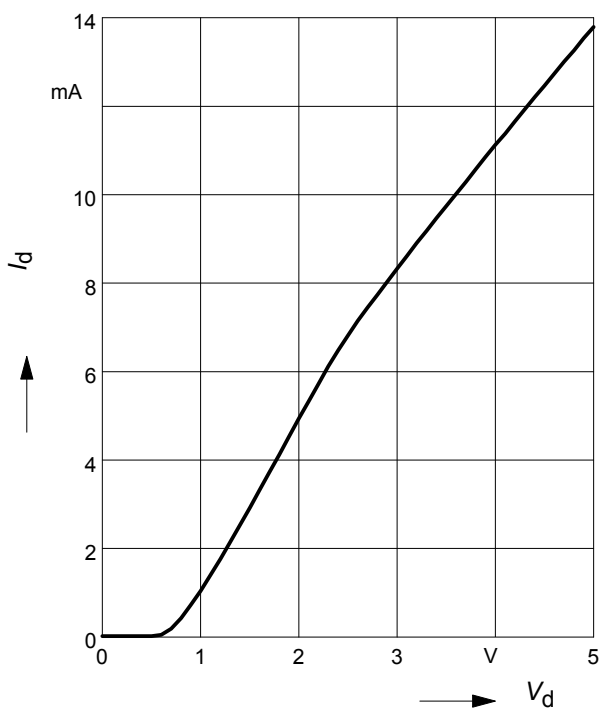
$g_{fs} = f(I_D)$, $V_{DS} = 5V$, $V_{G2S} = \text{Parameter}$
amp. A = amp. B


Drain current $I_D = f(V_{G1S})$

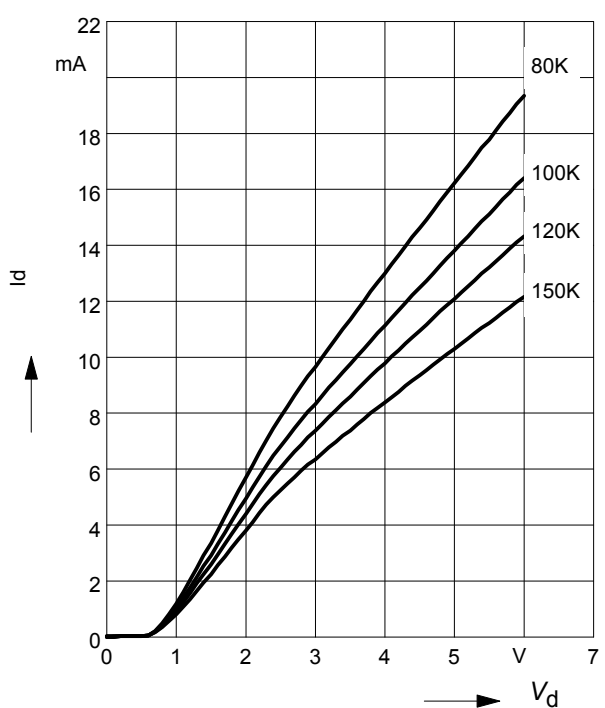
$V_{DS} = 5V$, $V_{G2S} = \text{Parameter}$
amp. A = amp. B

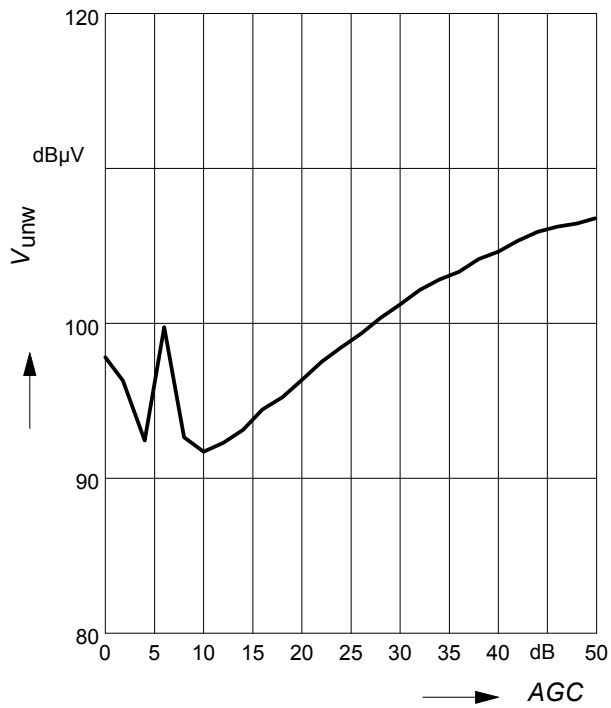

Drain current $I_D = f(V_{GG})$ amp.A

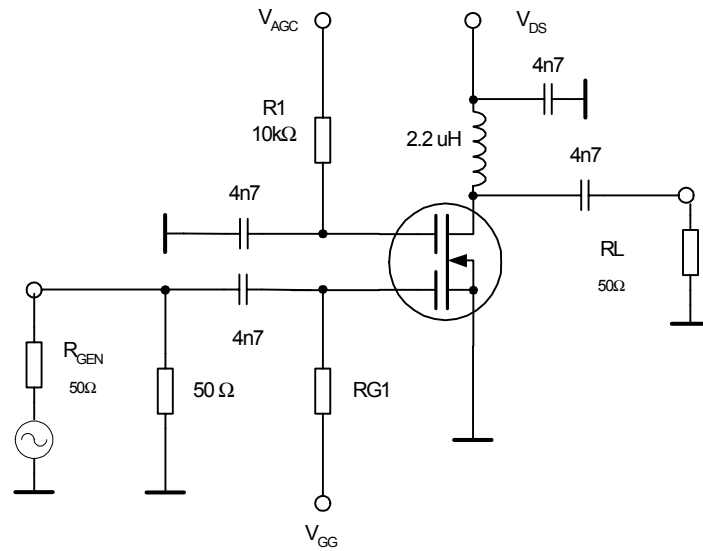
$V_{DS} = 5V$, $V_{G2S} = 4V$, $R_{G1} = 100k\Omega$
(connected to V_{GG} , $V_{GG} = \text{gate1 supply voltage}$)


Drain current $I_D = f(V_{GG})$

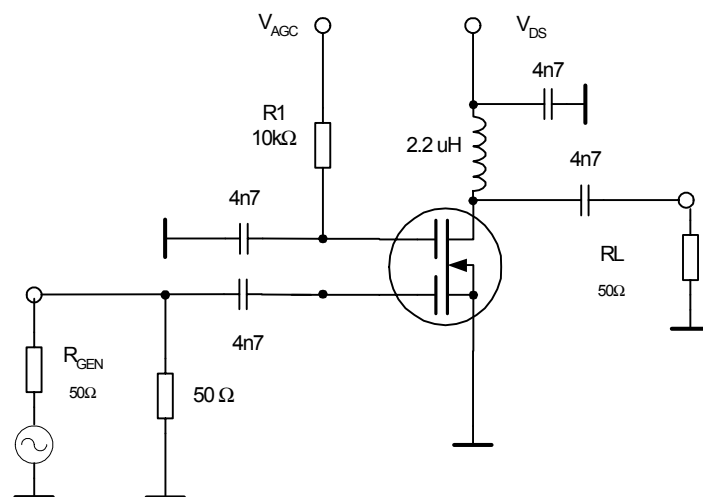
$V_{G2S} = 4V$, $R_{G1} = \text{Parameter in } k\Omega$
amp. A



Crossmodulation $V_{unw} = (AGC)$
 $V_{DS} = 5 \text{ V}$, amp. A = amp. B


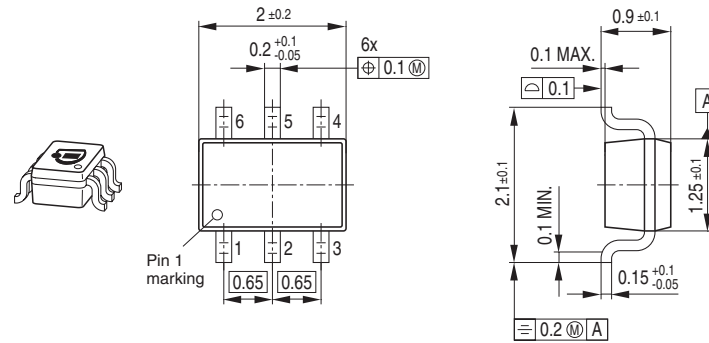
Crossmodulation test circuit


Semibiased



fullbiased

Package Outline



Foot Print



Marking Layout (Example)

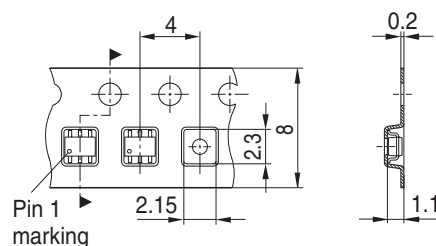
Small variations in positioning of Date code, Type code and Manufacture are possible.



Standard Packing

Reel $\varnothing 180 \text{ mm}$ = 3.000 Pieces/Reel
Reel $\varnothing 330 \text{ mm}$ = 10.000 Pieces/Reel

For symmetric types no defined Pin 1 orientation in reel.



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