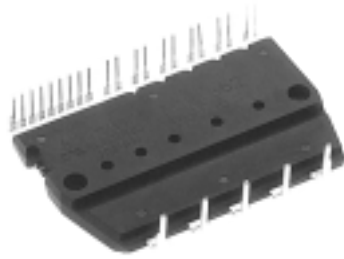


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INTEGRATED POWER FUNCTIONS

4th generation (planar) IGBT inverter bridge for three phase DC-to-AC power conversion.

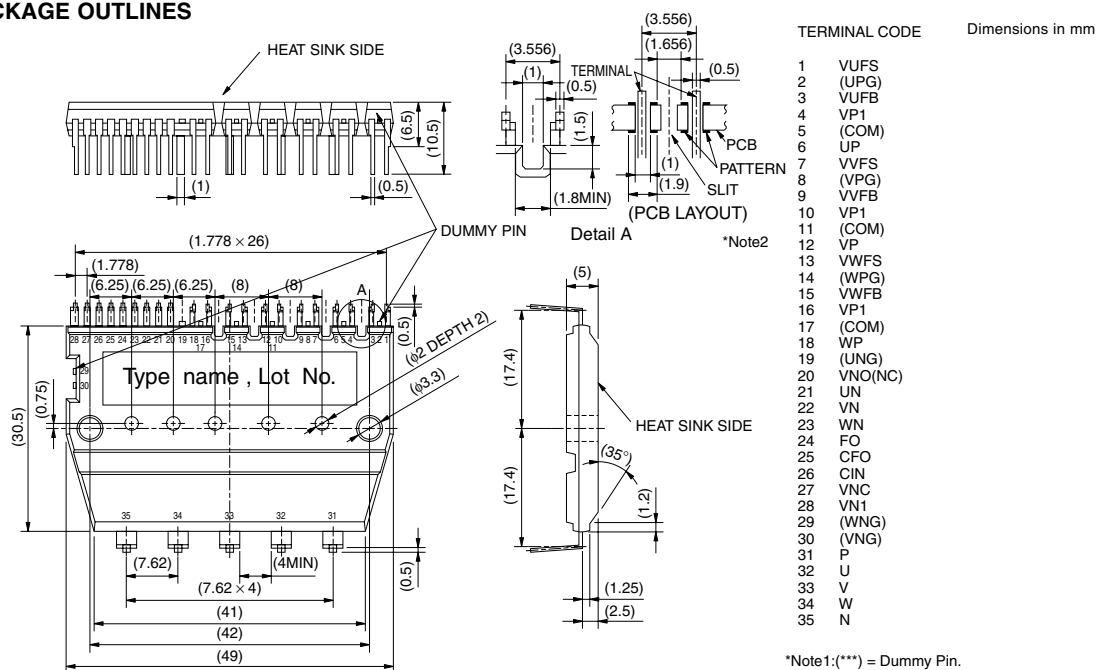
INTEGRATED DRIVE, PROTECTION AND SYSTEM CONTROL FUNCTIONS

- For upper-leg IGBTs : Drive circuit, High voltage isolated high-speed level shifting, Control circuit under-voltage (UV) protection.
Note : Bootstrap supply scheme can be applied.
- For lower-leg IGBTs : Drive circuit, Control circuit under-voltage protection (UV), Short-circuit protection (SC).
- Fault signaling : Corresponding to a SC fault (Low-side IGBT) or a UV fault (Low-side IGBT).
- Input interface : 5V line CMOS/TTL compatible, Schmitt Trigger receiver circuit.

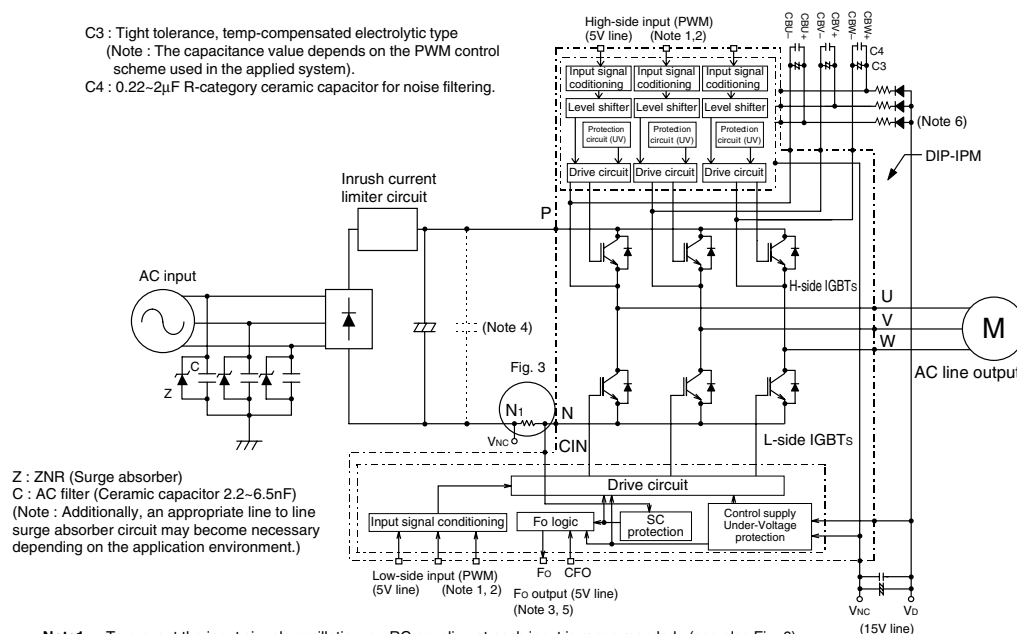
APPLICATION

AC100V~200V three-phase inverter drive for small power motor control.

Fig. 1 PACKAGE OUTLINES



C3 : Tight tolerance, temp-compensated electrolytic type
(Note : The capacitance value depends on the PWM control
scheme used in the applied system).
C4 : 0.22~2uF R-category ceramic capacitor for noise filtering.

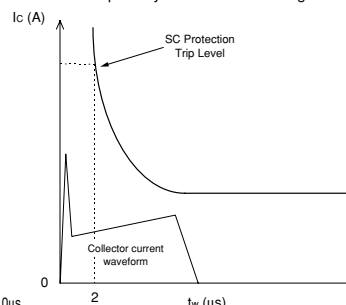


- Note1:** To prevent the input signals oscillation, an RC coupling at each input is recommended. (see also Fig. 6) (15V line)
- 2:** By virtue of integrating an application specific type HVIC inside the module, direct coupling to CPU terminals without any opto-coupler or transformer isolation is possible. (see also Fig. 6)
- 3:** This output is open collector type. The signal line should be pulled up to the positive side of the 5V power supply with approximately 5.1kΩ resistance. (see also Fig. 6)
- 4:** The wiring between the power DC link capacitor and the P/N1 terminals should be as short as possible to protect the DIP-IPM against catastrophic high surge voltages. For extra precaution, a small film type snubber capacitor (0.1~0.22μF, high voltage type) is recommended to be mounted close to these P and N1 DC power input terminals.
- 5:** Fo output pulse width should be decided by connecting external capacitor between CFO and V_{NC} terminals. (Example : CFO=22nF → tFO=1.8ms (Typ.))
- 6:** High voltage (600V or more) and fast recovery type (less than 100ns) diodes should be used in the bootstrap circuit.

The diagram illustrates the internal structure of a DIP-IPM. It features two main drive circuits, one for the upper half and one for the lower half, each containing three IGBTs (H-side and L-side) and three anti-parallel diodes. The module is connected to a three-phase supply (U, V, W) and a neutral point (N). An external protection circuit is shown, consisting of a shunt resistor (R) and a capacitor (C) connected between the supply and the module's input terminals (A, B, C). The protection circuit is also connected to the module's internal protection circuit, which includes a Vnc (negative common) terminal and a CIN (common input) terminal. The module is labeled DIP-IPM.

- Note1:** In the recommended external protection circuit, please select the RC time constant in the range 1.5~2.0μs.
2: To prevent erroneous protection operation, the wiring of A, B, C should be as short as possible.

Short Circuit Protective Function (SC) :
SC protection is achieved by sensing the L-side DC-Bus current (through the external shunt resistor) after allowing a suitable filtering time (defined by the RC circuit). When the sensed shunt voltage exceeds the SC trip-level, all the L-side IGBTs are turned OFF and a fault signal (Fo) is output. Since the SC fault may be repetitive, it is recommended to stop the system when the Fo signal is received and check the fault.



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MAXIMUM RATINGS (T_j = 25°C, unless otherwise noted)

INVERTER PART

Symbol	Parameter	Condition	Ratings	Unit
V _{CC}	Supply voltage	Applied between P-N	450	V
V _{CC(surge)}	Supply voltage (surge)	Applied between P-N	500	V
V _{CES}	Collector-emitter voltage		600	V
±I _C	Each IGBT collector current	T _f = 25°C	5	A
±I _{CP}	Each IGBT collector current (peak)	T _f = 25°C, instantaneous value (pulse)	10	A
P _C	Collector dissipation	T _f = 25°C, per 1 chip	20	W
T _j	Junction temperature	(Note 1)	-20~+150	°C

Note 1 : The maximum junction temperature rating of the power chips integrated within the DIP-IPM is 150°C (@ T_f ≤ 100°C). However, to ensure safe operation of the DIP-IPM, the average junction temperature should be limited to T_{j(ave)} ≤ 125°C (@ T_f ≤ 100°C).

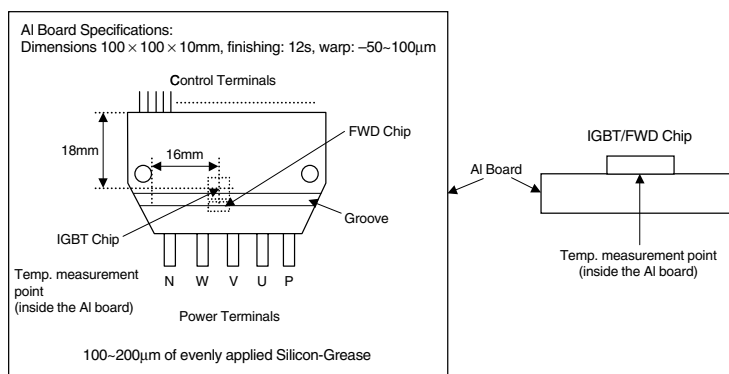
CONTROL (PROTECTION) PART

Symbol	Parameter	Condition	Ratings	Unit
V _D	Control supply voltage	Applied between VP1-VNC, VN1-VNC	20	V
V _{DB}	Control supply voltage	Applied between VUFB-VUFS, VVFB-VVFS, VWFB-VWFS	20	V
V _{CIN}	Input voltage	Applied between UP, VP, WP-VNC, UN, VN, WN-VNC	-0.5~+5.5	V
V _{FO}	Fault output supply voltage	Applied between FO-VNC	-0.5~V _D +0.5	V
I _{FO}	Fault output current	Sink current at FO terminal	15	mA
V _{SC}	Current sensing input voltage	Applied between CIN-VNC	-0.5~V _D +0.5	V

TOTAL SYSTEM

Symbol	Parameter	Condition	Ratings	Unit
V _{CC(Prot)}	Self protection supply voltage limit (short-circuit protection capability)	V _D = 13.5~16.5V, Inverter part T _j = 125°C, non-repetitive, less than 2 μs	400	V
T _f	Heat-fin operation temperature	(Note 2)	-20~+100	°C
T _{stg}	Storage temperature		-40~+125	°C
V _{iso}	Isolation voltage	60Hz, Sinusoidal, AC 1 minute, connection pins to heat-sink plate	1500	V _{rms}

Note 2 : T_f MEASUREMENT POINT



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THERMAL RESISTANCE

Symbol	Parameter	Condition	Limits			Unit
			Min.	Typ.	Max.	
R _{th(j-f)Q}	Junction-to-heat sink thermal resistance	Inverter IGBT part (per 1/6 module)	—	—	6.0	°C/W
R _{th(j-f)F}		Inverter FWD part (per 1/6 module)	—	—	6.5	

Note 3 : Grease with good thermal conductivity should be applied evenly about +100μm ~ +200μm on the contact surface of a DIP-IPM and a Heat sink.

ELECTRICAL CHARACTERISTICS (T_j = 25°C, unless otherwise noted)

INVERTER PART

Symbol	Parameter	Condition		Limits			Unit
				Min.	Typ.	Max.	
V _{CE(sat)}	Collector-emitter saturation voltage	V _D = V _{DB} = 15V V _{CIN} = 0V	I _C = 5A, T _j = 25°C I _C = 5A, T _j = 125°C	—	1.80 1.90	2.45 2.60	V
V _{EC}	FWD forward voltage	T _j = 25°C, -I _C = 5A, V _{CIN} = 5V		—	2.20	3.00	V
t _{on}	Switching times	V _{CC} = 300V, V _D = V _{DB} = 15V I _C = 5A, T _j = 125°C		0.10	0.60	1.10	μs
t _{rr}		Inductive load (upper-lower arm)		—	0.10	—	μs
t _{c(on)}		V _{CIN} = 5 ↔ 0V		—	0.20	0.60	μs
t _{off}				—	1.10	2.20	μs
t _{c(off)}				—	0.35	1.25	μs
I _{CES}	Collector-emitter cut-off current	V _{CE} = V _{CES}	T _j = 25°C T _j = 125°C	—	—	1 10	mA

CONTROL (PROTECTION) PART

Symbol	Parameter	Condition		Limits			Unit
				Min.	Typ.	Max.	
V _D	Control supply voltage	Applied between V _{P1} -V _{NC} , V _{N1} -V _{NC}		13.5	15.0	16.5	V
V _{DB}	Control supply voltage	Applied between V _{UFB} -V _{UFS} , V _{VFB} -V _{VFS} , V _{WFB} -V _{WFS}		13.5	15.0	16.5	V
I _D	Circuit current	V _D = V _{DB} = 15V V _{CIN} = 5V	Total of V _{P1} -V _{NC} , V _{N1} -V _{NC} V _{UFB} -V _{UFS} , V _{VFB} -V _{VFS} , V _{WFB} -V _{WFS}	—	—	8.50 1.00	mA
V _{FOH}	Fault output voltage	V _{SC} = 0V, F _O = 10kΩ 5V pull-up		4.9	—	—	V
V _{FOL}		V _{SC} = 1V, F _O = 10kΩ 5V pull-up		—	0.8	1.2	V
V _{FOsat}		V _{SC} = 1V, I _{FO} = 15mA		0.8	1.2	1.8	V
t _{dead}	Arm shoot-through blocking time	Relates to corresponding input signal for blocking arm shoot-through. -20°C ≤ T _j ≤ 100°C		3	—	—	μs
V _{SC(ref)}	Short-circuit trip level	T _j = 25°C, V _D = 15V (Note 4)		0.45	0.5	0.55	V
UVDBt	Supply circuit under-voltage protection	T _j ≤ 125°C	Trip level	10.0	—	12.0	V
UVDBr			Reset level	10.5	—	12.5	V
UVDt			Trip level	10.3	—	12.5	V
UVDr			Reset level	10.8	—	13.0	V
t _{FO}	Fault output pulse width	C _{FO} = 22nF (Note 5)		1.0	1.8	—	ms
V _{th(on)}	ON threshold voltage	Applied between:		0.8	1.4	2.0	V
V _{th(off)}	OFF threshold voltage	U _P , V _P , W _P -V _{NC} , U _N , V _N , W _N -V _{NC}		2.5	3.0	4.0	V

Note 4 : Short-circuit protection operates only at the low-arms. Please select the value of the external shunt resistor such that the SC trip level is less than 8.5A

5 : Fault signal is outputted when the low-arm short-circuit or control supply under-voltage protective functions operate. The fault output pulse-width t_{FO} depends on the capacitance value of C_{FO} according to the following approximate equation. : C_{FO} = (12.2 × 10⁻⁶) × t_{FO} [F]

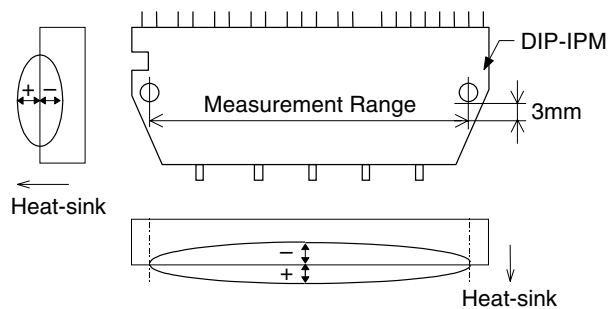
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MECHANICAL CHARACTERISTICS AND RATINGS

Parameter	Condition		Limits			Unit
			Min.	Typ.	Max.	
Mounting torque	Mounting screw : M3	—	0.59	0.78	0.98	N·m
Terminal pulling strength	Weight 9.8N	EIAJ-ED-4701	10	—	—	s
Bending strength	Weight 4.9N. 90deg bend	EIAJ-ED-4701	2	—	—	times
Weight		—	—	20	—	g
Heat-sink flatness	(Note 6)	—	-50	—	100	μm

Note 6: Measurement point of heat-sink flatness



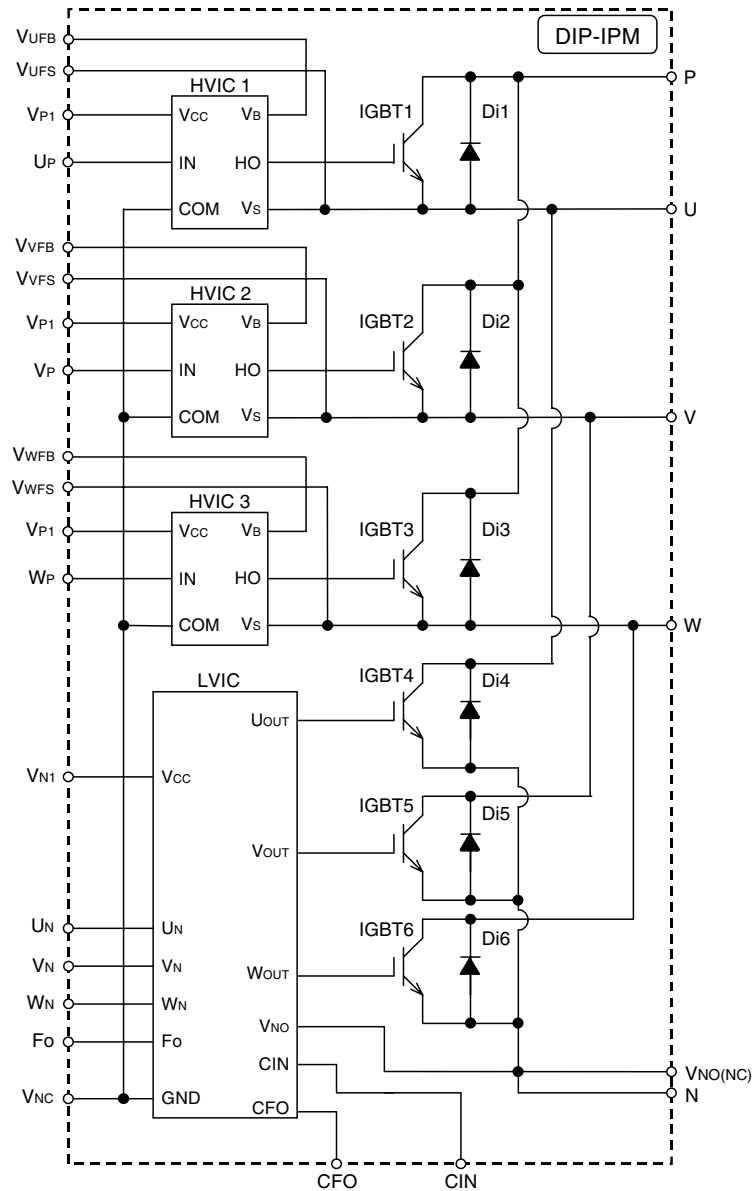
RECOMMENDED OPERATION CONDITIONS

Symbol	Parameter	Condition	Limits			Unit
			Min.	Typ.	Max.	
V _{CC}	Supply voltage	Applied between P-N	0	300	400	V
V _D	Control supply voltage	Applied between V _{P1} -V _{NC} , V _{N1} -V _{NC}	13.5	15.0	16.5	V
V _{DB}	Control supply voltage	Applied between V _{UFB} -V _{UFS} , V _{VFB} -V _{VFS} , V _{WFB} -V _{WFS}	13.5	15.0	16.5	V
ΔV _D , ΔV _{DB}	Control supply variation		-1	—	1	V/μs
t _{dead}	Arm shoot-through blocking time	Relates to corresponding input signal for blocking arm shoot-through	3	—	—	μs
f _{PWM}	PWM input frequency	T _J ≤ 125°C, T _I ≤ 100°C	—	15	—	kHz
V _{CIN(ON)}	Input ON voltage	Applied between U _P , V _P , W _P -V _{NC} , U _N , V _N , W _N -V _{NC}	0~0.65			V
V _{CIN(OFF)}	Input OFF voltage		4.0~5.5			V

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Fig. 4 THE DIP-IPM INTERNAL CIRCUIT

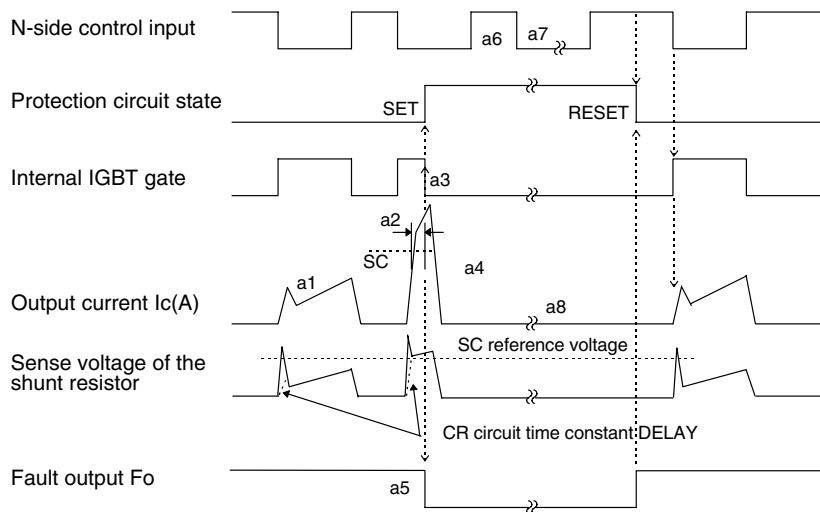


Note: The IGBTs gates and the HVICs COM terminals are connected to the dummy pins.

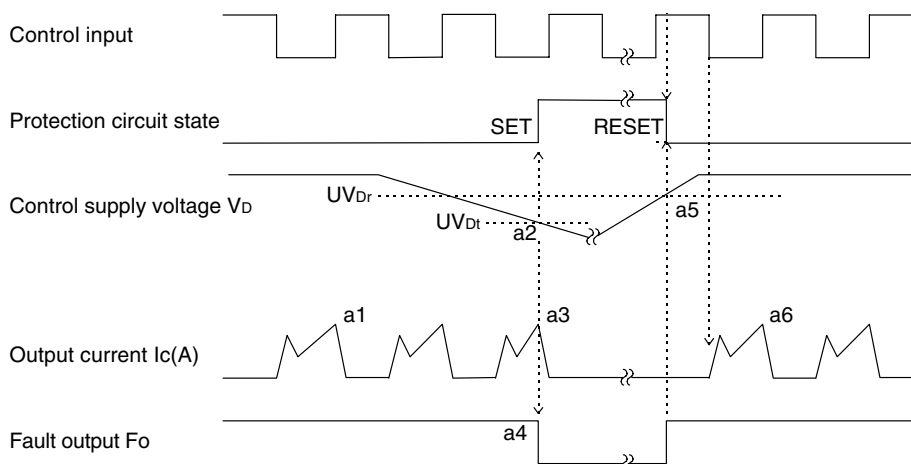
Fig. 5 TIMING CHARTS OF THE DIP-IPM PROTECTIVE FUNCTIONS
[A] Short-Circuit Protection (N-side only)

(For the external shunt resistor and CR connection, please refer to Fig. 3.)

- a1. Normal operation : IGBT ON and carrying current.
- a2. Short-circuit current detection (SC trigger).
- a3. IGBT gate interrupt.
- a4. IGBT turns OFF.
- a5. Fo timer operation starts : The pulse width of the Fo signal is set by the external capacitor C_{FO}.
- a6. Input "H" : IGBT OFF state.
- a7. Input "L" : IGBT ON state.
- a8. IGBT OFF state.


[B] Under-Voltage Protection (N-side, UV_D)

- a1. Normal operation : IGBT ON and carrying current.
- a2. Under-voltage trip (UV_{Dt}).
- a3. IGBT OFF in spite of control input condition.
- a4. Fo timer operation starts.
- a5. Under-voltage reset (UV_{Dr}).
- a6. Normal operation : IGBT ON and carrying current.



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[C] Under-Voltage Protection (P-side, V_{DB})

- a1. Control supply voltage rises : After the voltage level reaches UV_{DBr} , the circuits start to operate when the next input is applied.
- a2. Normal operation : IGBT ON and carrying current.
- a3. Under-voltage trip (UV_{DBt}).
- a4. IGBT OFF in spite of control input condition (there is no Fo signal output).
- a5. Under-voltage reset (UV_{DBr}).
- a6. Normal operation : IGBT ON and carrying current.

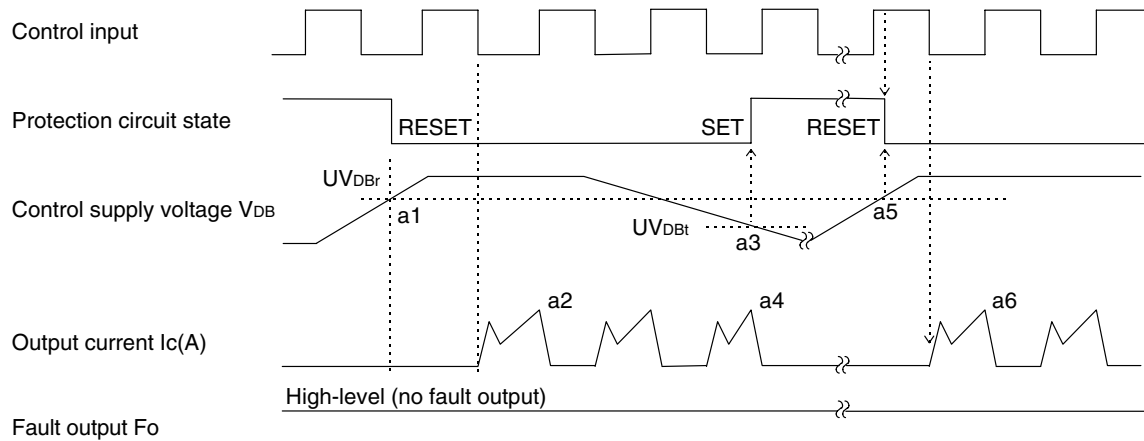
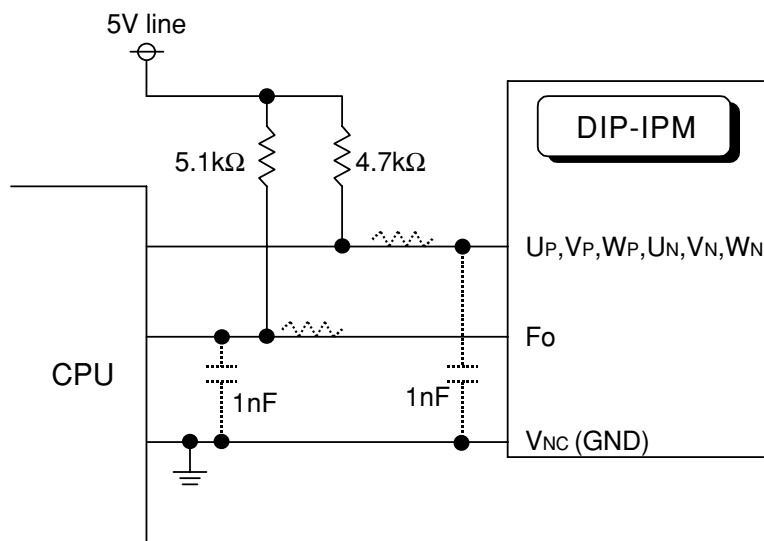


Fig. 6 RECOMMENDED CPU I/O INTERFACE CIRCUIT

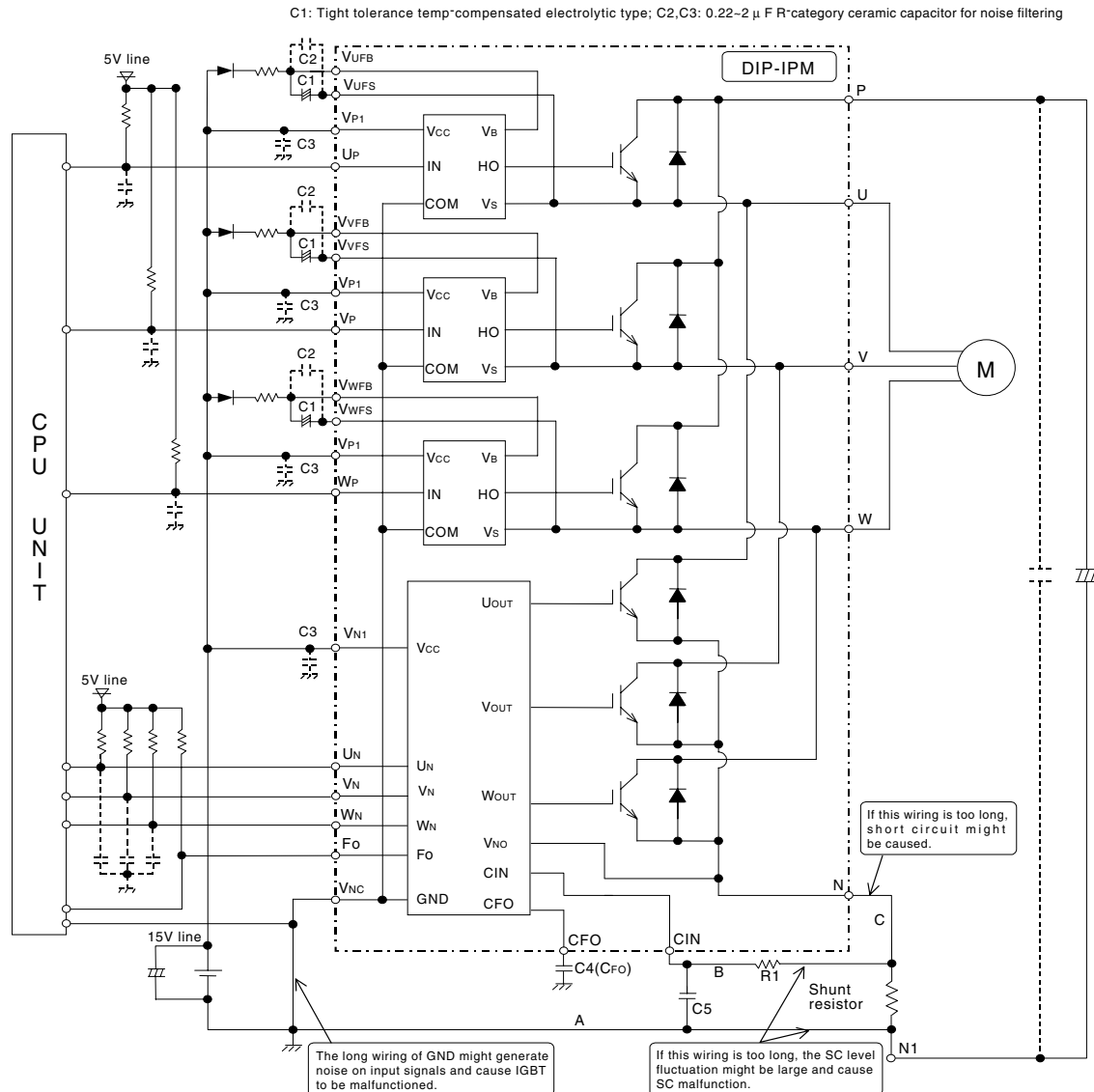


Note : RC coupling at each input (parts shown dotted) may change depending on the PWM control scheme used in the application and on the wiring impedance of the application's printed circuit board.

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Fig. 7 TYPICAL DIP-IPM APPLICATION CIRCUIT EXAMPLE



Note 1 : To prevent the input signals oscillation, an RC coupling at each input is recommended, and the wiring of each input should be as short as possible (less than 2cm).

2 : By virtue of integrating an application specific type HVIC inside the module, direct coupling to CPU terminals without any opto-coupler or transformer isolation is possible.

3 : Fo output is open collector type. This signal line should be pulled up to the positive side of the 5V power supply with approximately 5.1k Ω resistance.

4 : Fo output pulse width should be decided by connecting an external capacitor between CFO and VNC terminals (CFO). (Example : CFO = 22 nF $\rightarrow$ tFO = 1.8 ms (typ.))

5 : Each input signal line should be pulled up to the positive side of the 5V power supply with approximately 4.7k Ω resistance (other RC coupling circuits at each input may be needed depending on the PWM control scheme used and on the wiring impedances of the system's printed circuit board). Approximately a 0.22~2 μ F by-pass capacitor should be used across each power supply connection terminals.

6 : To prevent errors of the protection function, the wiring of A, B, C should be as short as possible.

7 : In the recommended protection circuit, please select the R1C5 time constant in the range of 1.5~2 μ s.

8 : Each capacitor should be put as nearby the terminals of the DIP-IPM as possible.

9 : To prevent surge destruction, the wiring between the smoothing capacitor and the P&N1 terminals should be as short as possible. Approximately a 0.1~0.22 μ F snubber capacitor between the P&N1 terminals is recommended.