

DUAL PROCESSOR SUPERVISORY CIRCUITS WITH POWER-FAIL

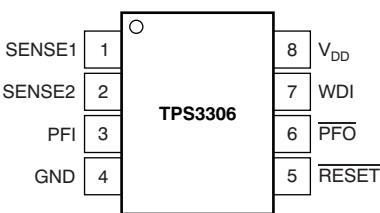
FEATURES

- Dual Supervisory Circuits With Power-Fail for DSP and Processor-Based Systems
- Voltage Monitor for Power-Fail or Low-Battery Warning
- Watchdog Timer With 0.8 Second Time-Out
- Power-On Reset Generator With Integrated 100 ms Delay Time
- Open-Drain Reset and Power-Fail Output
- Supply Current of 15 μ A (Typ.)
- Supply Voltage Range: 7 V to 6 V
- Defined **RESET** Output From $V_{DD} \geq 1.1$ V
- **MSOP-8** and **SO-8** Packages
- Temperature Range: -40°C to $+85^{\circ}\text{C}$

APPLICATIONS

- Multivoltage DSPs and Processors
- Portable Battery-Powered Equipment
- Embedded Control Systems
- Intelligent Instruments
- Automotive Systems

D OR DGK PACKAGE
(TOP VIEW)

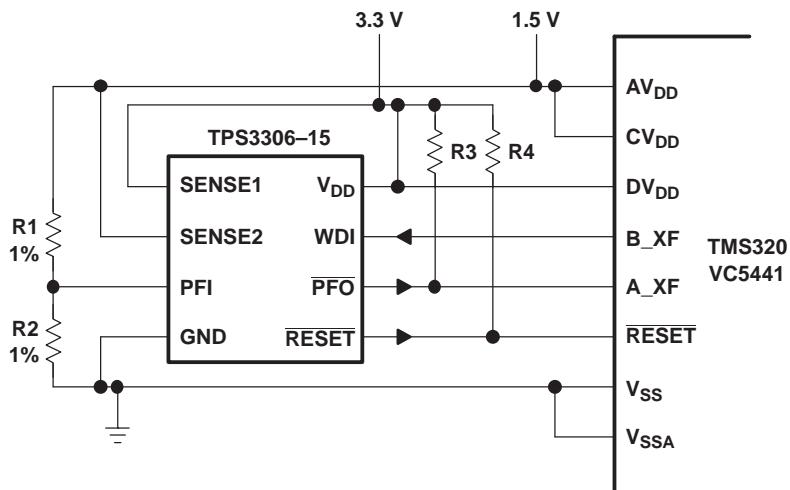


DESCRIPTION

The TPS3306 family is a series of supervisory circuits designed for circuit initialization which require two supply voltages, primarily in DSP and processor-based systems.

The product spectrum of the TPS3306-xx is designed for monitoring two independent supply voltages of 3.3 V/1.5 V, 3.3 V/1.8 V, 3.3 V/2 V, 3.3 V/2.5 V, or 3.3 V/5 V.

TYPICAL OPERATING CIRCUIT



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

All trademarks are the property of their respective owners.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.



ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

AVAILABLE OPTIONS

Table 1. SUPPLY VOLTAGE MONITORING

DEVICE	NOMINAL SUPERVISED VOLTAGE		THRESHOLD VOLTAGE (TYP)	
	SENSE1	SENSE2	SENSE1	SENSE2
TPS3306-15	3.3 V	1.5 V	2.93 V	1.4 V
TPS3306-18	3.3 V	1.8 V	2.93 V	1.68 V
TPS3306-20	3.3 V	2 V	2.93 V	1.85 V
TPS3306-25	3.3 V	2.5 V	2.93 V	2.25 V
TPS3306-33	5 V	3.3 V	4.55 V	2.93 V

For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

DESCRIPTION (CONTINUED)

The various supervisory circuits are designed to monitor the nominal supply voltage, as shown in the [Supply Voltage Monitoring](#) table.

During power-on, $\overline{\text{RESET}}$ is asserted when the supply voltage V_{DD} becomes higher than 1.1 V. Thereafter, the supervisory circuits monitor the SENSE_n inputs and keep $\overline{\text{RESET}}$ active as long as SENSE_n remains below the threshold voltage V_{IT} .

An internal timer delays the return of the $\overline{\text{RESET}}$ output to the inactive state (high) to ensure proper system reset. The delay time, $t_{d(\text{typ})} = 100$ ms, starts after SENSE_1 and SENSE_2 inputs have risen above the threshold voltage V_{IT} . When the voltage at SENSE_1 or SENSE_2 input drops below the threshold voltage V_{IT} , the output becomes active (low) again.

The integrated power-fail (PFI) comparator with separate open-drain ($\overline{\text{PFO}}$) output can be used for low-battery detection, power-fail warning, or for monitoring a power supply other than the main supply.

The TPS3306-xx devices integrate a watchdog timer that is periodically triggered by a positive or negative transition of WDI. When the supervising system fails to retrigger the watchdog circuit within the time-out interval, $t_{t(\text{out})} = 0.50$ s, $\overline{\text{RESET}}$ becomes active for the time period t_d . This event also reinitializes the watchdog timer. Leaving WDI unconnected disables the watchdog.

The TPS3306-xx devices are available in either 8-pin MSOP or standard 8-pin SO packages, and are characterized for operation over a temperature range of -40°C to $+85^\circ\text{C}$.

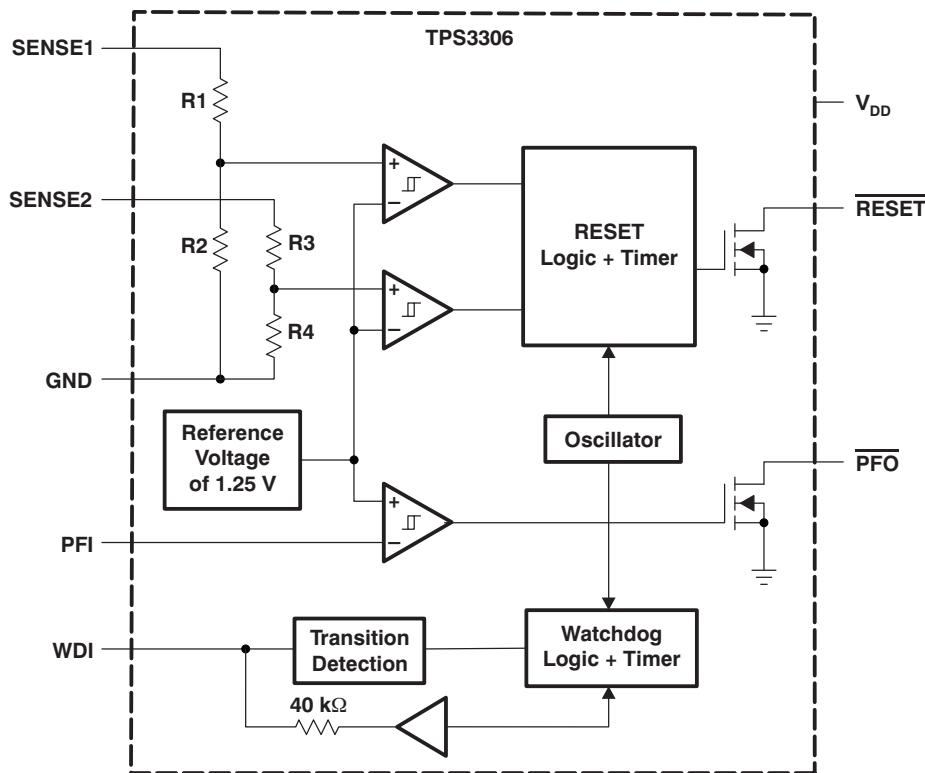
FUNCTION/TRUTH TABLES

SENSE1 > V_{IT1}	SENSE2 > V_{IT2}	RESET
0	0	L
0	1	L
1	0	L
1	1	H

FUNCTION/TRUTH TABLES

PFI > V_{IT}	PFO
0	L
1	H

FUNCTIONAL BLOCK DIAGRAM



TIMING DIAGRAM

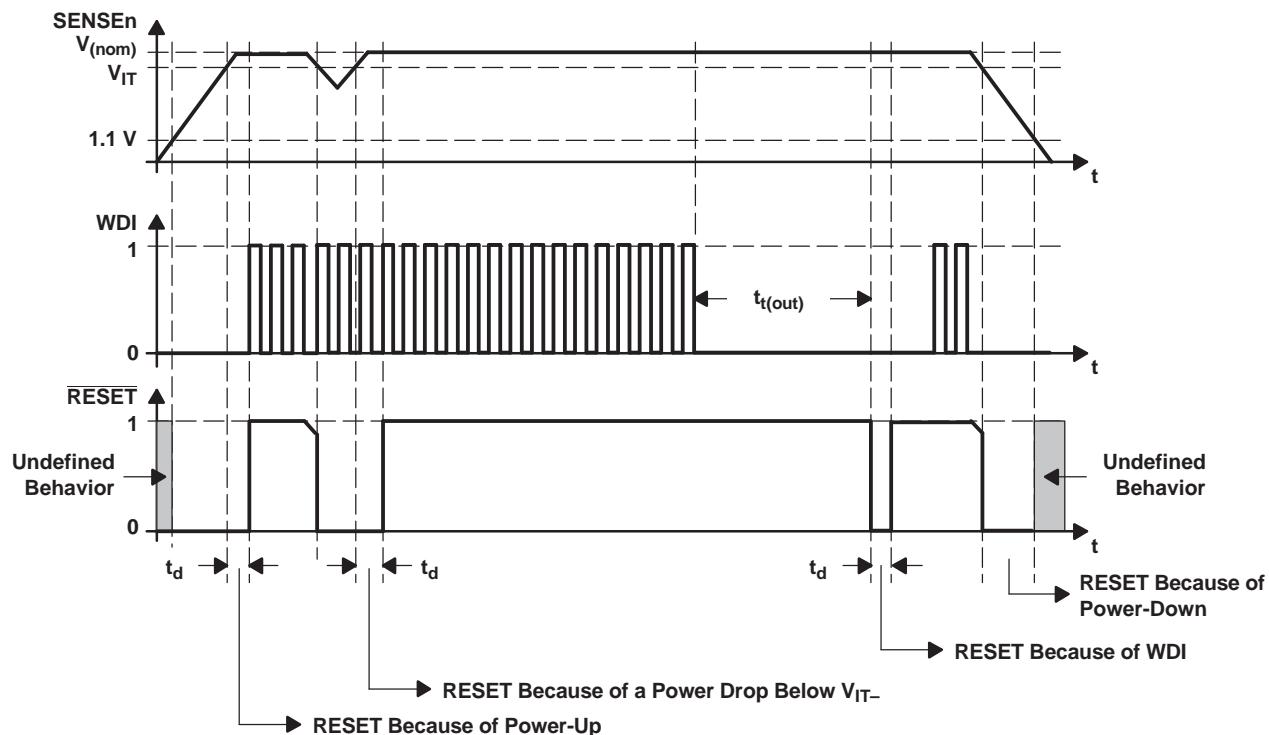


Table 4. Terminal Functions

TERMINAL NAME	NO.	I/O	DESCRIPTION
GND	4	I	Ground
PFI	3	I	Power-fail comparator input
PFO	6	O	Power-fail comparator output, open-drain
RESET	5	O	Active-low reset output, open-drain
SENSE1	1	I	Sense voltage input 1
SENSE2	2	I	Sense voltage input 2
WDI	7	I	Watchdog timer input
V_{DD}	8	I	Supply voltage

DETAILED DESCRIPTION

Watchdog

In a microprocessor- or DSP-based system, it is not only important to supervise the supply voltage, it is also important to ensure correct program execution. The task of a watchdog is to ensure that the program is not stalled in an indefinite loop. The microprocessor, microcontroller, or DSP typically has to toggle the watchdog input within 0.8 s to avoid a time-out occurring. Either a low-to-high or a high-to-low transition resets the internal watchdog timer. If the input is unconnected or tied with a high impedance driver, the watchdog is disabled and will be retriggered internally.

DETAILED DESCRIPTION (continued)

Saving Current While Using the Watchdog

The watchdog input is internally driven low during the first 7/8 of the watchdog time-out period, then momentarily pulses high, resetting the watchdog counter. For minimum watchdog input current (minimum overall power consumption), leave WDI low for the majority of the watchdog time-out period, pulsing it low-high-low once within 7/8 of the watchdog time-out period to reset the watchdog timer. If instead WDI is externally driven high for the majority of the time-out period, a current of $5\text{ V}/40\text{ k}\Omega = 125\text{ }\mu\text{A}$ can flow into WDI.

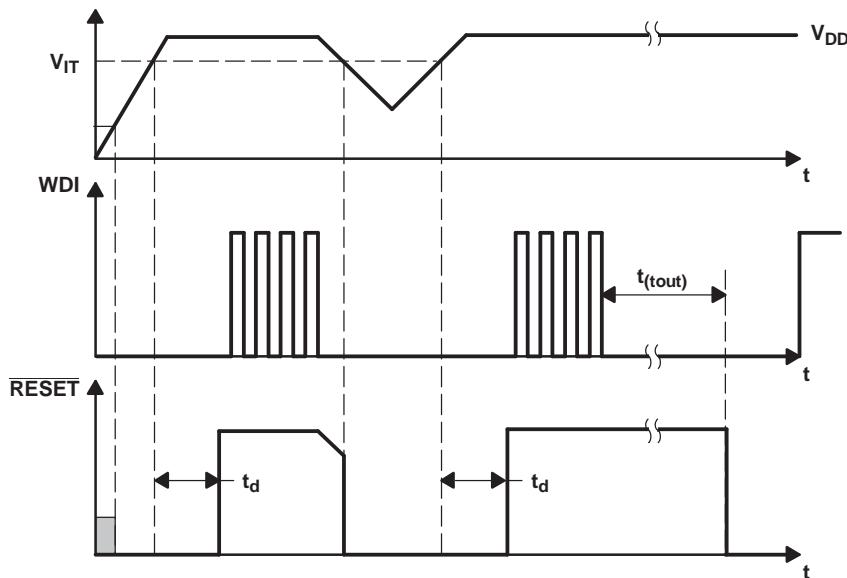
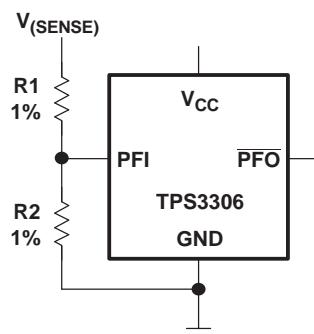


Figure 1. Watchdog Timing

Power-Fail Comparator (PFI and PFO)

An additional comparator is provided to monitor voltages other than the nominal supply voltage. The power-fail-input (PFI) will be compared with an internal voltage reference of 1.25 V. If the input voltage falls below the power-fail threshold (V_{PFI}) of typ. 1.25 V, the power-fail output (\overline{PFO}) goes low. If it goes above 1.25 V plus about 10 mV hysteresis, the output returns to high. By connecting two external resistors, it is possible to supervise any voltages above 1.25 V. The sum of both resistors should be about 1 MΩ, to minimize power consumption and also to assure that the current in the PFI pin can be neglected compared with the current through the resistor network. The tolerance of the external resistors should be not more than 1% to ensure minimal variation of sensed voltage. If the power-fail comparator is unused, connect PFI to ground and leave PFO unconnected.



$$V_{PFI,trip} = 1.25\text{ V} \times \frac{R_1 + R_2}{R_2}$$

ABSOLUTE MAXIMUM RATINGS

Over operating free-air temperature range (unless otherwise noted).⁽¹⁾

	UNIT
Supply voltage, V_{DD} (see ⁽²⁾)	7 V
PFI pin	−0.3 V to V_{DD} + 0.3 V
All other pins (see ⁽²⁾)	−0.3 V to 7 V
Maximum low output current, I_{OL}	5 mA
Maximum high output current, I_{OH}	−5 mA
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{DD}$)	±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{DD}$)	±20 mA
Continuous total power dissipation	See Dissipation Rating Table
Operating free-air temperature range, T_A	−40°C to +85°C
Storage temperature range, T_{stg}	−65°C to +150°C
Soldering temperature	260°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltage values are with respect to GND. For reliable operation, the device must not be operated at 7 V for more than $t = 1000$ h continuously.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq +25^\circ\text{C}$ POWER RATING	DERATING FACTOR ABOVE $T_A = +25^\circ\text{C}$	$T_A = +70^\circ\text{C}$ POWER RATING	$T_A = +85^\circ\text{C}$ POWER RATING
DGK	424 mW	3.4 mW/°C	271 mW	220 mW
D	725 mW	5.8 mW/°C	464 mW	377 mW

RECOMMENDED OPERATING CONDITIONS

At specified temperature range.

	MIN	MAX	UNIT
Supply voltage, V_{DD}	2.7	6	V
Input voltage at WDI and PFI, V_I	0	$V_{DD} + 0.3$	V
Input voltage at SENSE1 and SENSE2, V_I	0	$(V_{DD} + 0.3)V_{IT}/1.25$ V	V
High-level input voltage at WDI, V_{IH}	$0.7 \times V_{DD}$		V
Low-level input voltage at WDI, V_{IL}		$0.3 \times V_{DD}$	V
Operating free-air temperature range, T_A	−40	+85	°C

ELECTRICAL CHARACTERISTICS

Over recommended operating free-air temperature range (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT		
V _{OL}	Low-level output voltage	RESET, PFO	V _{DD} = 2.7 V to 6 V, I _{OL} = 20 μ A		0.2	V		
			V _{DD} = 3.3 V, I _{OL} = 2 mA		0.4			
			V _{DD} = 6 V, I _{OL} = 3 mA		0.4			
Power-up reset voltage (see ⁽¹⁾)		V _{DD} \geq 1.1 V, I _{OL} = 20 μ A			0.4	V		
V _{IT}	Negative-going input threshold voltage (see ⁽²⁾)	V _{SENSE1} , V _{SENSE2}	V _{DD} = 2.7 V to 6 V T _A = 0°C to +85°C	1.37	1.40	1.43	V	
				1.64	1.68	1.72		
				1.81	1.85	1.89		
				2.20	2.25	2.30		
				2.86	2.93	3		
				4.46	4.55	4.64		
		PFI		1.22	1.25	1.28		
		V _{DD} = 2.7 V to 6 V T _A = -40°C to +85°C	1.37	1.40	1.44	V		
			1.64	1.68	1.73			
			1.81	1.85	1.90			
			2.20	2.25	2.32			
			2.86	2.93	3.02			
			PFI		4.46	4.55	4.67	V
					1.22	1.25	1.29	
V _{hys}	Hysteresis	PFI	V _{IT} = 1.25 V		10	mV		
		V _{SENSEn}	V _{IT} = 1.40 V		15			
			V _{IT} = 1.68 V		15			
			V _{IT} = 1.86 V		20			
			V _{IT} = 2.25 V		20			
			V _{IT} = 2.93 V		30			
			V _{IT} = 4.55 V		40			
I _{H(AV)}	Average high-level input current	WDI	WDI = V _{DD} = 6 V, Time average (dc = 88%)		100	150	μ A	
I _{L(AV)}	Average low-level input current		WDI = 0 V, V _{DD} = 6 V, Time average (dc = 12%)		-15	-20		
I _H	High-level input current	WDI	WDI = V _{DD} = 6 V		120	170	μ A	
		SENSE1	V _{SENSE1} = V _{DD} = 6 V		5	8		
		SENSE2	V _{SENSE2} = V _{DD} = 6 V		6	9		
I _L	Low-level input current	WDI	WDI = 0 V, V _{DD} = 6 V		-120	-170	μ A	
I _I	Input current	PFI	V _{DD} = 6 V, 0 V \leq V _I \leq V _{DD}		-25	25	nA	
I _{DD}	Supply current				15	40	μ A	
C _i	Input capacitance		V _I = 0 V to V _{DD}		10		pF	

(1) The lowest supply voltage at which RESET becomes active. t_r, V_{DD} \geq 15 μ s/V.

(2) To ensure best stability of the threshold voltage, a bypass capacitor (ceramic 0.1 μ F) should be placed close to the supply terminals.

TIMING REQUIREMENTS

at $V_{DD} = 2.7$ V to 6 V, $R_L = 1$ M Ω , $C_L = 50$ pF, $T_A = 25^\circ$ C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_w Pulse width	SENSEN	$V_{SENSEN_L} = V_{IT} - 0.2$ V, $V_{SENSEN_H} = V_{IT} + 0.2$ V	6			μ s
	WDI	$V_{IH} = 0.7 \times V_{DD}$, $V_{IL} = 0.3 \times V_{DD}$	100			ns

SWITCHING CHARACTERISTICS

at $V_{DD} = 2.7$ V to 6 V, $R_L = 1$ M Ω , $C_L = 50$ pF, $T_A = 25^\circ$ C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{t(out)}$	Watchdog time-out	$V_{I(SENSEN)} \geq V_{IT} + 0.2$ V, See Timing Diagram	0.5	0.8	1.2	s
t_d	Delay time	$V_{I(SENSEN)} \geq V_{IT} + 0.2$ V, See Timing Diagram	70	100	140	ms
t_{PHL}	Propagation (delay) time, high-to-low level output	$V_{IH} = V_{IT} + 0.2$ V, $V_{IL} = V_{IT} - 0.2$ V	1	5		μ s
t_{PLH}	Propagation (delay) time, high-to-low level output	PFI to \overline{PFO}	0.5	1		μ s
t_{PLH}	Propagation (delay) time, low-to-high level output					

TYPICAL CHARACTERISTICS

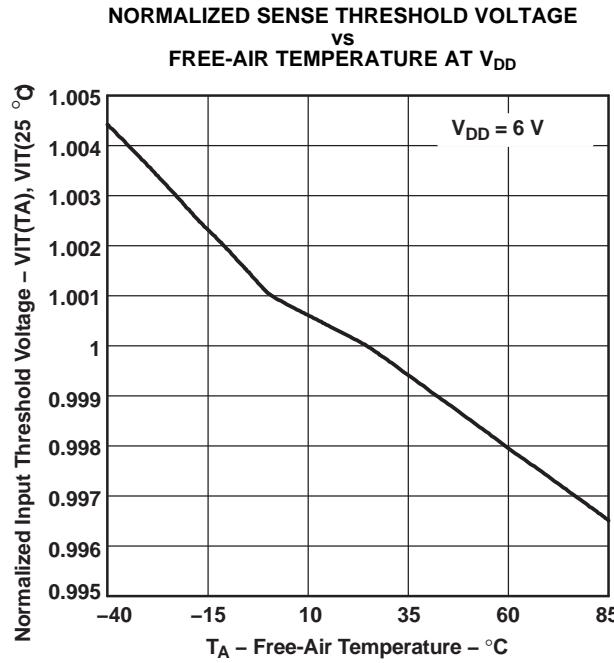


Figure 2.

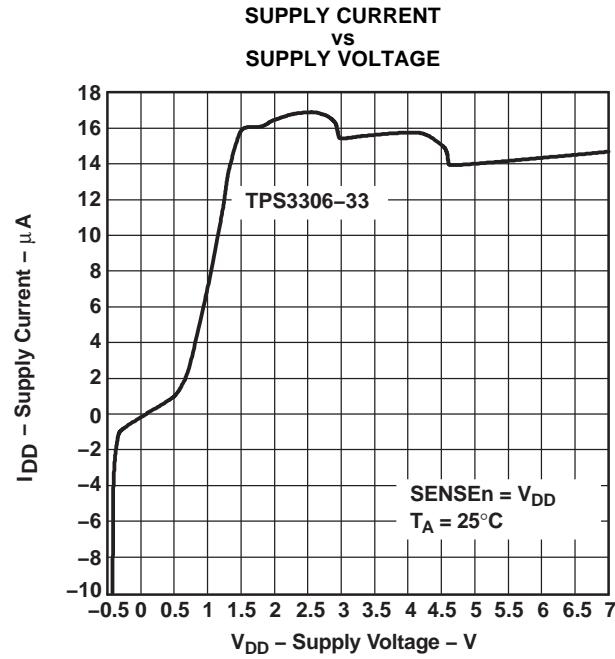


Figure 3.

TYPICAL CHARACTERISTICS (continued)

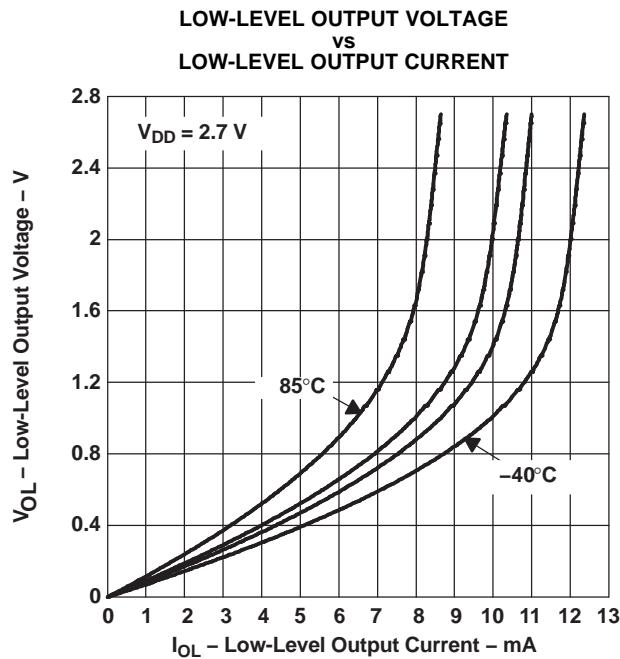


Figure 4.

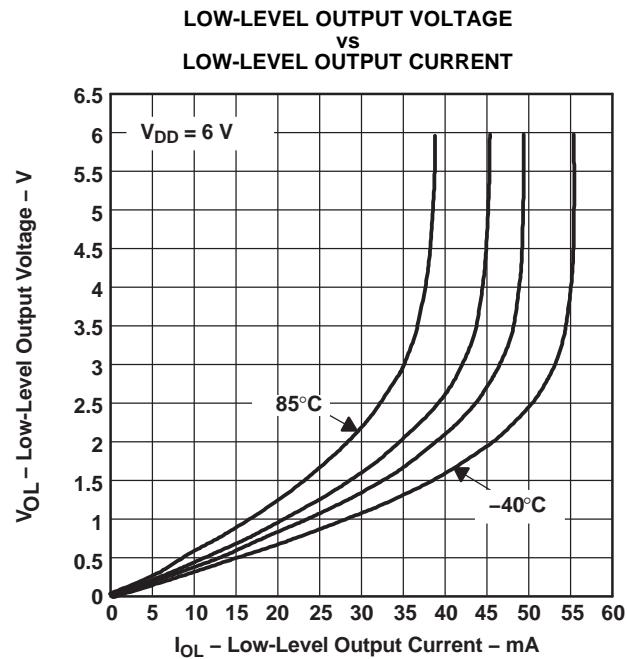


Figure 5.

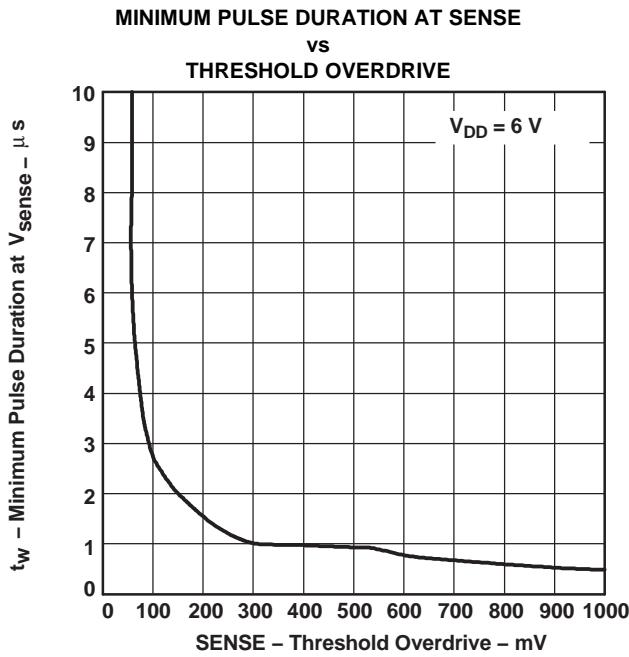


Figure 6.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS3306-15D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	30615	Samples
TPS3306-15DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	30615	Samples
TPS3306-15DGK	ACTIVE	VSSOP	DGK	8	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AIC	Samples
TPS3306-15DGKG4	ACTIVE	VSSOP	DGK	8	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AIC	Samples
TPS3306-15DGKR	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AIC	Samples
TPS3306-15DGKRG4	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AIC	Samples
TPS3306-15DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	30615	Samples
TPS3306-15DRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	30615	Samples
TPS3306-18D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	30618	Samples
TPS3306-18DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	30618	Samples
TPS3306-18DGK	ACTIVE	VSSOP	DGK	8	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AID	Samples
TPS3306-18DGKG4	ACTIVE	VSSOP	DGK	8	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AID	Samples
TPS3306-18DGKR	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AID	Samples
TPS3306-18DGKRG4	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AID	Samples
TPS3306-18DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	30618	Samples
TPS3306-18DRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	30618	Samples
TPS3306-20D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	30620	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS3306-25D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	30625	Samples
TPS3306-25DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	30625	Samples
TPS3306-25DGK	ACTIVE	VSSOP	DGK	8	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AIF	Samples
TPS3306-25DGKG4	ACTIVE	VSSOP	DGK	8	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AIF	Samples
TPS3306-25DGKR	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AIF	Samples
TPS3306-25DGKRG4	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AIF	Samples
TPS3306-25DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	30625	Samples
TPS3306-33D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	30633	Samples
TPS3306-33DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	30633	Samples
TPS3306-33DGK	ACTIVE	VSSOP	DGK	8	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AIG	Samples
TPS3306-33DGKG4	ACTIVE	VSSOP	DGK	8	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AIG	Samples
TPS3306-33DGKR	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AIG	Samples
TPS3306-33DGKRG4	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AIG	Samples
TPS3306-33DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	30633	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TPS3306 :

- Automotive: [TPS3306-Q1](#)

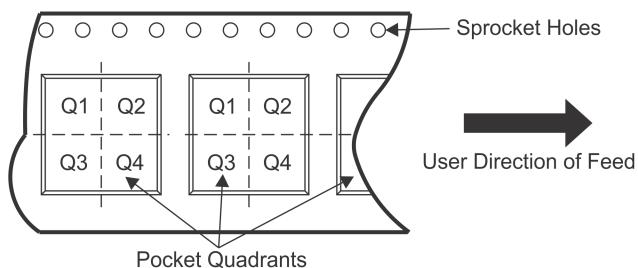
NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION
REEL DIMENSIONS

TAPE DIMENSIONS


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS3306-15DGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TPS3306-15DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TPS3306-18DGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TPS3306-18DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TPS3306-25DGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TPS3306-25DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TPS3306-33DGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TPS3306-33DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

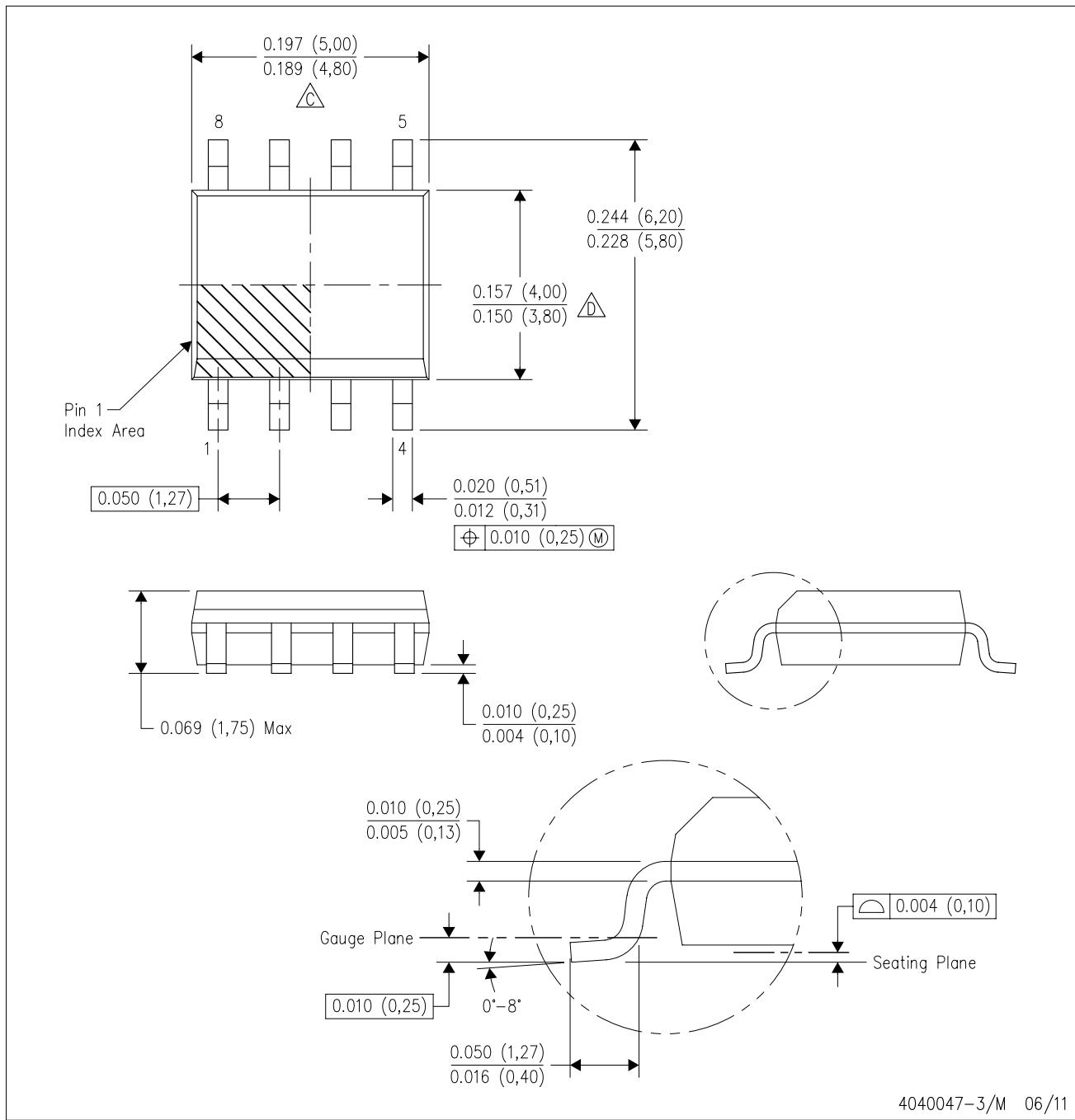
TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS3306-15DGKR	VSSOP	DGK	8	2500	358.0	335.0	35.0
TPS3306-15DR	SOIC	D	8	2500	367.0	367.0	38.0
TPS3306-18DGKR	VSSOP	DGK	8	2500	358.0	335.0	35.0
TPS3306-18DR	SOIC	D	8	2500	367.0	367.0	38.0
TPS3306-25DGKR	VSSOP	DGK	8	2500	358.0	335.0	35.0
TPS3306-25DR	SOIC	D	8	2500	367.0	367.0	38.0
TPS3306-33DGKR	VSSOP	DGK	8	2500	358.0	335.0	35.0
TPS3306-33DR	SOIC	D	8	2500	367.0	367.0	38.0

D (R-PDSO-G8)

PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

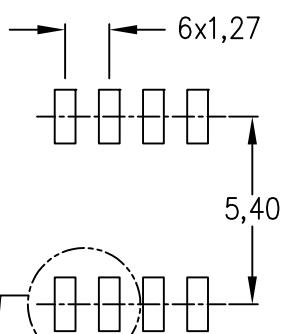
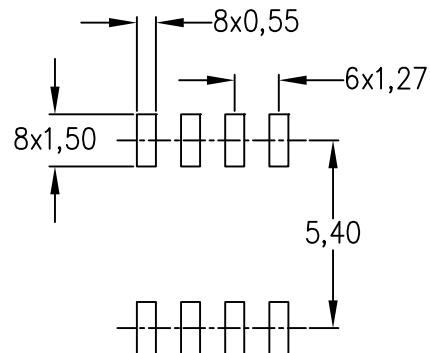
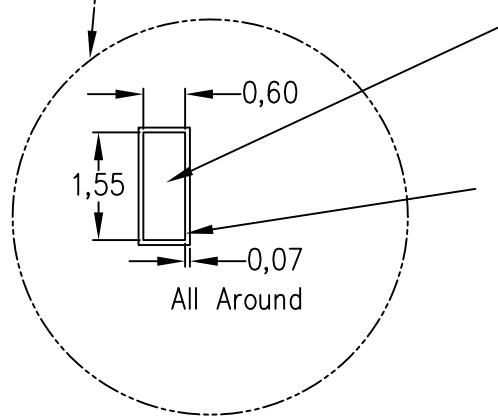
△C Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0.15) each side.

△D Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0.43) each side.

E. Reference JEDEC MS-012 variation AA.

D (R-PDSO-G8)

PLASTIC SMALL OUTLINE

Example Board Layout
(Note C)Stencil Openings
(Note D)Example
Non Soldermask Defined PadExample
Pad Geometry
(See Note C)Example
Solder Mask Opening
(See Note E)

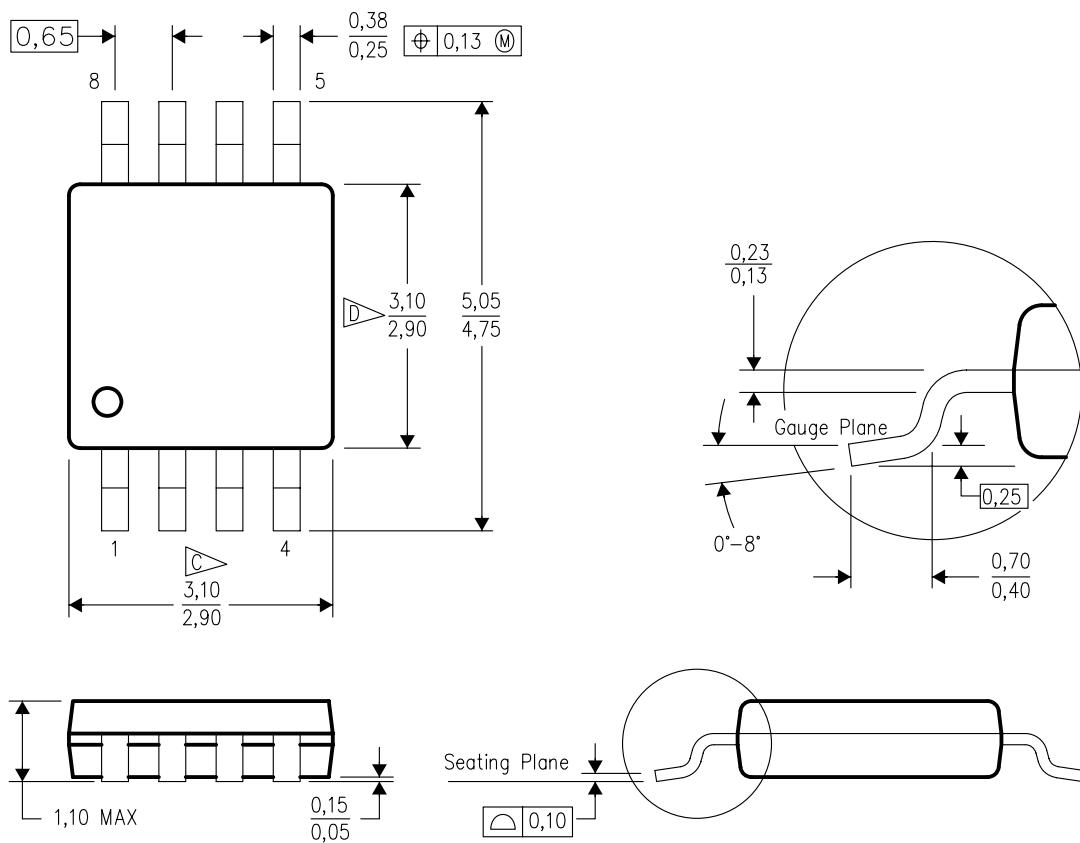
4211283-2/E 08/12

NOTES:

- All linear dimensions are in millimeters.
- This drawing is subject to change without notice.
- Publication IPC-7351 is recommended for alternate designs.
- Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

DGK (S-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE



4073329/E 05/06

NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

 Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.

 Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.

E. Falls within JEDEC MO-187 variation AA, except interlead flash.

IMPORTANT NOTICE

Texas Instruments Incorporated (TI) reserves the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete.

TI's published terms of sale for semiconductor products (<http://www.ti.com/sc/docs/stdterms.htm>) apply to the sale of packaged integrated circuit products that TI has qualified and released to market. Additional terms may apply to the use or sale of other types of TI products and services.

Reproduction of significant portions of TI information in TI data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such reproduced documentation. Information of third parties may be subject to additional restrictions. Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyers and others who are developing systems that incorporate TI products (collectively, "Designers") understand and agree that Designers remain responsible for using their independent analysis, evaluation and judgment in designing their applications and that Designers have full and exclusive responsibility to assure the safety of Designers' applications and compliance of their applications (and of all TI products used in or for Designers' applications) with all applicable regulations, laws and other applicable requirements. Designer represents that, with respect to their applications, Designer has all the necessary expertise to create and implement safeguards that (1) anticipate dangerous consequences of failures, (2) monitor failures and their consequences, and (3) lessen the likelihood of failures that might cause harm and take appropriate actions. Designer agrees that prior to using or distributing any applications that include TI products, Designer will thoroughly test such applications and the functionality of such TI products as used in such applications.

TI's provision of technical, application or other design advice, quality characterization, reliability data or other services or information, including, but not limited to, reference designs and materials relating to evaluation modules, (collectively, "TI Resources") are intended to assist designers who are developing applications that incorporate TI products; by downloading, accessing or using TI Resources in any way, Designer (individually or, if Designer is acting on behalf of a company, Designer's company) agrees to use any particular TI Resource solely for this purpose and subject to the terms of this Notice.

TI's provision of TI Resources does not expand or otherwise alter TI's applicable published warranties or warranty disclaimers for TI products, and no additional obligations or liabilities arise from TI providing such TI Resources. TI reserves the right to make corrections, enhancements, improvements and other changes to its TI Resources. TI has not conducted any testing other than that specifically described in the published documentation for a particular TI Resource.

Designer is authorized to use, copy and modify any individual TI Resource only in connection with the development of applications that include the TI product(s) identified in such TI Resource. NO OTHER LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE TO ANY OTHER TI INTELLECTUAL PROPERTY RIGHT, AND NO LICENSE TO ANY TECHNOLOGY OR INTELLECTUAL PROPERTY RIGHT OF TI OR ANY THIRD PARTY IS GRANTED HEREIN, including but not limited to any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information regarding or referencing third-party products or services does not constitute a license to use such products or services, or a warranty or endorsement thereof. Use of TI Resources may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

TI RESOURCES ARE PROVIDED "AS IS" AND WITH ALL FAULTS. TI DISCLAIMS ALL OTHER WARRANTIES OR REPRESENTATIONS, EXPRESS OR IMPLIED, REGARDING RESOURCES OR USE THEREOF, INCLUDING BUT NOT LIMITED TO ACCURACY OR COMPLETENESS, TITLE, ANY EPIDEMIC FAILURE WARRANTY AND ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, AND NON-INFRINGEMENT OF ANY THIRD PARTY INTELLECTUAL PROPERTY RIGHTS. TI SHALL NOT BE LIABLE FOR AND SHALL NOT DEFEND OR INDEMNIFY DESIGNER AGAINST ANY CLAIM, INCLUDING BUT NOT LIMITED TO ANY INFRINGEMENT CLAIM THAT RELATES TO OR IS BASED ON ANY COMBINATION OF PRODUCTS EVEN IF DESCRIBED IN TI RESOURCES OR OTHERWISE. IN NO EVENT SHALL TI BE LIABLE FOR ANY ACTUAL, DIRECT, SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF TI RESOURCES OR USE THEREOF, AND REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES.

Unless TI has explicitly designated an individual product as meeting the requirements of a particular industry standard (e.g., ISO/TS 16949 and ISO 26262), TI is not responsible for any failure to meet such industry standard requirements.

Where TI specifically promotes products as facilitating functional safety or as compliant with industry functional safety standards, such products are intended to help enable customers to design and create their own applications that meet applicable functional safety standards and requirements. Using products in an application does not by itself establish any safety features in the application. Designers must ensure compliance with safety-related requirements and standards applicable to their applications. Designer may not use any TI products in life-critical medical equipment unless authorized officers of the parties have executed a special contract specifically governing such use. Life-critical medical equipment is medical equipment where failure of such equipment would cause serious bodily injury or death (e.g., life support, pacemakers, defibrillators, heart pumps, neurostimulators, and implantables). Such equipment includes, without limitation, all medical devices identified by the U.S. Food and Drug Administration as Class III devices and equivalent classifications outside the U.S.

TI may expressly designate certain products as completing a particular qualification (e.g., Q100, Military Grade, or Enhanced Product). Designers agree that it has the necessary expertise to select the product with the appropriate qualification designation for their applications and that proper product selection is at Designers' own risk. Designers are solely responsible for compliance with all legal and regulatory requirements in connection with such selection.

Designer will fully indemnify TI and its representatives against any damages, costs, losses, and/or liabilities arising out of Designer's non-compliance with the terms and provisions of this Notice.