

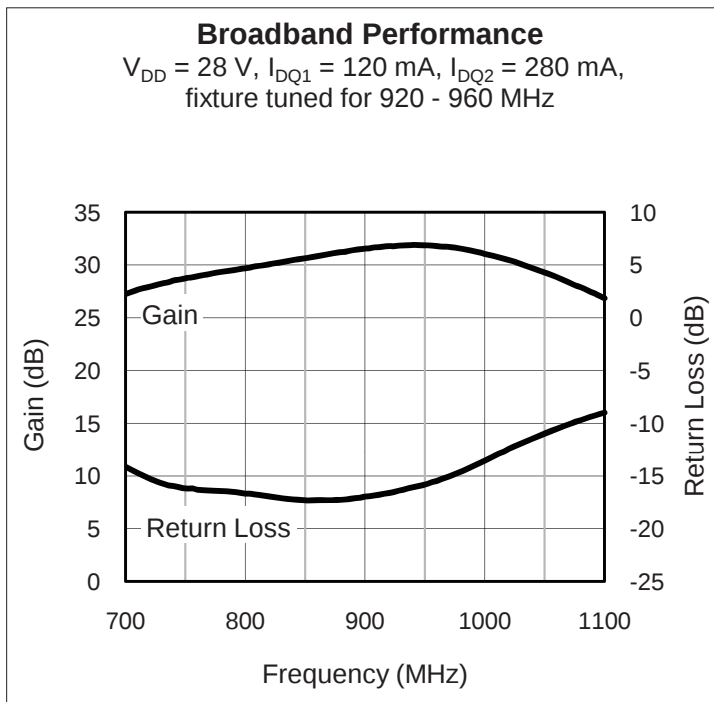
Wideband RF LDMOS Integrated Power Amplifier

30 W, 28 V, 700 – 1000 MHz

Description

The PTMA080302M is a wideband, matched, 30-watt, 2-stage LDMOS integrated amplifier intended for use in all typical modulation formats from 700 to 1000 MHz. This device is offered in a 20-lead, thermally-enhanced, overmolded package for cool and reliable operation.

PTMA080302M
Package PG-DSO-20-63



Features

- Designed for wide RF modulation bandwidths, and low memory effects
- On-chip matching, integrated input DC block, 50-ohm input and ~ 8-ohm output
- Typical GSM/EDGE performance, 940 MHz, 28 V
 - Output power = 15 W Avg.
 - Linear gain = 31 dB
 - Power added efficiency = 36%
 - EVM at 15 W = 1.7 %
 - ACPR at 400 kHz = -61 dBc
 - ACPR at 600 kHz = -73 dBc
- Typical CW performance at 940 MHz, 28 V
 - Output power at P_{1dB} = 32 W
 - Linear gain (1 W) = 31 dB
 - Power added efficiency = 46%
- Capable of handling 10:1 VSWR @ 28 V, 30 W (CW) output power
- Integrated ESD protection. Meets HBM Class 1B (minimum), per JESD22-A114F
- RoHS-compliant package

RF Characteristics

GSM/EDGE Specifications (not subject to production test—verified by design/characterization in Infineon test fixture)

$V_{DD} = 28\text{ V}$, $I_{DQ1} = 120\text{ mA}$, $I_{DQ2} = 280\text{ mA}$, $f = 920\text{ to }960\text{ MHz}$, $P_{OUT} = 15\text{ W Avg.}$

Characteristic	Symbol	Min	Typ	Max	Unit
Gain	G_{ps}	—	31	—	dB
Power-added Efficiency	PAE	—	36	—	%
Error Vector Magnitude	EVM (RMS)	—	1.7	—	%

table continued next page

All published data at $T_{CASE} = 25^\circ\text{C}$ unless otherwise indicated

ESD: Electrostatic discharge sensitive device—observe handling precautions!

RF Characteristics (cont.)

GSM/EDGE Specifications (cont.)

$V_{DD} = 28\text{ V}$, $I_{DQ1} = 150\text{ mA}$, $I_{DQ2} = 280\text{ mA}$, $f = 920\text{ to }960\text{ MHz}$, $P_{OUT} = 15\text{ W Avg.}$

Characteristic		Symbol	Min	Typ	Max	Unit
Modulation Spectrum	400 kHz offset	$ACPR_1$	—	−61	—	dBc
	600 kHz offset	$ACPR_2$	—	−73	—	dBc
Gain Flatness		ΔG	—	0.2	—	dB

Two-tone Measurements (tested in Infineon test fixture)

$V_{DD} = 28\text{ V}$, $I_{DQ1} = 150\text{ mA}$, $I_{DQ2} = 280\text{ mA}$, $P_{OUT} = 15\text{ W Avg.}$, $f = 940\text{ MHz}$, tone spacing = 1 MHz

Characteristic		Symbol	Min	Typ	Max	Unit
Gain		G_{ps}	31	32	—	dB
Drain Efficiency		η_D	32.5	35	—	%
Third Order Intermodulation Distortion		IMD3	—	−33	−29	dBc

Single-tone Specifications (not subject to production test—verified by design/characterization in Infineon test fixture)

$V_{DD} = 28\text{ V}$, $I_{DQ1} = 150\text{ mA}$, $I_{DQ2} = 280\text{ mA}$, $f = 940\text{ MHz}$

Characteristic		Symbol	Min	Typ	Max	Unit
Gain		G_{ps}	—	32	—	dB
Power-added Efficiency		PAE	—	46	—	%
Output Power		P_{1dB}	—	31	—	W

DC Characteristics

Stage 1 Characteristics	Conditions	Symbol	Min	Typ	Max	Unit
Drain Leakage Current	$V_{DS} = 28\text{ V}$, $V_{GS} = 0\text{ V}$	I_{DSS}	—	—	1.0	μA
	$V_{DS} = 63\text{ V}$, $V_{GS} = 0\text{ V}$	I_{DSS}	—	—	10.0	μA
Gate Leakage Current	$V_{GS} = 10\text{ V}$, $V_{DS} = 0\text{ V}$	I_{GSS}	—	—	1.0	μA
On-state Resistance	$V_{GS} = 10\text{ V}$, $V_{DS} = 0.1\text{ V}$	$R_{DS(on)}$	—	1.85	—	Ω
Operating Gate Voltage	$V_{DS} = 28\text{ V}$, $I_{DQ1} = 120\text{ mA}$	V_{GS}	2.0	2.5	3.0	V

DC Characteristics (cont.)

Stage 2 Characteristics	Conditions	Symbol	Min	Typ	Max	Unit
Drain-source Breakdown Voltage	$V_{GS} = 0\text{ V}$, $I_{DS} = 10\text{ mA}$	$V_{(BR)DSS}$	65	—	—	V
Drain Leakage Current	$V_{DS} = 28\text{ V}$, $V_{GS} = 0\text{ V}$	I_{DSS}	—	—	1.0	μA
	$V_{DS} = 63\text{ V}$, $V_{GS} = 0\text{ V}$	I_{DSS}	—	—	10.0	μA
Gate Leakage Current	$V_{GS} = 10\text{ V}$, $V_{DS} = 0\text{ V}$	I_{GSS}	—	—	1.0	μA
On-state Resistance	$V_{GS} = 10\text{ V}$, $V_{DS} = 0.1\text{ V}$	$R_{DS(on)}$	—	0.25	—	Ω
Operating Gate Voltage	$V_{DS} = 28\text{ V}$, $I_{DQ2} = 280\text{ mA}$	V_{GS}	2.0	2.5	3.0	V

Maximum Ratings

Parameter	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	65	V
Gate-Source Voltage	V_{GS}	−0.5 to +12	V
Junction Temperature	T_J	200	$^{\circ}\text{C}$
Input Power	P_{IN}	16	dBm
Total Device Dissipation	P_D	129.5	W
Above 25 $^{\circ}\text{C}$ derate by		0.74	W/ $^{\circ}\text{C}$
Storage Temperature Range	T_{STG}	−40 to +150	$^{\circ}\text{C}$
Thermal Resistance ($T_{CASE} = 70^{\circ}\text{C}$)	Stage 1	$R_{\theta JC}$	6.7 $^{\circ}\text{C/W}$
	Stage 2	$R_{\theta JC}$	1.7 $^{\circ}\text{C/W}$

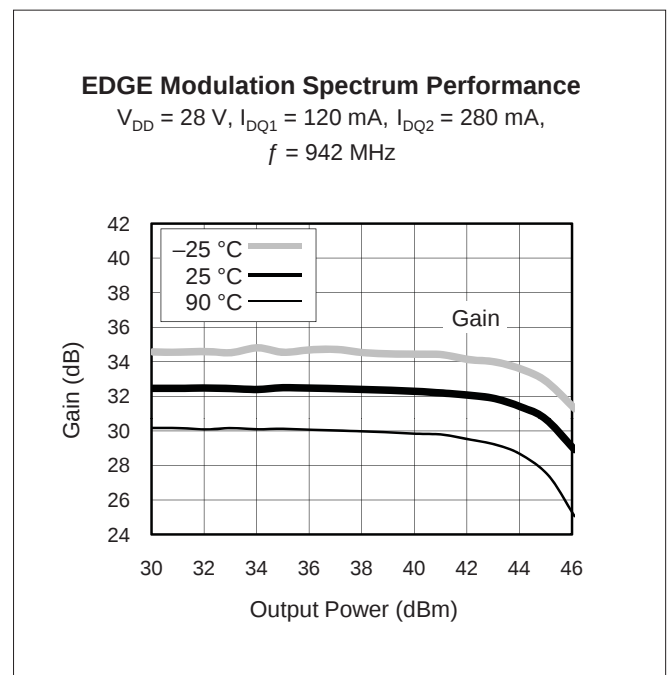
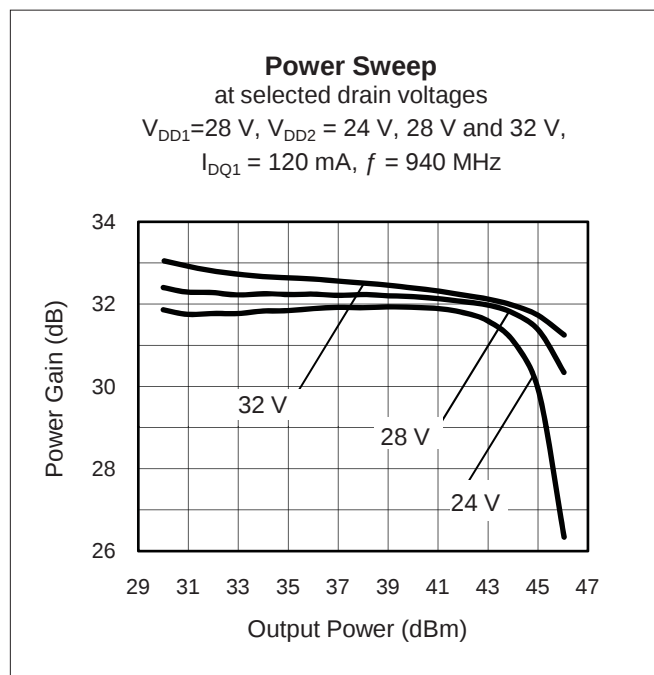
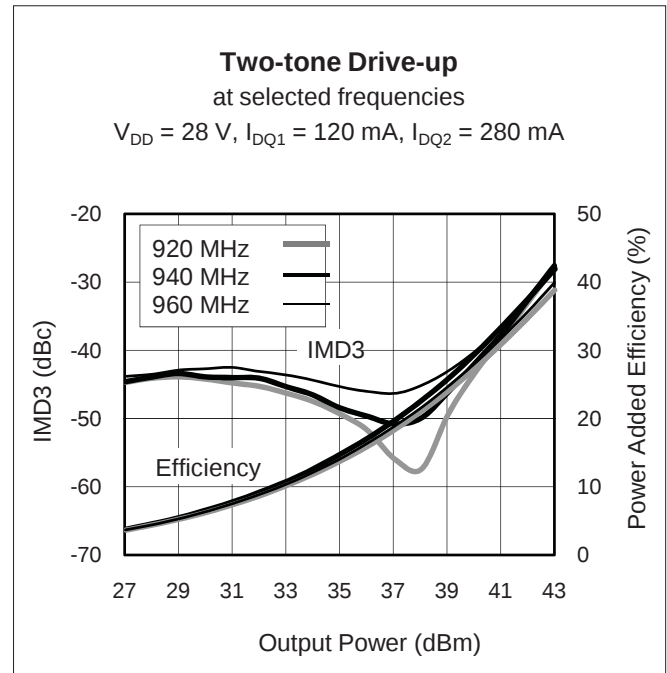
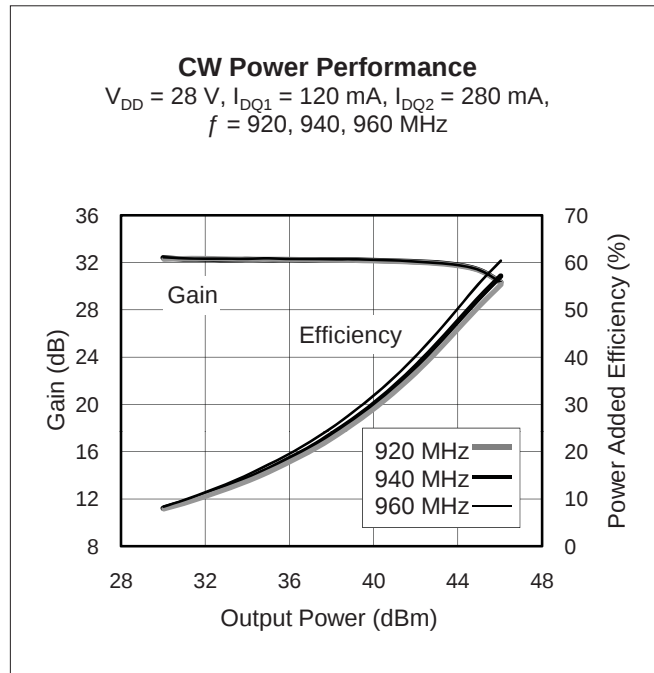
Moisture Sensitivity Level

Level	Test Standard	Package Temperature	Unit
3	IPC/JEDEC J-STD-020	260	$^{\circ}\text{C}$

Ordering Information

Type and Version	Package Outline	Package Description	Shipping
PTMA080302M V1	PG-DSO-20-63	Copper heat slug, plastic EMC body	Tape

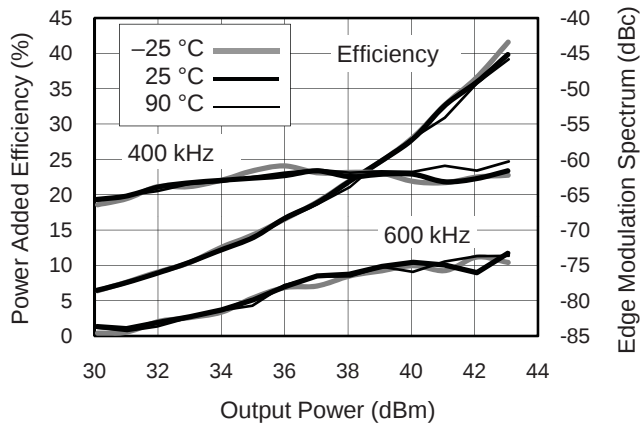
Typical Performance (data taken in a production test fixture)



Typical Performance (cont.)

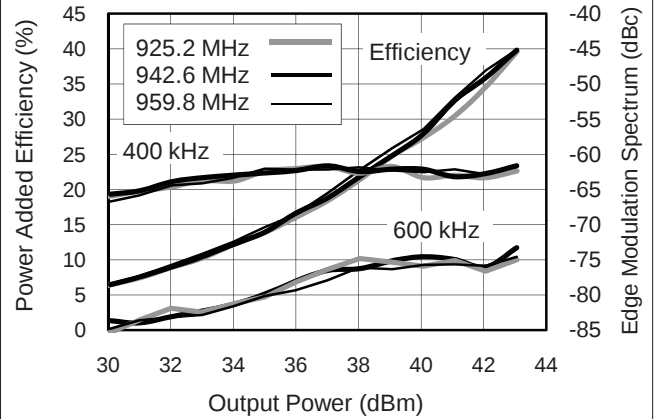
EDGE Modulation Spectrum Performance

at selected temperatures
 $V_{DD} = 28\text{ V}$, $I_{DQ1} = 120\text{ mA}$, $I_{DQ2} = 280\text{ mA}$,
 $f = 942\text{ MHz}$



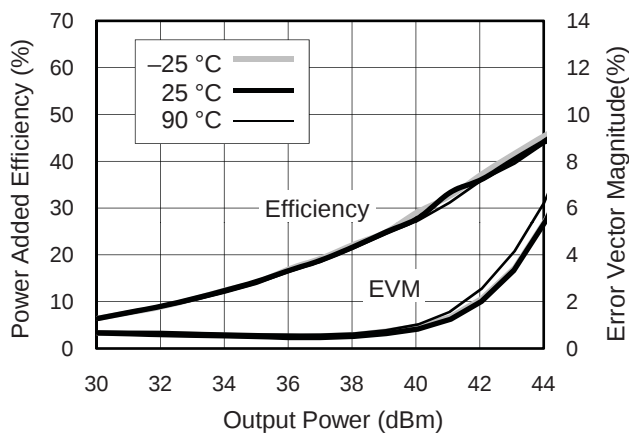
EDGE Modulation Spectrum Performance

at selected frequencies
 $V_{DD} = 28\text{ V}$, $I_{DQ1} = 120\text{ mA}$, $I_{DQ2} = 280\text{ mA}$



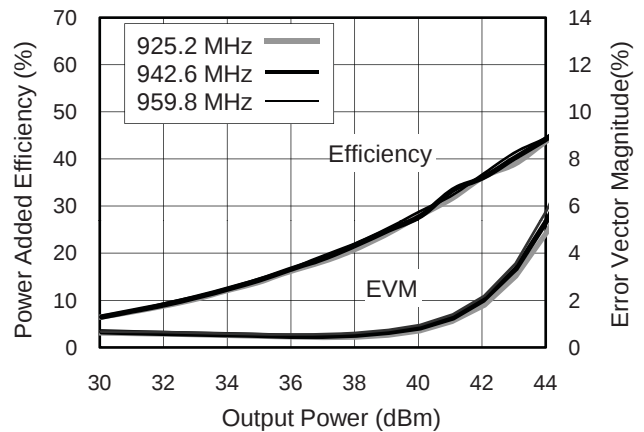
EDGE EVM

at selected temperatures
 $V_{DD} = 28\text{ V}$, $I_{DQ1} = 120\text{ mA}$, $I_{DQ2} = 280\text{ mA}$,
series show $f = 942\text{ MHz}$

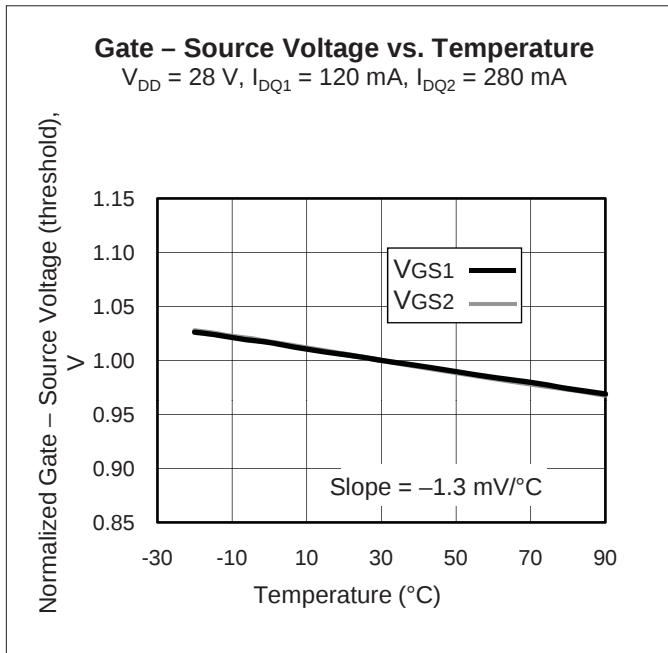


EDGE EVM

$V_{DD} = 28\text{ V}$, $I_{DQ1} = 120\text{ mA}$, $I_{DQ2} = 280\text{ mA}$,
series are at selected frequencies

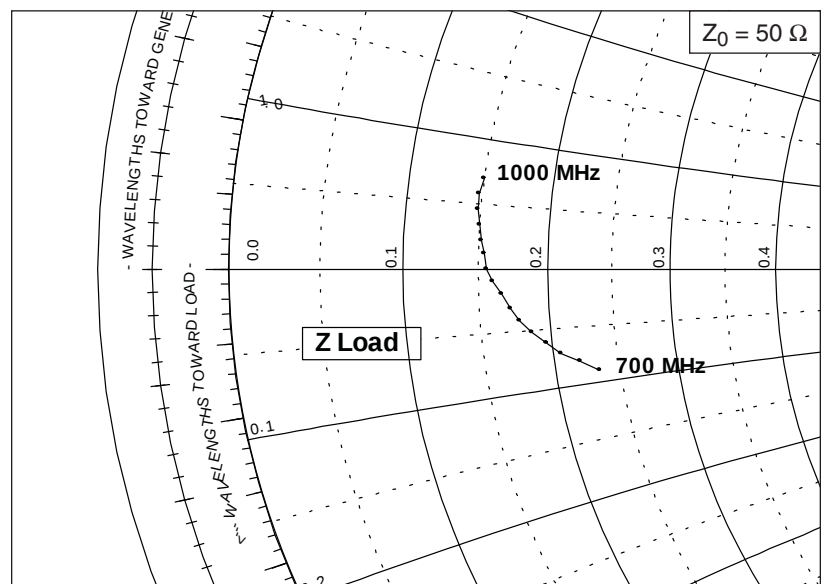
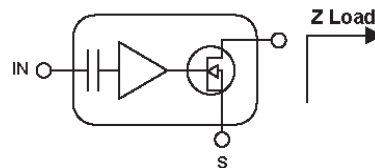


Typical Performance (cont.)

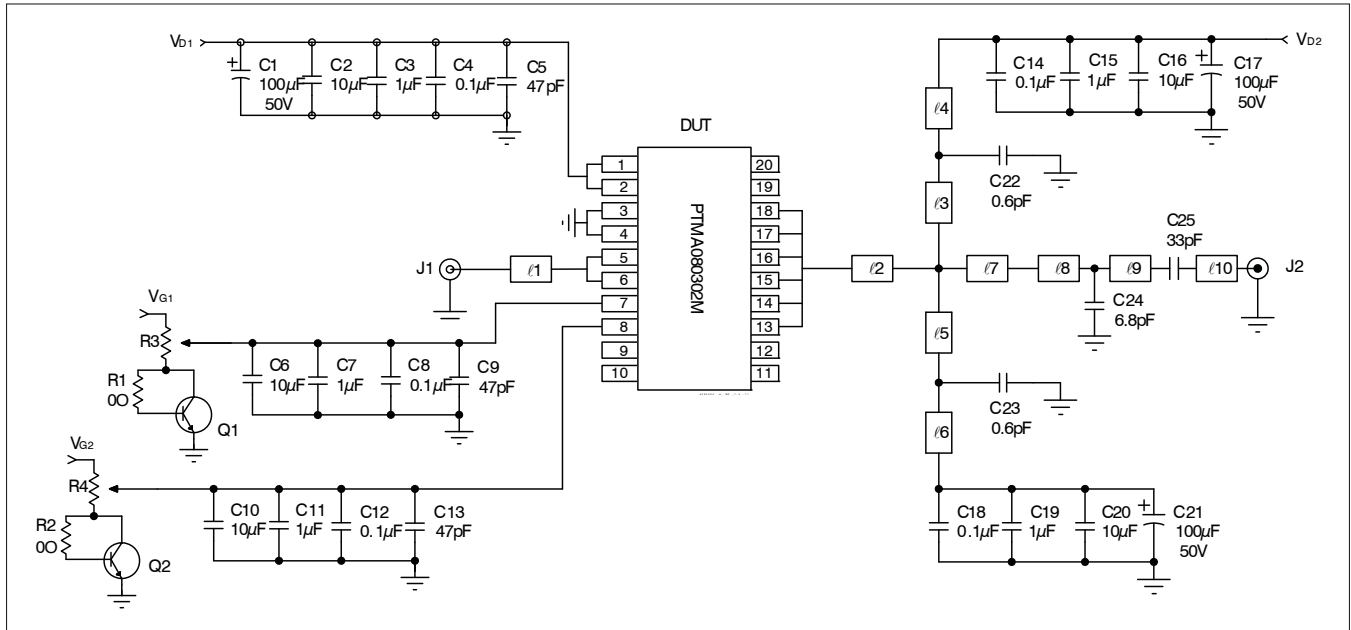


Broadband Circuit Impedance

Frequency MHz	Z Load Ω	
	R	jX
700	11.7	-4.5
720	11.0	-4.0
740	10.3	-3.6
760	9.8	-3.1
780	9.3	-2.6
800	8.9	-2.1
820	8.6	-1.6
840	8.3	-1.0
860	8.0	-0.5
880	7.8	0.0
900	7.7	0.6
920	7.6	1.1
940	7.5	1.7
960	7.4	2.3
980	7.4	2.9
1000	7.5	3.5



Reference Circuit — for evaluation only



Reference circuit schematic for $f = 940 \text{ MHz}$

Circuit Description

DUT PTMA080302M

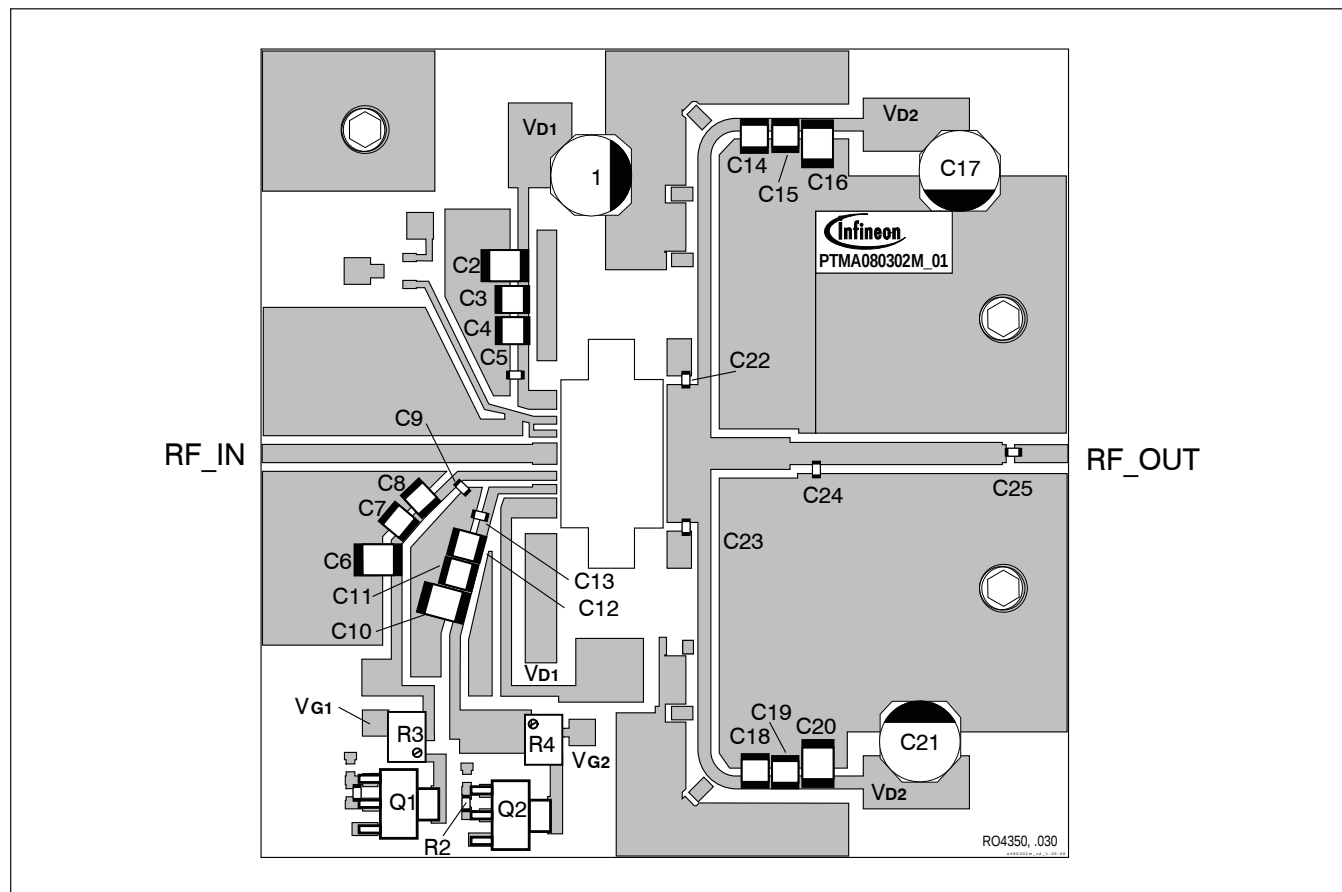
PCB Rogers 4350, 0.76 mm [.030"] thick, $\epsilon_r = 3.48$, 1 oz. copper

Test Fixture Part No. LTN/PTMA080302M

Find Gerber files for this test fixture on the Infineon Web site at <http://www.infineon.com/rfpower>

Microstrip	Electrical Characteristics at 940 MHz	Dimensions: L x W (mm)	Dimensions: L x W (in.)
$\ell 1$	0.143λ , 50.0Ω	27.76×1.70	1.093×0.067
$\ell 2$	0.012λ , 10.4Ω	2.01×13.00	0.079×0.512
$\ell 3, \ell 5$	0.012λ , 10.4Ω	2.06×13.00	0.081×0.512
$\ell 4, \ell 6$	0.156λ , 60.0Ω	30.61×1.22	1.205×0.048
$\ell 7$	0.040λ , 34.0Ω	7.52×3.00	0.296×0.118
$\ell 8$	0.020λ , 43.3Ω	3.81×2.11	0.150×0.083
$\ell 9$	0.086λ , 43.3Ω	16.43×2.11	0.647×0.083
$\ell 10$	0.026λ , 50.0Ω	5.03×1.70	0.198×0.067

Reference Circuit (cont.)



Reference circuit assembly diagram (not to scale)

Component	Description	Suggested Manufacturer	P/N or Comment
C1, C17, C21	Electrolytic capacitor, 100 μ F, 50 V		Digi-Key PCE3718CT-ND
C2, C6, C10, C16, C20	Ceramic capacitor, 10 μ F	Murata	GRM422Y5V106Z050AL
C3, C7, C11, C15, C19	Ceramic capacitor, 1 μ F	Digi-Key	445-1411-2-ND
C4, C8, C12, C14, C18	Capacitor, 0.1 μ F	Digi-Key	399-1267-2-ND
C5, C9, C13	Ceramic capacitor, 47 pF	ATC	600F470JT
C22, C23	Ceramic capacitor, 0.6 pF	ATC	600S0R6BT
C24	Ceramic capacitor, 6.8 pF	ATC	600S6R8CT
C25	Ceramic capacitor, 33 pF	ATC	600F330JT
Q1, Q2	Transistor	Infineon Technologies	BCP56
R1, R2	Resistor, 0 Ω	Digi-Key	603
R3, R4	Potentiometer 2k Ω	Digi-Key	3224W-202ETR-ND

Package Outline Specifications

Package PG-DSO-20-63

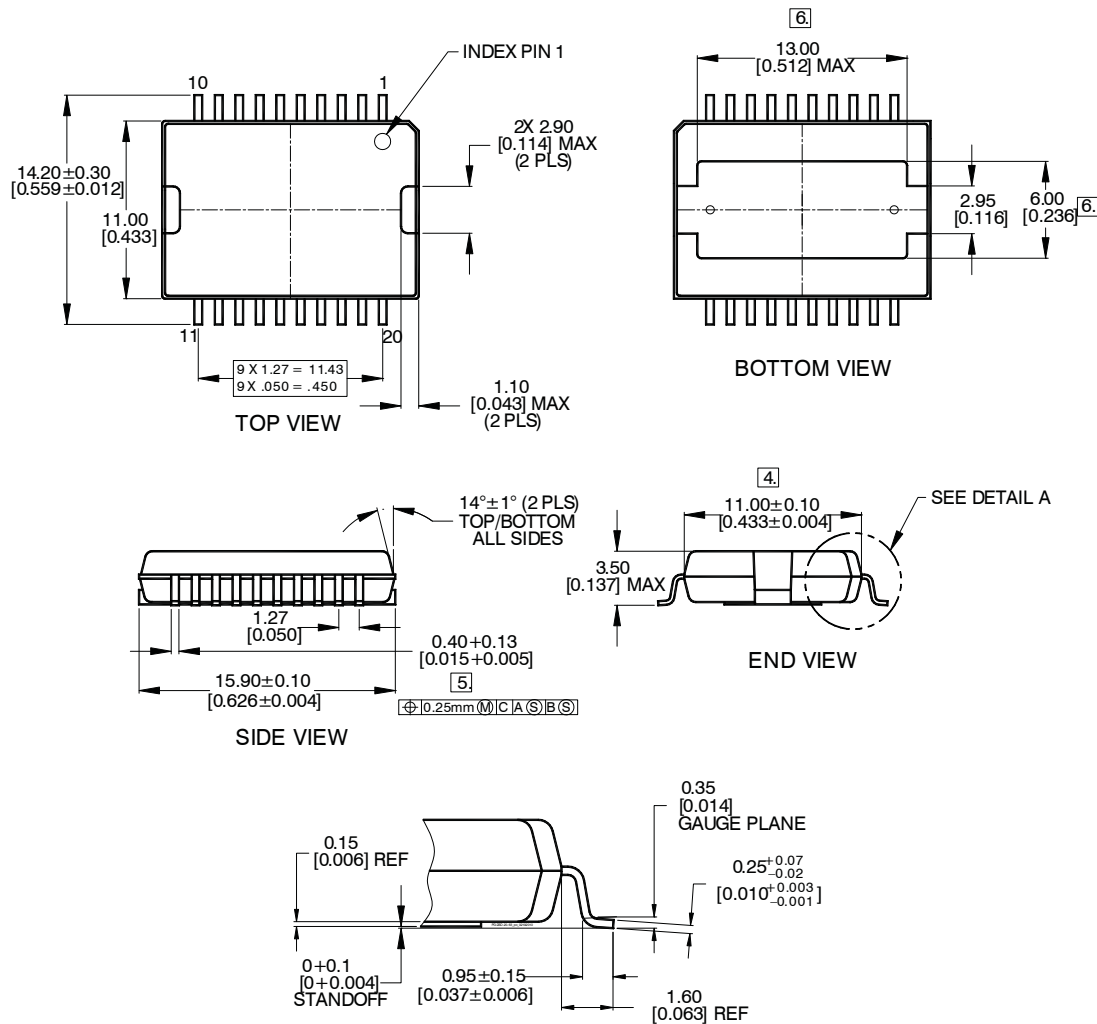
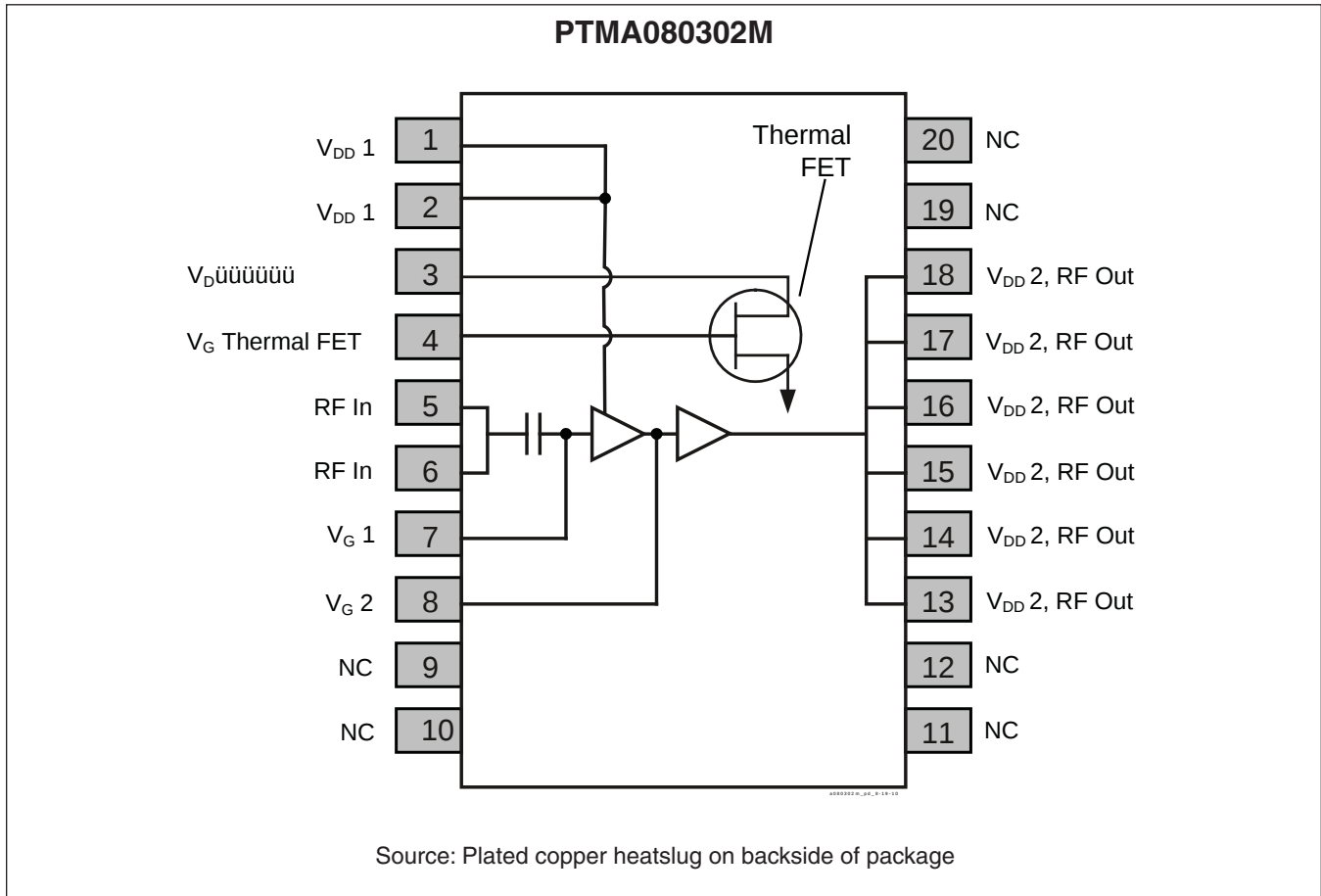


Diagram Notes—unless otherwise specified:

- Interpret dimensions and tolerances per ASME Y14.5M-1994.
- Package dimensions: 11.0 mm by 15.9 mm by 3.35 mm.
- JEDEC drawing number: MO-166.
- Does not include plastic or metal protrusion of 0.15 mm max per side.
- Does not include dambar protrusion; maximum allowable dambar protrusion shall be 0.08 mm.
- Bottom metallization. Sn plating (matte) : 5 – 15 micron [196.85 – 590.55 microinch].

Refer to Application Note "Recommendations for Printed Circuit Board Assembly of Infineon DSO and SSOP Packages" for additional information.

Pinout Diagram



Find the latest and most complete information about products and packaging at the Infineon Internet page
<http://www.infineon.com/rfpower>

Revision History: 2011-08-10

Data Sheet

Previous Version: 2010-11-09, Data Sheet

Page	Subjects (major changes since last revision)
2	Changes to $V_{(BR)DSS}$ and $RDS(on)$ on DC table and updates to RF table.

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Any information within this document that you feel is wrong, unclear or missing at all?

Your feedback will help us to continuously improve the quality of this document.

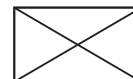
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