



3.3V CMOS DUAL NEGATIVE-EDGE-TRIGGERED J-K FLIP-FLOP WITH CLEAR AND PRESET, 5 VOLT TOLERANT I/O

IDT74LVC112A

FEATURES:

- 0.5 MICRON CMOS Technology
- ESD > 2000V per MIL-STD-883, Method 3015;
> 200V using machine model (C = 200pF, R = 0)
- 1.27mm pitch SOIC, 0.635mm pitch QSOP,
0.65mm pitch SSOP, 0.65mm pitch TSSOP packages
- Extended commercial range of -40°C to $+85^{\circ}\text{C}$
- $V_{CC} = 3.3\text{V} \pm 0.3\text{V}$, Normal Range
- $V_{CC} = 2.3\text{V}$ to 3.6V , Extended Range
- CMOS power levels ($0.4\mu\text{W}$ typ. static)
- Rail-to-Rail output swing for increased noise margin
- All inputs, outputs and I/O are 5 Volt tolerant
- Supports hot insertion

Drive Features for LVC112A:

- High Output Drivers: $\pm 24\text{mA}$
- Reduced system switching noise

APPLICATIONS:

- 5V and 3.3V mixed voltage systems
- Data communication and telecommunication systems

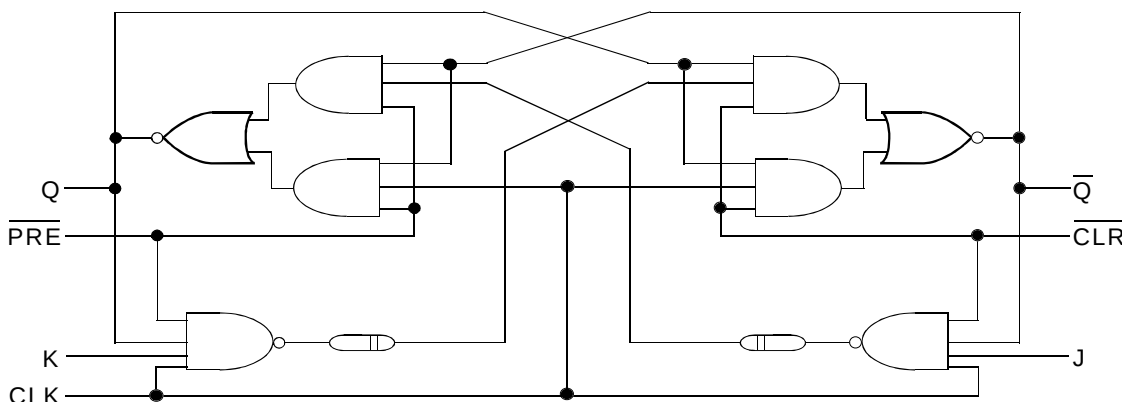
DESCRIPTION:

This dual negative-edge-triggered J-K flip-flop is built using advanced dual metal CMOS technology. A low level at the preset ($\overline{\text{PRE}}$) or clear ($\overline{\text{CLR}}$) inputs sets or resets the outputs, regardless of the levels of the other inputs. When $\overline{\text{PRE}}$ and $\overline{\text{CLR}}$ are inactive (high), data at the J and K inputs meeting the setup time requirements is transferred to the outputs on the negative-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold-time interval, data at the J and K inputs can be changed without affecting the levels at the outputs. The LVC112A can perform as a toggle flip-flop by tying J and K high.

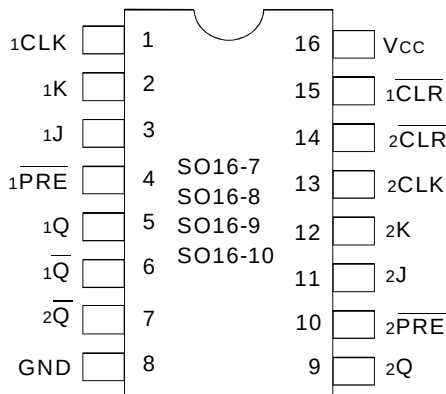
Inputs can be driven from either 3.3V or 5V devices. This feature allows the use of this device as a translator in a mixed 3.3V/5V supply system.

The LVC112A has been designed with a $\pm 24\text{mA}$ output driver. This driver is capable of driving a moderate to heavy load while maintaining speed performance.

Functional Block Diagram



PIN CONFIGURATION



QSOP/ SOIC/ SSOP/ TSSOP
TOP VIEW

ABSOLUTE MAXIMUM RATINGS ⁽¹⁾

Symbol	Description	Max.	Unit
V _{TERM} ⁽²⁾	Terminal Voltage with Respect to GND	– 0.5 to +6.5	V
V _{TERM} ⁽³⁾	Terminal Voltage with Respect to GND	– 0.5 to +6.5	V
T _{STG}	Storage Temperature	– 65 to +150	°C
I _{OUT}	DC Output Current	– 50 to +50	mA
I _{IK} I _{OK}	Continuous Clamp Current, V _I < 0 or V _O < 0	– 50	mA
I _{CC} I _{SS}	Continuous Current through each V _{CC} or GND	±100	mA

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NOTES:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- V_{CC} terminals.
- All terminals except V_{CC}.

PIN DESCRIPTION

Pin Names	Description
xCLK	CLK Inputs
xCLR-bar	Clear Inputs (Active LOW)
xPRE-bar	Preset Inputs (Active LOW)
xJ, xK	Data Inputs
xQ, xQ-bar	Data Outputs

FUNCTION TABLE ⁽¹⁾

Inputs					Outputs	
xPRE-bar	xCLR-bar	xCLK	xJ	xK	xQ	xQ-bar
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H ⁽²⁾	H ⁽²⁾
H	H	↓	L	L	Q ₀	Q ₀ -bar
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	Toggle	
H	H	H	X	X	Q ₀	Q ₀ -bar

NOTES:

- H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
Q₀ = Level of Q before the indicated steady-state input conditions were established.
Q₀-bar = Complement of Q₀ or level of Q-bar before the indicated steady-state input conditions were established.
- The output levels in this configuration may not meet the minimum levels for VOH. Furthermore, this configuration is unstable; that is, it does not persist when either PRE-bar or CLR-bar returns to its inactive (high) level.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter ⁽¹⁾	Conditions	Typ.	Max.	Unit
C _{IN}	Input Capacitance	V _{IN} = 0V	4.5	6	pF
C _{OUT}	Output Capacitance	V _{OUT} = 0V	5.5	8	pF
C _{I/O}	I/O Port Capacitance	V _{IN} = 0V	6.5	8	pF

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NOTE:

- As applicable to the device type.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Operating Condition: $T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$

Symbol	Parameter	Test Conditions		Min.	Typ. ⁽¹⁾	Max.	Unit
V_{IH}	Input HIGH Voltage Level	$V_{CC} = 2.3\text{V to } 2.7\text{V}$		1.7	—	—	V
		$V_{CC} = 2.7\text{V to } 3.6\text{V}$		2	—	—	
V_{IL}	Input LOW Voltage Level	$V_{CC} = 2.3\text{V to } 2.7\text{V}$		—	—	0.7	V
		$V_{CC} = 2.7\text{V to } 3.6\text{V}$		—	—	0.8	
I_{IH} I_{IL}	Input Leakage Current	$V_{CC} = 3.6\text{V}$	$V_I = 0 \text{ to } 5.5\text{V}$	—	—	± 5	μA
I_{OZH} I_{OZL}	High Impedance Output Current (3-State Output pins)	$V_{CC} = 3.6\text{V}$	$V_O = 0 \text{ to } 5.5\text{V}$	—	—	± 10	μA
I_{OFF}	Input/Output Power Off Leakage	$V_{CC} = 0\text{V}$, V_{IN} or $V_O \leq 5.5\text{V}$		—	—	± 50	μA
V_{IK}	Clamp Diode Voltage	$V_{CC} = 2.3\text{V}$, $I_{IN} = -18\text{mA}$		—	-0.7	-1.2	V
V_H	Input Hysteresis	$V_{CC} = 3.3\text{V}$		—	100	—	mV
I_{CCL} I_{CCH} I_{CCZ}	Quiescent Power Supply Current	$V_{CC} = 3.6\text{V}$	$V_{IN} = \text{GND or } V_{CC}$	—	—	10	μA
ΔI_{CC}	Quiescent Power Supply Current Variation	One input at $V_{CC} - 0.6\text{V}$ other inputs at V_{CC} or GND		—	—	500	μA

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NOTE:

- Typical values are at $V_{CC} = 3.3\text{V}$, $+25^{\circ}\text{C}$ ambient.

OUTPUT DRIVE CHARACTERISTICS

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	$V_{CC} = 2.3\text{V to } 3.6\text{V}$	$I_{OH} = -0.1\text{mA}$	$V_{CC} - 0.2$	—	V
		$V_{CC} = 2.3\text{V}$	$I_{OH} = -6\text{mA}$	2	—	
		$V_{CC} = 2.3\text{V}$	$I_{OH} = -12\text{mA}$	1.7	—	
		$V_{CC} = 2.7\text{V}$		2.2	—	
		$V_{CC} = 3.0\text{V}$		2.4	—	
		$V_{CC} = 3.0\text{V}$	$I_{OH} = -24\text{mA}$	2.2	—	
V_{OL}	Output LOW Voltage	$V_{CC} = 2.3\text{V to } 3.6\text{V}$	$I_{OL} = 0.1\text{mA}$	—	0.2	V
		$V_{CC} = 2.3\text{V}$	$I_{OL} = 6\text{mA}$	—	0.4	
			$I_{OL} = 12\text{mA}$	—	0.7	
		$V_{CC} = 2.7\text{V}$	$I_{OL} = 12\text{mA}$	—	0.4	
		$V_{CC} = 3.0\text{V}$	$I_{OL} = 24\text{mA}$	—	0.55	

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NOTE:

- V_{IH} and V_{IL} must be within the min. or max. range shown in the DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE table for the appropriate V_{CC} range. $T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$.

OPERATING CHARACTERISTICS, $T_A = 25^\circ\text{C}$

Symbol	Parameter	Test Conditions	V _{CC} = 2.5V±0.2V	V _{CC} = 3.3V±0.3V	Unit
			Typical	Typical	
CPD	Power Dissipation Capacitance per Flip-Flop	CL = 0pF, f = 10Mhz	—	24	pF

SWITCHING CHARACTERISTICS ⁽¹⁾

Symbol	Parameter	V _{CC} = 2.5V±0.2V		V _{CC} = 2.7V		V _{CC} = 3.3V±0.3V		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
f _{MAX}		—	—	150	—	150	—	MHz
t _{PLH} t _{PHL}	Propagation Delay x $\overline{\text{CLR}}$ or $\overline{\text{PRE}}$ to xQ or x $\overline{\text{Q}}$	—	—	—	5.5	1	4.8	ns
t _{PLH} t _{PHL}	Propagation Delay x $\overline{\text{CLK}}$ to xQ or x $\overline{\text{Q}}$	—	—	—	7.1	1	5.9	ns
t _{SU}	Setup Time, Data before CLK↓	—	—	2.3	—	3.1	—	ns
t _{SU}	Setup Time, $\overline{\text{PRE}}$ or $\overline{\text{CLR}}$ inactive	—	—	1.1	—	2.4	—	ns
t _H	Hold Time, data after CLK↓	—	—	0.7	—	2.5	—	ns
t _w	Pulse Width, CLK HIGH or LOW	—	—	3.3	—	3.3	—	ns
t _{SK(0)}	Output Skew ⁽²⁾	—	—	—	—	—	500	ps

NOTES:

1. See test circuits and waveforms. $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$.
2. Skew between any two outputs of the same package and switching in the same direction.

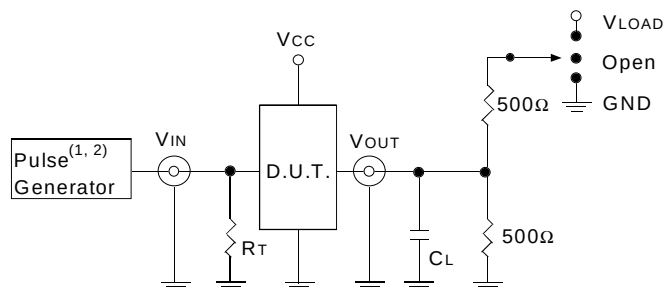
TEST CIRCUITS AND WAVEFORMS

TEST CONDITIONS

Symbol	V _{CC} (1)= 2.5V ±0.2V	V _{CC} (2)= 3.3V ±0.3V & 2.7V	Unit
V _{LOAD}	2 x V _{CC}	6	V
V _{IH}	V _{CC}	2.7	V
V _T	V _{CC} / 2	1.5	V
V _{LZ}	150	300	mV
V _{HZ}	150	300	mV
C _L	30	50	pF

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TEST CIRCUITS FOR ALL OUTPUTS



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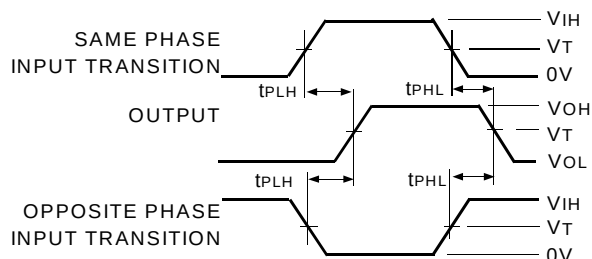
DEFINITIONS:

C_L = Load capacitance: includes jig and probe capacitance.
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

NOTES:

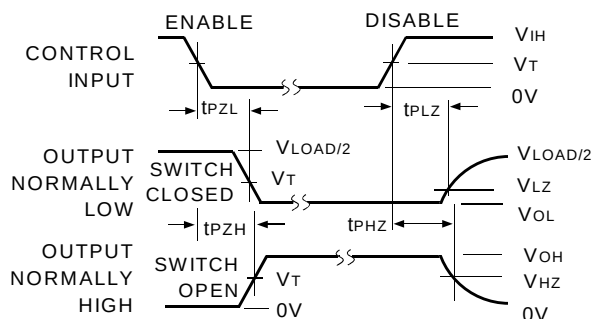
1. Pulse Generator for All Pulses: Rate ≤ 10MHz; t_F ≤ 2ns; t_R ≤ 2ns.
2. Pulse Generator for All Pulses: Rate ≤ 10MHz; t_F ≤ 2.5ns; t_R ≤ 2.5ns.

PROPAGATION DELAY



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ENABLE AND DISABLE TIMES



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NOTE:

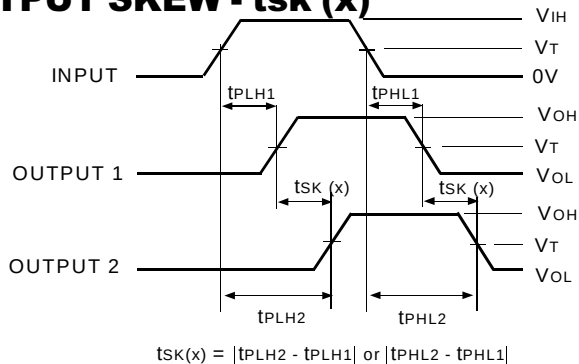
1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.

SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	V _{LOAD}
Disable High Enable High	GND
All Other tests	Open

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OUTPUT SKEW - t_{SK}(x)



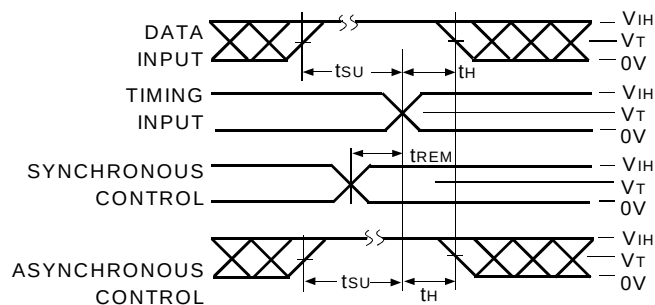
$$t_{SK}(x) = |t_{PLH2} - t_{PLH1}| \text{ or } |t_{PHL2} - t_{PHL1}|$$

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NOTES:

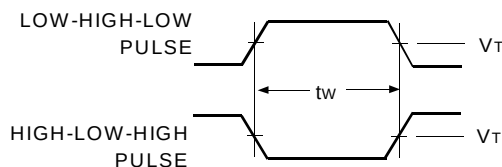
1. For t_{SK}(o) OUTPUT1 and OUTPUT2 are any two outputs.
2. For t_{SK}(b) OUTPUT1 and OUTPUT2 are in the same bank.

SET-UP, HOLD, AND RELEASE TIMES



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PULSE WIDTH



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ORDERING INFORMATION

IDT	XX	LVC	XXXX	XX	
Temp. Range	Device Type	Package			
				Q	Quarter Size Outline Package (SO16-7)
				DC	Small Outline IC (SO16-8)
				PY	Shrink Small Outline Package (SO16-9)
				PG	Thin Shrink Small Outline Package (SO16-10)
				112A	Dual Negative-Edge-Triggered J-K Flip-Flop with Clear and Preset
				74	-40°C to +85°C



CORPORATE HEADQUARTERS
 2975 Stender Way
 Santa Clara, CA 95054

for SALES:
 800-345-7015 or 408-727-6116
 fax: 408-492-8674
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