User's Guide

TPS51117 Buck Controller Evaluation Module User's Guide

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1 Introduction

1.1 Description

The TPS51117 evaluation module (EVM) is designed to evaluate the performance and characteristics of TI's cost-optimized, D-CAP™ mode, synchronous buck TPS51117 controller. The evaluation module uses 6-V to 21-V input and delivers 1.05-V output at 10 A.

1.2 Features

- Multiple footprint designs support multiple MOSFET configurations
- Abundant test points provide users with great convenience. See Table 2-1.
- Although two TPS51117 package styles are available, the EVM is designed to demonstrate the QFN14 package.

1.3 Operating Specification

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input Characteristics					
Voltage range (V5IN)	V_{IN}	4.5		5.5	V
Voltage range (V_{BAT})	V_{IN}	6		21	
Output Characteristics					
Output voltage	Configuration of EVM		1.05		V
Output voltage regulation	Line regulation			0.1%	
	Load regulation			0.3%	
Output voltage ripple	V5IN = 5 V, V_{BAT} = 12 V			35	mVpp
Output current				10	A
Current limit			15		
Systems Characteristics					
Switching frequency			350	400	kHz
Peak efficiency	V5IN = 5 V, V_{BAT} = 12 V, 1.05 V/1 A		89.4%		
Full load efficiency	V5IN = 5 V, V_{BAT} = 12 V, 1.05 V/10 A		82.3%		
Operating temperature			25		°C

1.4 Schematic

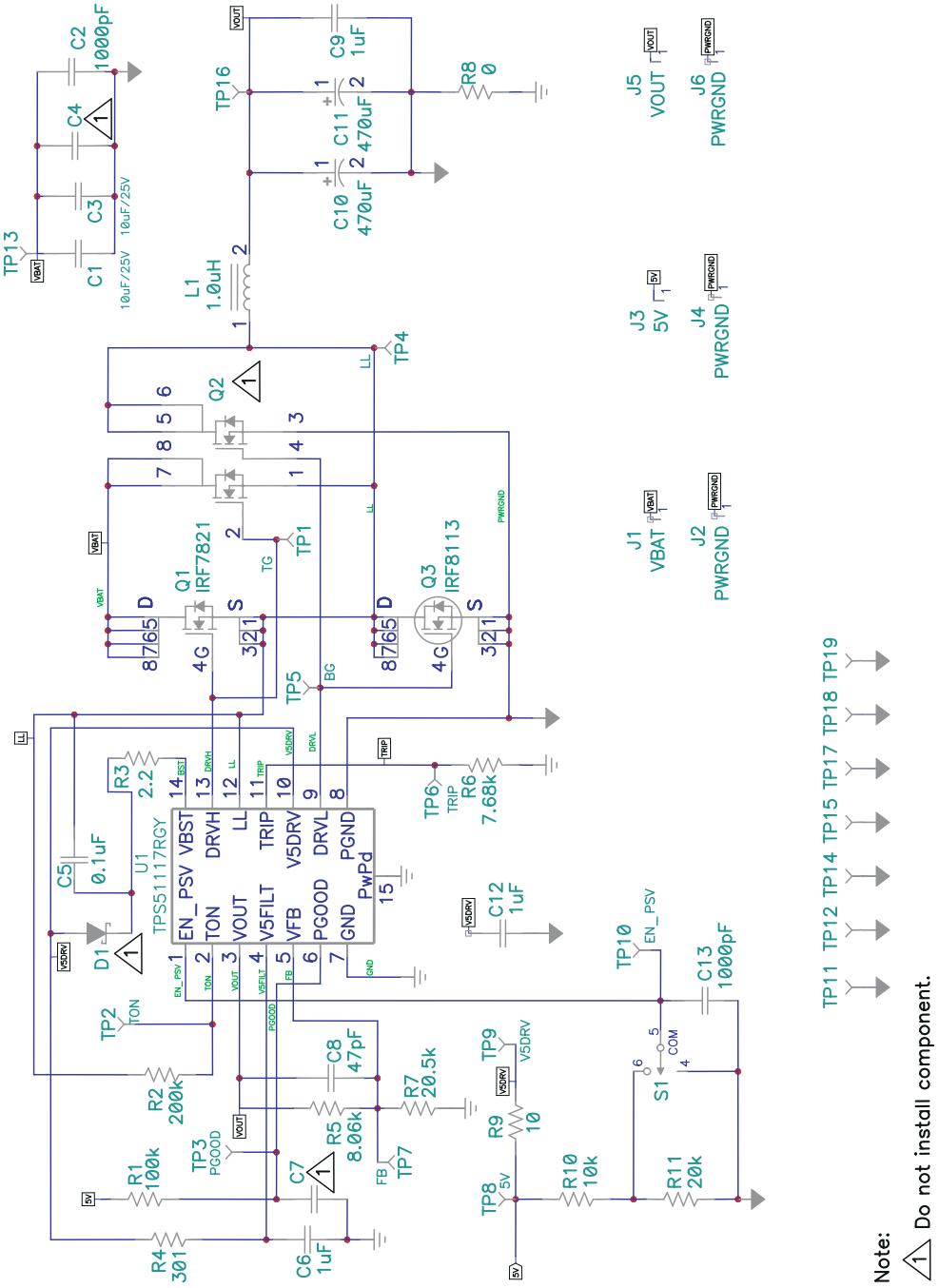

Figure 1-1. TPS51117RGY Evaluation Module (1.05 V at 10 A) Schematic Diagram

2 Test Setup

2.1 Test Equipment

Voltage Source: Two power supplies are needed, one capable of supplying 21 VDC at 5 A connected at J1 and J2, the other 5 V at 1 A connected at J3 and J4. The minimum recommended wire size is AWG #16 with the total length of wire less than four feet (2-feet input, 2-feet return) to connect the TPS51117 EVM board.

Loads: One electronic load is needed that should be capable of sinking 10 A at 1 V to test specified output and 16 A maximum to test current limit. The minimum recommended wire size is AWG #16 with the total length of wire less than four feet (2-feet input, 2-feet return) to connect the TPS51117 EVM board at J5 and J6.

Meters: Three digital multi-meters are required.

Oscilloscope: A minimum 50-MHz digital oscilloscope with one voltage probe is required.

2.2 Test Points

Table 2-1. Test Point Functions

TEST POINTS	NAME	DESCRIPTION
TP1	DRVH	High-side gate drive
TP2 (NP)	TON	On-time / frequency measurement
TP3	PGOOD	Power good
TP4	LL	High-side gate driver return / anode for overcurrent comparator
TP5	DRVL	Low-side gate drive
TP6	TRIP	Overcurrent trip point set input
TP7 (NP)	FB	Feedback input
TP8	5V	5-V supply voltage
TP9	V5DRV	5-V power supply input for FET gate drivers
TP10	EN_PSV	Enable power save
TP11 (NP)	GND	Ground
TP12	GND	Ground
TP13	VBAT	V_{IN} supply voltage
TP14	GND	Ground
TP15	GND	Ground
TP16	VOUT	Output voltage
T17	GND	Ground
TP18	GND	Ground
TP19 (NP)	GND	Ground

2.3 Recommended Test Setup

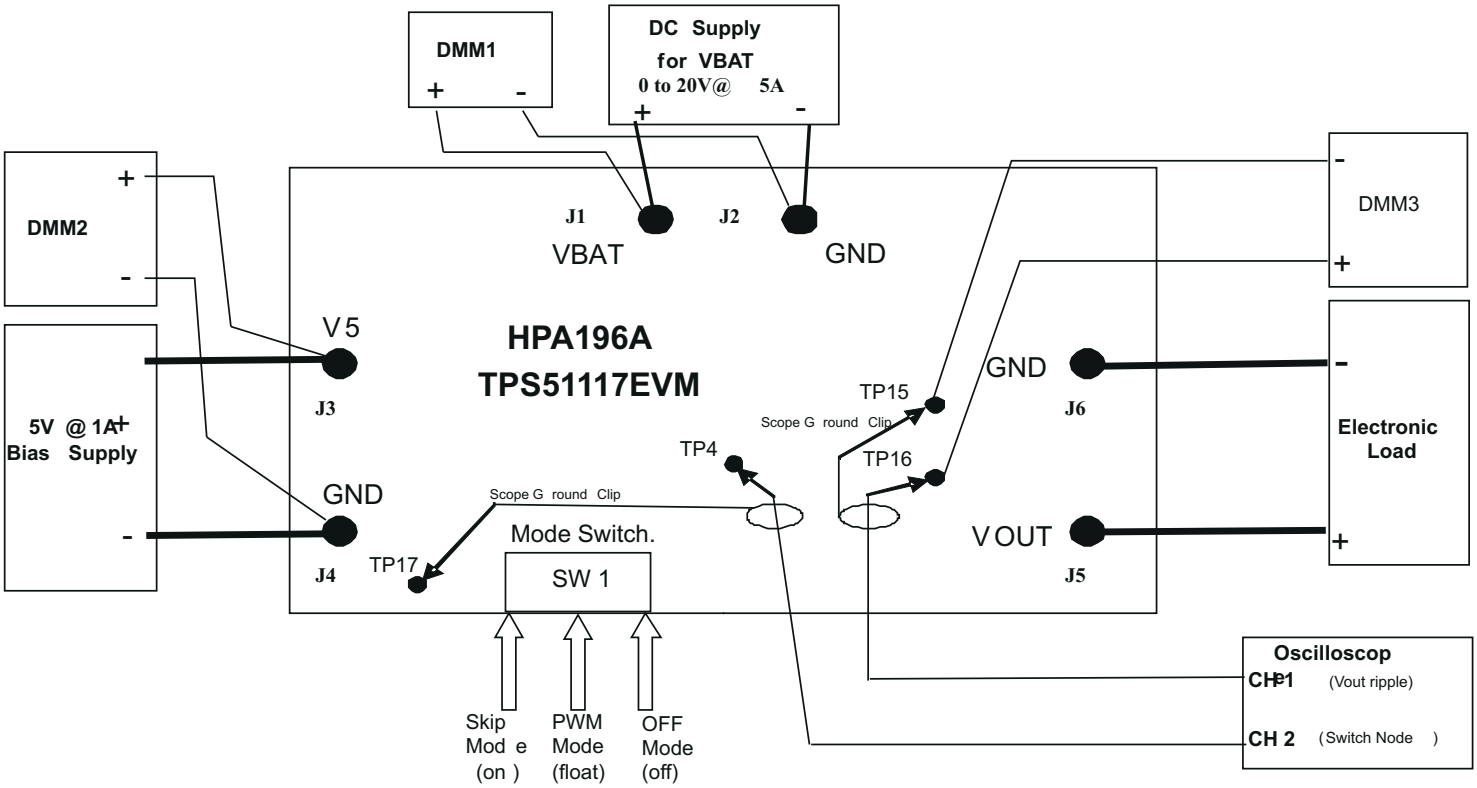

Figure 2-1. Test Setup

Figure 2-1 shows the recommended test setup to evaluate the TPS51117EVM. Working at an ESD workstation, make sure that any wrist straps or mats are connected referencing the user-to-earth ground before power is applied to the EVM.

2.4 Standard Test Procedures

2.4.1 Line/Load Regulation

1. Ensure the load is set to constant current mode and set to 0 A_{DC}.
2. Make sure the switch SW 1 is in the “OFF” position.
3. Turn on V_{BAT} supply, increase to 12 V, and use DMM1 to measure the voltage.
4. Turn on 5.0-V bias supply, increase to 5 V, and use DMM2 to measure the voltage.
5. Turn on SW1 to skip mode (On) and verify output voltage on DMM3.
6. Vary the load from 0 A_{DC} to 10 A_{DC}. V_{OUT} should remain in load regulation.
7. Move the SW1 to PWM mode (float) and repeat step 6.
8. With load still at 10 A_{DC}, vary the V_{BAT} supply from 6 V to 21 V. V_{OUT} should remain in line regulation.
9. Turn SW1 to the OFF position. Verify V_{OUT} is 0 V.
10. Decrease the load to 0 A.
11. Decrease bias supply and V_{BAT} supply to 0 V.

2.4.2 Output Ripple Measurement

1. Ensure the load is set to constant current mode and set to 0 A_{DC}.
2. Make sure the switch SW 1 is in the “OFF” position.
3. Turn on V_{BAT} supply, increase to 12 V, and use DMM1 to measure the voltage.
4. Turn on the 5.0-V bias supply, increase to 5 V, and use DMM2 to measure the voltage.
5. Set the load to 10 A_{DC}.
6. Attach an oscilloscope probe to TP16 and ground to TP15.
7. Set the oscilloscope as follows:
   a. Horizontal sweep: 2 µs/div
   b. Trigger mode: auto, falling edge
   c. Channel should be set to AC coupled, bandwidth 20 Mhz

   Measurement should be similar to Figure 3-5.

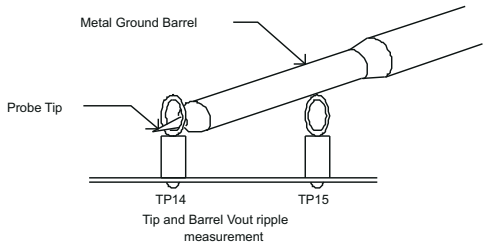

Figure 2-2. Tip and Barrel Measurement for V_{OUT} Ripple

3 Performance Data and Typical Characteristic Curves

Figure 3-1 through Figure 3-6 present typical performance curves for TPS51117EVM-001.

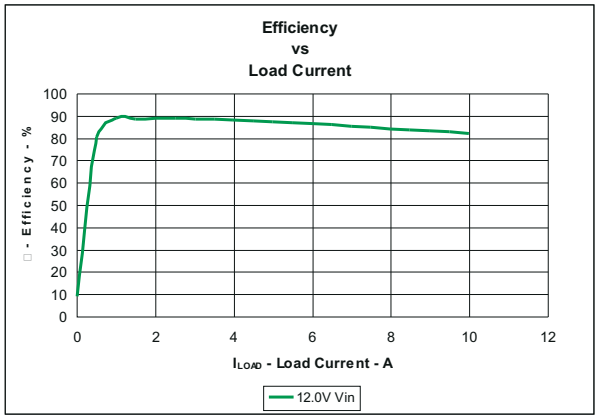

Figure 3-1. Efficiency

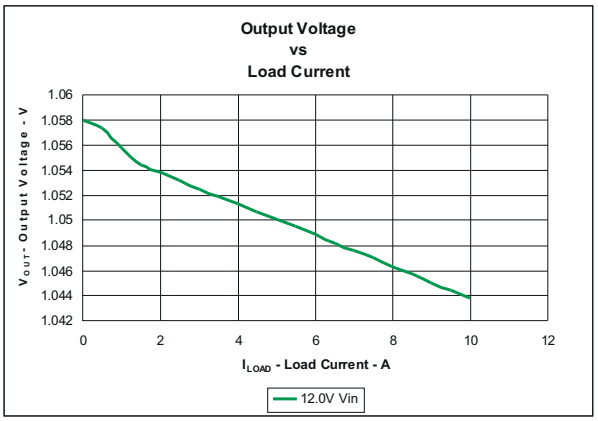

Figure 3-2. Load Regulation

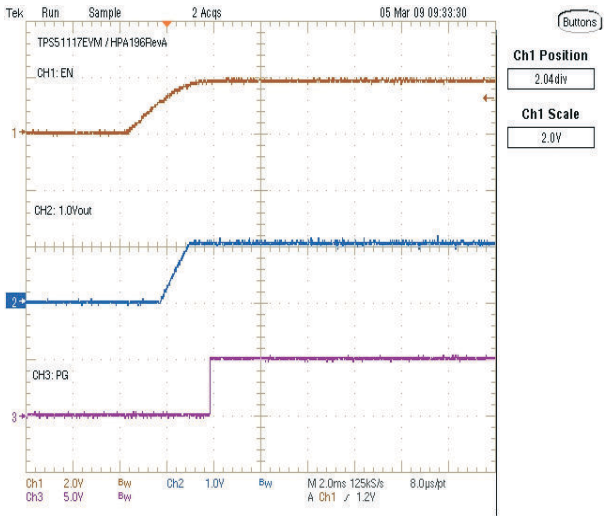

Figure 3-3. Enable Turn-On (12 V_{IN}, 1.05 V/10 A)

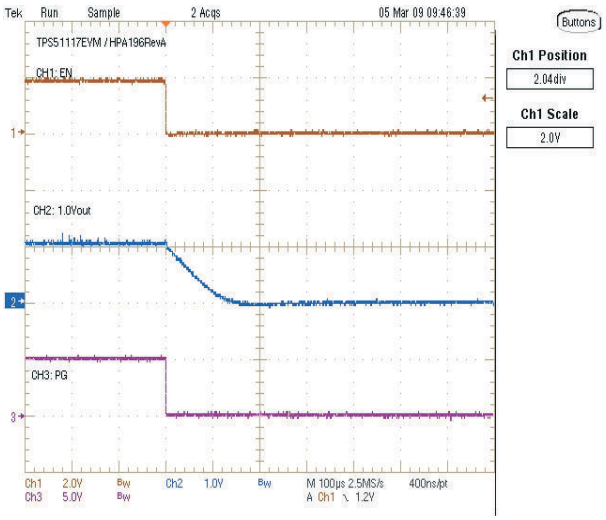

Figure 3-4. Enable Turn-Off (12 V_{IN}, 1.05 V/10 A)

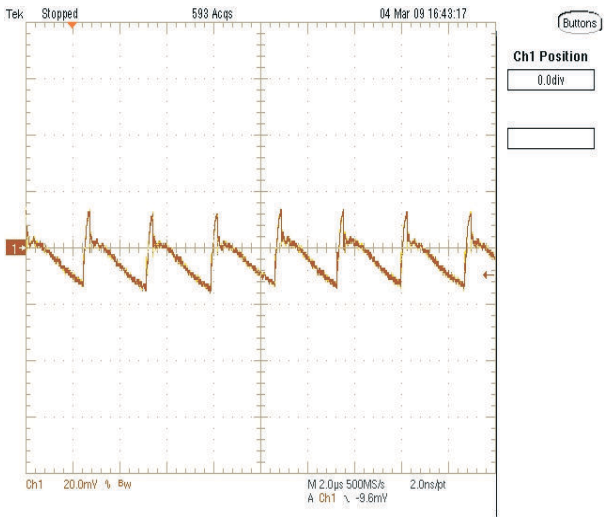

Figure 3-5. Output Ripple (12 V_{IN}, 1.05 V/10 A)

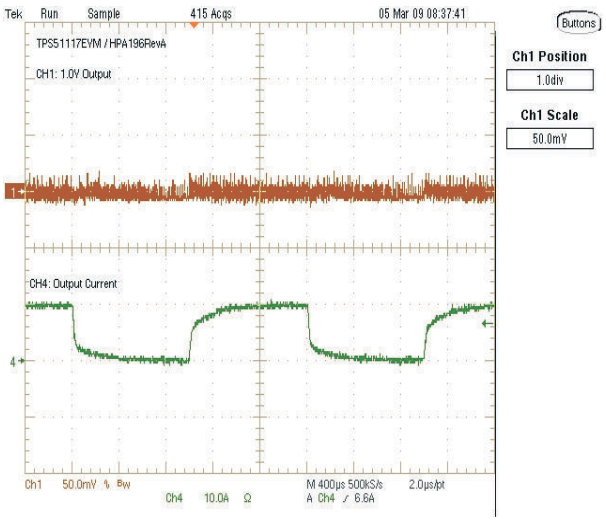

Figure 3-6. Load Transient (12 V_{IN} 1.05 V/0 A–10 A)

4 Board Layout Using TPS51117RGY (QFN 14)

Figure 4-1 through Figure 4-4 show the design of the TPS51117EVM printed circuit board. The EVM has been designed using four layers on a two-ounce copper circuit board.

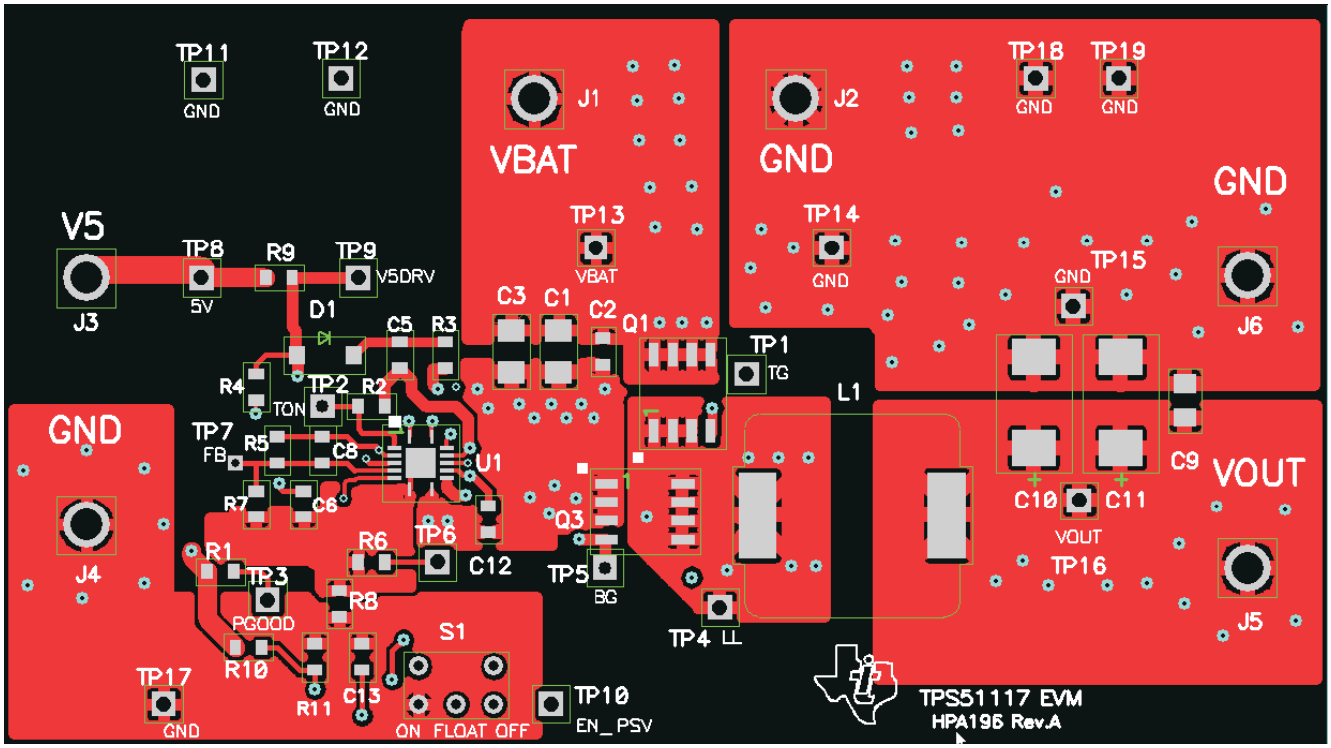

Figure 4-1. Top Layer Copper

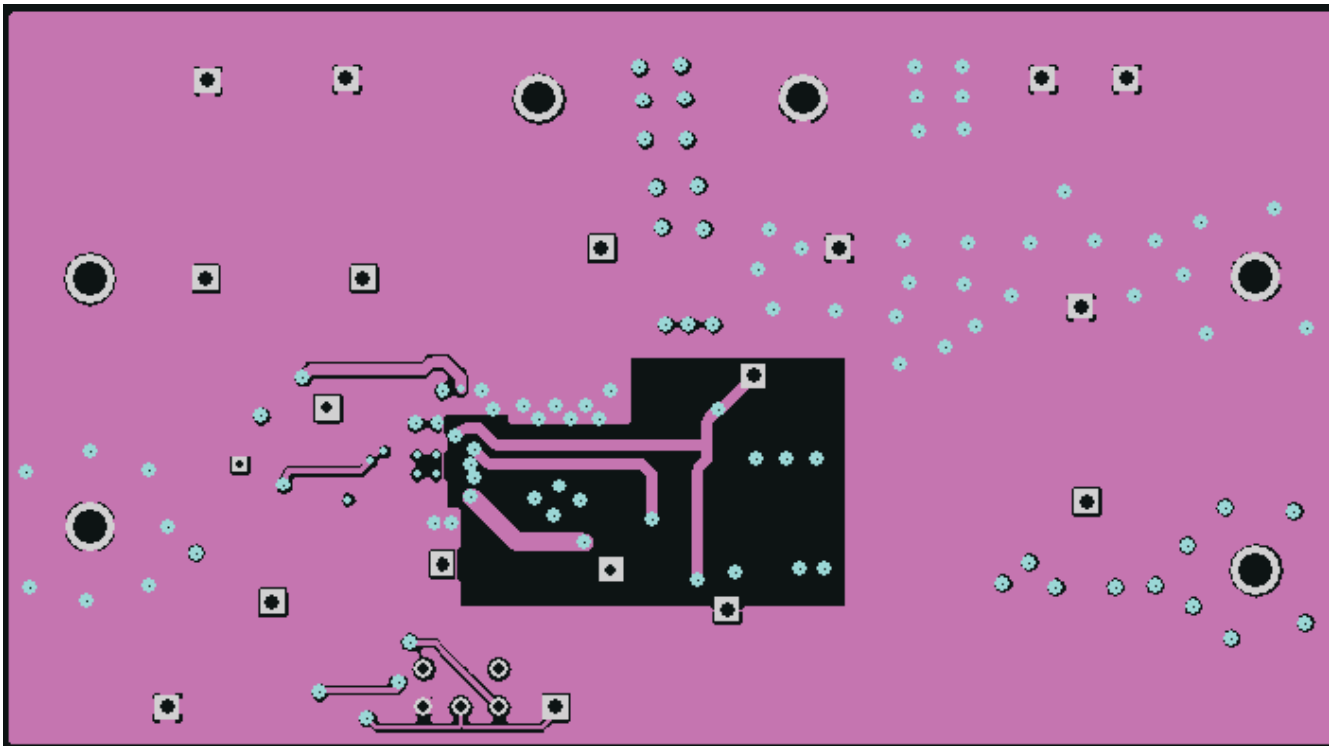

Figure 4-2. Layer 2 (Internal 1) Copper

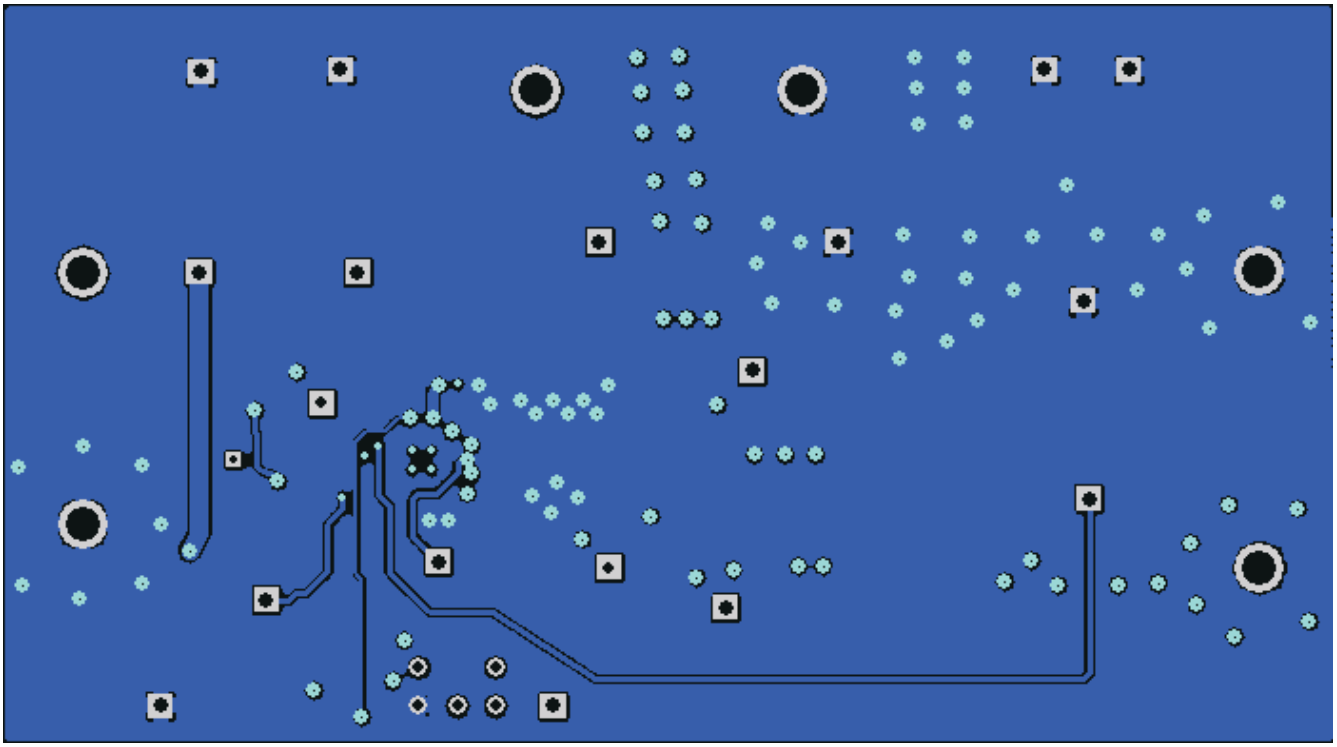

Figure 4-3. Layer 3 (Internal 2) Copper

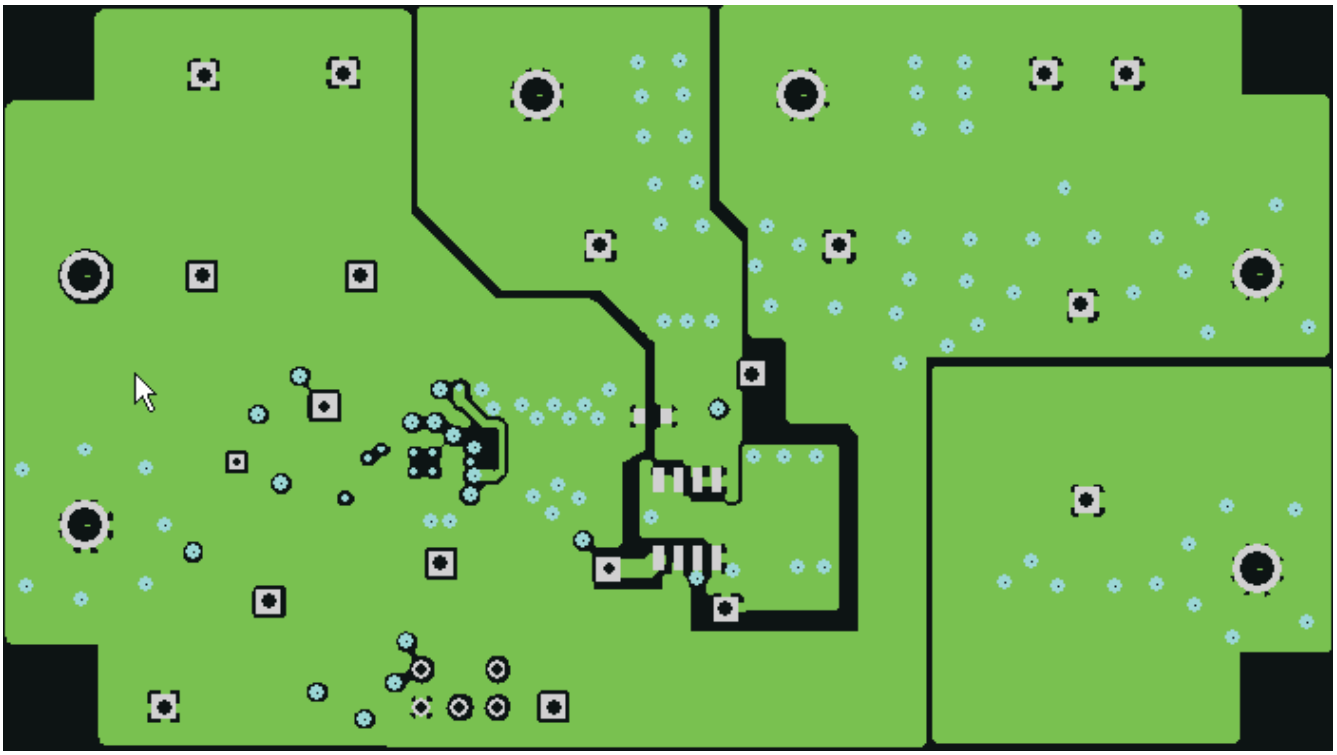

Figure 4-4. Bottom Layer Copper

5 List of Materials

The TPS51117EVM List of Materials.

Table 5-1. List of Materials

REFDES	PATTERN NAME	VALUE	PART NUMBER	MFR
EVM Configuration 1.05 V at 10 A BOM				
C5	C603	0.1 µF	VJ0603Y104KXXAC	Vishay
C12, C6	C603	1 µF, 16 V	C1608X7R1C105K	TDK
C8	C603	47 pF	VJ0603A470JXAAC	Vishay
C2, C13	C603	1000 pF	VJ0603Y102KXAAC	Vishay
C4	C603	Not Installed	VJ0603Y102KXAAC	Vishay
C7	C603	Not Installed	VJ0603Y103KXAAC	Vishay
C9	C0805	1 µF, 25 V	C2012X7R1E105K	TDK
C1, C3	C1206	10 µF, 25 V	ECJ-3YB1E106K	Panasonic
C10, C11	CAP_POSCAP_D	470 µF	2R5TPE470MC	Sanyo
J3	HEADER_8952	5 V	1582-2	Keystone
J2	HEADER_8952	PWRGND	1582-2	Keystone
J4	HEADER_8952	PWRGND	1582-2	Keystone
J6	HEADER_8952	PWRGND	1582-2	Keystone
J1	HEADER_8952	VBAT	1582-2	Keystone
J5	HEADER_8952	VOUT	1582-2	Keystone
D1	SOD-123	Not Installed	MBR0530Tx	On Semi
Q2	SO8	Not Installed	Si4944DY	Siliconix
L1	IND_IHLP-5050	1.0 µH	IHLP5050CEER1R0M01	Vishay
Q1	SO8	IRF7821	IRF7821	IR
Q3	SO8	IRF8113	IRF8113	IR
R8	R603	0 Ω	STD	Vishay
R3	R603	2.21 Ω	STD	Vishay
R6	R603	7.68 kΩ	STD	Vishay
R5	R603	8.06 kΩ	STD	Vishay
R9	R603	10 Ω	STD	Vishay
R4	R603	301 Ω	STD	Vishay
R10	R603	10 kΩ	STD	Vishay
R11	R603	20 kΩ	STD	Vishay
R7	R603	20.5 kΩ	STD	Vishay
R1	R603	100 kΩ	STD	Vishay
R2	R603	200 kΩ	CRCW06032003FKTA	Vishay
S1	SW_1P3T	G13AP	G13AP	NKK
U1	QFN14	TPS51117RGY	TPS51117RGY	TI

6 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (April 2009) to Revision B (February 2022) **Page**

- Updated the numbering format for tables, figures, and cross-references throughout the document. 2
- Updated the user's guide title 2

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