



128K x 8 Static RAM

Features

- 4.5V–5.5V operation
- CMOS for optimum speed/power
- Low active power (70 ns, LL version)
— 82.5 mW (max.) (15 mA)
- Low standby power (70 ns, LL version)
— 110 μ W (max.) (15 μ A)
- Automatic power-down when deselected
- TTL-compatible inputs and outputs
- Easy memory expansion with $\overline{CE_1}$, $\overline{CE_2}$, and $\overline{OE}$ options

Functional Description

The CY62128B is a high-performance CMOS static RAM organized as 131,072 words by 8 bits. Easy memory expansion is provided by an active LOW Chip Enable ($\overline{CE_1}$), an active HIGH Chip Enable ($\overline{CE_2}$), an active LOW Output Enable ($\overline{OE}$), and three-state drivers. This device has an automatic

power-down feature that reduces power consumption by more than 75% when deselected.

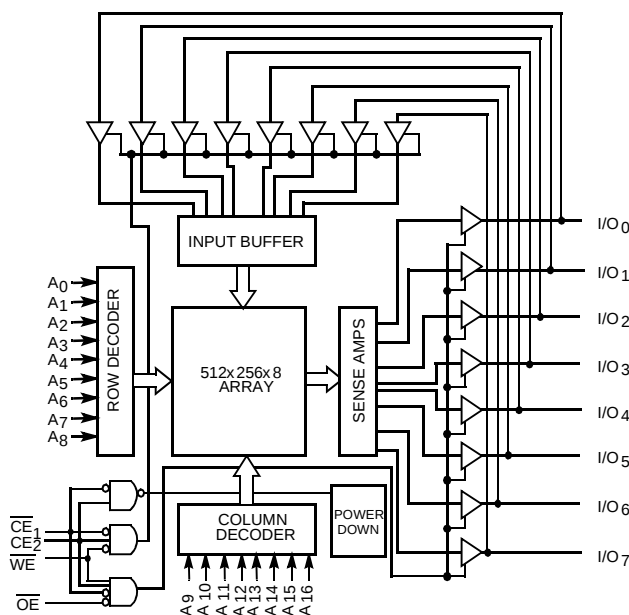
Writing to the device is accomplished by taking Chip Enable One ($\overline{CE_1}$) and Write Enable ($\overline{WE}$) inputs LOW and Chip Enable Two ($\overline{CE_2}$) input HIGH. Data on the eight I/O pins (I/O_0 through I/O_7) is then written into the location specified on the address pins (A_0 through A_{16}).

Reading from the device is accomplished by taking Chip Enable One ($\overline{CE_1}$) and Output Enable ($\overline{OE}$) LOW while forcing Write Enable ($\overline{WE}$) and Chip Enable Two ($\overline{CE_2}$) HIGH. Under these conditions, the contents of the memory location specified by the address pins will appear on the I/O pins.

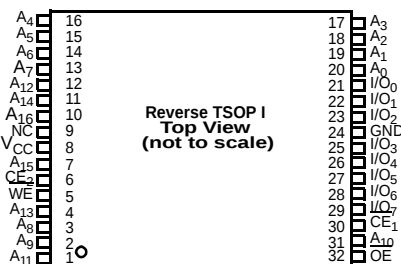
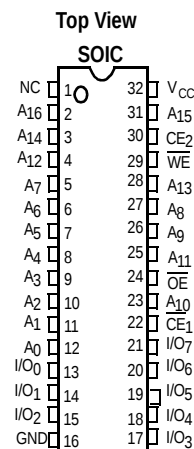
The eight input/output pins (I/O_0 through I/O_7) are placed in a high-impedance state when the device is deselected ($\overline{CE_1}$ HIGH or $\overline{CE_2}$ LOW), the outputs are disabled ($\overline{OE}$ HIGH), or during a write operation ($\overline{CE_1}$ LOW, $\overline{CE_2}$ HIGH, and $\overline{WE}$ LOW).

The CY62128B is available in a standard 450-mil-wide SOIC, 32-pin TSOP type I and STSOP packages.

Logic Block Diagram



Pin Configurations



STSOP Top View (not to scale)

TSOP I Top View (not to scale)

Selection Guide

			CY62128B-55	CY62128B-70	Unit
Maximum Access Time			55	70	ns
Maximum Operating Current (I_{CC})	Industrial	LL	20	15	mA
	Commercial	LL	20	15	mA
Maximum CMOS Standby Current (I_{SB2})	Industrial	LL	15	15	μ A
	Commercial	LL	15	15	μ A

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature -65°C to $+150^{\circ}\text{C}$

Ambient Temperature with
Power Applied..... -55°C to $+125^{\circ}\text{C}$

Supply Voltage on V_{CC} to Relative GND^[1] -0.5V to $+7.0\text{V}$

DC Voltage Applied to Outputs
in High Z State^[1] -0.5V to $V_{CC} + 0.5\text{V}$

DC Input Voltage^[1]..... -0.5V to $V_{CC} + 0.5\text{V}$

Current into Outputs (LOW) 20 mA

Static Discharge Voltage..... $>2001\text{V}$
(per MIL-STD-883, Method 3015)

Latch-Up Current..... $>200\text{ mA}$

Operating Range

Range	Ambient Temperature ^[2]	V
Industrial	-40°C to $+85^{\circ}\text{C}$	$5\text{V} \pm 10\%$
Commercial	0°C to $+70^{\circ}\text{C}$	$5\text{V} \pm 10\%$

Notes:

- V_{IL} (min.) = -2.0V for pulse durations of less than 20 ns.
- T_A is the "Instant On" case temperature.

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	62128B-55			62128B-70			Unit
			Min.	Typ. ^[3]	Max.	Min.	Typ. ^[3]	Max.	
V _{OH}	Output HIGH Voltage	V _{CC} = Min., I _{OH} = -1.0 mA	2.4			2.4			V
V _{OL}	Output LOW Voltage	V _{CC} = Min., I _{OL} = 2.1 mA			0.4			0.4	V
V _{IH}	Input HIGH Voltage		2.2		V _{CC} + 0.3	2.2		V _{CC} + 0.3	V
V _{IL}	Input LOW Voltage ^[1]		-0.3		0.8	-0.3		0.8	V
I _{IX}	Input Load Current	GND ≤ V _I ≤ V _{CC}	-1		+1	-1		+1	μA
I _{OZ}	Output Leakage Current	GND ≤ V _I ≤ V _{CC} , Output Disabled	-1		+1	-1		+1	μA
I _{OS}	Output Short Circuit Current ^[4]	V _{CC} = Max., V _{OUT} = GND			-300			-300	mA
I _{CC}	V _{CC} Operating Supply Current	V _{CC} = Max., I _{OUT} = 0 mA, f = f _{MAX} = 1/t _{RC}		7.5	20		6	15	mA
I _{SB1}	Automatic CE Power-Down Current —TTL Inputs	Max. V _{CC} , CE ₁ ≥ V _{IH} or CE ₂ ≤ V _{IL} , V _{IN} ≥ V _{IH} or V _{IN} ≤ V _{IL} , f = f _{MAX}		0.1	2		0.1	1	mA
I _{SB2}	Automatic CE Power-Down Current —CMOS Inputs	Max. V _{CC} , CE ₁ ≥ V _{CC} - 0.3V, or CE ₂ ≤ 0.3V, V _{IN} ≥ V _{CC} - 0.3V, or V _{IN} ≤ 0.3V, f = 0		2.5	15		2.5	15	μA
I _{CC}	V _{CC} Operating Supply Current	V _{CC} = Max., I _{OUT} = 0 mA, f = f _{MAX} = 1/t _{RC}		7.5	20		6	15	mA
I _{SB1}	Automatic CE Power-Down Current —TTL Inputs	Max. V _{CC} , CE ₁ ≥ V _{IH} or CE ₂ ≤ V _{IL} , V _{IN} ≥ V _{IH} or V _{IN} ≤ V _{IL} , f = f _{MAX}		0.1	2		0.1	1	mA
I _{SB2}	Automatic CE Power-Down Current —CMOS Inputs	Max. V _{CC} , CE ₁ ≥ V _{CC} - 0.3V, or CE ₂ ≤ 0.3V, V _{IN} ≥ V _{CC} - 0.3V, or V _{IN} ≤ 0.3V, f = 0		2.5	15		2.5	15	μA

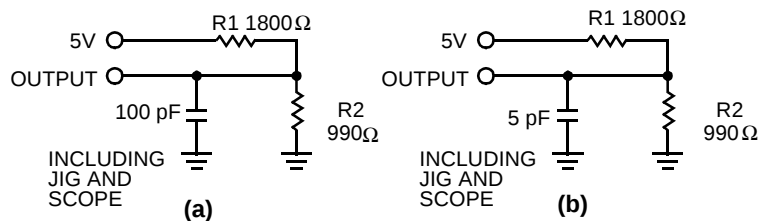
Capacitance^[5]

Parameter	Description	Test Conditions	Max.	Unit
C _{IN}	Input Capacitance	T _A = 25°C, f = 1 MHz, V _{CC} = 5.0V	9	pF
C _{OUT}	Output Capacitance		9	pF

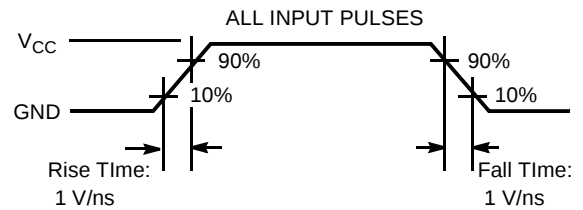
Notes:

- Typical values are included for reference only and are not tested or guaranteed. Typical values are an average of the distribution across normal production variations as measured at V_{CC} = 5.0V, T_A = 25°C, and t_{AA} = 70 ns
- Not more than one output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
- Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms



Equivalent to: THÉVENIN EQUIVALENT
 OUTPUT — 639 Ω — 1.77V



Switching Characteristics^[6] Over the Operating Range

Parameter	Description	62128B-55		62128B-70		Unit
		Min.	Max.	Min.	Max.	
READ CYCLE						
t _{RC}	Read Cycle Time	55		70		ns
t _{AA}	Address to Data Valid		55		70	ns
t _{OHA}	Data Hold from Address Change	5		5		ns
t _{ACE}	$\overline{CE}_1$ LOW to Data Valid, CE ₂ HIGH to Data Valid		55		70	ns
t _{DOE}	$\overline{OE}$ LOW to Data Valid		20		35	ns
t _{LZOE}	$\overline{OE}$ LOW to Low Z	0		0		ns
t _{HZOE}	$\overline{OE}$ HIGH to High Z ^[7, 8]		20		25	ns
t _{LZCE}	$\overline{CE}_1$ LOW to Low Z, CE ₂ HIGH to Low Z ^[8]	5		5		ns
t _{HZCE}	$\overline{CE}_1$ HIGH to High Z, CE ₂ LOW to High Z ^[7, 8]		20		25	ns
t _{PU}	$\overline{CE}_1$ LOW to Power-Up, CE ₂ HIGH to Power-Up	0		0		ns
t _{PD}	$\overline{CE}_1$ HIGH to Power-Down, CE ₂ LOW to Power-Down		55		70	ns
WRITE CYCLE ^[9]						
t _{WC}	Write Cycle Time	55		70		ns
t _{SCE}	$\overline{CE}_1$ LOW to Write End, CE ₂ HIGH to Write End	45		60		ns
t _{AW}	Address Set-Up to Write End	45		60		ns
t _{HA}	Address Hold from Write End	0		0		ns
t _{SA}	Address Set-Up to Write Start	0		0		ns
t _{PWE}	$\overline{WE}$ Pulse Width	45		50		ns
t _{SD}	Data Set-Up to Write End	25		30		ns
t _{HD}	Data Hold from Write End	0		0		ns
t _{LZWE}	$\overline{WE}$ HIGH to Low Z ^[8]	5		5		ns
t _{HZWE}	$\overline{WE}$ LOW to High Z ^[7, 8]		20		25	ns

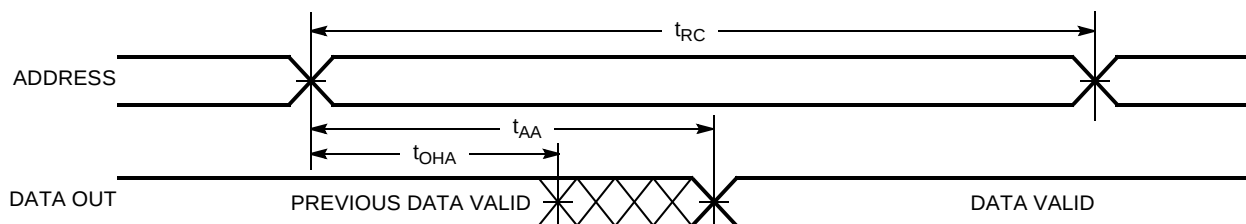
Notes:

- Test conditions assume signal transition time of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 100-pF load capacitance.
- t_{HZOE} , t_{HZCE} , and t_{HZWE} are specified with a load capacitance of 5 pF as in part (b) of AC Test Loads. Transition is measured ± 500 mV from steady-state voltage.
- At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE} , t_{HZOE} is less than t_{LZOE} , and t_{HZWE} is less than t_{LZWE} for any given device.
- The internal write time of the memory is defined by the overlap of $\overline{CE}_1$ LOW, CE_2 HIGH, and $\overline{WE}$ LOW. $\overline{CE}_1$ and $\overline{WE}$ must be LOW and CE_2 HIGH to initiate a write, and the transition of any of these signals can terminate the write. The input data set-up and hold timing should be referenced to the leading edge of the signal that terminates the write.

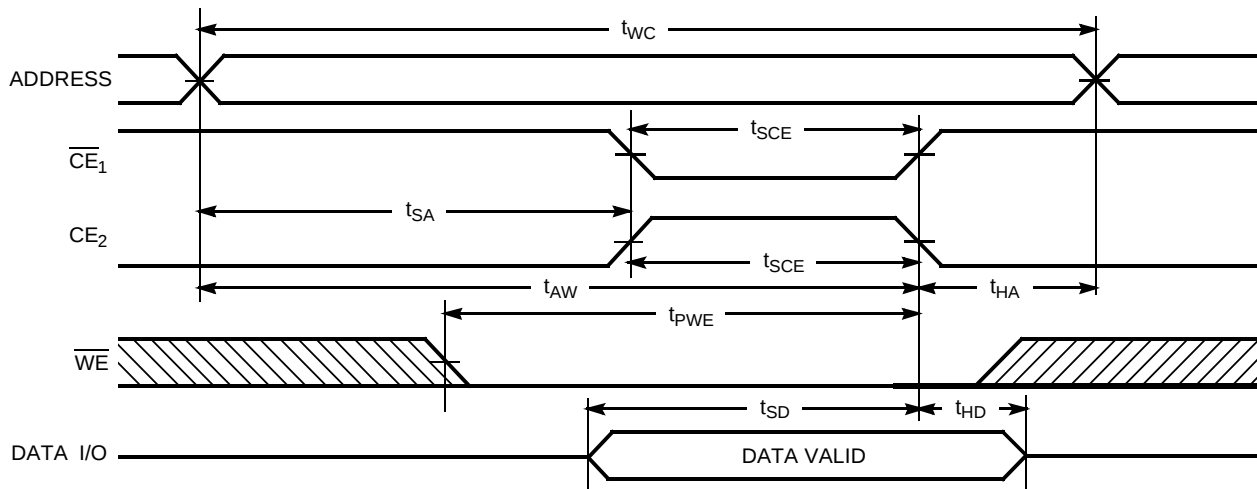
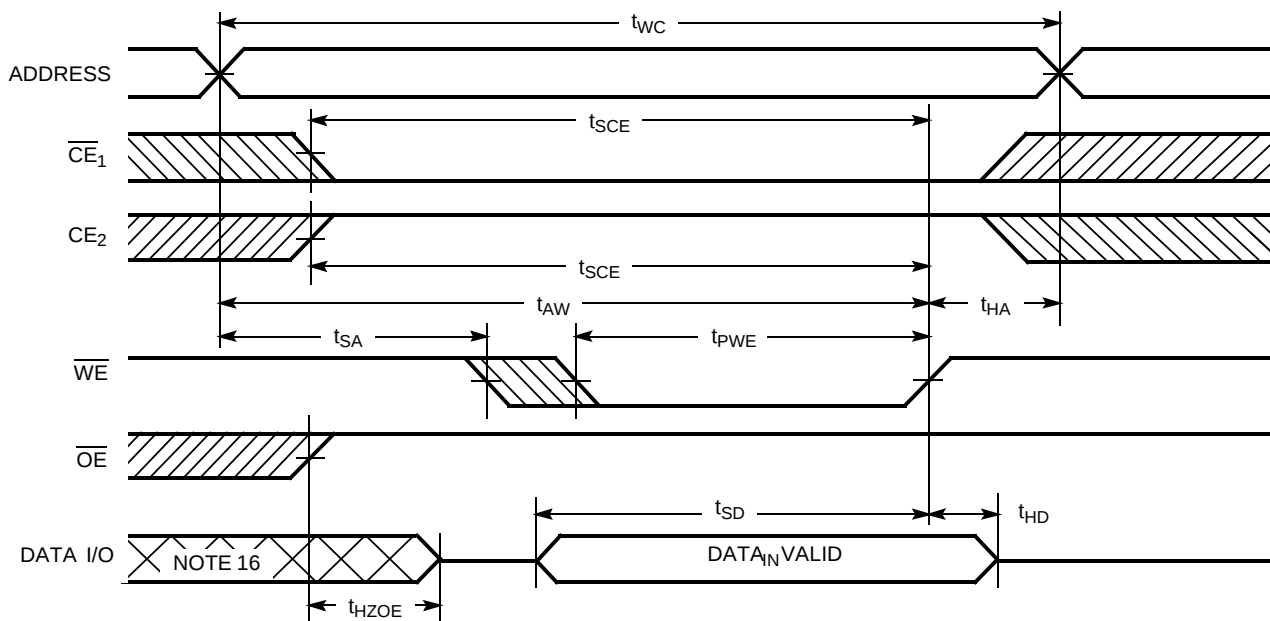


Parameter	Description			Conditions ^[10]	Min.	Typ.	Max.	Unit
V _{DR}	V _{CC} for Data Retention				2.0			V
I _{CCDR}	Data Retention Current	Ind.'I	LL	V _{CC} = V _{DR} = 3.0V, CE ≥ V _{CC} − 0.3V, V _{IN} ≥ V _{CC} − 0.3V or, V _{IN} ≤ 0.3V		1.5	15	μA
I _{CCDR}	Data Retention Current	Com.	LL	V _{CC} = V _{DR} = 3.0V, CE ≥ V _{CC} − 0.3V, V _{IN} ≥ V _{CC} − 0.3V or, V _{IN} ≤ 0.3V		1.5	15	μA
t _{CDR} ^[3]	Chip Deselect to Data Retention Time				0			ns
t _R ^[3]	Operation Recovery Time				70			ns

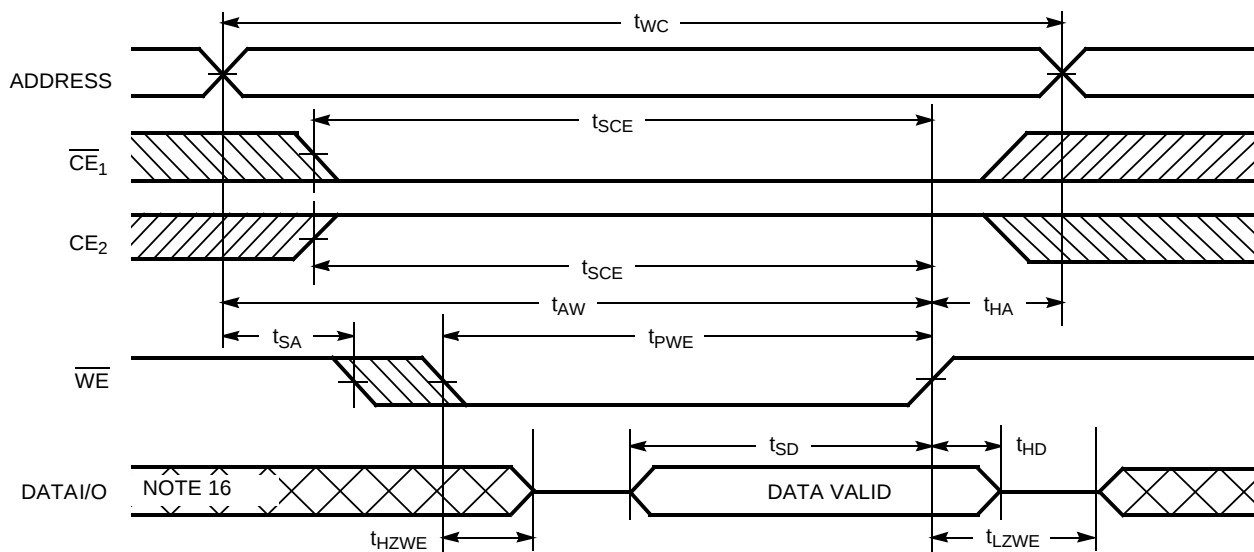
Read Cycle No.1^[11, 12]



10. No input may exceed $V_{CC} + 0.5V_{CC}$.
11. Device is continuously selected. OE, $\overline{CE}_1 = V_{IL}$, $CE_2 = V_{IH}$.
12. WE is HIGH for read cycle.
13. Address valid prior to or coincident with $\overline{CE}_1$ transition LOW and CE_2 transition HIGH.

Switching Waveforms (continued)
Write Cycle No. 1 ($\overline{CE}_1$ or CE_2 Controlled)^[14, 15]

Write Cycle No. 2 ($\overline{WE}$ Controlled, $\overline{OE}$ HIGH During Write)^[14, 15]

Notes:

14. Data I/O is high impedance if $\overline{OE} = V_{IH}$.
15. If $\overline{CE}_1$ goes HIGH or CE_2 goes LOW simultaneously with $\overline{WE}$ going HIGH, the output remains in a high-impedance state.
16. During this period the I/Os are in the output state and input signals should not be applied.

Switching Waveforms (continued)
Write Cycle No.3 ($\overline{\text{WE}}$ Controlled, $\overline{\text{OE}}$ LOW)^[14, 15]

Truth Table

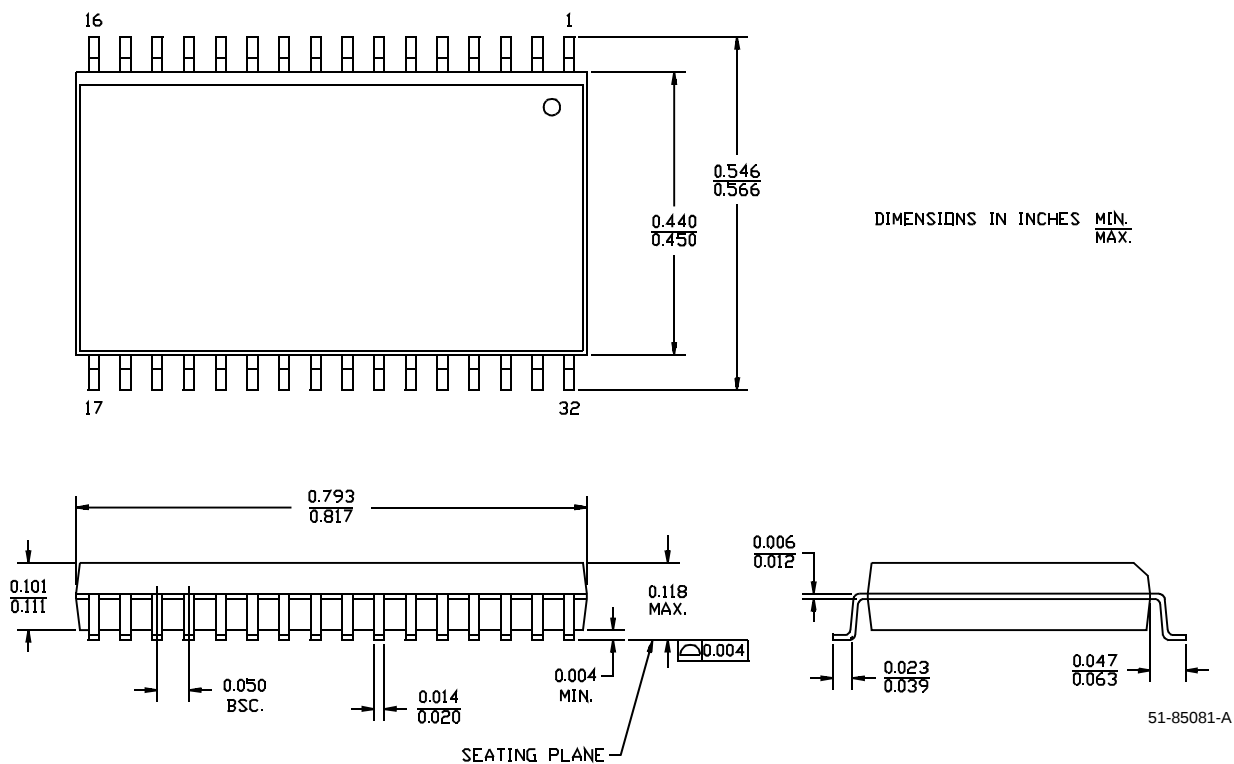
$\overline{\text{CE}}_1$	CE_2	$\overline{\text{OE}}$	$\overline{\text{WE}}$	I/O ₀ –I/O ₇	Mode	Power
H	X	X	X	High Z	Power-Down	Standby (I_{SB})
X	L	X	X	High Z	Power-Down	Standby (I_{SB})
L	H	L	H	Data Out	Read	Active (I_{CC})
L	H	X	L	Data In	Write	Active (I_{CC})
L	H	H	H	High Z	Selected, Outputs Disabled	Active (I_{CC})

Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
55	CY62128BLL-55SI	S34	32-Lead 450-Mil SOIC	Industrial
	CY62128BLL-55SC	S34	32-Lead 450-Mil SOIC	Commercial
	CY62128BLL-55ZI	Z32	32-Lead TSOP Type I	Industrial
	CY62128BLL-55ZC	Z32	32-Lead TSOP Type I	Commercial
	CY62128BLL-55ZAI	ZA32	32-Lead STSOP Type I	Industrial
	CY62128BLL-55ZAC	ZA32	32-Lead STSOP Type I	Commercial
	CY62128BLL-70ZRI	ZR32	32-Lead Reverse TSOP Type I	Industrial
	CY62128BLL-70ZRC	ZR32	32-Lead Reverse TSOP Type I	Commercial
70	CY62128BLL-70SI	S34	32-Lead 450-Mil SOIC I	Industrial
	CY62128BLL-70SC	S34	32-Lead 450-Mil SOIC I	Commercial
	CY62128BLL-70ZI	Z32	32-Lead TSOP Type I	Industrial
	CY62128BLL-70ZC	Z32	32-Lead TSOP Type I	Commercial
	CY62128BLL-70ZAI	ZA32	32-Lead STSOP Type I	Industrial
	CY62128BLL-70ZAC	ZA32	32-Lead STSOP Type I	Commercial
	CY62128BLL-70ZRI	ZR32	32-Lead Reverse TSOP Type I	Industrial
	CY62128BLL-70ZRC	ZR32	32-Lead Reverse TSOP Type I	Commercial

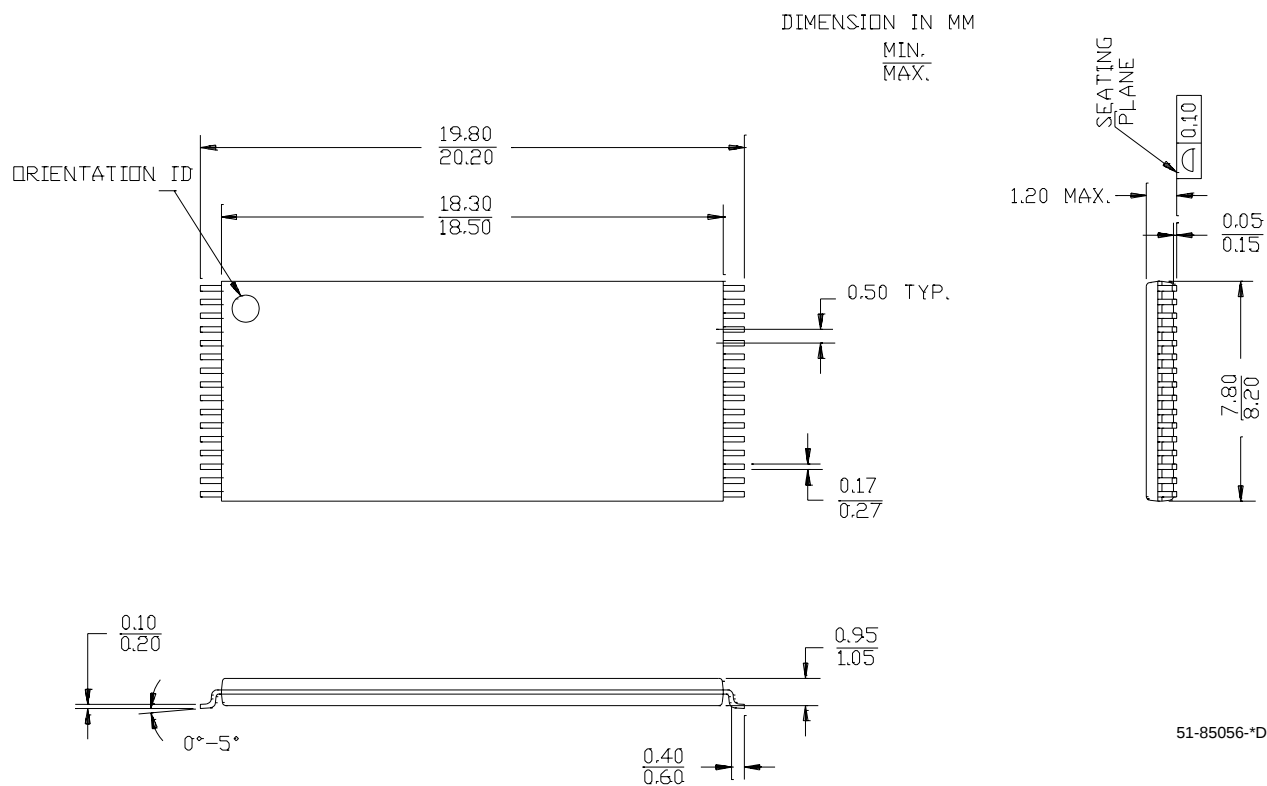
Package Diagrams

32-Lead (450 Mil) Molded SOIC S34



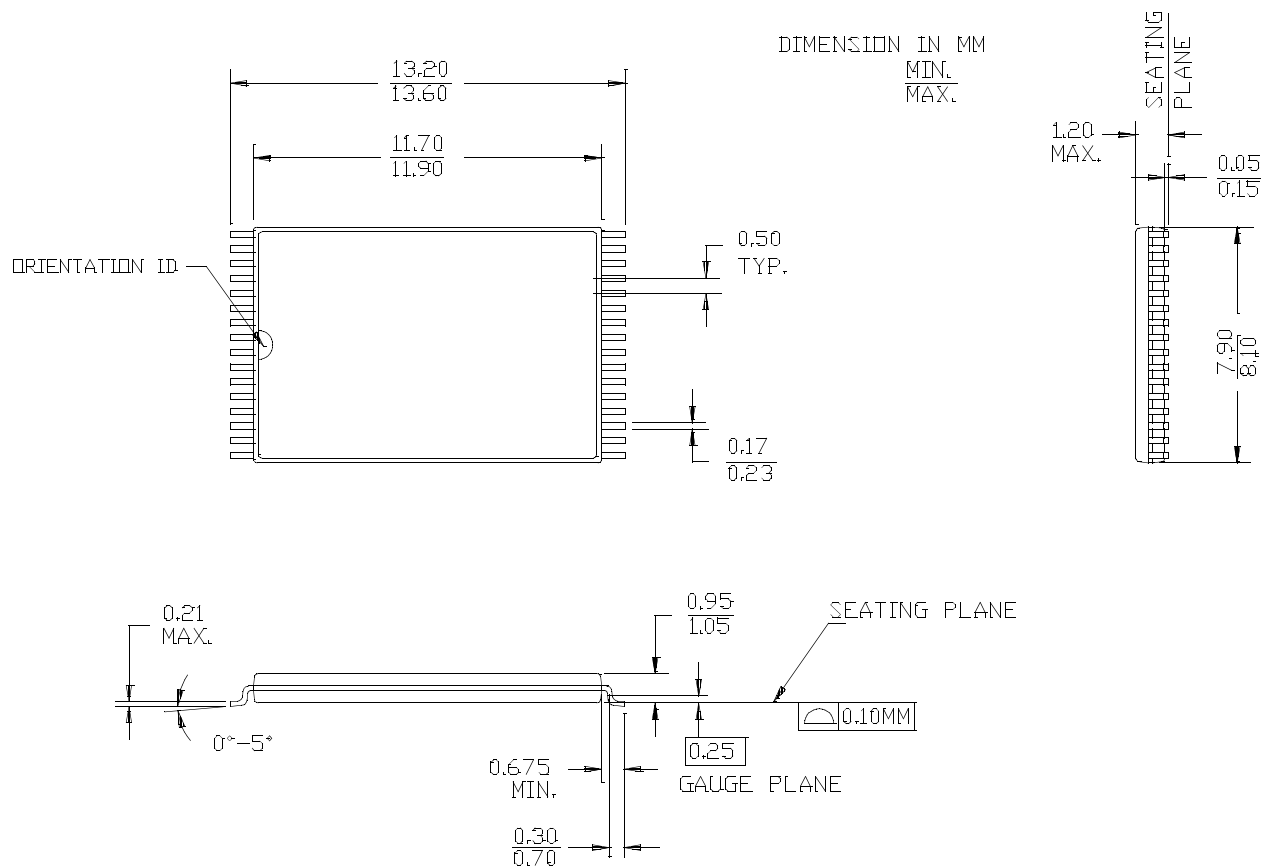
Package Diagrams (continued)

32-Lead Thin Small Outline Package Type I (8x20 mm) Z32



Package Diagrams (continued)

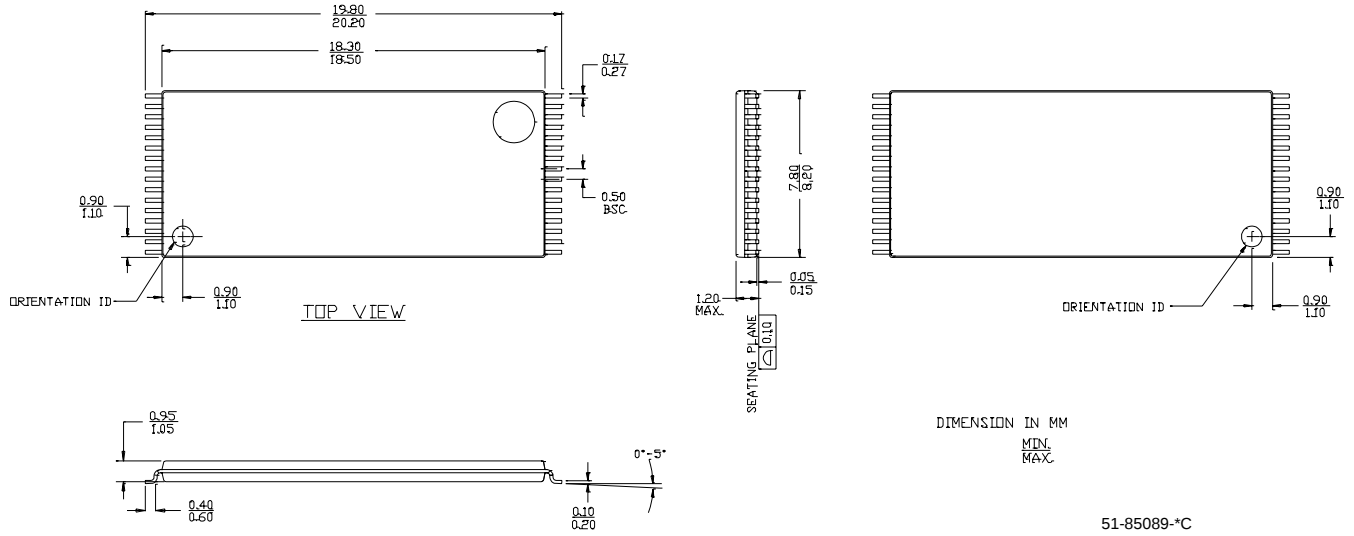
32-Lead Shrink Thin Small Outline Package (8x13.4 mm) ZA32



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Package Diagrams (continued)

32-Lead Reverse Thin Small Outline Package ZR32





Document Title: CY62128B MoBL[®] 128K x 8 Static RAM Document Number: 38-05300				
REV.	ECN NO.	Issue Date	Orig. of Change	Description of Change
**	116566	06/20/02	DSG	Change from Spec number: 38-00524 to 38-05300