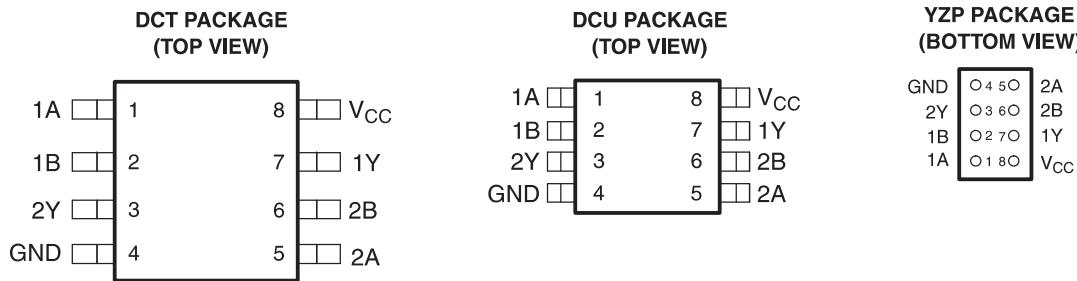


## FEATURES

- Available in the Texas Instruments NanoFree™ Package
- Optimized for 1.8-V Operation and Is 3.6-V I/O Tolerant to Support Mixed-Mode Signal Operation
- $I_{off}$  Supports Partial Power-Down-Mode Operation
- Sub-1-V Operable
- Max  $t_{pd}$  of 1.8 ns at 1.8 V
- Low Power Consumption, 10  $\mu$ A at 1.8 V
- $\pm 8$ -mA Output Drive at 1.8 V
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)



See mechanical drawings for dimensions.

## DESCRIPTION/ORDERING INFORMATION

This dual 2-input positive-NOR gate is operational at 0.8-V to 2.7-V  $V_{CC}$ , but is designed specifically for 1.65-V to 1.95-V  $V_{CC}$  operation.

The SN74AUC2G02 performs the Boolean function  $Y = \overline{A} + \overline{B}$  or  $Y = \overline{A} \bullet \overline{B}$  in positive logic.

NanoFree™ package technology is a major breakthrough in IC packaging concepts, using the die as the package.

This device is fully specified for partial-power-down applications using  $I_{off}$ . The  $I_{off}$  circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

## ORDERING INFORMATION

$T_A$	PACKAGE <sup>(1)</sup>	ORDERABLE PART NUMBER	TOP-SIDE MARKING <sup>(2)</sup>
−40°C to 85°C	NanoFree™ – W CSP (DSBGA) 0.23-mm Large Bump – YZP (Pb-free)	Reel of 3000	SN74AUC2G02YZPR _ _ _ UB _
	SSOP – DCT	Reel of 3000	SN74AUC2G02DCTR U02_
	VSSOP – DCU	Reel of 3000	SN74AUC2G02DCUR U02_

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).

(2) DCT: The actual top-side marking has three additional characters that designate the year, month, and assembly/test site.  
 DCU: The actual top-side marking has one additional character that designates the assembly/test site.  
 YZP: The actual top-side marking has three preceding characters to denote year, month, and sequence code, and one following character to designate the assembly/test site.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

NanoFree is a trademark of Texas Instruments.

**SN74AUC2G02**  
**DUAL 2-INPUT POSITIVE-NOR GATE**

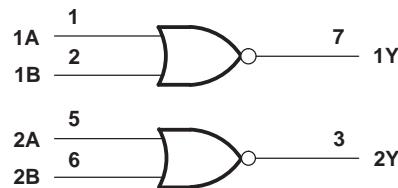
SCES441C—MAY 2003—REVISED JANUARY 2007

 **TEXAS  
INSTRUMENTS**  
[www.ti.com](http://www.ti.com)

**FUNCTION TABLE  
(each gate)**

INPUTS		OUTPUT
A	B	Y
H	X	L
X	H	L
L	L	H

**LOGIC DIAGRAM (POSITIVE LOGIC)**



**Absolute Maximum Ratings<sup>(1)</sup>**

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
$V_{CC}$	Supply voltage range	-0.5	3.6	V
$V_I$	Input voltage range <sup>(2)</sup>	-0.5	3.6	V
$V_O$	Voltage range applied to any output in the high-impedance or power-off state <sup>(2)</sup>	-0.5	3.6	V
$V_O$	Output voltage range <sup>(2)</sup>	-0.5	$V_{CC} + 0.5$	V
$I_{IK}$	Input clamp current	$V_I < 0$	-50	mA
$I_{OK}$	Output clamp current	$V_O < 0$	-50	mA
$I_O$	Continuous output current		$\pm 20$	mA
	Continuous current through $V_{CC}$ or GND		$\pm 100$	mA
$\theta_{JA}$	Package thermal impedance <sup>(3)</sup>	DCT package	220	°C/W
		DCU package	227	
		YZP package	102	
$T_{stg}$	Storage temperature range	-65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.

(3) The package thermal impedance is calculated in accordance with JESD 51-7.

**Recommended Operating Conditions<sup>(1)</sup>**

			MIN	MAX	UNIT
$V_{CC}$	Supply voltage		0.8	2.7	V
$V_{IH}$	High-level input voltage	$V_{CC} = 0.8\text{ V}$	$V_{CC}$		V
		$V_{CC} = 1.1\text{ V to }1.95\text{ V}$	$0.65 \times V_{CC}$		
		$V_{CC} = 2.3\text{ V to }2.7\text{ V}$	1.7		
$V_{IL}$	Low-level input voltage	$V_{CC} = 0.8\text{ V}$	0		V
		$V_{CC} = 1.1\text{ V to }1.95\text{ V}$	$0.35 \times V_{CC}$		
		$V_{CC} = 2.3\text{ V to }2.7\text{ V}$	0.7		
$V_I$	Input voltage		0	3.6	V
$V_O$	Output voltage		0	$V_{CC}$	V
$I_{OH}$	High-level output current	$V_{CC} = 0.8\text{ V}$		-0.7	mA
		$V_{CC} = 1.1\text{ V}$		-3	
		$V_{CC} = 1.4\text{ V}$		-5	
		$V_{CC} = 1.65\text{ V}$		-8	
		$V_{CC} = 2.3\text{ V}$		-9	
$I_{OL}$	Low-level output current	$V_{CC} = 0.8\text{ V}$		0.7	mA
		$V_{CC} = 1.1\text{ V}$		3	
		$V_{CC} = 1.4\text{ V}$		5	
		$V_{CC} = 1.65\text{ V}$		8	
		$V_{CC} = 2.3\text{ V}$		9	
$\Delta t/\Delta v$	Input transition rise or fall rate			20	ns/V
$T_A$	Operating free-air temperature			-40	85 °C

(1) All unused inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

**Electrical Characteristics**

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	$V_{CC}$	MIN	TYP <sup>(1)</sup>	MAX	UNIT
$V_{OH}$	$I_{OH} = -100\text{ }\mu\text{A}$	0.8 V to 2.7 V	$V_{CC} - 0.1$			V
	$I_{OH} = -0.7\text{ mA}$	0.8 V		0.55		
	$I_{OH} = -3\text{ mA}$	1.1 V		0.8		
	$I_{OH} = -5\text{ mA}$	1.4 V		1		
	$I_{OH} = -8\text{ mA}$	1.65 V		1.2		
	$I_{OH} = -9\text{ mA}$	2.3 V		1.8		
$V_{OL}$	$I_{OL} = 100\text{ }\mu\text{A}$	0.8 V to 2.7 V		0.2		V
	$I_{OL} = 0.7\text{ mA}$	0.8 V		0.25		
	$I_{OL} = 3\text{ mA}$	1.1 V		0.3		
	$I_{OL} = 5\text{ mA}$	1.4 V		0.4		
	$I_{OL} = 8\text{ mA}$	1.65 V		0.45		
	$I_{OL} = 9\text{ mA}$	2.3 V		0.6		
$I_I$	A or B inputs	$V_I = V_{CC}$ or GND	0 to 2.7 V		$\pm 5$	$\mu\text{A}$
$I_{off}$		$V_I$ or $V_O = 2.7\text{ V}$	0		$\pm 10$	$\mu\text{A}$
$I_{CC}$		$V_I = V_{CC}$ or GND, $I_O = 0$	0.8 V to 2.7 V		10	$\mu\text{A}$
$C_i$		$V_I = V_{CC}$ or GND	2.5 V		2.5	pF

(1) All typical values are at  $T_A = 25^\circ\text{C}$ .

# SN74AUC2G02

## DUAL 2-INPUT POSITIVE-NOR GATE

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### Switching Characteristics

over recommended operating free-air temperature range,  $C_L = 15 \text{ pF}$  (unless otherwise noted) (see [Figure 1](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 0.8 \text{ V}$	$V_{CC} = 1.2 \text{ V} \pm 0.1 \text{ V}$		$V_{CC} = 1.5 \text{ V} \pm 0.1 \text{ V}$		$V_{CC} = 1.8 \text{ V} \pm 0.15 \text{ V}$		$V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$		UNIT	
			TYP	MIN	MAX	MIN	MAX	MIN	TYP	MAX	MIN	MAX	
$t_{pd}$	A or B	Y	8	0.8	3.5	0.6	2.2	0.5	1	1.8	0.5	1.3	ns

### Switching Characteristics

over recommended operating free-air temperature range,  $C_L = 30 \text{ pF}$  (unless otherwise noted) (see [Figure 1](#))

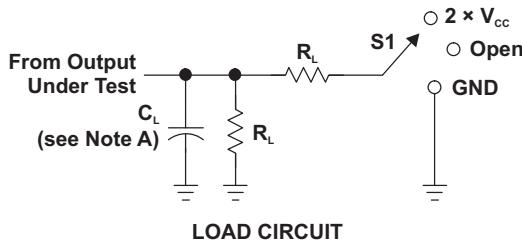
PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 1.8 \text{ V} \pm 0.15 \text{ V}$			$V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
$t_{pd}$	A or B	Y	1	1.6	2.4	0.8	1.9	ns	

### Operating Characteristics

$T_A = 25^\circ\text{C}$

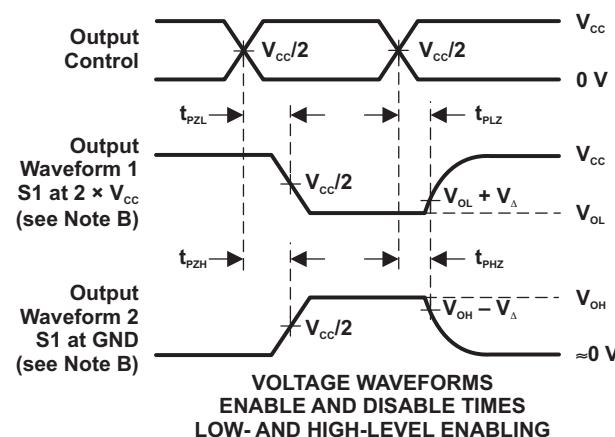
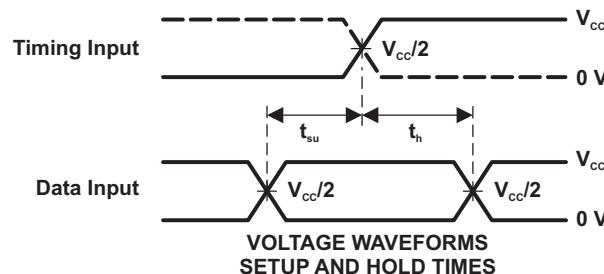
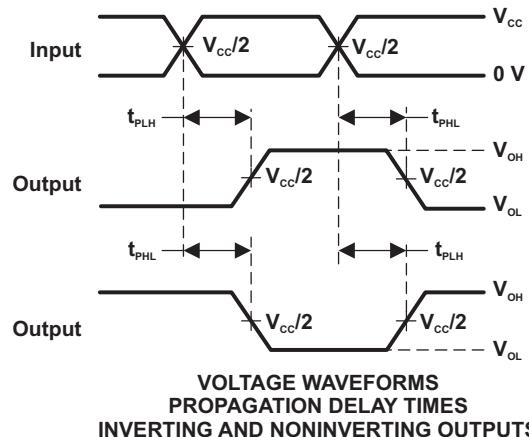
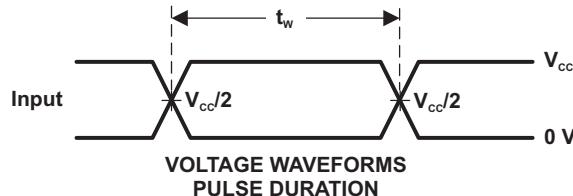
PARAMETER	TEST CONDITIONS	$V_{CC} = 0.8 \text{ V}$	$V_{CC} = 1.2 \text{ V}$	$V_{CC} = 1.5 \text{ V}$	$V_{CC} = 1.8 \text{ V}$	$V_{CC} = 2.5 \text{ V}$	UNIT
		TYP	TYP	TYP	TYP	TYP	
$C_{pd}$	Power dissipation capacitance	f = 10 MHz	13	13	14	14	14 pF

PARAMETER MEASUREMENT INFORMATION



TEST	S1
$t_{PLH}/t_{PHL}$	Open
$t_{PLZ}/t_{PZL}$	$2 \times V_{CC}$
$t_{PHZ}/t_{PZH}$	GND

$V_{CC}$	$C_L$	$R_L$	$V_{\Delta}$
0.8 V	15 pF	2 k $\Omega$	0.1 V
1.2 V $\pm$ 0.1 V	15 pF	2 k $\Omega$	0.1 V
1.5 V $\pm$ 0.1 V	15 pF	2 k $\Omega$	0.1 V
1.8 V $\pm$ 0.15 V	15 pF	2 k $\Omega$	0.15 V
2.5 V $\pm$ 0.2 V	15 pF	2 k $\Omega$	0.15 V
1.8 V $\pm$ 0.15 V	30 pF	1 k $\Omega$	0.15 V
2.5 V $\pm$ 0.2 V	30 pF	500 $\Omega$	0.15 V



- NOTES:
- A.  $C_L$  includes probe and jig capacitance.
  - B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
  - C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz,  $Z_o = 50 \Omega$ , slew rate  $\geq 1$  V/ns.
  - D. The outputs are measured one at a time, with one transition per measurement.
  - E.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
  - F.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
  - G.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .

Figure 1. Load Circuit and Voltage Waveforms

**PACKAGING INFORMATION**

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74AUC2G02DCTR	Active	Production	SSOP (DCT)   8	3000   LARGE T&R	Yes	NIPDAU   SN	Level-1-260C-UNLIM	-40 to 85	(2X65, U02) (R, Z)
SN74AUC2G02DCTR.B	Active	Production	SSOP (DCT)   8	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	(2X65, U02) (R, Z)
SN74AUC2G02DCUR	Active	Production	VSSOP (DCU)   8	3000   LARGE T&R	Yes	NIPDAU   SN	Level-1-260C-UNLIM	-40 to 85	(U02Q, U02R) UR
SN74AUC2G02DCUR.B	Active	Production	VSSOP (DCU)   8	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	(U02Q, U02R) UR
SN74AUC2G02YZPR	Active	Production	DSBGA (YZP)   8	3000   LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	UBN
SN74AUC2G02YZPR.B	Active	Production	DSBGA (YZP)   8	3000   LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	UBN

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

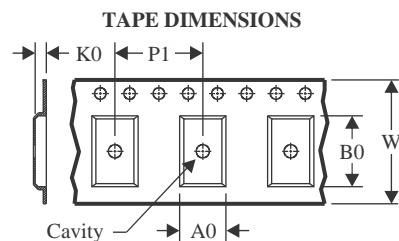
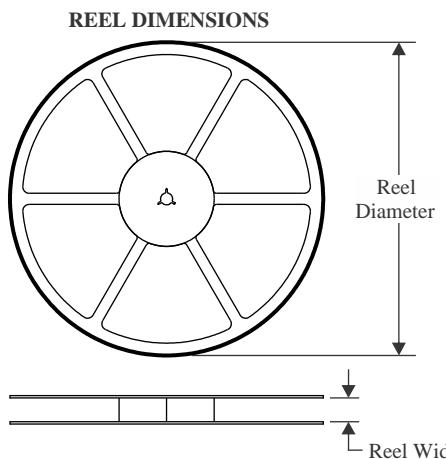
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative

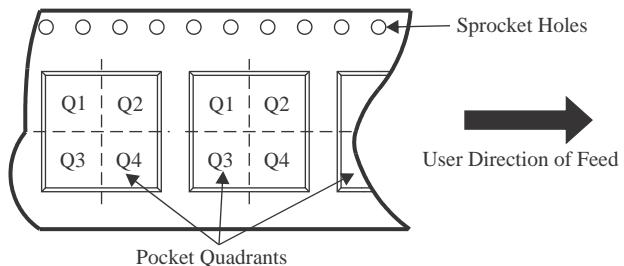
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and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

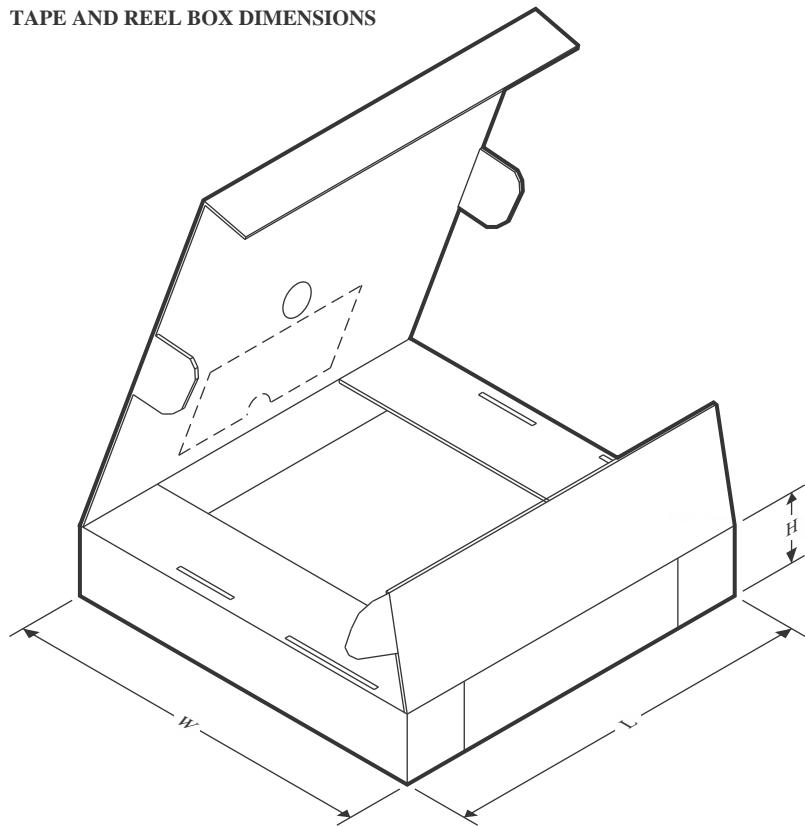
**TAPE AND REEL INFORMATION**


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AUC2G02DCTR	SSOP	DCT	8	3000	180.0	13.0	3.35	4.5	1.55	4.0	12.0	Q3
SN74AUC2G02DCUR	VSSOP	DCU	8	3000	180.0	8.4	2.25	3.35	1.05	4.0	8.0	Q3
SN74AUC2G02DCUR	VSSOP	DCU	8	3000	178.0	9.5	2.25	3.35	1.05	4.0	8.0	Q3
SN74AUC2G02YZPR	DSBGA	YZP	8	3000	178.0	9.2	1.02	2.02	0.63	4.0	8.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AUC2G02DCTR	SSOP	DCT	8	3000	182.0	182.0	20.0
SN74AUC2G02DCUR	VSSOP	DCU	8	3000	202.0	201.0	28.0
SN74AUC2G02DCUR	VSSOP	DCU	8	3000	202.0	201.0	28.0
SN74AUC2G02YZPR	DSBGA	YZP	8	3000	220.0	220.0	35.0

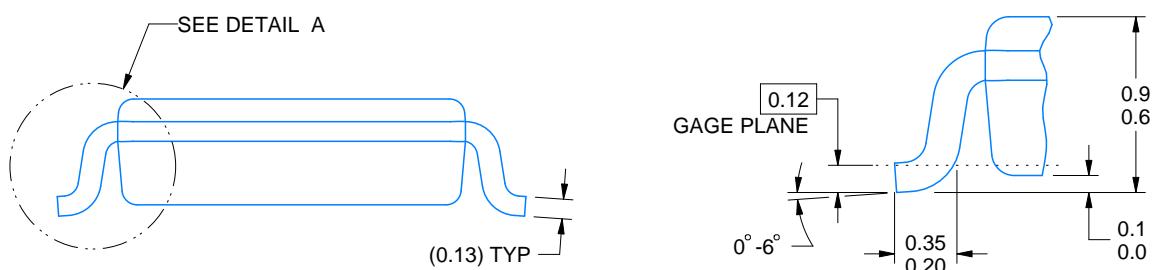
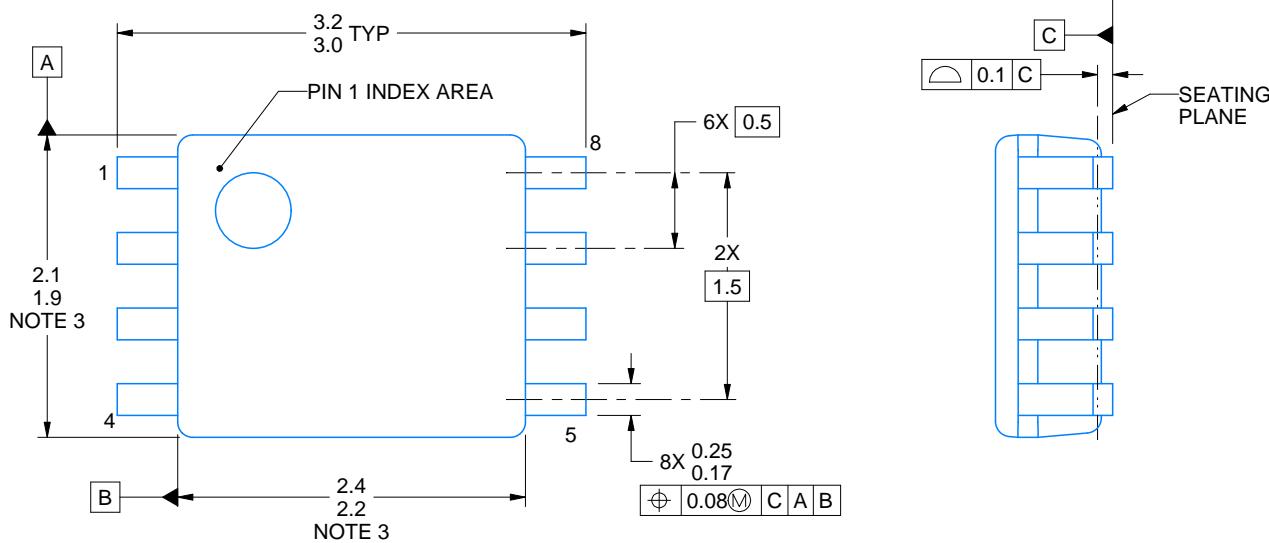
## PACKAGE OUTLINE

**DCU0008A**



## **VSSOP - 0.9 mm max height**

## SMALL OUTLINE PACKAGE



## DETAIL A TYPICAL

## NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
  2. This drawing is subject to change without notice.
  3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
  4. Reference JEDEC registration MO-187 variation CA.

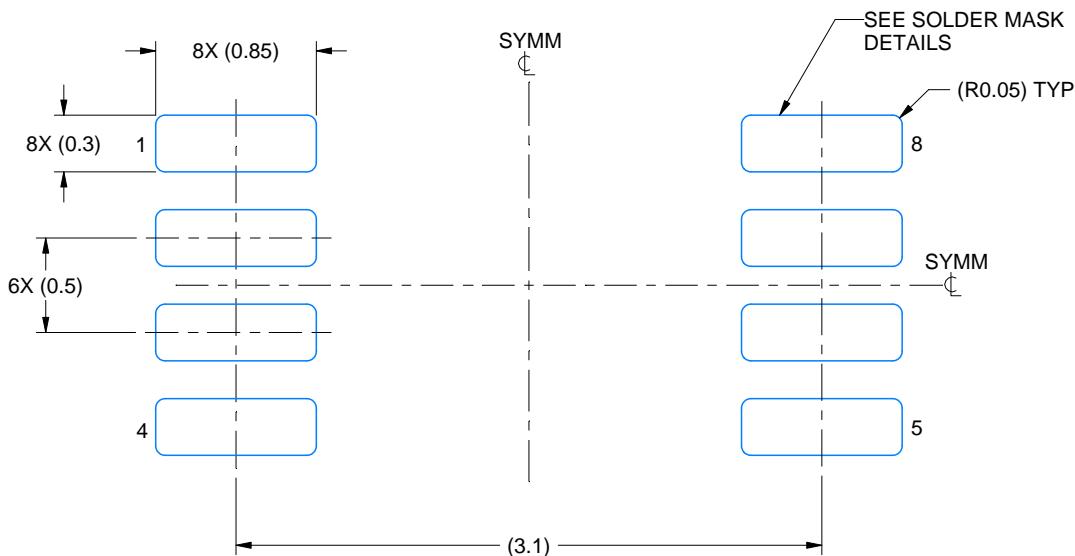
4225266/A 09/2014

# EXAMPLE BOARD LAYOUT

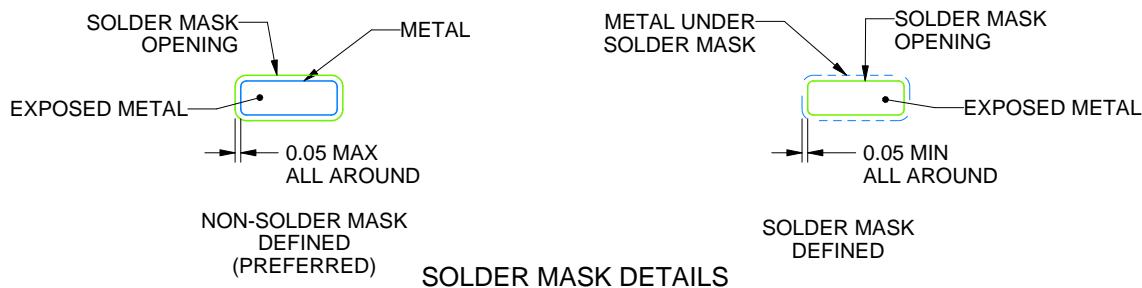
DCU0008A

VSSOP - 0.9 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 25X



4225266/A 09/2014

NOTES: (continued)

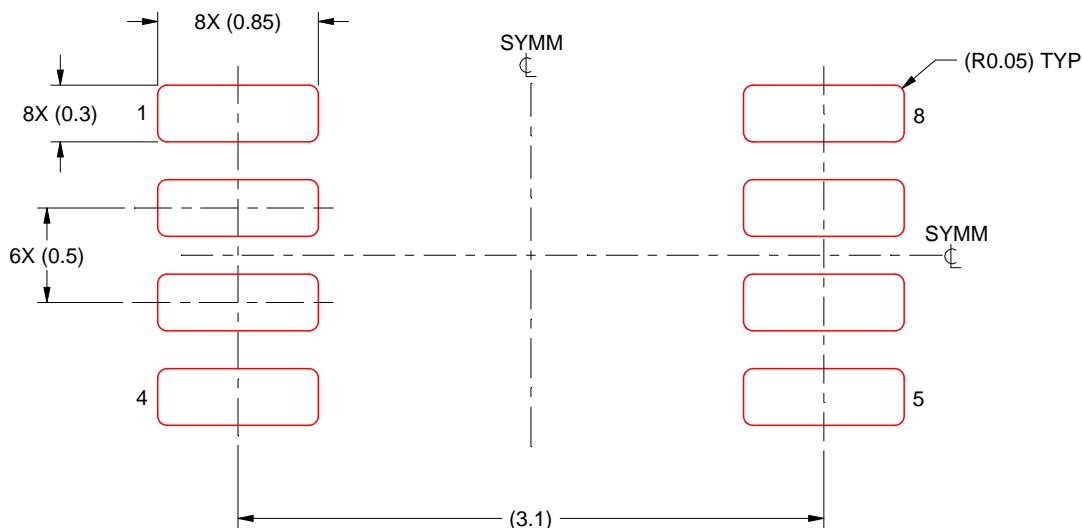
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DCU0008A

VSSOP - 0.9 mm max height

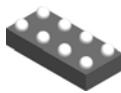
SMALL OUTLINE PACKAGE



4225266/A 09/2014

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

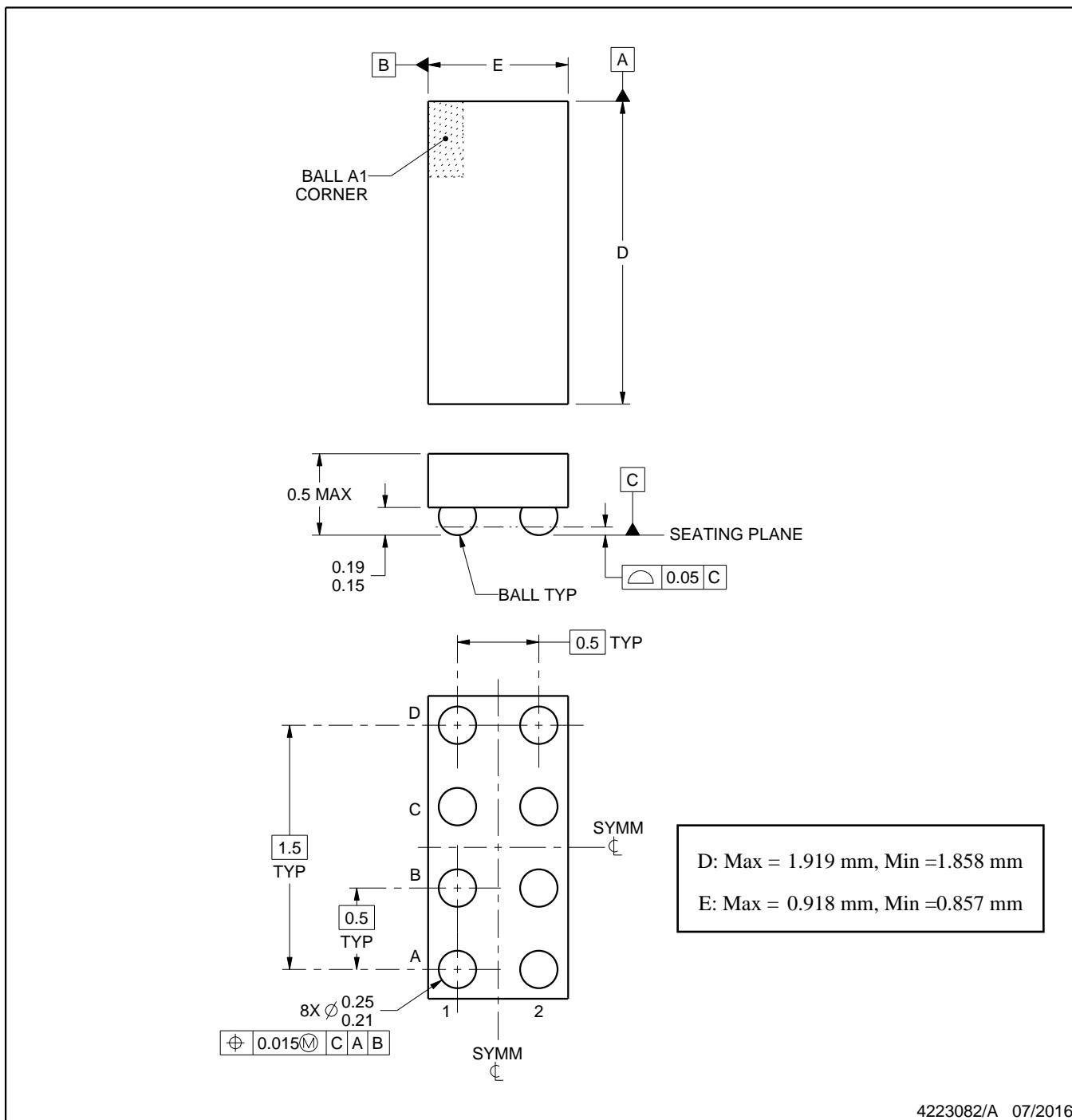


# PACKAGE OUTLINE

YZP0008

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



## NOTES:

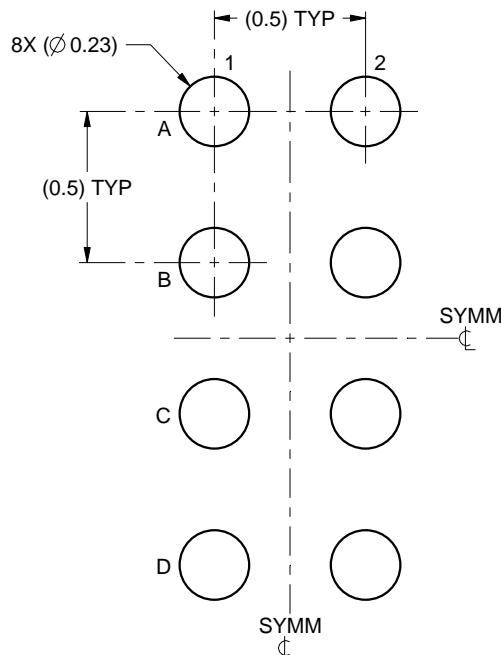
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

# EXAMPLE BOARD LAYOUT

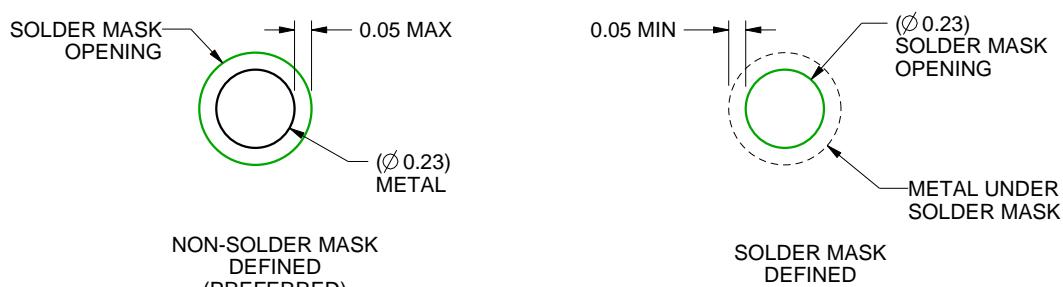
YZP0008

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



LAND PATTERN EXAMPLE  
SCALE:40X



SOLDER MASK DETAILS  
NOT TO SCALE

4223082/A 07/2016

NOTES: (continued)

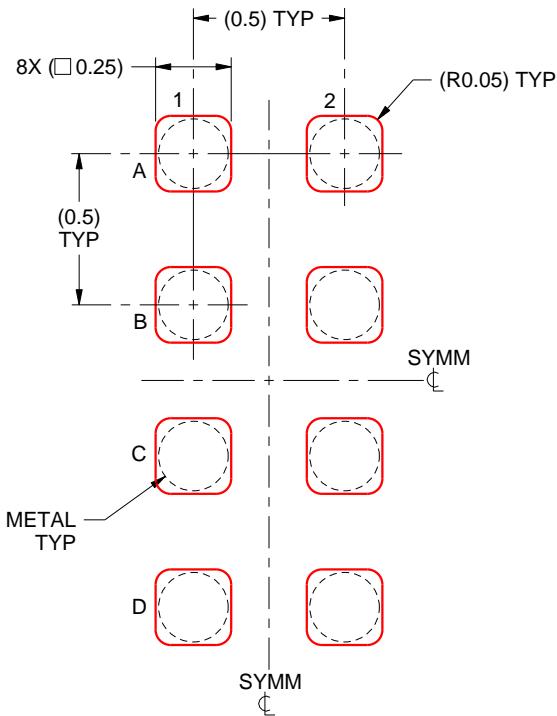
3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SNVA009 ([www.ti.com/lit/snva009](http://www.ti.com/lit/snva009)).

# EXAMPLE STENCIL DESIGN

YZP0008

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



SOLDER PASTE EXAMPLE  
BASED ON 0.1 mm THICK STENCIL  
SCALE:40X

4223082/A 07/2016

NOTES: (continued)

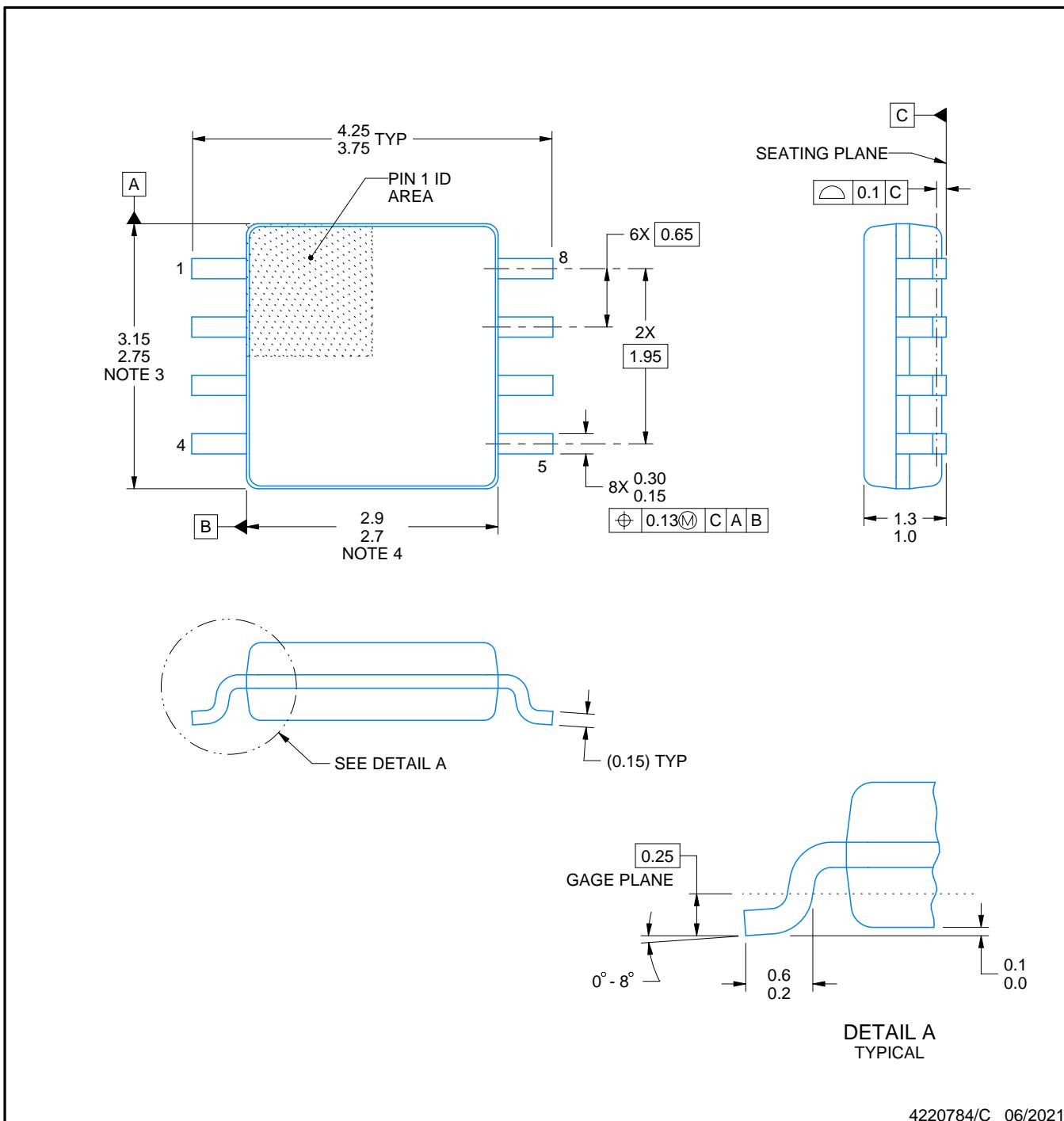
4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.



# PACKAGE OUTLINE

## SSOP - 1.3 mm max height

SMALL OUTLINE PACKAGE



### NOTES:

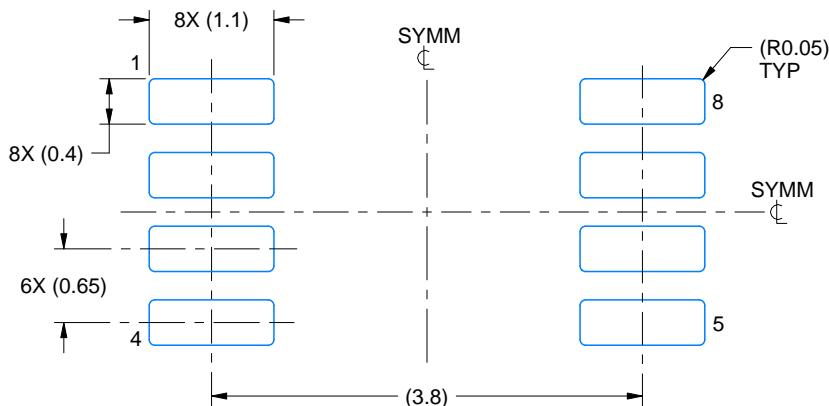
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.

# EXAMPLE BOARD LAYOUT

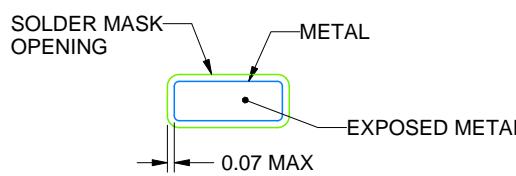
DCT0008A

SSOP - 1.3 mm max height

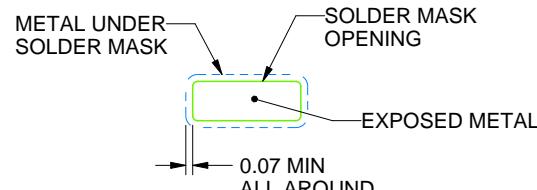
SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:15X



NON SOLDER MASK  
DEFINED



SOLDER MASK  
DEFINED

SOLDER MASK DETAILS

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NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.

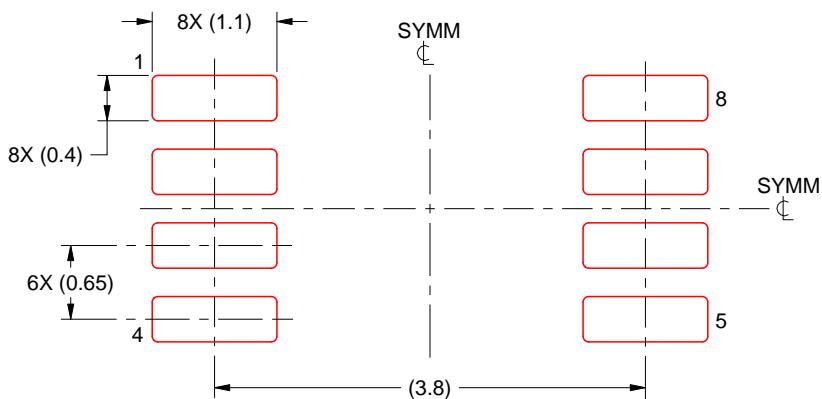
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DCT0008A

SSOP - 1.3 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:15X

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NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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