

LMV321-Q1 SINGLE, LMV358-Q1 DUAL, LMV324-Q1 QUAD LOW-VOLTAGE RAIL-TO-RAIL OUTPUT OPERATIONAL AMPLIFIERS

SLOS415E – JUNE 2003 – REVISED APRIL 2008

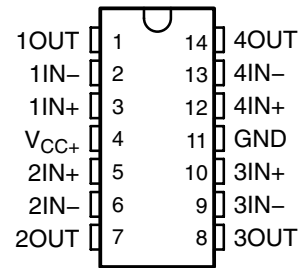
- **Qualified for Automotive Applications**
- **2.7-V and 5-V Performance**
- **No Crossover Distortion**
- **Low Supply Current:**
 - LMV321 . . . 130 μ A Typ
 - LMV358 . . . 210 μ A Typ
 - LMV324 . . . 410 μ A Typ
- **Rail-to-Rail Output Swing**

description/ordering information

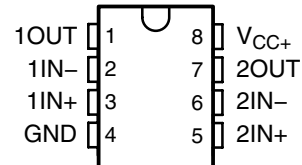
The LMV321, LMV358, and LMV324 are single, dual, and quad low-voltage (2.7 V to 5.5 V) operational amplifiers with rail-to-rail output swing.

The LMV321, LMV358, and LMV324 are the most cost-effective solution for applications where low-voltage operation, space saving, and low price are required. These amplifiers were designed specifically for low-voltage (2.7 V to 5 V) operation, with performance specifications meeting or exceeding the LM358 and LM324 devices that operate from 5 V to 30 V. Additional features of the LMV3xx devices are a common-mode input voltage range that includes ground, 1-MHz unity-gain bandwidth, and 1-V/ μ s slew rate.

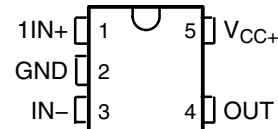
**LMV324 . . . D OR PW PACKAGE
(TOP VIEW)**



**LMV358 . . . D OR PW PACKAGE
(TOP VIEW)**



**LMV321 . . . DBV PACKAGE
(TOP VIEW)**



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



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SLOS415E – JUNE 2003 – REVISED APRIL 2008

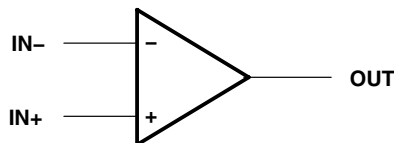
ORDERING INFORMATION[†]

T _A		PACKAGE [‡]		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	Single	SOT23-5 (DBV)	Reel of 3000	LMV321IDBVRQ1	RC1B
–40°C to 85°C	Dual	SOIC (D)	Tube of 75	LMV358IDQ1	358IQ1
			Reel of 2500	LMV358IDRQ1	
		TSSOP (PW)	Reel of 2000	LMV358IPWRQ1	358IQ1
–40°C to 85°C	Quad	SOIC (D)	Tube of 50	LMV324IDQ1	LMV324IQ1
			Reel of 2500	LMV324IDRQ1	
		TSSOP (PW)	Reel of 2000	LMV324IPWRQ1	V324IQ1
–40°C to 125°C	Single	SOT23-5 (DBV)	Reel of 3000	LMV321QDBVRQ1	RCCB
–40°C to 125°C	Dual	SOIC (D)	Tube of 75	LMV358QDQ1	V358Q1
			Reel of 2500	LMV358QDRQ1	
		TSSOP (PW)	Reel of 2000	LMV358QPWRQ1	V358Q1
–40°C to 125°C	Quad	SOIC (D)	Tube of 50	LMV324QDQ1	LMV324Q1
			Reel of 2500	LMV324QDRQ1	
		TSSOP (PW)	Reel of 2000	LMV324QPWRQ1	MV324Q1

[†] For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at <http://www.ti.com>.

[‡] Package drawings, thermal data, and symbolization are available at <http://www.ti.com/packaging>.

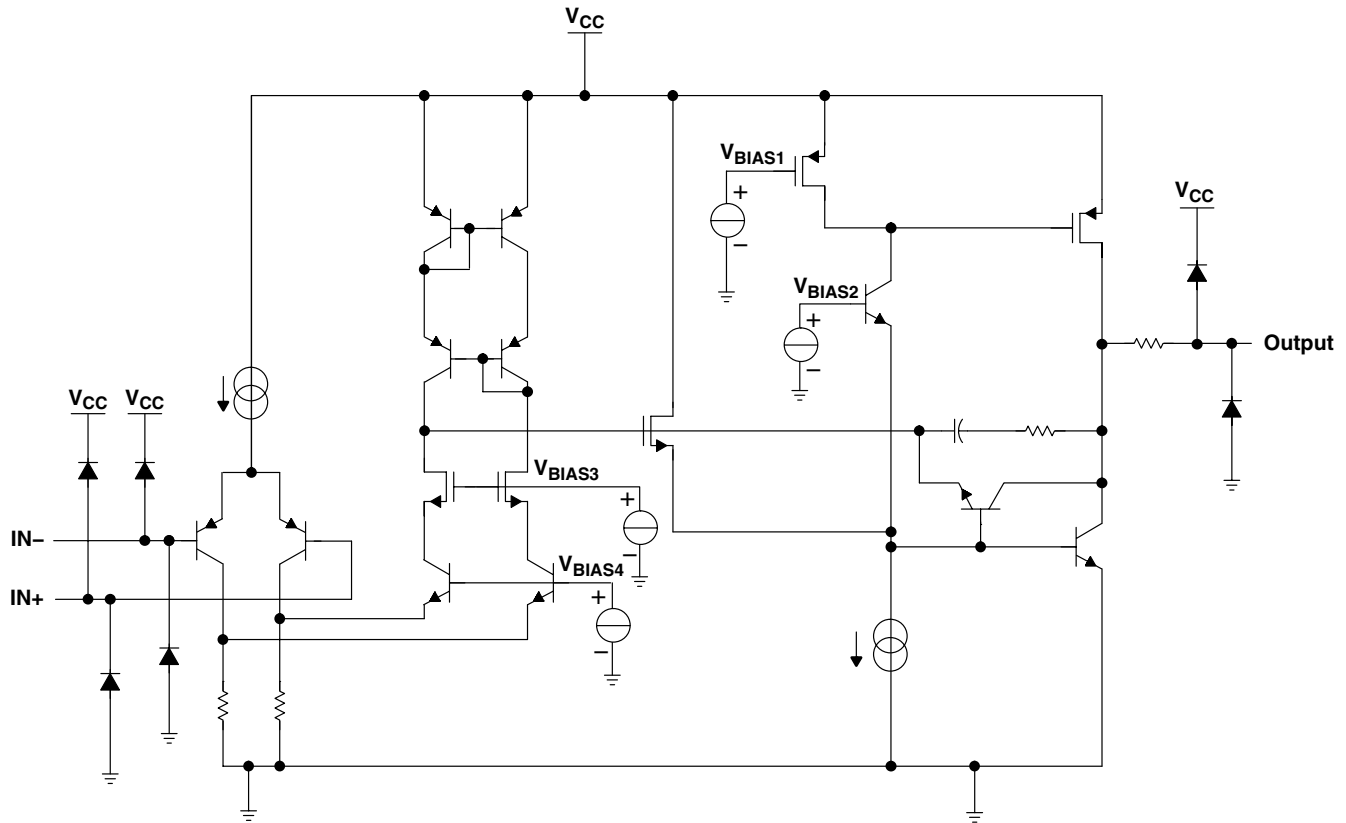
symbol (each amplifier)



LMV321-Q1 SINGLE, LMV358-Q1 DUAL, LMV324-Q1 QUAD LOW-VOLTAGE RAIL-TO-RAIL OUTPUT OPERATIONAL AMPLIFIERS

SLOS415E – JUNE 2003 – REVISED APRIL 2008

LMV324 simplified schematic



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage, V_{CC} (see Note 1)	5.5 V
Differential input voltage, V_{ID} (see Note 2)	± 5.5 V
Input voltage, V_I (either input)	0 to 5.5 V
Duration of output short circuit (one amplifier) to ground at (or below) $T_A = 25^\circ\text{C}$, $V_{CC} \leq 5.5$ V (see Note 3)	Unlimited
Package thermal impedance, θ_{JA} (see Notes 4 and 5):	
D (8-pin) package	97°C/W
D (14-pin) package	86°C/W
DBV (5-pin) package	206°C/W
PW (8-pin) package	149°C/W
PW (14-pin) package	113°C/W
Operating virtual junction temperature, T_J	150°C
Storage temperature range, T_{stg}	-65 to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES:
1. All voltage values (except differential voltages and V_{CC} specified for the measurement of I_{OQ}) are with respect to the network GND.
 2. Differential voltages are at IN+ with respect to IN-.
 3. Short circuits from outputs to V_{CC} can cause excessive heating and eventual destruction.
 4. Maximum power dissipation is a function of $T_J(\text{max})$, θ_{JA} , and T_A . The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(\text{max}) - T_A)/\theta_{JA}$. Selecting the maximum of 150°C can affect reliability.
 5. The package thermal impedance is calculated in accordance with JESD 51-7.



LMV321-Q1 SINGLE, LMV358-Q1 DUAL, LMV324-Q1 QUAD LOW-VOLTAGE RAIL-TO-RAIL OUTPUT OPERATIONAL AMPLIFIERS

SLOS415E – JUNE 2003 – REVISED APRIL 2008

recommended operating conditions (see Note 6)

		MIN	MAX	UNIT
V _{CC}	Supply voltage (single-supply operation)	2.7	5.5	V
V _{IH}	Amplifier turn-on voltage level	V _{CC} = 2.7 V	1.7	V
		V _{CC} = 5 V	3.5	
V _{IL}	Amplifier turn-off voltage level	V _{CC} = 2.7 V	0.7	V
		V _{CC} = 5 V	1.5	
T _A	Operating free-air temperature	I suffix	–40	°C
		Q suffix	–40	

NOTE 6: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics at T_A = 25°C, V_{CC+} = 2.7 V (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V _{IO}	Input offset voltage		1.7	7	mV
α _{V_{IO}}	Average temperature coefficient of input offset voltage		5		μV/°C
I _{IB}	Input bias current		11	250	nA
I _{IO}	Input offset current		5	50	nA
CMRR	Common-mode rejection ratio	V _{CM} = 0 to 1.7 V	50	63	dB
k _{SVR}	Supply-voltage rejection ratio	V _{CC} = 2.7 V to 5 V, V _O = 1 V	50	60	dB
V _{ICR}	Common-mode input voltage range	CMRR ≥ 50 dB	0 to 1.7	–0.2 to 1.9	V
Output swing	R _L = 10 kΩ to 1.35 V	High level	V _{CC} – 100	V _{CC} – 10	mV
		Low level	60	180	
I _{CC}	LMV321		80	170	μA
	LMV358 (both amplifiers)		140	340	
	LMV324 (all four amplifiers)		260	680	
B ₁	Unity-gain bandwidth	C _L = 200 pF	1		MHz
φ _m	Phase margin		60		deg
G _m	Gain margin		10		dB
V _n	Equivalent input noise voltage	f = 1 kHz	46		nV/√Hz
I _n	Equivalent input noise current	f = 1 kHz	0.17		pA/√Hz



LMV321-Q1 SINGLE, LMV358-Q1 DUAL, LMV324-Q1 QUAD LOW-VOLTAGE RAIL-TO-RAIL OUTPUT OPERATIONAL AMPLIFIERS

SLOS415E – JUNE 2003 – REVISED APRIL 2008

electrical characteristics at specified free-air temperature range, $V_{CC+} = 5\text{ V}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T _A [†]	MIN	TYP	MAX	UNIT	
V _{IO}	Input offset voltage			25°C	1.7			7	mV
				Full range	9				
α _{V_{IO}}	Average temperature coefficient of input offset voltage			25°C	5			μV/°C	
I _{IB}	Input bias current			25°C	15			250	nA
				Full range	500				
I _{IO}	Input offset current			25°C	5			50	nA
				Full range	150				
CMRR	Common-mode rejection ratio	V _{CM} = 0 to 4 V		25°C	50	65		dB	
k _{SVR}	Supply-voltage rejection ratio	V _{CC} = 2.7 V to 5 V, V _O = 1 V, V _{CM} = 1 V		25°C	50	60		dB	
V _{ICR}	Common-mode input voltage range	CMMR ≥ 50 dB		25°C	0 to 4 −0.2 to 4.2			V	
Output swing	R _L = 2 kΩ to 2.5 V	High level	25°C	V _{CC} − 300	V _{CC} − 40			mV	
			Full range	V _{CC} − 400					
		Low level	25°C	120			300		
			Full range	400					
	R _L = 10 kΩ to 2.5 V	High level	25°C	V _{CC} − 100	V _{CC} − 10				
			Full range	V _{CC} − 200					
		Low level	25°C	65			180		
			Full range	280					
A _{VD}	Large-signal differential voltage gain	R _L = 2 kΩ		25°C	15	100		V/mV	
				Full range	10				
I _{OS}	Output short-circuit current	Sourcing, V _O = 0 V		25°C	5	60		mA	
		Sinking, V _O = 5 V			10	160			
I _{CC}	Supply current	LMV321		25°C	130			250	μA
				Full range	350				
		LMV358 (both amplifiers)		25°C	210			440	
				Full range	615				
		LMV324 (all four amplifiers)		25°C	410			830	
				Full range	1160				
B ₁	Unity-gain bandwidth	C _L = 200 pF		25°C	1			MHz	
φ _m	Phase margin			25°C	60			deg	
G _m	Gain margin			25°C	10			dB	
V _n	Equivalent input noise voltage	f = 1 kHz		25°C	39			nV/√Hz	
I _n	Equivalent input noise current	f = 1 kHz		25°C	0.21			pA/√Hz	
SR	Slew rate			25°C	1			V/μs	

† Full range is -40°C to 85°C for I-level part, -40°C to 125°C for Q-level part.



LMV321-Q1 SINGLE, LMV358-Q1 DUAL, LMV324-Q1 QUAD LOW-VOLTAGE RAIL-TO-RAIL OUTPUT OPERATIONAL AMPLIFIERS

SLOS415E – JUNE 2003 – REVISED APRIL 2008

TYPICAL CHARACTERISTICS

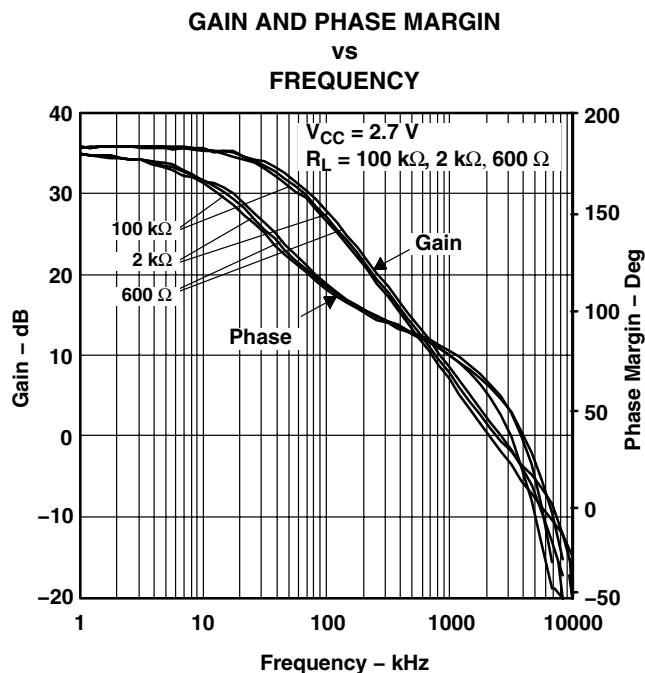


Figure 1

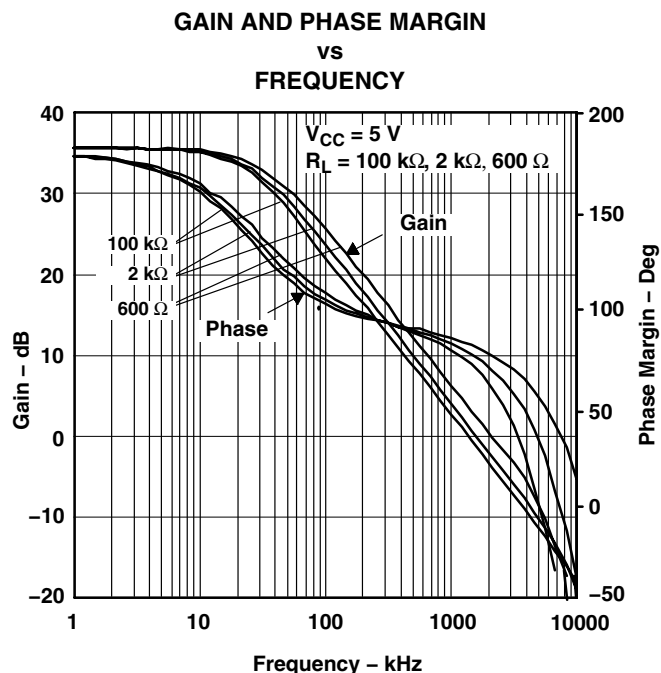


Figure 2

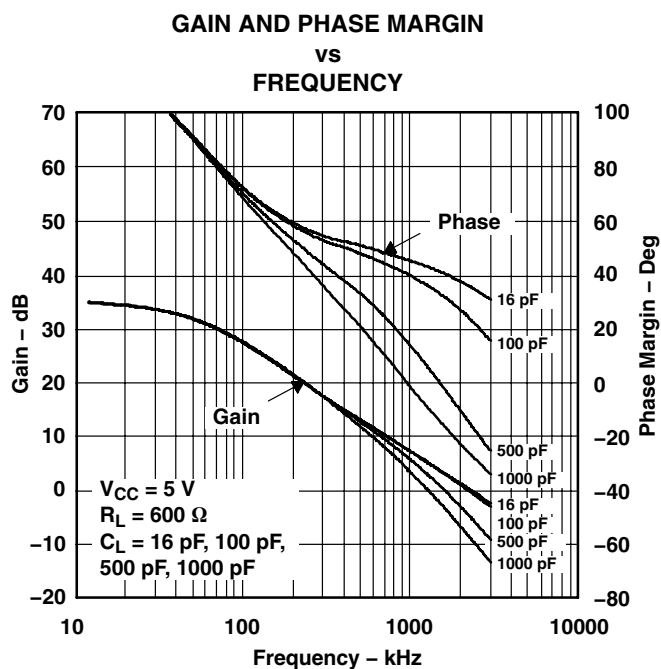


Figure 3

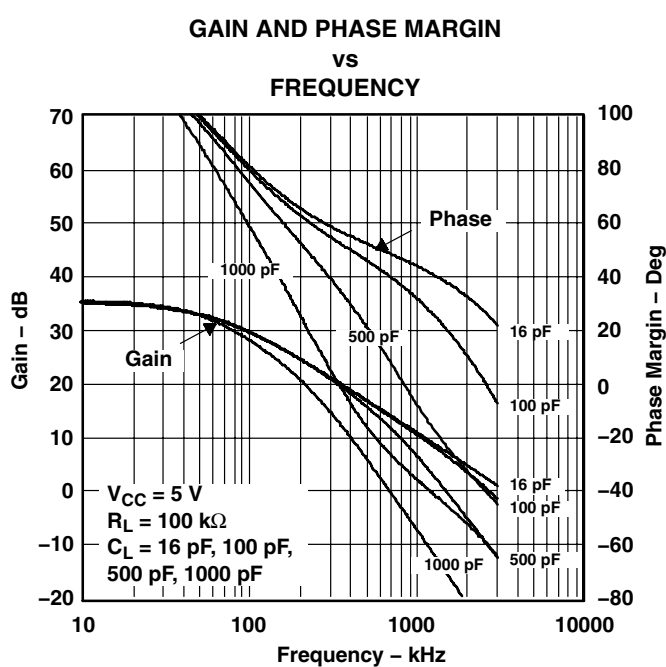


Figure 4



LMV321-Q1 SINGLE, LMV358-Q1 DUAL, LMV324-Q1 QUAD LOW-VOLTAGE RAIL-TO-RAIL OUTPUT OPERATIONAL AMPLIFIERS

SLOS415E – JUNE 2003 – REVISED APRIL 2008

TYPICAL CHARACTERISTICS

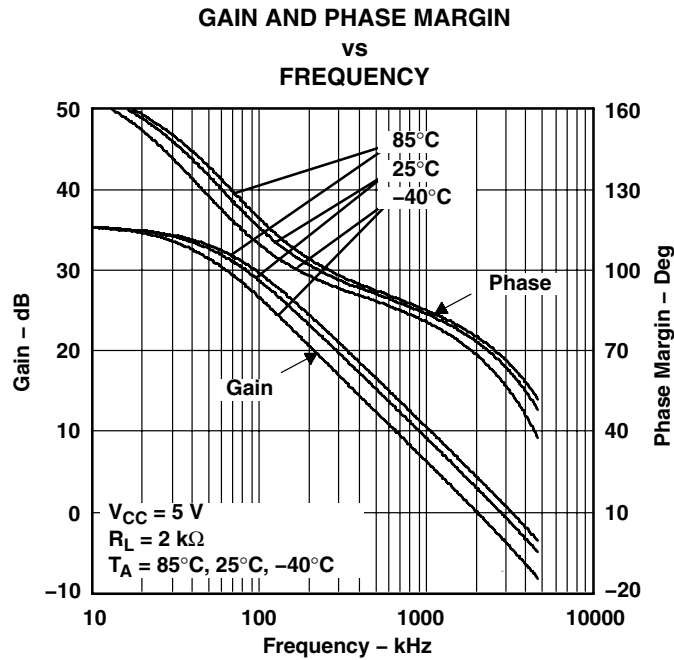


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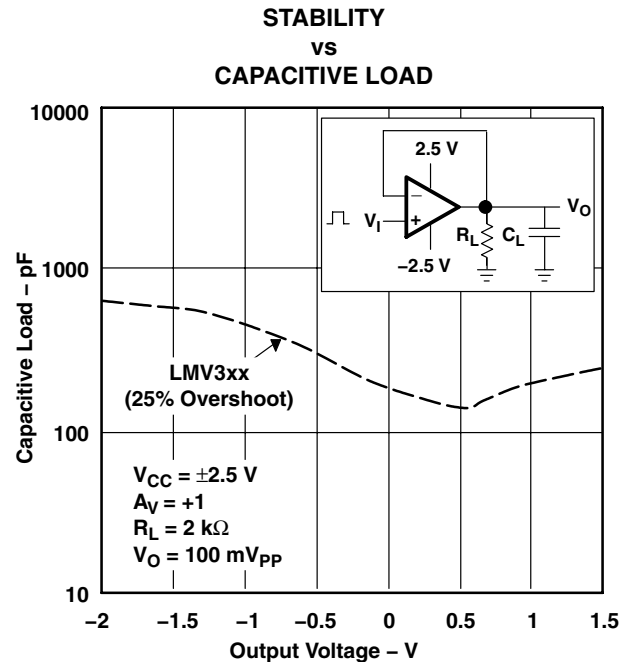


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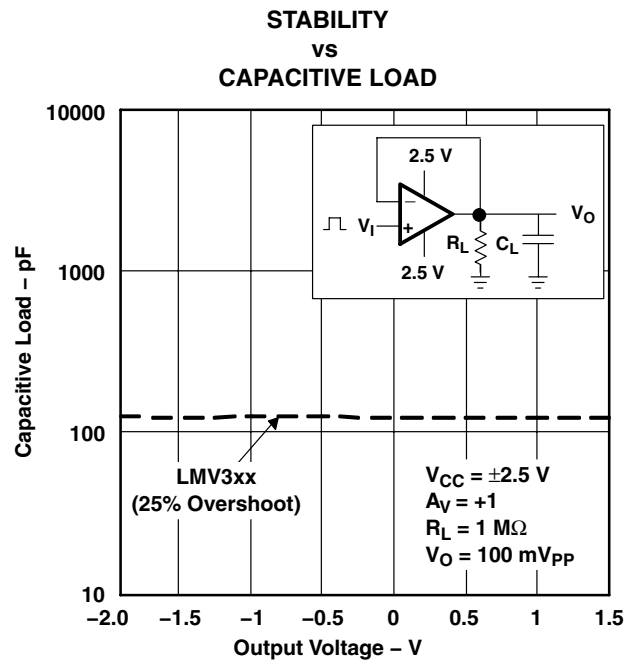


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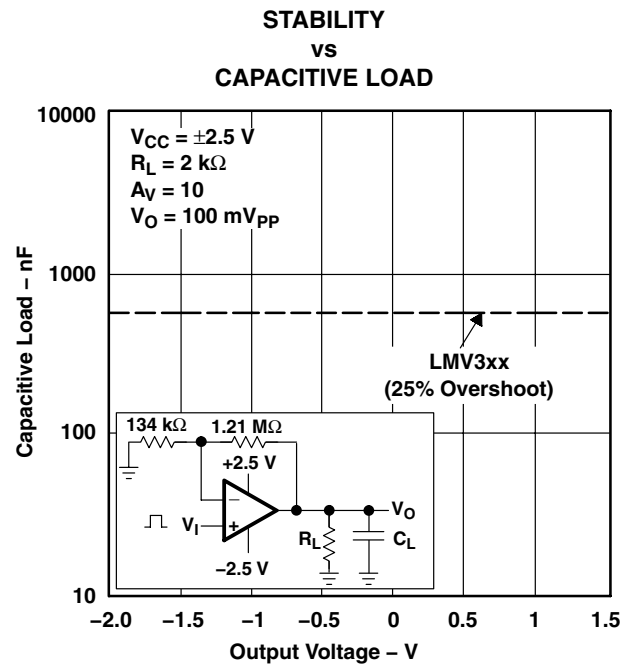


Figure 8



LMV321-Q1 SINGLE, LMV358-Q1 DUAL, LMV324-Q1 QUAD LOW-VOLTAGE RAIL-TO-RAIL OUTPUT OPERATIONAL AMPLIFIERS

SLOS415E – JUNE 2003 – REVISED APRIL 2008

TYPICAL CHARACTERISTICS

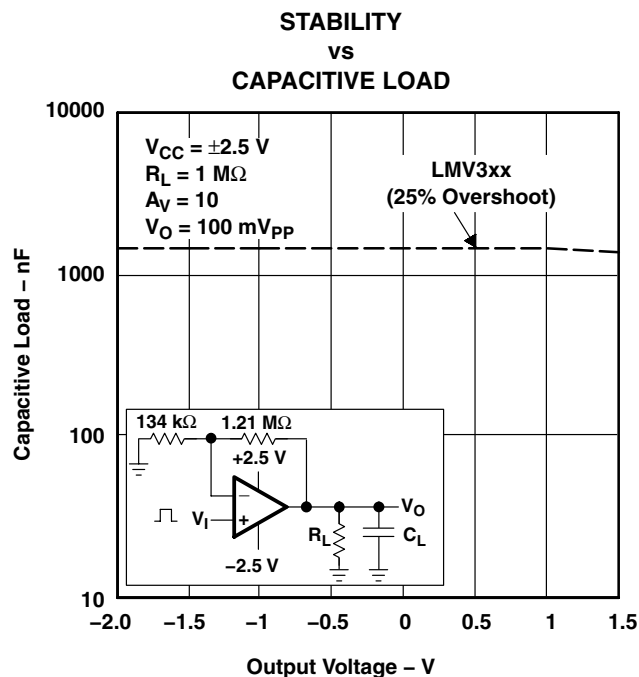


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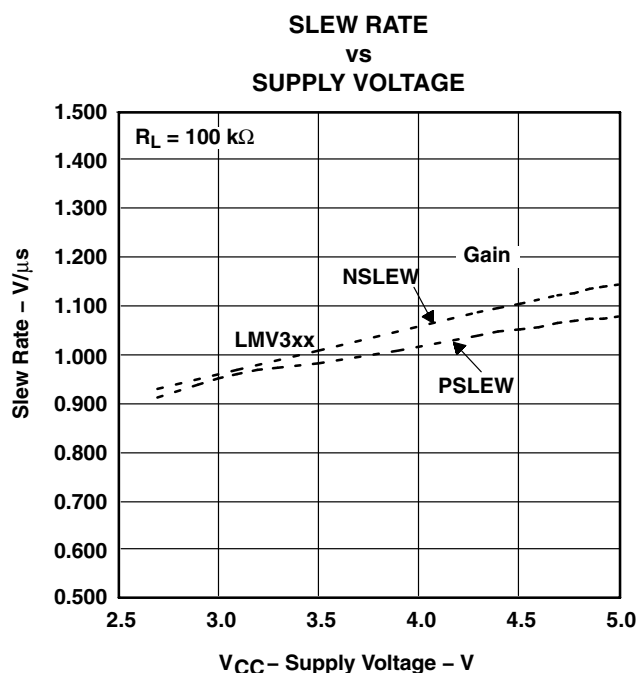


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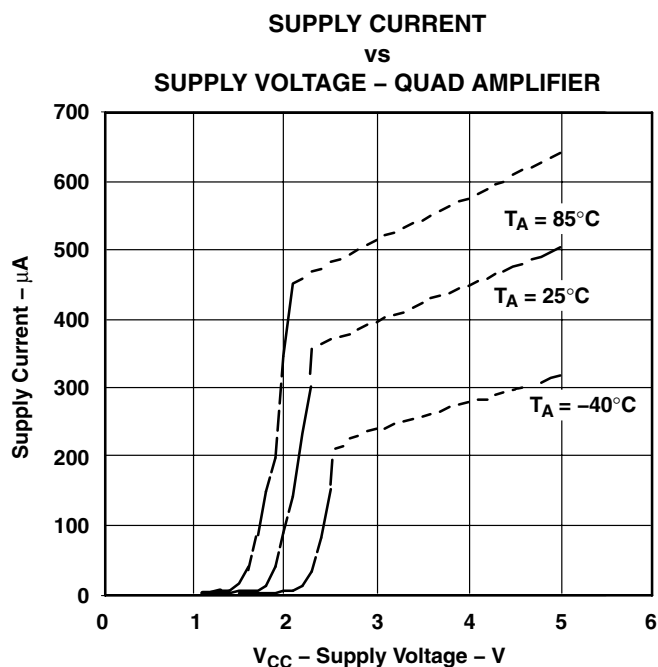


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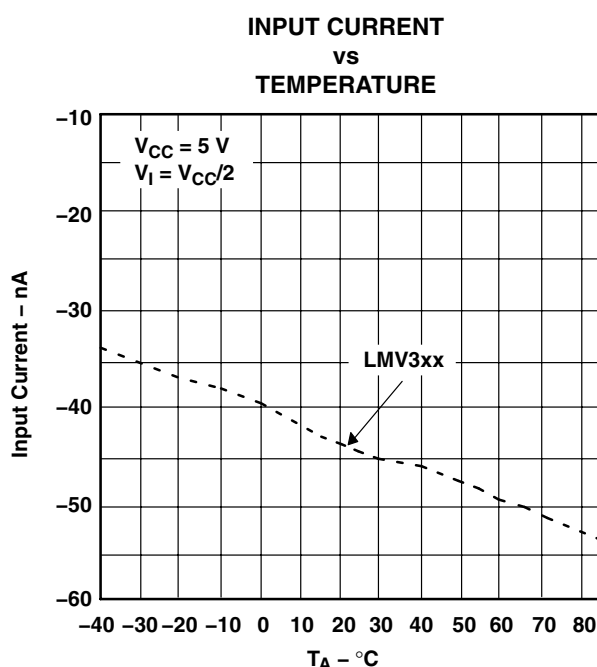


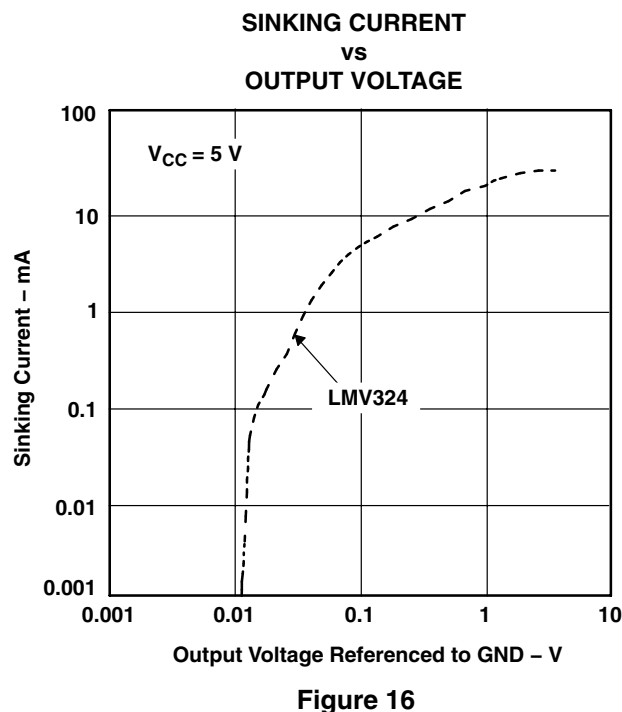
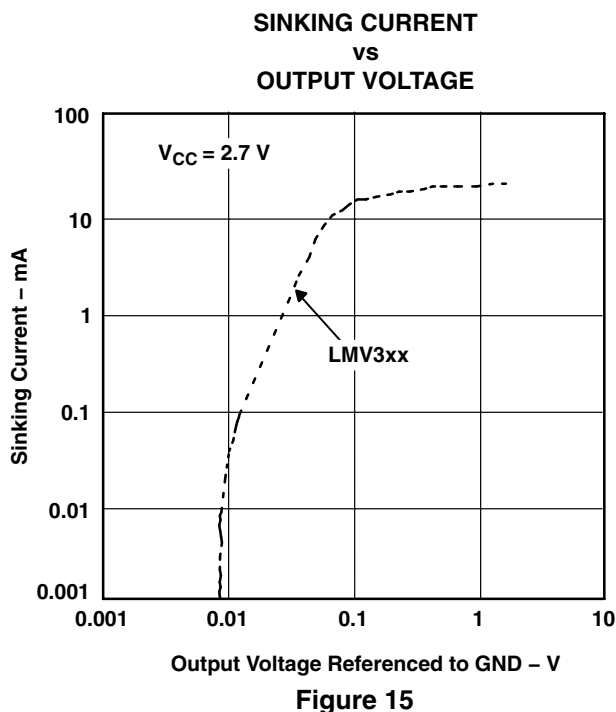
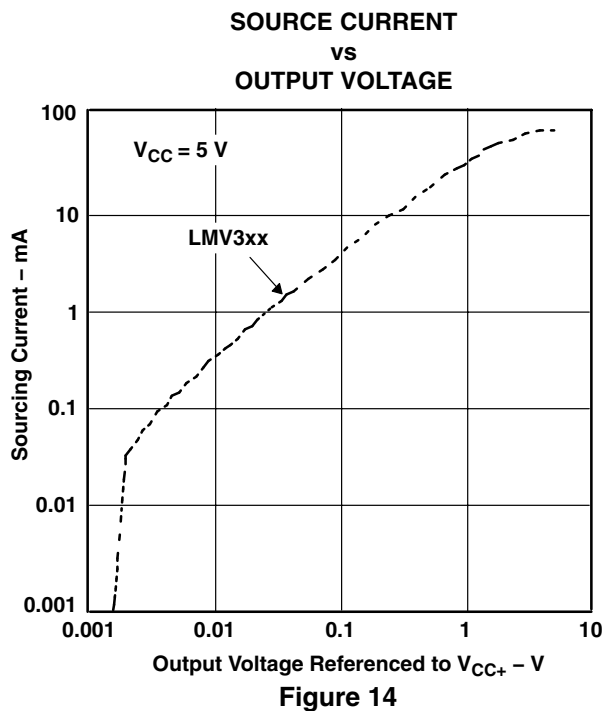
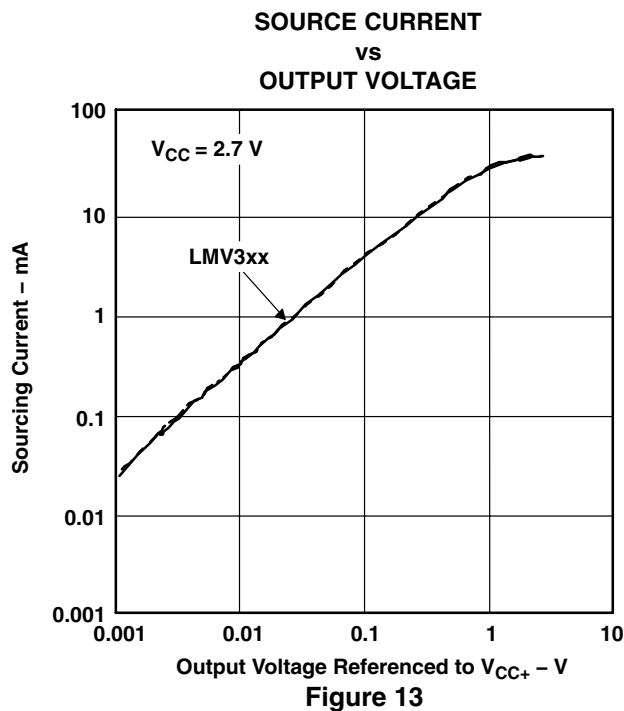
Figure 12



LMV321-Q1 SINGLE, LMV358-Q1 DUAL, LMV324-Q1 QUAD LOW-VOLTAGE RAIL-TO-RAIL OUTPUT OPERATIONAL AMPLIFIERS

SLOS415E – JUNE 2003 – REVISED APRIL 2008

TYPICAL CHARACTERISTICS



LMV321-Q1 SINGLE, LMV358-Q1 DUAL, LMV324-Q1 QUAD LOW-VOLTAGE RAIL-TO-RAIL OUTPUT OPERATIONAL AMPLIFIERS

SLOS415E – JUNE 2003 – REVISED APRIL 2008

TYPICAL CHARACTERISTICS

SHORT-CIRCUIT CURRENT

vs
TEMPERATURE

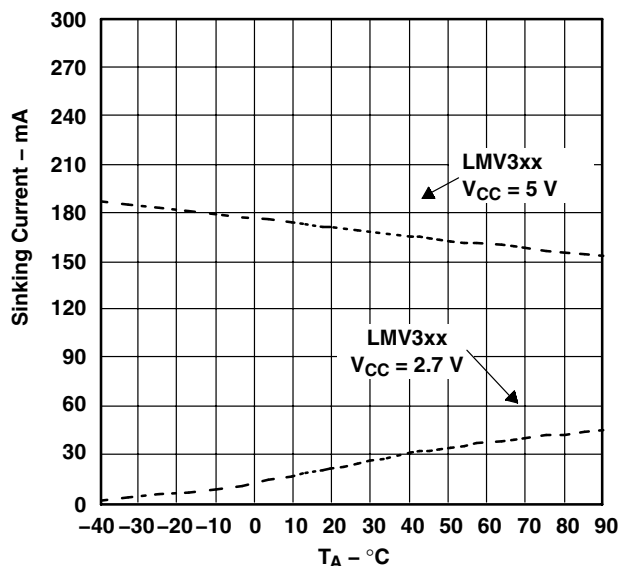


Figure 17

SHORT-CIRCUIT CURRENT

vs
TEMPERATURE

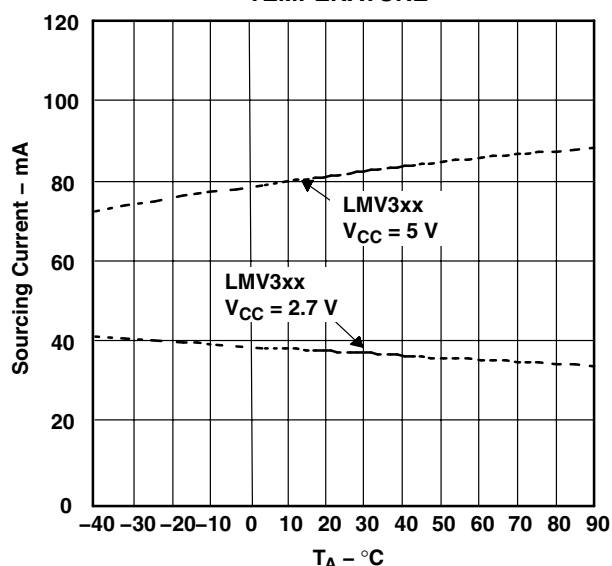


Figure 18

$-k_{SVR}$
vs
FREQUENCY

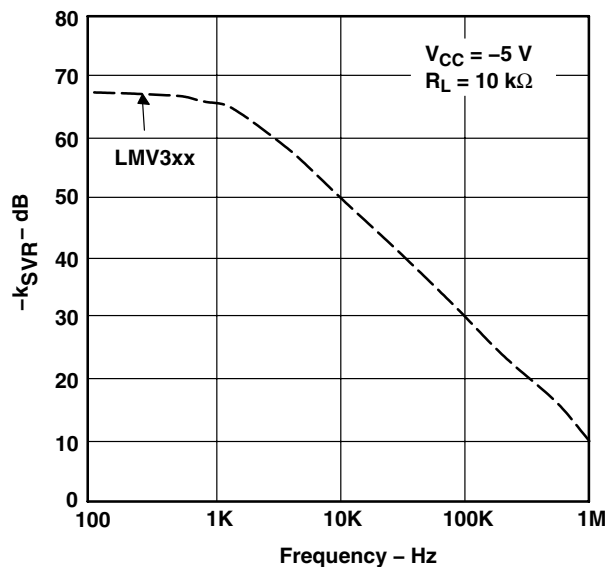


Figure 19

$+k_{SVR}$
vs
FREQUENCY

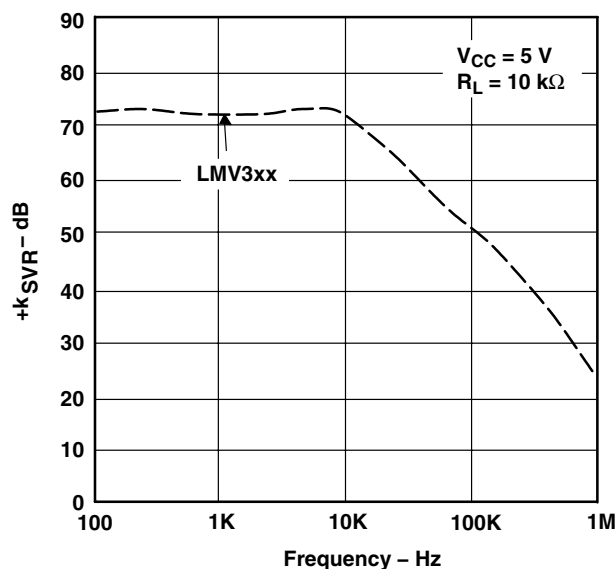
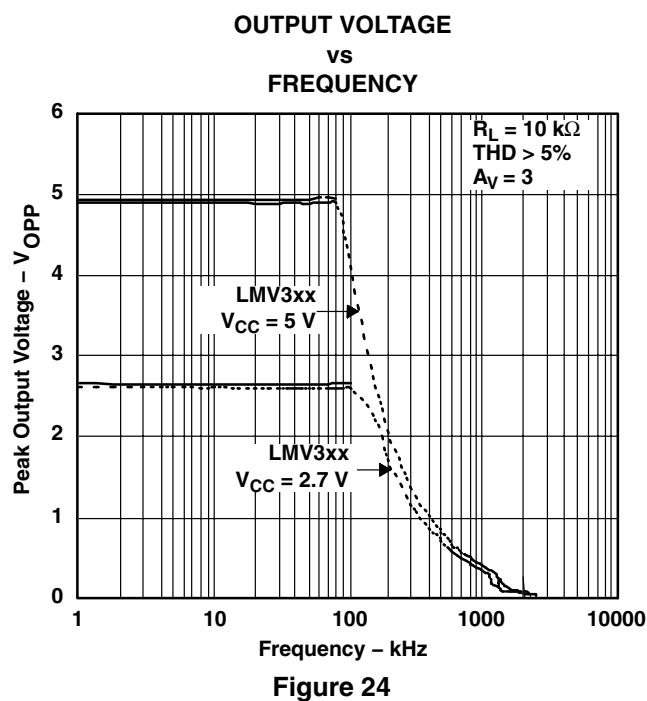
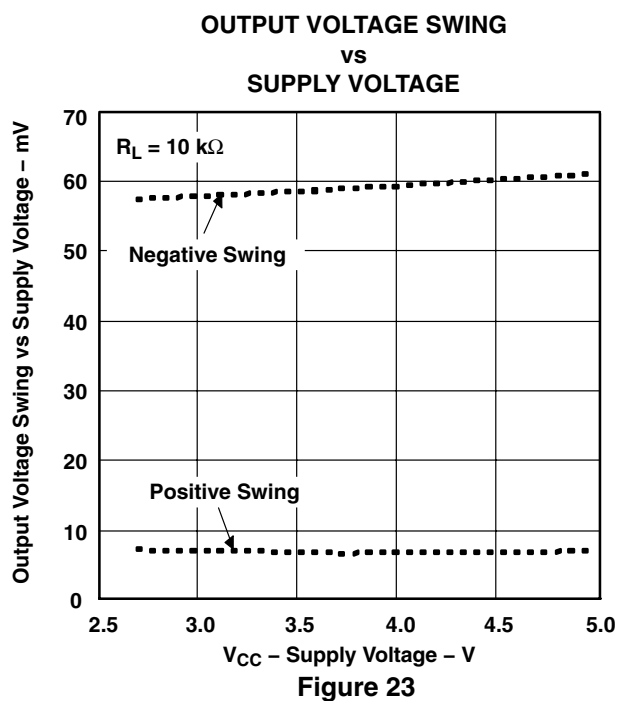
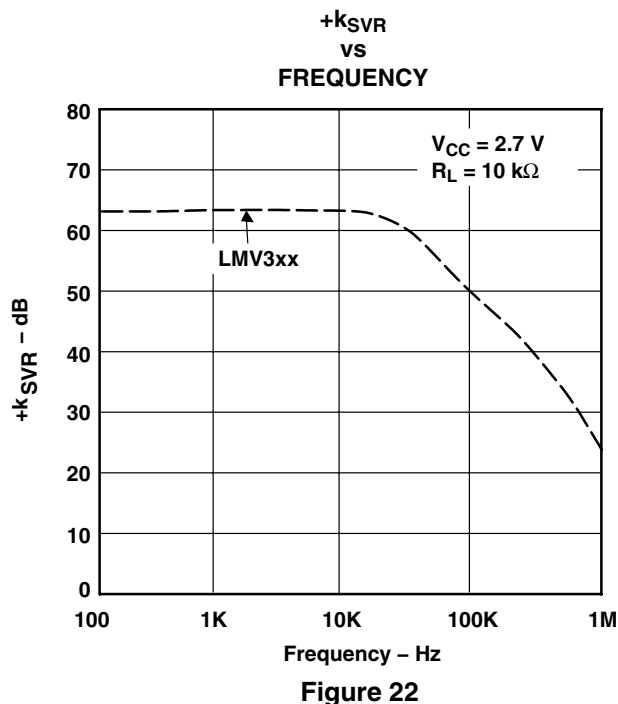
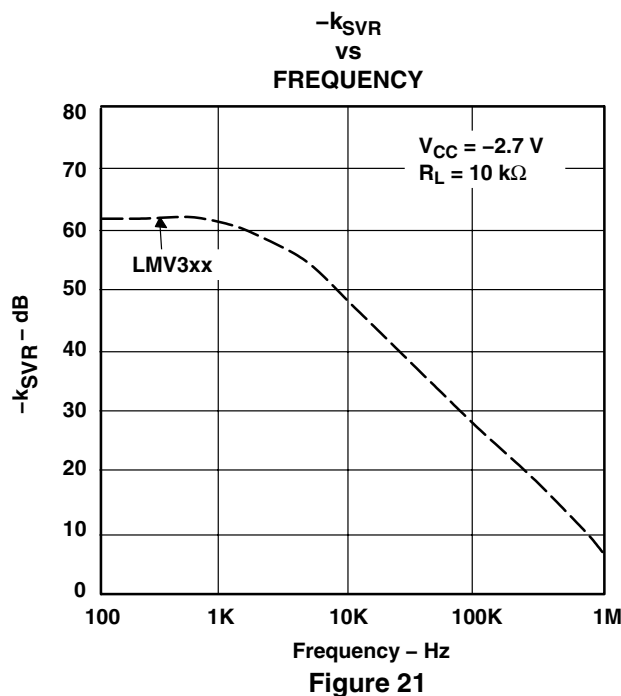


Figure 20

LMV321-Q1 SINGLE, LMV358-Q1 DUAL, LMV324-Q1 QUAD LOW-VOLTAGE RAIL-TO-RAIL OUTPUT OPERATIONAL AMPLIFIERS

SLOS415E – JUNE 2003 – REVISED APRIL 2008

TYPICAL CHARACTERISTICS



LMV321-Q1 SINGLE, LMV358-Q1 DUAL, LMV324-Q1 QUAD LOW-VOLTAGE RAIL-TO-RAIL OUTPUT OPERATIONAL AMPLIFIERS

SLOS415E – JUNE 2003 – REVISED APRIL 2008

TYPICAL CHARACTERISTICS

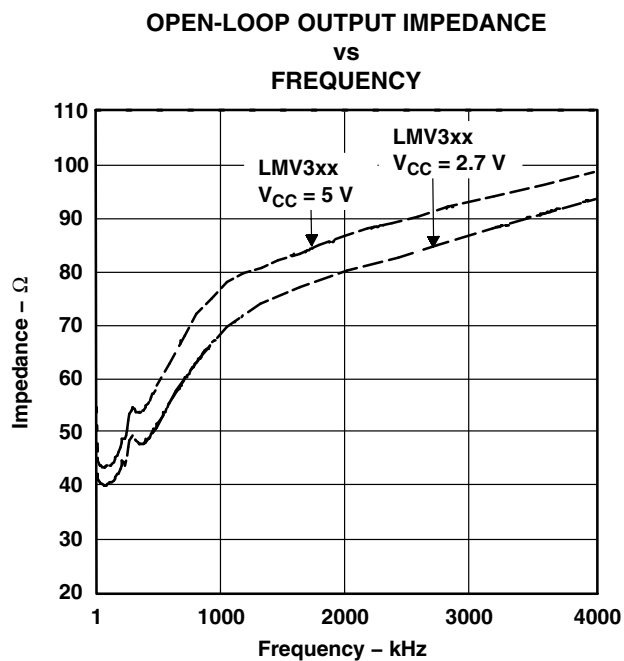


Figure 25

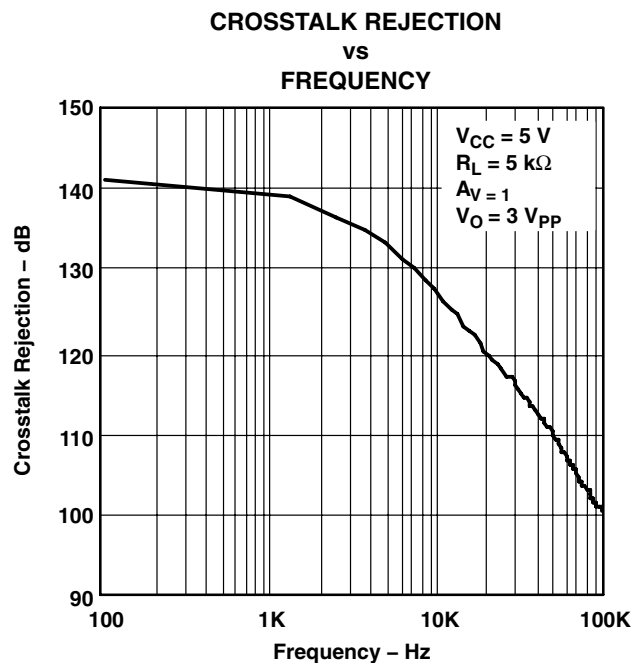


Figure 26



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LOW-VOLTAGE RAIL-TO-RAIL OUTPUT
OPERATIONAL AMPLIFIERS

SLOS415E – JUNE 2003 – REVISED APRIL 2008

TYPICAL CHARACTERISTICS

NONINVERTING LARGE-SIGNAL
PULSE RESPONSE

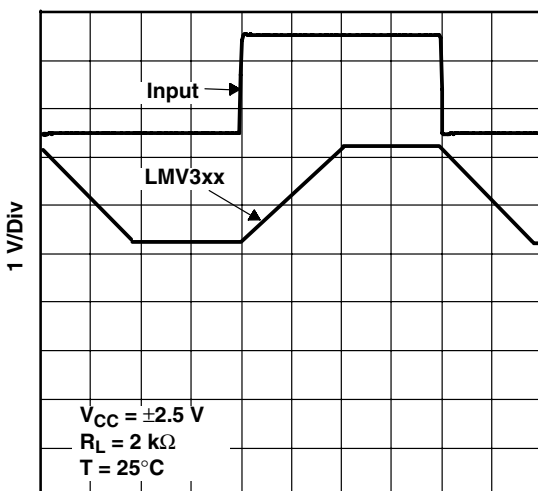


Figure 27

NONINVERTING LARGE-SIGNAL
PULSE RESPONSE

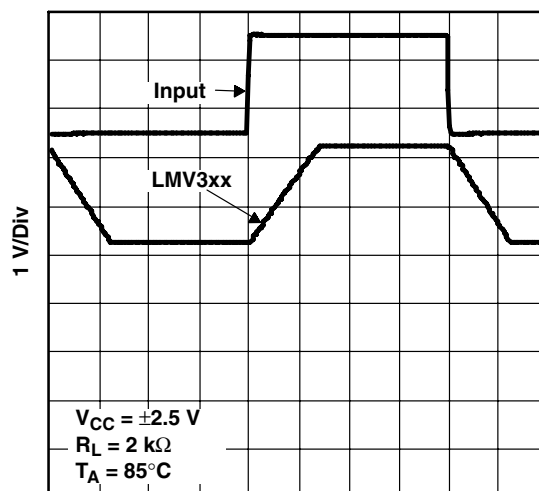


Figure 28

NONINVERTING LARGE-SIGNAL
PULSE RESPONSE

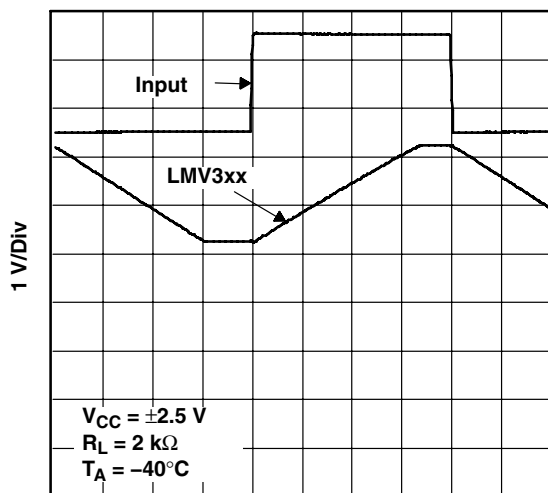


Figure 29

LMV321-Q1 SINGLE, LMV358-Q1 DUAL, LMV324-Q1 QUAD LOW-VOLTAGE RAIL-TO-RAIL OUTPUT OPERATIONAL AMPLIFIERS

SLOS415E – JUNE 2003 – REVISED APRIL 2008

TYPICAL CHARACTERISTICS

NONINVERTING SMALL-SIGNAL
PULSE RESPONSE

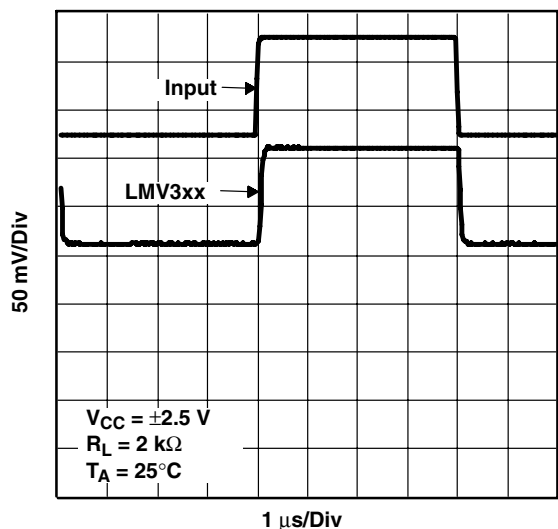


Figure 30

NONINVERTING SMALL-SIGNAL
PULSE RESPONSE

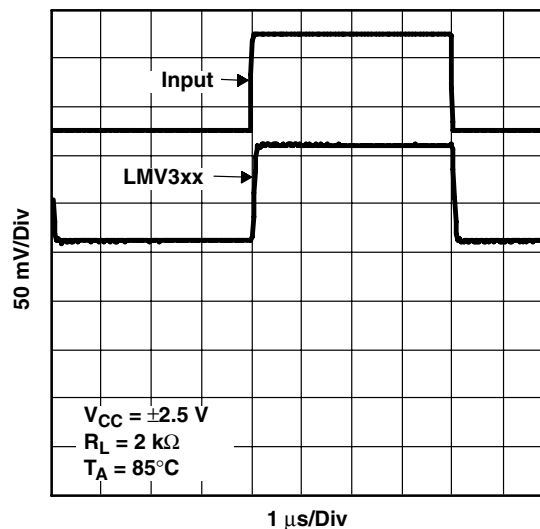


Figure 31

NONINVERTING SMALL-SIGNAL
PULSE RESPONSE

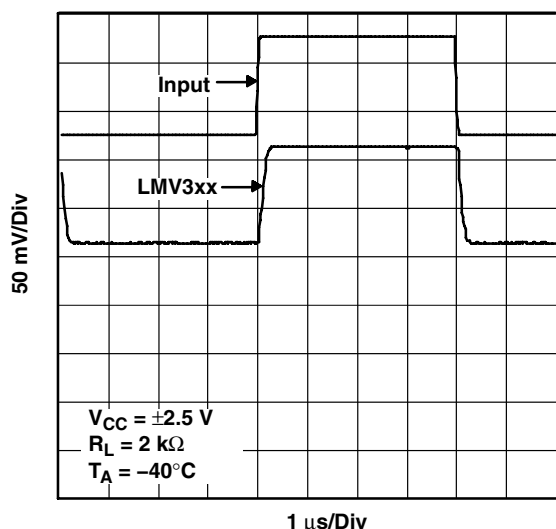


Figure 32

LMV321-Q1 SINGLE, LMV358-Q1 DUAL, LMV324-Q1 QUAD
LOW-VOLTAGE RAIL-TO-RAIL OUTPUT
OPERATIONAL AMPLIFIERS

SLOS415E – JUNE 2003 – REVISED APRIL 2008

TYPICAL CHARACTERISTICS

INVERTING LARGE-SIGNAL
PULSE RESPONSE

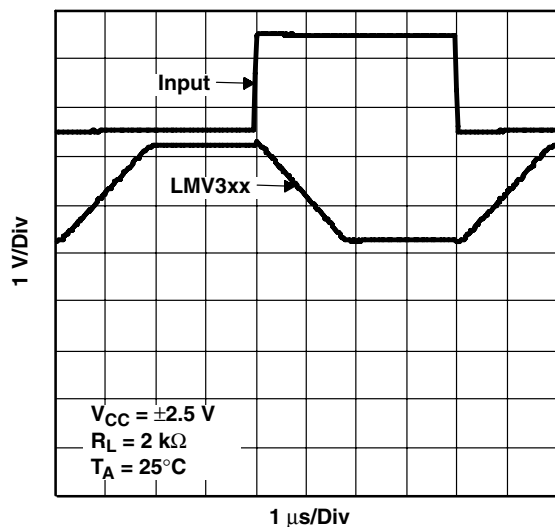


Figure 33

INVERTING LARGE-SIGNAL
PULSE RESPONSE

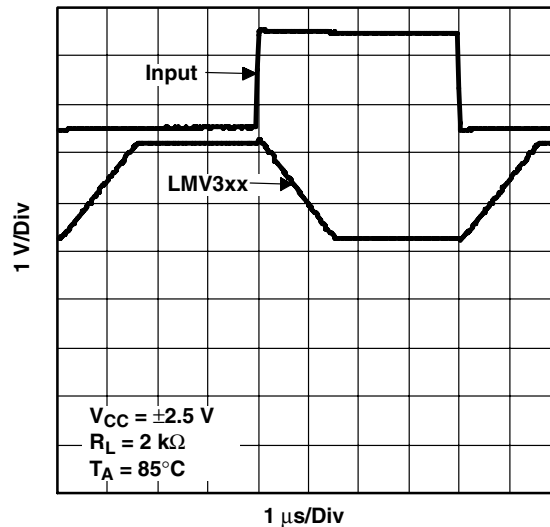


Figure 34

INVERTING LARGE-SIGNAL
PULSE RESPONSE

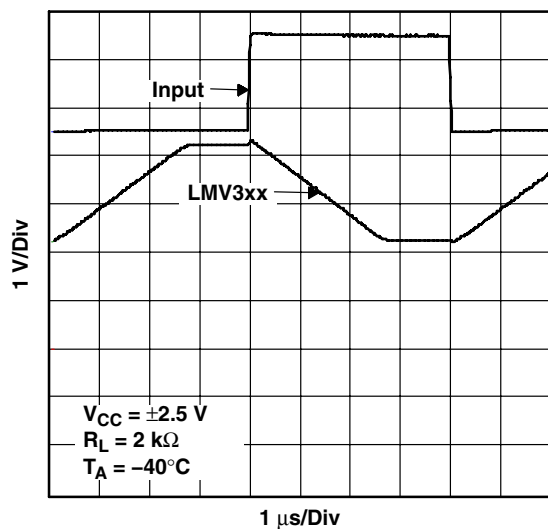


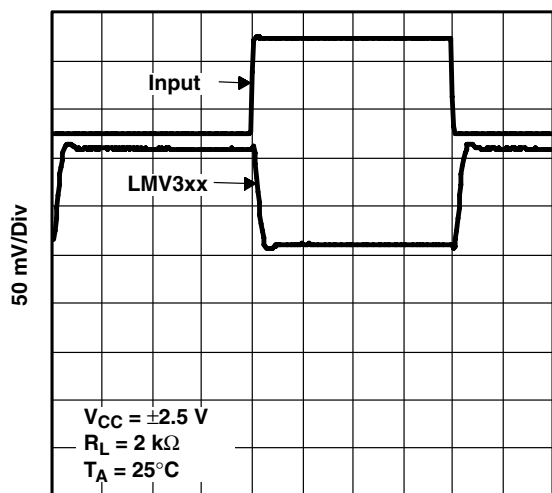
Figure 35

LMV321-Q1 SINGLE, LMV358-Q1 DUAL, LMV324-Q1 QUAD LOW-VOLTAGE RAIL-TO-RAIL OUTPUT OPERATIONAL AMPLIFIERS

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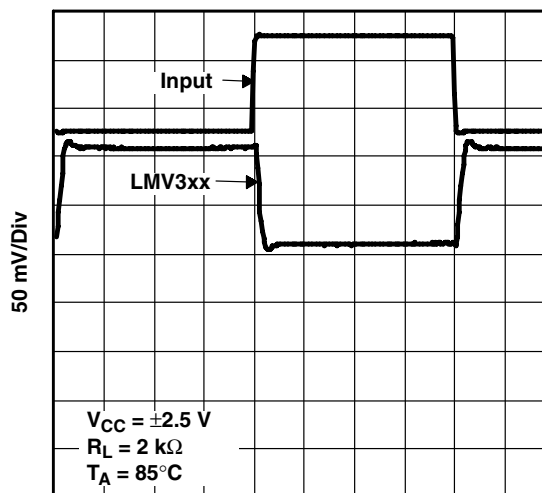
TYPICAL CHARACTERISTICS

INVERTING SMALL-SIGNAL
PULSE RESPONSE



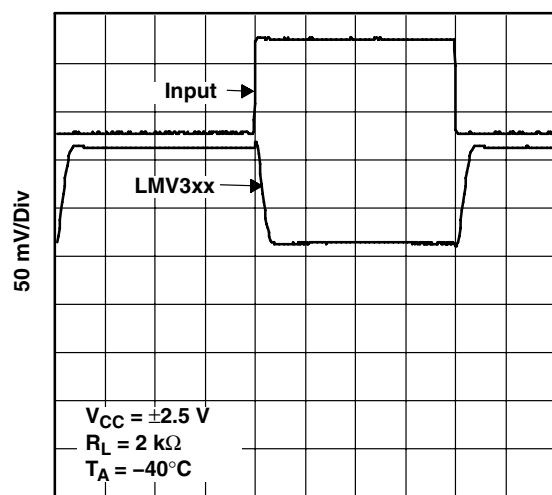
1 $\mu\text{s/Div}$
Figure 36

INVERTING SMALL-SIGNAL
PULSE RESPONSE



1 $\mu\text{s/Div}$
Figure 37

INVERTING SMALL-SIGNAL
PULSE RESPONSE



1 $\mu\text{s/Div}$
Figure 38

LMV321-Q1 SINGLE, LMV358-Q1 DUAL, LMV324-Q1 QUAD
LOW-VOLTAGE RAIL-TO-RAIL OUTPUT
OPERATIONAL AMPLIFIERS

SLOS415E – JUNE 2003 – REVISED APRIL 2008

TYPICAL CHARACTERISTICS

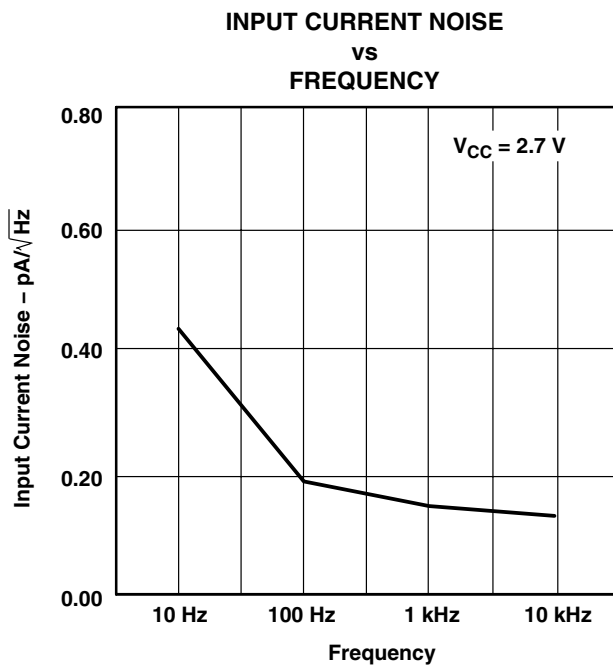


Figure 39

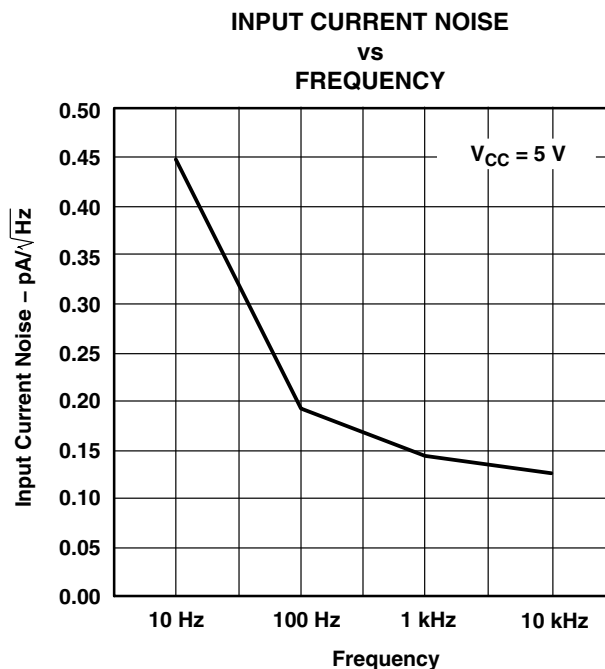


Figure 40

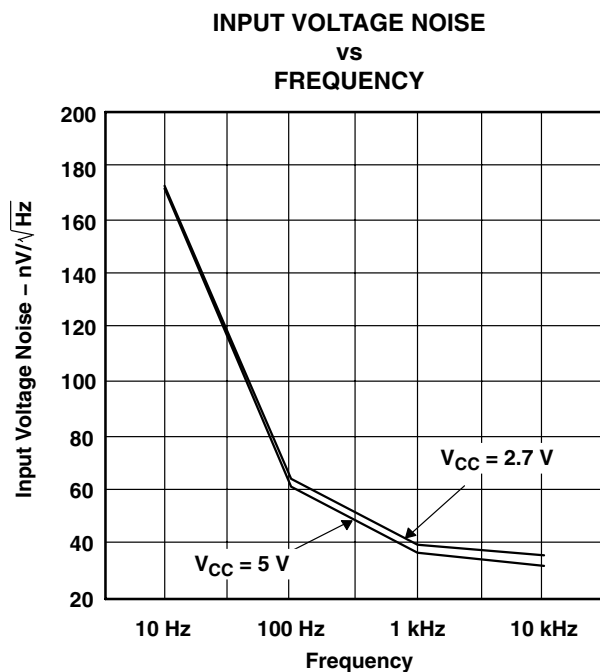


Figure 41



LMV321-Q1 SINGLE, LMV358-Q1 DUAL, LMV324-Q1 QUAD LOW-VOLTAGE RAIL-TO-RAIL OUTPUT OPERATIONAL AMPLIFIERS

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TYPICAL CHARACTERISTICS

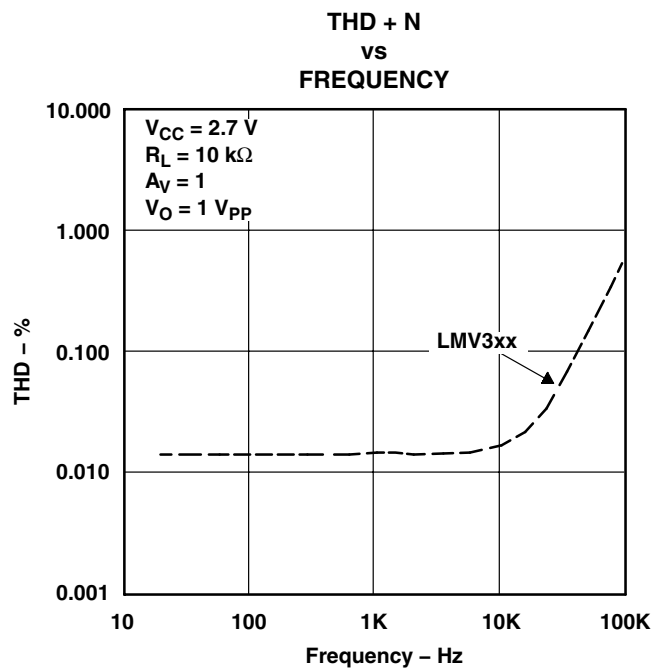


Figure 42

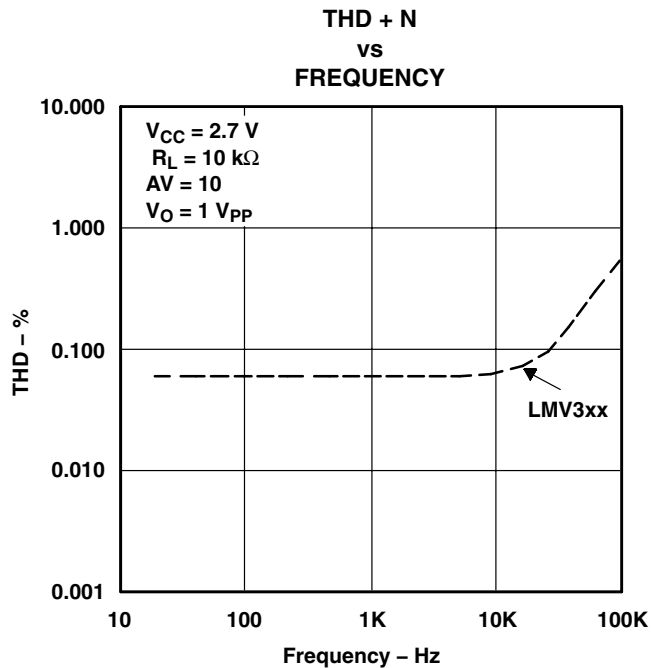


Figure 43

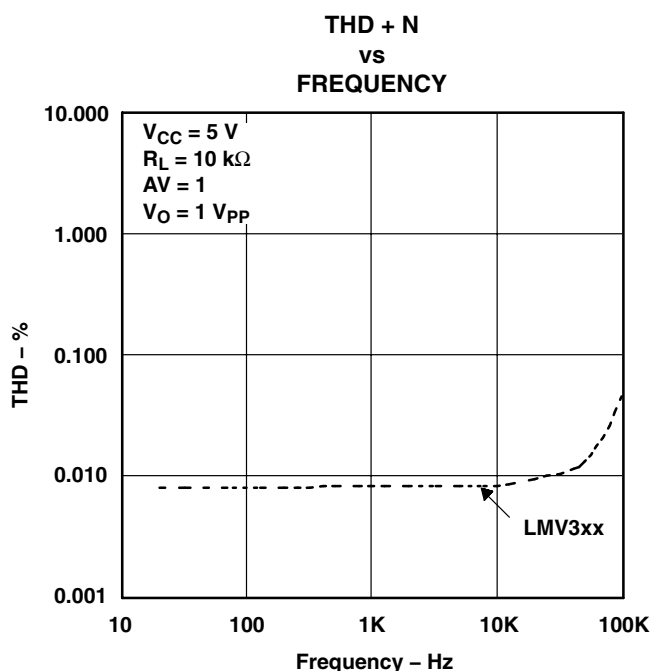


Figure 44

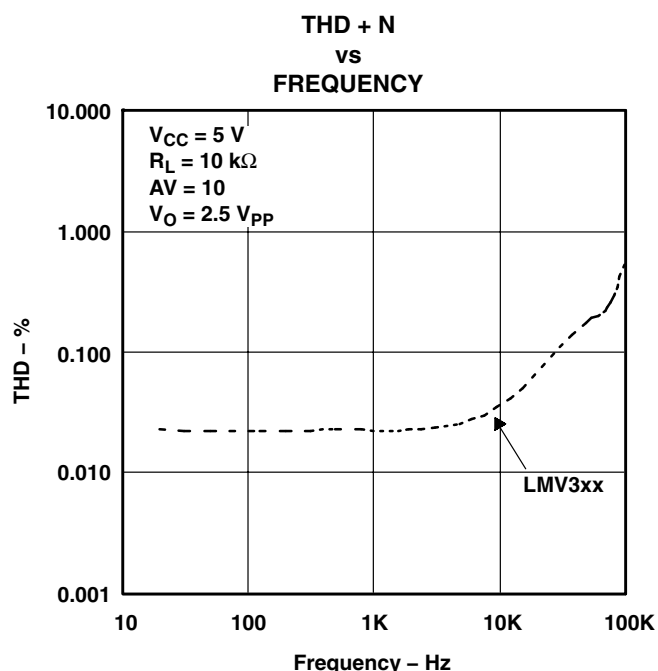


Figure 45



PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/ Ball Finish	MSL Peak Temp ⁽³⁾	Samples (Requires Login)
LMV321IDBVRQ1	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LMV321QDBVRQ1	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LMV324IDRG4Q1	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LMV324IDRQ1	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LMV324IPWRG4Q1	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LMV324IPWRQ1	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LMV324QDQ1	OBSOLETE	SOIC	D	14		TBD	Call TI	Call TI	
LMV324QDRG4Q1	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LMV324QDRQ1	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LMV324QPWRG4Q1	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LMV324QPWRQ1	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LMV358IDRG4Q1	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LMV358IDRQ1	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LMV358IPWRG4Q1	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LMV358IPWRQ1	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LMV358QDQ1	OBSOLETE	SOIC	D	8		TBD	Call TI	Call TI	
LMV358QDRG4Q1	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LMV358QDRQ1	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/ Ball Finish	MSL Peak Temp ⁽³⁾	Samples (Requires Login)
LMV358QPWQ1	OBSOLETE	TSSOP	PW	8		TBD	Call TI	Call TI	
LMV358QPWRG4Q1	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LMV358QPWRQ1	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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OTHER QUALIFIED VERSIONS OF LMV321-Q1, LMV324-Q1, LMV358-Q1 :

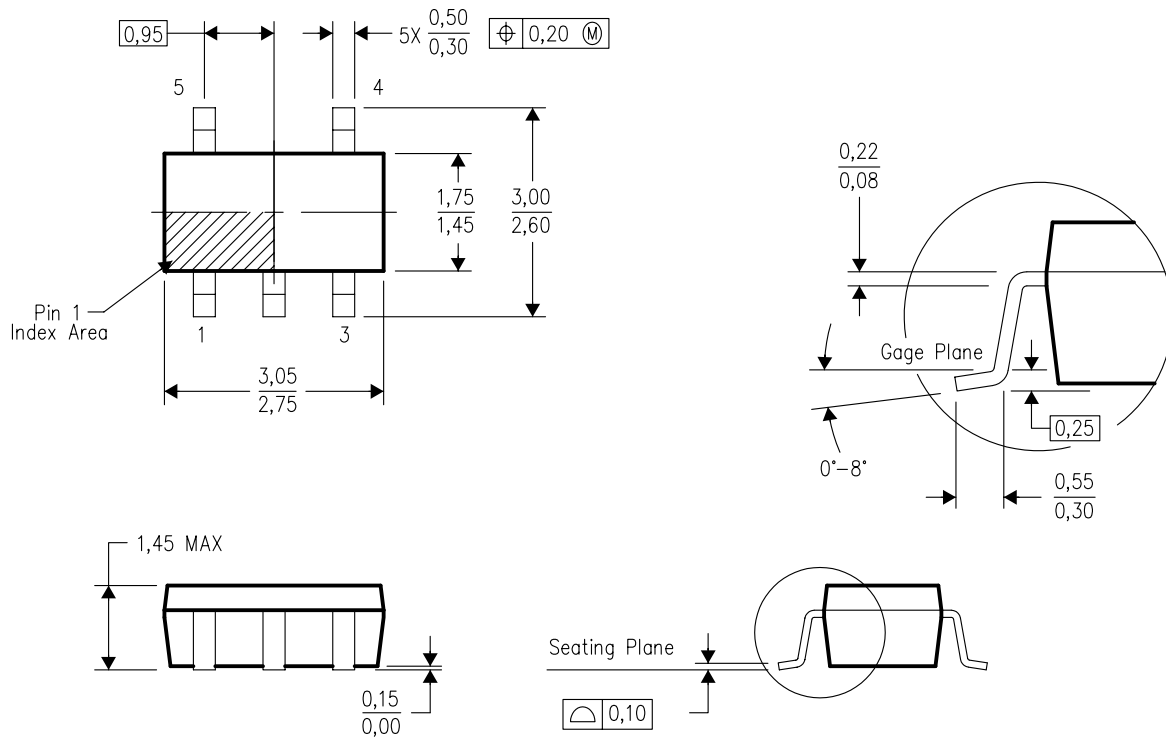
- Catalog: [LMV321](#), [LMV324](#), [LMV358](#)

NOTE: Qualified Version Definitions:

-
- Catalog - TI's standard catalog product

DBV (R-PDSO-G5)

PLASTIC SMALL-OUTLINE PACKAGE

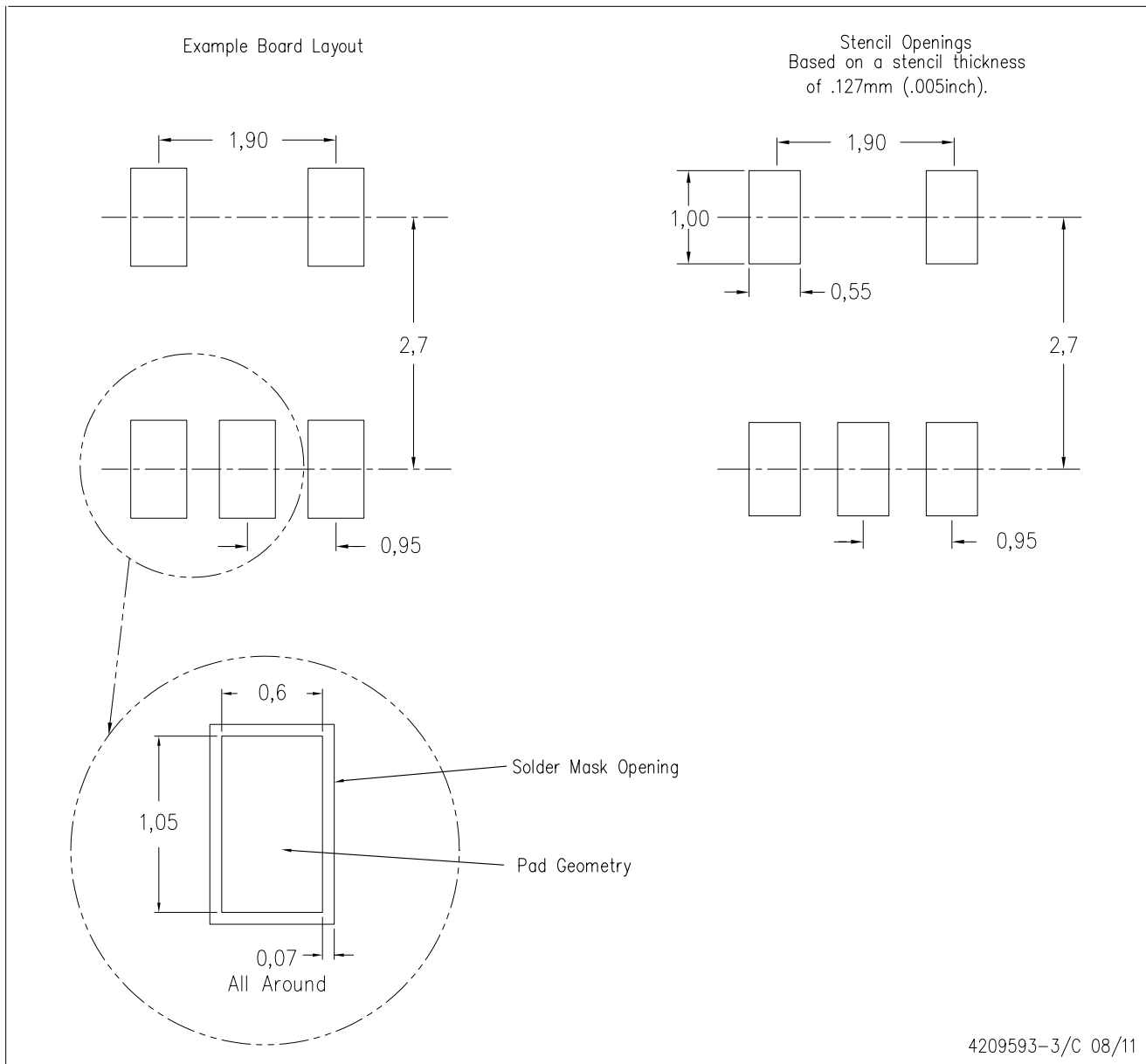


4073253-4/K 03/2006

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
 - D. Falls within JEDEC MO-178 Variation AA.

DBV (R-PDSO-G5)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
 - D. Publication IPC-7351 is recommended for alternate designs.
 - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE

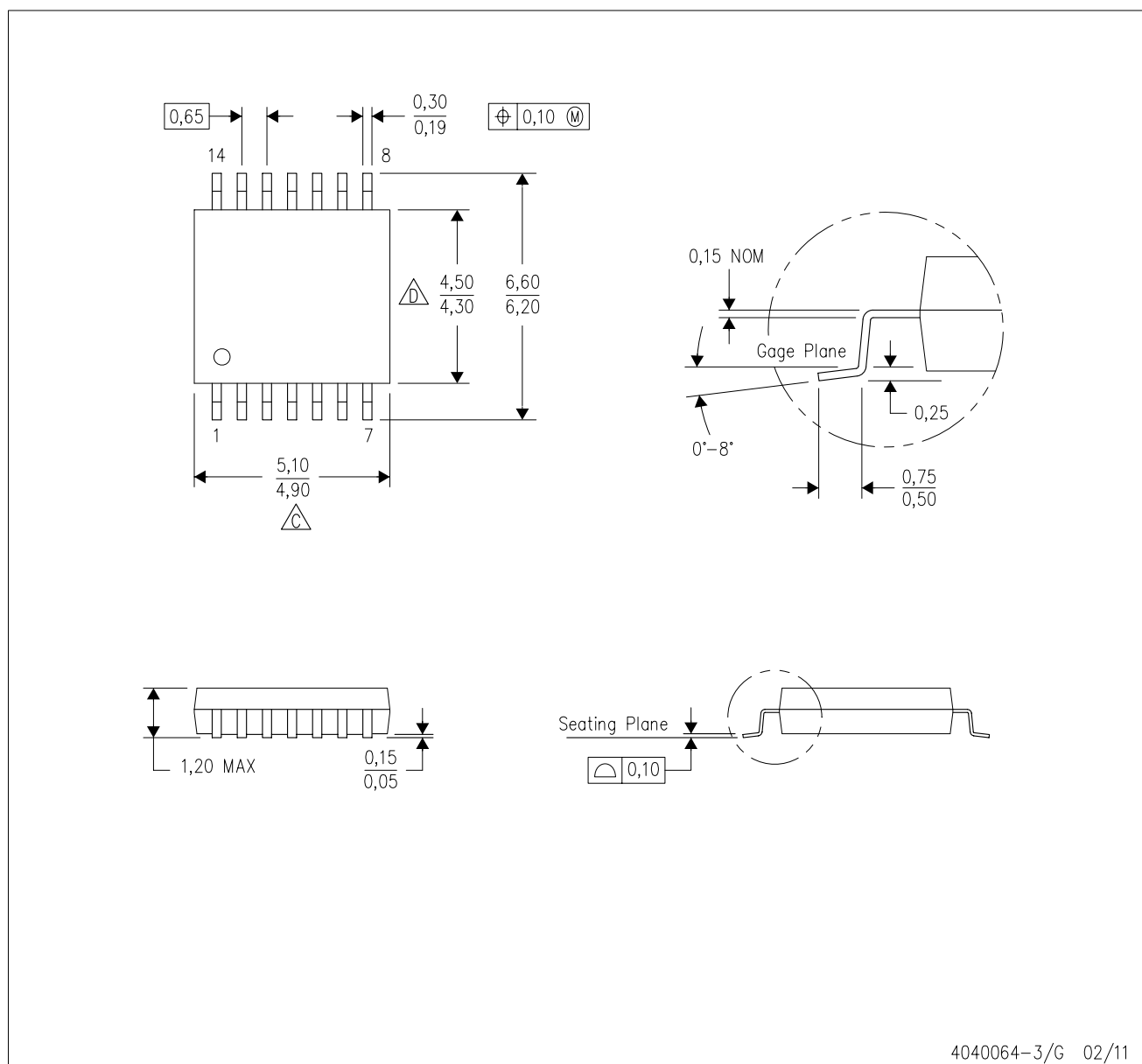


NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AB.

PW (R-PDSO-G14)

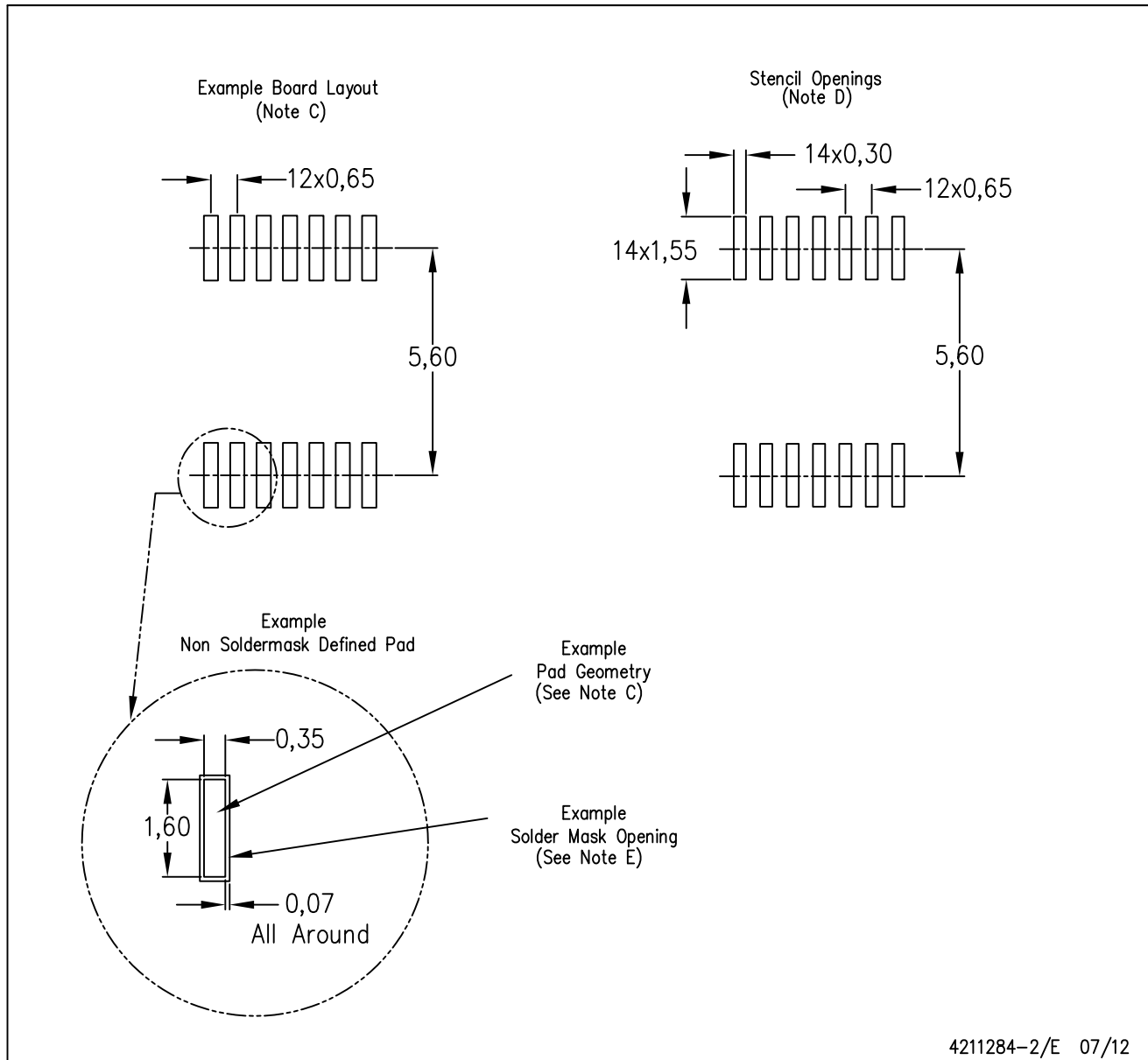
PLASTIC SMALL OUTLINE



4040064-3/G 02/11

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



4211284-2/E 07/12

- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

D (R-PDSO-G8)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - $\triangle C$ Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 - $\triangle D$ Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AA.

D (R-PDSO-G8)

PLASTIC SMALL OUTLINE

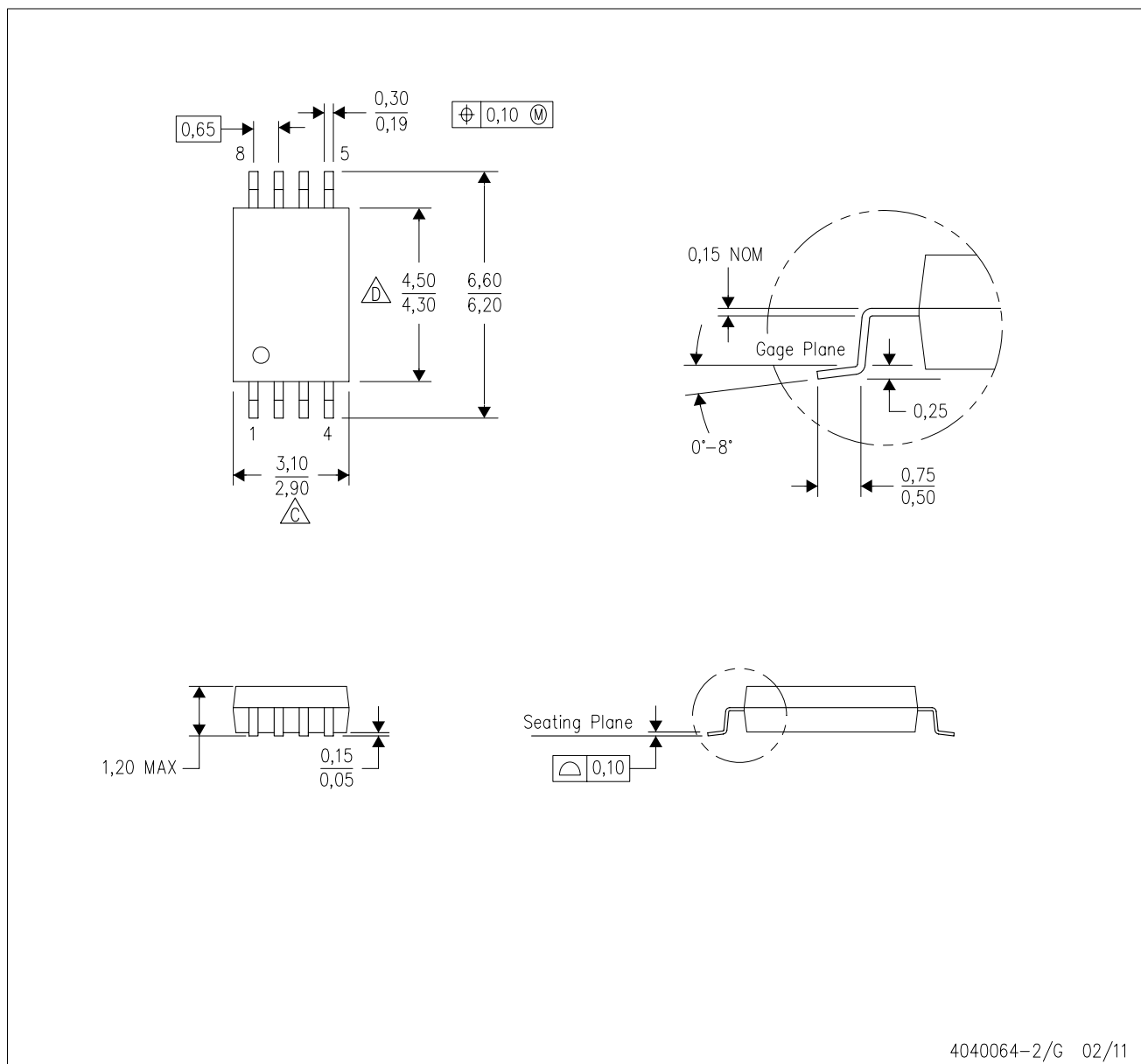


4211283-2/E 08/12

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R-PDSO-G8)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
 - E. Falls within JEDEC MO-153

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