HM628512BI Series

4 M SRAM (512-kword × 8-bit)

HITACHI

ADE-203-935C (Z)
Rev. 2.0
Aug. 24, 1999

Description

The Hitachi HM628512BI is a 4-Mbit static RAM organized 512-kword × 8-bit. HM628512BI Series has realized higher density, higher performance and low power consumption by employing Hi-CMOS process technology. The HM628512BI Series offers low power standby power dissipation; therefore, it is suitable for battery backup systems. It has packaged in 32-pin SOP, 32-pin TSOP II and 32-pin DIP.

Features

- Single 5 V supply
- Access time: 70/85 ns (max)
- Power dissipation
  - — Active: 50 mW/MHz (typ)
  - — Standby: 10 μW (typ)
- Completely static memory. No clock or timing strobe required
- Equal access and cycle times
- Common data input and output: Three state output
- Directly TTL compatible: All inputs and outputs
- Battery backup operation
- Operating temperature: –40 to +85˚C

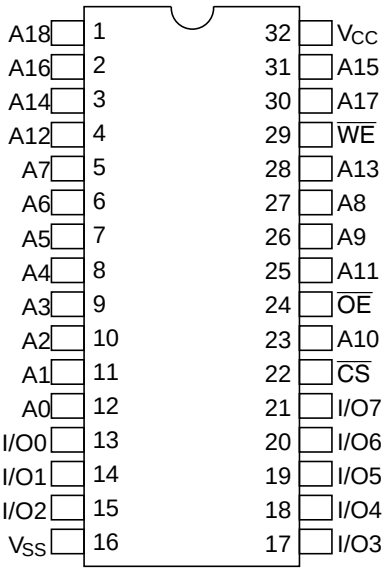
Hitachi semiconductor

Ordering Information

Type No.	Access time	Package
HM628512BLPI-7 HM628512BLPI-8	70 ns 85 ns	600-mil 32-pin plastic DIP (DP-32)
HM628512BLFPI-7 HM628512BLFPI-8	70 ns 85 ns	525-mil 32-pin plastic SOP (FP-32D)
HM628512BLTTI-7 HM628512BLTTI-8	70 ns 85 ns	400-mil 32-pin plastic TSOP II (TTP-32D)
HM628512BLRRI-7 HM628512BLRRI-8	70 ns 85 ns	400-mil 32-pin plastic TSOP II reverse (TTP-32DR)

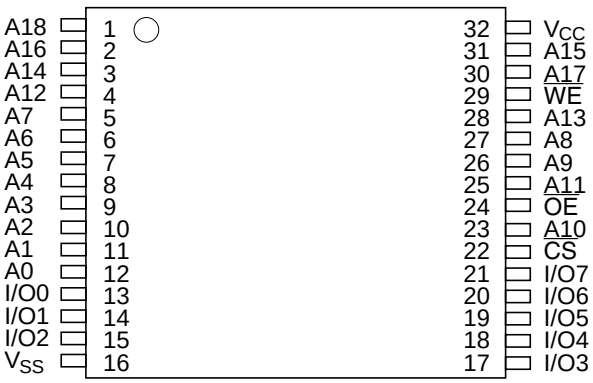
Pin Arrangement

HM628512BLPI Series
HM628512BLFPI Series



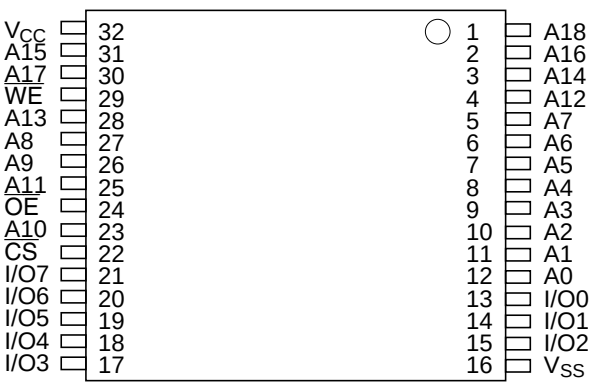
(Top view)

HM628512BLTTI Series



(Top view)

HM628512BLRRI Series

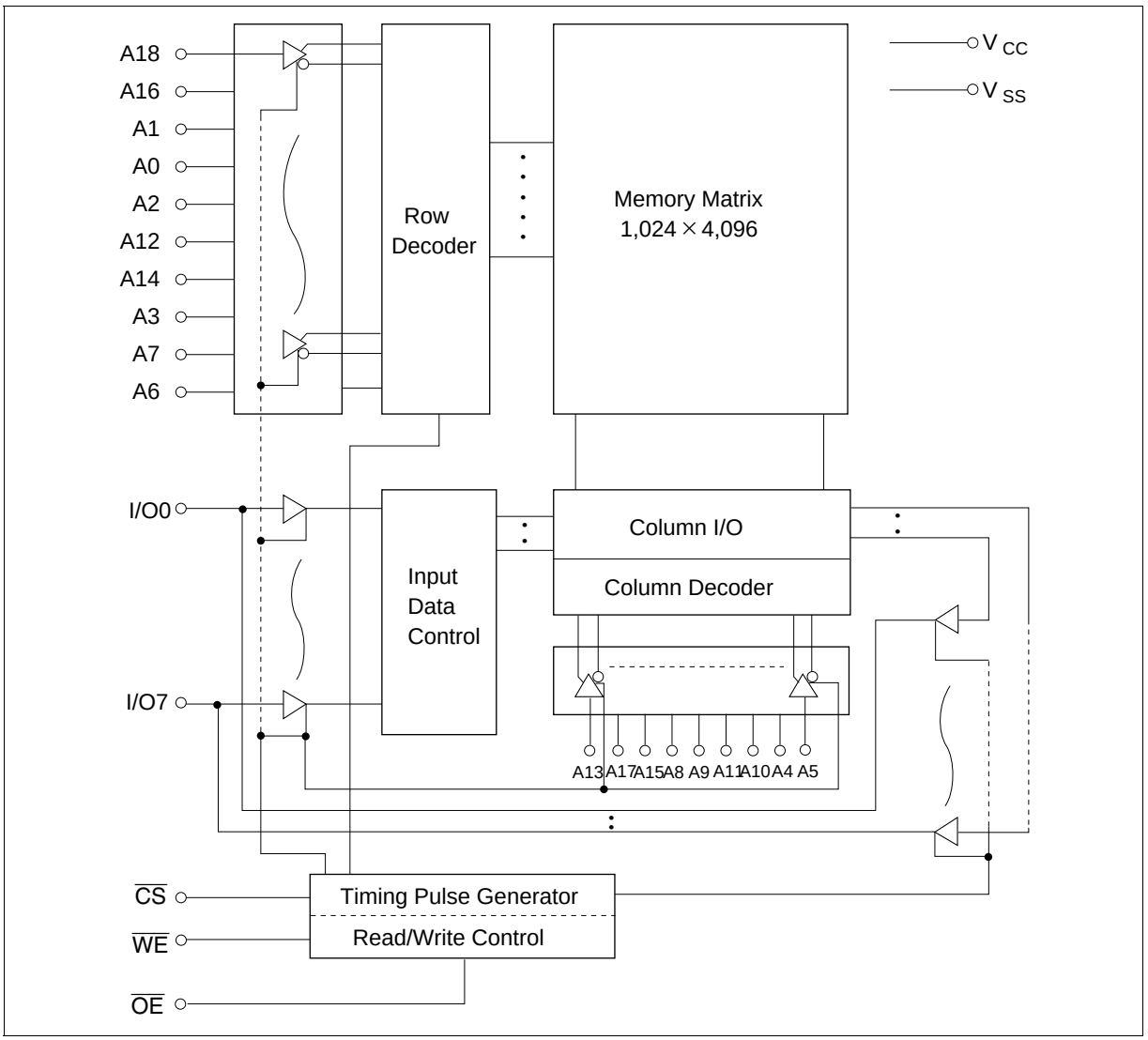


(Top view)

Pin Description

Pin name	Function
A0 to A18	Address input
I/O0 to I/O7	Data input/output
$\overline{CS}$	Chip select
$\overline{OE}$	Output enable
$\overline{WE}$	Write enable
V_{CC}	Power supply
V_{SS}	Ground

Block Diagram



Function Table

$\overline{WE}$	$\overline{CS}$	$\overline{OE}$	Mode	V_{CC} current	Dout pin	Ref. cycle
×	H	×	Not selected	I_{SB}, I_{SB1}	High-Z	—
H	L	H	Output disable	I_{CC}	High-Z	—
H	L	L	Read	I_{CC}	Dout	Read cycle
L	L	H	Write	I_{CC}	Din	Write cycle (1)
L	L	L	Write	I_{CC}	Din	Write cycle (2)

Note: ×: H or L

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Power supply voltage	V_{CC}	–0.5 to +7.0	V
Voltage on any pin relative to V_{SS}	V_T	–0.5*[1] to V_{CC} + 0.3*[2]	V
Power dissipation	P_T	1.0	W
Operating temperature	Topr	–40 to +85	°C
Storage temperature	Tstg	–55 to +125	°C
Storage temperature under bias	Tbias	–40 to +85	°C

Notes: 1. –3.0 V for pulse half-width ≤ 30 ns
2. Maximum voltage is 7.0 V

Recommended DC Operating Conditions (Ta = –40 to +85°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input high voltage	V_{IH}	2.4	—	V_{CC} + 0.3	V
Input low voltage	V_{IL}	–0.3*[1]	—	0.6	V

Note: 1. –3.0 V for pulse half-width ≤ 30 ns

DC Characteristics (Ta = –40 to +85°C, V_{CC} = 5 V ±10% , V_{SS} = 0 V)

Parameter	Symbol	Min	Typ*[1]	Max	Unit	Test conditions
Input leakage current	$\|I_{LI}\|$	—	—	1	µA	Vin = V_{SS} to V_{CC}
Output leakage current	$\|I_{LO}\|$	—	—	1	µA	$\overline{CS}$ = V_{IH} or $\overline{OE}$ = V_{IH} or $\overline{WE}$ = V_{IL}, $V_{I/O}$ = V_{SS} to V_{CC}
Operating power supply current: DC	I_{CC}	—	8	15	mA	$\overline{CS}$ = V_{IL}, others = V_{IH}/V_{IL}, $I_{I/O}$ = 0 mA
Operating power supply current	I_{CC1}	—	45	70	mA	Min cycle, duty = 100% $\overline{CS}$ = V_{IL}, others = V_{IH}/V_{IL} $I_{I/O}$ = 0 mA
Operating power supply current	I_{CC2}	—	10	20	mA	Cycle time = 1 µs, duty = 100% $I_{I/O}$ = 0 mA, $\overline{CS}$ ≤ 0.2 V V_{IH} ≥ V_{CC} – 0.2 V, V_{IL} ≤ 0.2 V
Standby power supply current: DC	I_{SB}	—	1	3	mA	$\overline{CS}$ = V_{IH}
Standby power supply current (1): DC	I_{SB1}	—	2	100	µA	Vin ≥ 0 V, $\overline{CS}$ ≥ V_{CC} – 0.2 V
Output low voltage	V_{OL}	—	—	0.4	V	I_{OL} = 2.1 mA
Output high voltage	V_{OH}	2.4	—	—	V	I_{OH} = –1.0 mA

Note: 1. Typical values are at V_{CC} = 5.0 V, Ta = +25°C and specified loading, and not guaranteed.

Capacitance (Ta = +25°C, f = 1 MHz)

Parameter	Symbol	Typ	Max	Unit	Test conditions
Input capacitance*[1]	Cin	—	8	pF	Vin = 0 V
Input/output capacitance*[1]	$C_{I/O}$	—	10	pF	$V_{I/O}$ = 0 V

Note: 1. This parameter is sampled and not 100% tested.

AC Characteristics (Ta = –40 to +85°C, V_{CC} = 5 V ± 10%, unless otherwise noted.)

Test Conditions

- Input pulse levels: 0.5 V to 2.5 V
- Input rise and fall time: 5 ns
- Input and output timing reference levels: 1.5 V
- Output load: 1 TTL Gate + C_L (100 pF) (Including scope and jig)

Read Cycle

		HM628512BI					
		-7		-8			
Parameter	Symbol	Min	Max	Min	Max	Unit	Notes
Read cycle time	t_{RC}	70	—	85	—	ns	
Address access time	t_{AA}	—	70	—	85	ns	
Chip select access time	t_{CO}	—	70	—	85	ns	
Output enable to output valid	t_{OE}	—	35	—	45	ns	
Chip selection to output in low-Z	t_{LZ}	10	—	10	—	ns	2
Output enable to output in low-Z	t_{OLZ}	5	—	5	—	ns	2
Chip deselection to output in high-Z	t_{HZ}	0	25	0	30	ns	1, 2
Output disable to output in high-Z	t_{OHZ}	0	25	0	30	ns	1, 2
Output hold from address change	t_{OH}	10	—	10	—	ns	

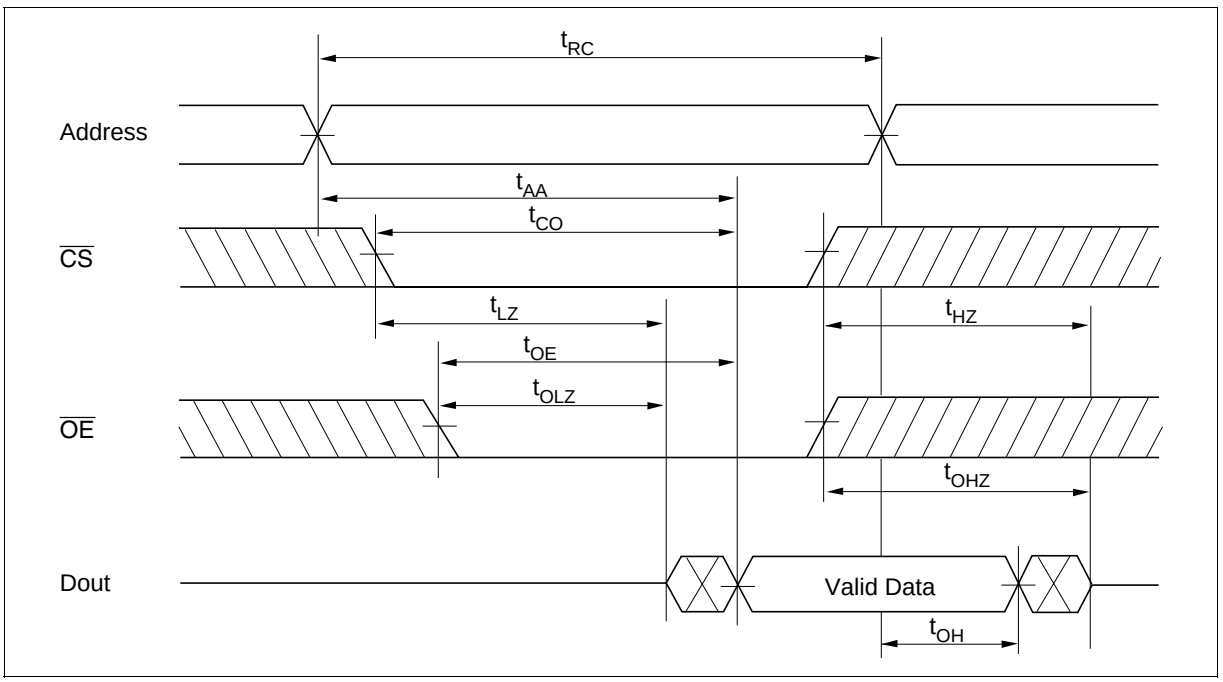
Write Cycle

		HM628512BI					
		-7		-8			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
Write cycle time	t_{WC}	70	—	85	—	ns	
Chip selection to end of write	t_{CW}	60	—	75	—	ns	4
Address setup time	t_{AS}	0	—	0	—	ns	5
Address valid to end of write	t_{AW}	60	—	75	—	ns	
Write pulse width	t_{WP}	50	—	55	—	ns	3, 12
Write recovery time	t_{WR}	0	—	0	—	ns	6
$\overline{WE}$ to output in high-Z	t_{WHZ}	0	25	0	30	ns	1, 2, 7
Data to write time overlap	t_{DW}	30	—	35	—	ns	
Data hold from write time	t_{DH}	0	—	0	—	ns	
Output active from output in high-Z	t_{OW}	5	—	5	—	ns	2
Output disable to output in high-Z	t_{OHZ}	0	25	0	30	ns	1, 2, 7

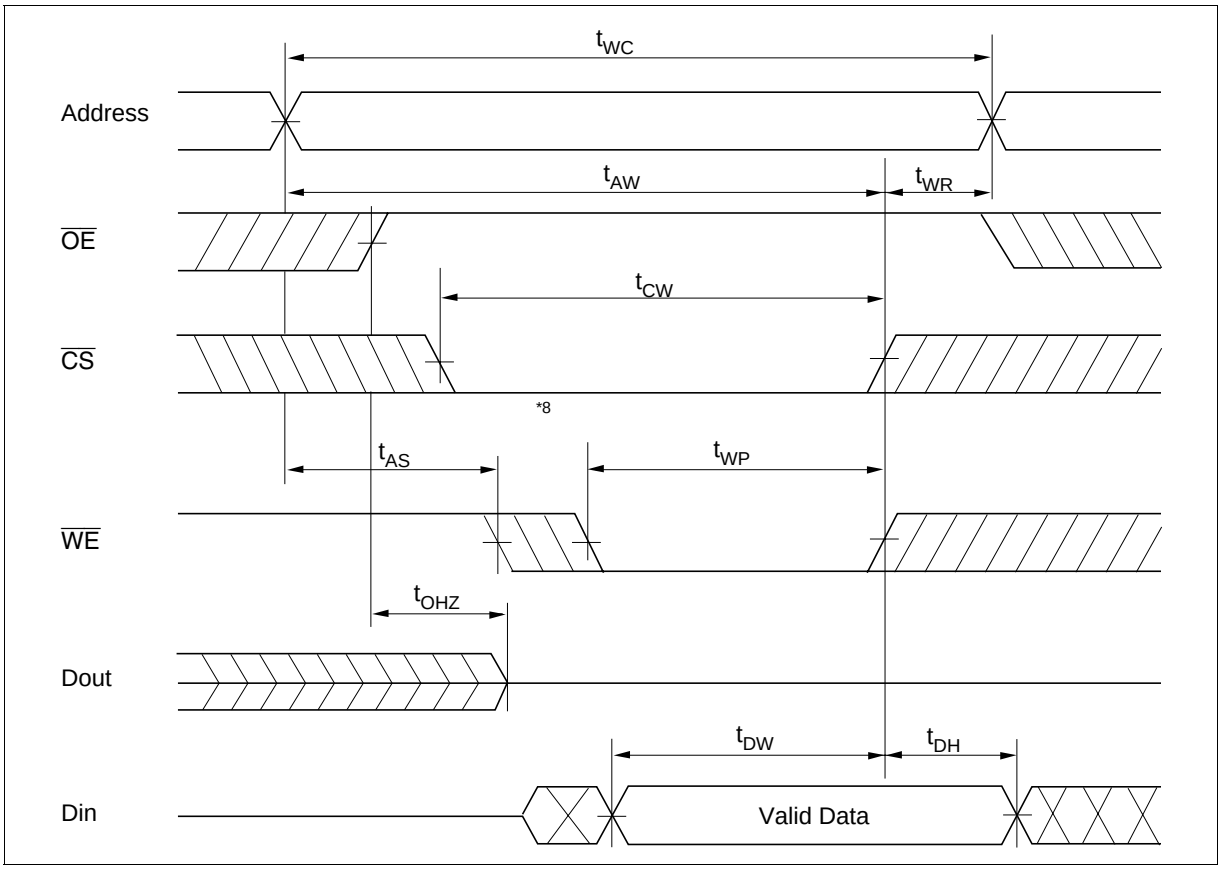
Notes:
1. t_{HZ}, t_{OHZ} and t_{WHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referred to output voltage levels.
2. This parameter is sampled and not 100% tested.
3. A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ and a low $\overline{WE}$. A write begins at the later transition of $\overline{CS}$ going low or $\overline{WE}$ going low. A write ends at the earlier transition of $\overline{CS}$ going high or $\overline{WE}$ going high. t_{WP} is measured from the beginning of write to the end of write.
4. t_{CW} is measured from $\overline{CS}$ going low to the end of write.
5. t_{AS} is measured from the address valid to the beginning of write.
6. t_{WR} is measured from the earlier of $\overline{WE}$ or $\overline{CS}$ going high to the end of write cycle.
7. During this period, I/O pins are in the output state so that the input signals of the opposite phase to the outputs must not be applied.
8. If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transition or after the $\overline{WE}$ transition, the output remain in a high impedance state.
9. Dout is the same phase of the write data of this write cycle.
10. Dout is the read data of next address.
11. If $\overline{CS}$ is low during this period, I/O pins are in the output state. Therefore, the input signals of the opposite phase to the outputs must not be applied to them.
12. In the write cycle with $\overline{OE}$ low fixed, t_{WP} must satisfy the following equation to avoid a problem of data bus contention. $t_{WP} \geq t_{DW}$ min + t_{WHZ} max

Timing Waveforms

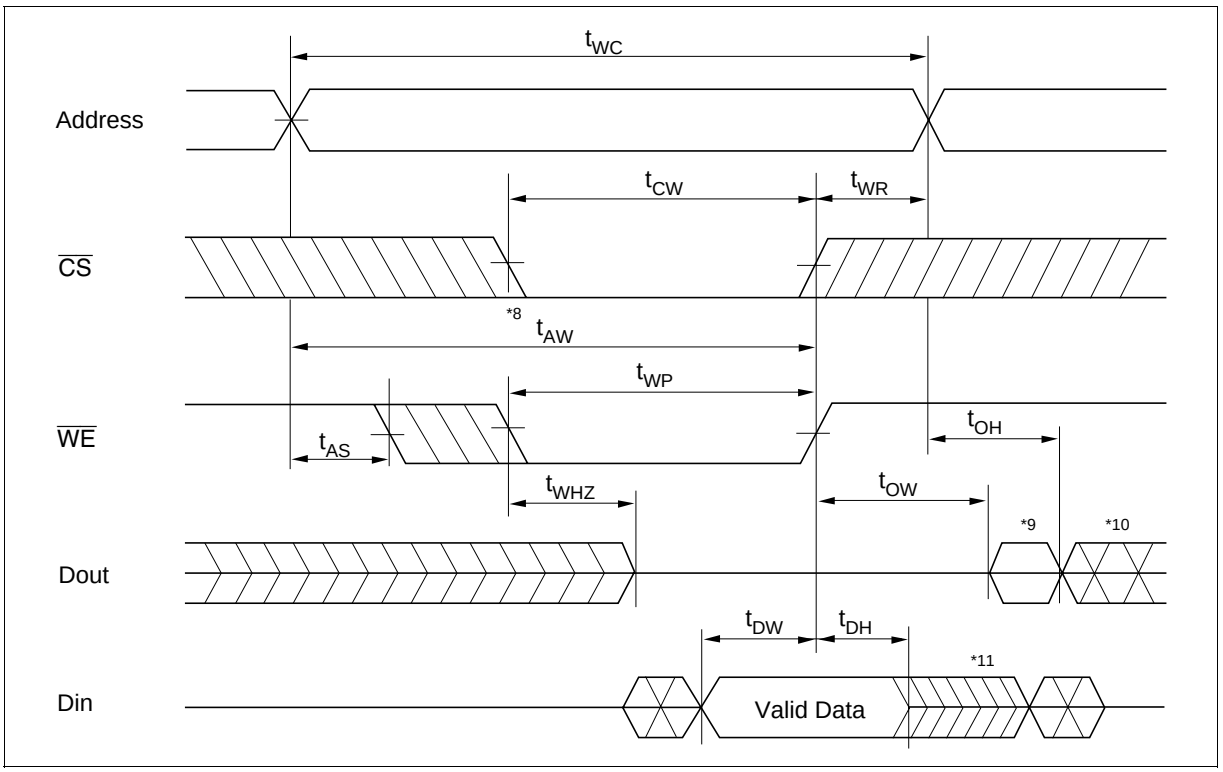
Read Timing Waveform ($\overline{WE}$ = V_{IH})



Write Timing Waveform (1) ($\overline{OE}$ Clock)



Write Timing Waveform (2) ($\overline{OE}$ Low Fixed)

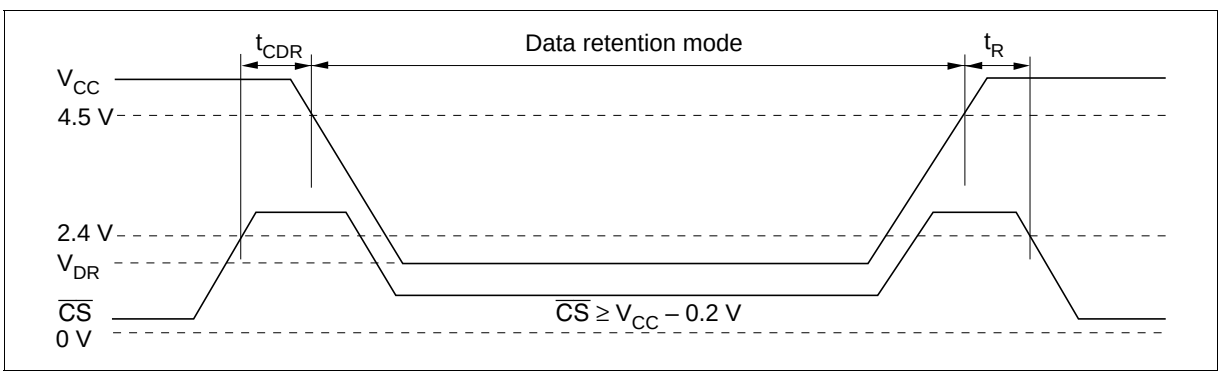


Low V_{CC} Data Retention Characteristics (Ta = –40 to +85°C)

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions*[2]
V_{CC} for data retention	V_{DR}	2	—	—	V	$\overline{CS} \geq V_{CC} - 0.2$ V, Vin ≥ 0 V
Data retention current	I_{CCDR}	—	1*[3]	50*[1]	µA	V_{CC} = 3.0 V, Vin ≥ 0 V $\overline{CS} \geq V_{CC} - 0.2$ V
Chip deselect to data retention time	t_{CDR}	0	—	—	ns	See retention waveform
Operation recovery time	t_R	t_{RC}*[4]	—	—	ns	

Notes: 1. For L-version and 20 µA (max.) at Ta = –40 to +40°C.
2. $\overline{CS}$ controls address buffer, $\overline{WE}$ buffer, $\overline{OE}$ buffer, and Din buffer. In data retention mode, Vin levels (address, $\overline{WE}$, $\overline{OE}$, I/O) can be in the high impedance state.
3. Typical values are at V_{CC} = 3.0 V, Ta = +25°C and specified loading, and not guaranteed.
4. t_{RC} = read cycle time.

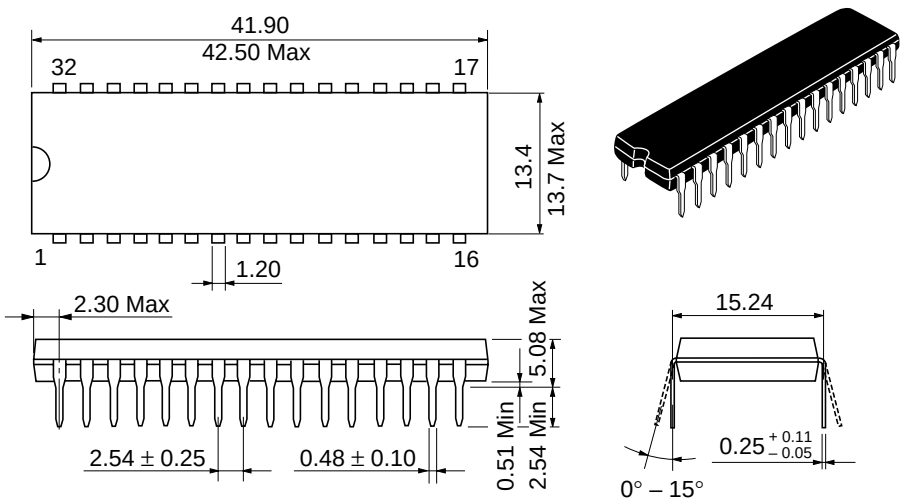
Low V_{CC} Data Retention Timing Waveform ($\overline{CS}$ Controlled)



Package Dimensions

HM628512BLPI Series (DP-32)

Unit: mm

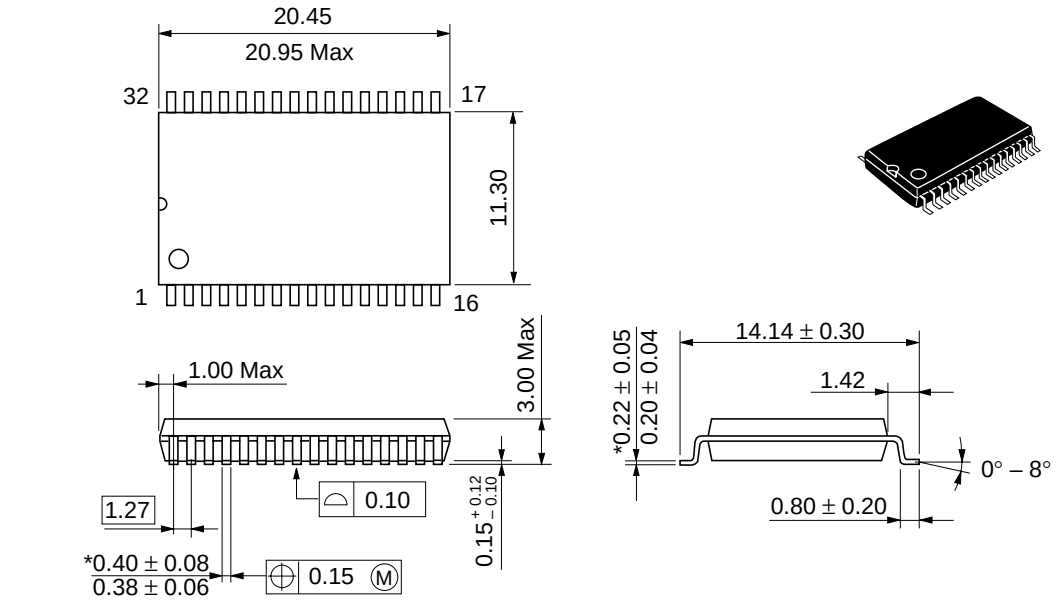


Hitachi Code	DP-32
JEDEC	—
EIAJ	Conforms
Weight (reference value)	5.1 g

Package Dimensions (cont.)

HM628512BLFPI Series (FP-32D)

Unit: mm



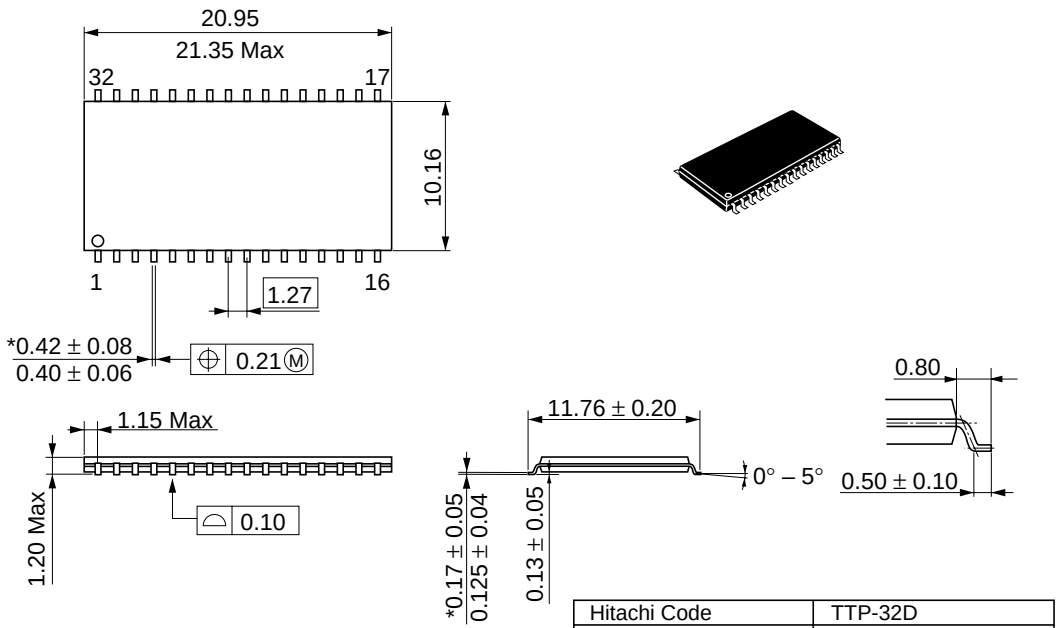
*Dimension including the plating thickness
Base material dimension

Hitachi Code	FP-32D
JEDEC	Conforms
EIAJ	—
Weight (reference value)	1.3 g

Package Dimensions (cont.)

HM628512BLTTI Series (TTP-32D)

Unit: mm



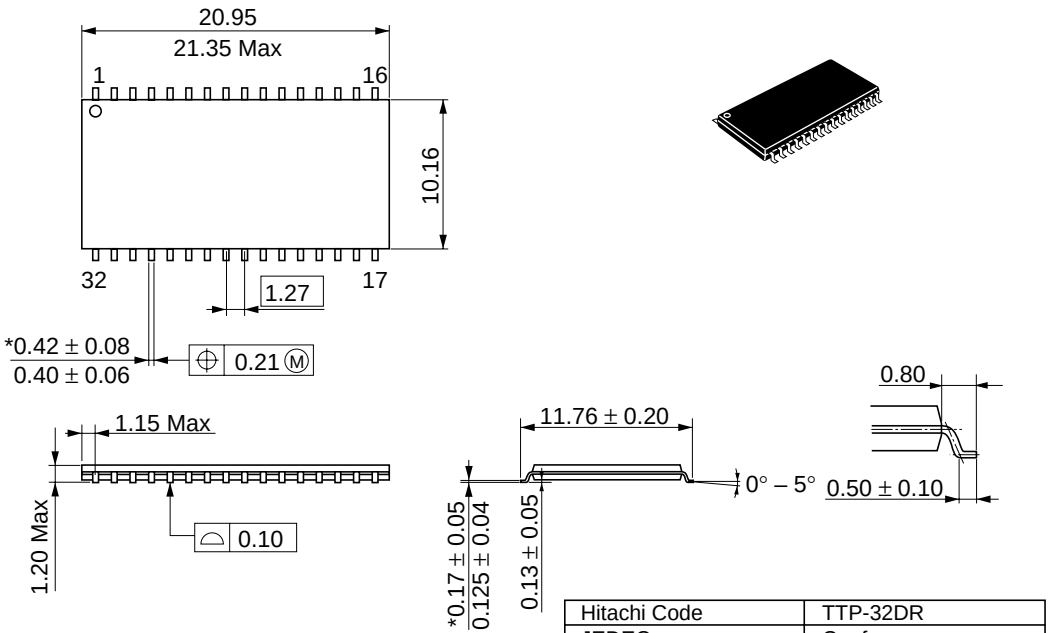
*Dimension including the plating thickness
Base material dimension

Hitachi Code	TTP-32D
JEDEC	Conforms
EIAJ	—
Weight (reference value)	0.51 g

Package Dimensions (cont.)

HM628512BLRRI Series (TTP-32DR)

Unit: mm



*Dimension including the plating thickness
Base material dimension

Hitachi Code	TTP-32DR
JEDEC	Conforms
EIAJ	—
Weight (reference value)	0.51 g

Cautions

1. Hitachi neither warrants nor grants licenses of any rights of Hitachi's or any third party's patent, copyright, trademark, or other intellectual property rights for information contained in this document. Hitachi bears no responsibility for problems that may arise with third party's rights, including intellectual property rights, in connection with use of the information contained in this document.
2. Products and product specifications may be subject to change without notice. Confirm that you have received the latest product standards or specifications before final design, purchase or use.
3. Hitachi makes every attempt to ensure that its products are of high quality and reliability. However, contact Hitachi's sales office before using the product in an application that demands especially high quality and reliability or where its failure or malfunction may directly threaten human life or cause risk of bodily injury, such as aerospace, aeronautics, nuclear power, combustion control, transportation, traffic, safety equipment or medical equipment for life support.
4. Design your application so that the product is used within the ranges guaranteed by Hitachi particularly for maximum rating, operating supply voltage range, heat radiation characteristics, installation conditions and other characteristics. Hitachi bears no responsibility for failure or damage when used beyond the guaranteed ranges. Even within the guaranteed ranges, consider normally foreseeable failure rates or failure modes in semiconductor devices and employ systemic measures such as fail-safes, so that the equipment incorporating Hitachi product does not cause bodily injury, fire or other consequential damage due to operation of the Hitachi product.
5. This product is not designed to be radiation resistant.
6. No one is permitted to reproduce or duplicate, in any form, the whole or part of this document without written approval from Hitachi.
7. Contact Hitachi's sales office for any questions regarding this document or Hitachi semiconductor products.

HITACHI

Hitachi, Ltd.
Semiconductor & Integrated Circuits.
Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100-0004, Japan
Tel: Tokyo (03) 3270-2111 Fax: (03) 3270-5109

URL
NorthAmerica : http:semiconductor.hitachi.com/
Europe : http://www.hitachi-eu.com/hel/ecg
Asia (Singapore) : http://www.has.hitachi.com.sg/grp3/sicd/index.htm
Asia (Taiwan) : http://www.hitachi.com.tw/E/Product/SICD_Frame.htm
Asia (HongKong) : http://www.hitachi.com.hk/eng/bo/grp3/index.htm
Japan : http://www.hitachi.co.jp/Sicd/indx.htm

For further information write to:

Hitachi Semiconductor
(America) Inc.
179 East Tasman Drive,
San Jose,CA 95134
Tel: <1> (408) 433-1990
Fax: <1>(408) 433-0223

Hitachi Europe GmbH
Electronic components Group
Dornacher Straße 3
D-85622 Feldkirchen, Munich
Germany
Tel: <49> (89) 9 9180-0
Fax: <49> (89) 9 29 30 00

Hitachi Europe Ltd.
Electronic Components Group.
Whitebrook Park
Lower Cookham Road
Maidenhead
Berkshire SL6 8YA, United Kingdom
Tel: <44> (1628) 585000
Fax: <44> (1628) 778322

Hitachi Asia Pte. Ltd.
16 Collyer Quay #20-00
Hitachi Tower
Singapore 049318
Tel: 535-2100
Fax: 535-1533

Hitachi Asia Ltd.
Taipei Branch Office
3F, Hung Kuo Building. No.167,
Tun-Hwa North Road, Taipei (105)
Tel: <886> (2) 2718-3666
Fax: <886> (2) 2718-8180

Hitachi Asia (Hong Kong) Ltd.
Group III (Electronic Components)
7/F., North Tower, World Finance Centre,
Harbour City, Canton Road, Tsim Sha Tsui,
Kowloon, Hong Kong
Tel: <852> (2) 735 9218
Fax: <852> (2) 730 0281
Telex: 40815 HITEC HX

Revision Record

Rev.	Date	Contents of Modification	Drawn by	Approved by
0.0	Nov. 2, 1998	Initial issue	K. Imato	K. Imato
0.1	Dec. 14, 1998	DC Characteristics I_{CC1}: —/40/60 mA to —/45/70 mA I_{SB1} max: 40 µA to 100 µA Low V_{CC} Data Retention Characteristics I_{CCDR} max: 20 µA to 50 µA t_R min: 5 ms to t_{RC} ms Change of note1 Addition of note4	S. Kunito	K. Imato
1.0	Jul. 2, 1999	Deletion of Preliminary	S. Kunito	K. Imato
2.0	Aug. 24, 1999	Low V_{CC} Data Retention Characteristics Correct error: t_R unit ms to ns		