

SN74AVCBH164245
16-BIT DUAL-SUPPLY BUS TRANSCEIVER
WITH CONFIGURABLE VOLTAGE TRANSLATION AND 3-STATE OUTPUTS

SCES393A – JUNE 2002 – REVISED MAY 2004

- Member of the Texas Instruments Widebus™ Family
- DOC™ Circuitry Dynamically Changes Output Impedance, Resulting in Noise Reduction Without Speed Degradation
- Dynamic Drive Capability Is Equivalent to Standard Outputs With I_{OH} and I_{OL} of ± 24 mA at 2.5-V V_{CC}
- Control Inputs V_{IH}/V_{IL} Levels are Referenced to V_{CCB} Voltage
- If Either V_{CC} Input Is at GND, Both Ports Are in the High-Impedance State
- Overvoltage-Tolerant Inputs/Outputs Allow Mixed-Voltage-Mode Data Communications
- I_{off} Supports Partial-Power-Down Mode Operation
- Fully Configurable Dual-Rail Design Allows Each Port to Operate Over the Full 1.4-V to 3.6-V Power-Supply Range
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)

description/ordering information

This 16-bit (dual-octal) noninverting bus transceiver uses two separate configurable power-supply rails. The A-port is designed to track V_{CCA} . V_{CCA} accepts any supply voltage from 1.4 V to 3.6 V. The B-port is designed to track V_{CCB} . V_{CCB} accepts any supply voltage from 1.4 V to 3.6 V. This allows for universal low-voltage bidirectional translation between any of the 1.5-V, 1.8-V, 2.5-V, and 3.3-V voltage nodes.

The SN74AVCBH164245 is designed for asynchronous communication between data buses. The device transmits data from the A bus to the B bus or from the B bus to the A bus, depending on the logic level at the direction-control (DIR) input. The output-enable (\overline{OE}) input can be used to disable the outputs so the buses are effectively isolated.

The SN74AVCBH164245 is designed so that the control pins (1DIR, 2DIR, 1 \overline{OE} , and 2 \overline{OE}) are supplied by V_{CCB} .

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level. Use of pullup or pulldown resistors with the bus-hold circuitry is not recommended.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CCB} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

This device is fully specified for partial-power-down applications using I_{off} . The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down. If either V_{CC} input is at GND, both ports are in the high-impedance state.

ORDERING INFORMATION

TA	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 85°C	TSSOP – DGG	Tape and reel	SN74AVCBH164245GR	AVCBH164245
	TVSOP – DGV	Tape and reel	SN74AVCBH164245VR	WBH4245
	VFBGA – GQL	Tape and reel	SN74AVCBH164245KR	WBH4245

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



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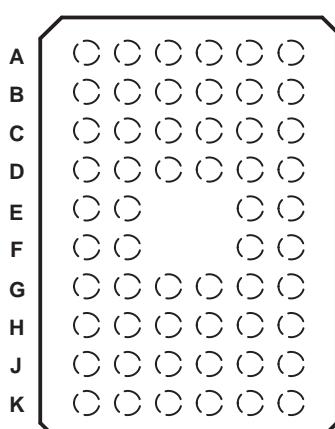
terminal assignments

**DGG OR DGV PACKAGE
(TOP VIEW)**

1DIR	1	48	1OE
1B1	2	47	1A1
1B2	3	46	1A2
GND	4	45	GND
1B3	5	44	1A3
1B4	6	43	1A4
VCCB	7	42	VCCA
1B5	8	41	1A5
1B6	9	40	1A6
GND	10	39	GND
1B7	11	38	1A7
1B8	12	37	1A8
2B1	13	36	2A1
2B2	14	35	2A2
GND	15	34	GND
2B3	16	33	2A3
2B4	17	32	2A4
VCCB	18	31	VCCA
2B5	19	30	2A5
2B6	20	29	2A6
GND	21	28	GND
2B7	22	27	2A7
2B8	23	26	2A8
2DIR	24	25	2OE

**GQL PACKAGE
(TOP VIEW)**

1 2 3 4 5 6



terminal assignments

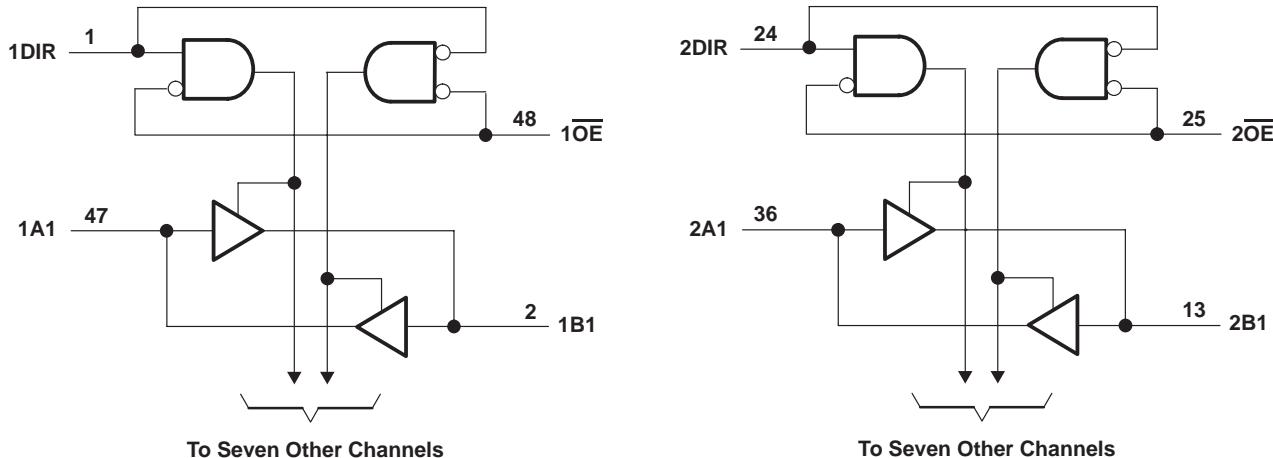
	1	2	3	4	5	6
A	1DIR	NC	NC	NC	NC	1OE
B	1B2	1B1	GND	GND	1A1	1A2
C	1B4	1B3	VCCB	VCCA	1A3	1A4
D	1B6	1B5	GND	GND	1A5	1A6
E	1B8	1B7			1A7	1A8
F	2B1	2B2			2A2	2A1
G	2B3	2B4	GND	GND	2A4	2A3
H	2B5	2B6	VCCB	VCCA	2A6	2A5
J	2B7	2B8	GND	GND	2A8	2A7
K	2DIR	NC	NC	NC	NC	2OE

NC – No internal connection

FUNCTION TABLE (each 8-bit section)

INPUTS		OPERATION
OE	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

logic diagram (positive logic)



Pin numbers shown are for the DGG and DGV packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
 2. The output positive-voltage rating may be exceeded up to 4.6 V maximum if the output current rating is observed.
 3. The package thermal impedance is calculated in accordance with JESD 51-7.

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recommended operating conditions (see Notes 4 through 6)

		V _{CCI}	V _{CCO}	MIN	MAX	UNIT	
V _{CCA}	Supply voltage			1.4	3.6	V	
V _{CCB}	Supply voltage			1.4	3.6	V	
V _{IH}	High-level input voltage	Data inputs	1.4 V to 1.95 V	V _{CCI} × 0.65		V	
			1.95 V to 2.7 V	1.7			
			2.7 V to 3.6 V	2			
V _{IL}	Low-level input voltage	Data inputs	1.4 V to 1.95 V	V _{CCI} × 0.35		V	
			1.95 V to 2.7 V	0.7			
			2.7 V to 3.6 V	0.8			
V _{IH}	High-level input voltage	Control inputs (Referenced to V _{CCB})	1.4 V to 1.95 V	V _{CCB} × 0.65		V	
			1.95 V to 2.7 V	1.7			
			2.7 V to 3.6 V	2			
V _{IL}	Low-level input voltage	Control inputs (Referenced to V _{CCB})	1.4 V to 1.95 V	V _{CCB} × 0.35		V	
			1.95 V to 2.7 V	0.7			
			2.7 V to 3.6 V	0.8			
V _I	Input voltage			0	3.6	V	
V _O	Output voltage	Active state		0	V _{CCO}	V	
		3-state		0	3.6		
I _{OH}	High-level output current		1.4 V to 1.6 V	-2		mA	
			1.65 V to 1.95 V	-4			
			2.3 V to 2.7 V	-8			
			3 V to 3.6 V	-12			
I _{OL}	Low-level output current		1.4 V to 1.6 V	2		mA	
			1.65 V to 1.95 V	4			
			2.3 V to 2.7 V	8			
			3 V to 3.6 V	12			
Δt/Δv	Input transition rise or fall rate			5		ns/V	
T _A	Operating free-air temperature			-40	85	°C	

NOTES: 4. V_{CCI} is the V_{CC} associated with the data input port.5. V_{CCO} is the V_{CC} associated with the output port.6. All unused data inputs of the device must be held at V_{CCI} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Note 7)

PARAMETER		TEST CONDITIONS	V _{CCA}	V _{CCB}	MIN	TYP†	MAX	UNIT
V _{OH}	I _{OH} = -100 µA	V _I = V _{IH}	1.4 V to 3.6 V	1.4 V to 3.6 V	V _{CCO} –0.2 V			V
	I _{OH} = -2 mA	V _I = V _{IH}	1.4 V	1.4 V	1.05			
	I _{OH} = -4 mA	V _I = V _{IH}	1.65 V	1.65 V	1.2			
	I _{OH} = -8 mA	V _I = V _{IH}	2.3 V	2.3 V	1.75			
	I _{OH} = -12 mA	V _I = V _{IH}	3 V	3 V	2.3			
V _{OL}	I _{OH} = 100 µA	V _I = V _{IL}	1.4 V to 3.6 V	1.4 V to 3.6 V		0.2		V
	I _{OH} = 2 mA	V _I = V _{IL}	1.4 V	1.4 V		0.35		
	I _{OH} = 4 mA	V _I = V _{IL}	1.65 V	1.65 V		0.45		
	I _{OH} = 8 mA	V _I = V _{IL}	2.3 V	2.3 V		0.55		
	I _{OH} = 12 mA	V _I = V _{IL}	3 V	3 V		0.7		
I _I	Control inputs	V _I = V _{CCB} or GND	1.4 V to 3.6 V	3.6 V		±2.5		µA
I _{BHL} ‡	V _I = 0.49 V		1.4 V	1.4 V	11			µA
	V _I = 0.57 V		1.65 V	1.65 V	25			
	V _I = 0.7 V		2.3 V	2.3 V	45			
	V _I = 0.8 V		3 V	3 V	75			
I _{BHH} §	V _I = 0.91 V		1.4 V	1.4 V	-11			µA
	V _I = 1.07 V		1.65 V	1.65 V	-25			
	V _I = 1.7 V		2.3 V	2.3 V	-45			
	V _I = 2 V		3 V	3 V	-75			
I _{BHLO} ¶	V _I = 0 to V _{CC}	1.6 V	1.6 V	100				µA
		1.95 V	1.95 V	200				
		2.7 V	2.7 V	300				
		3.6 V	3.6 V	525				
I _{BHHO} #	V _I = 0 to V _{CC}	1.6 V	1.6 V	-100				µA
		1.95 V	1.95 V	-200				
		2.7 V	2.7 V	-300				
		3.6 V	3.6 V	-525				
I _{off}	A port	V _I or V _O = 0 to 3.6 V	0 V	0 to 3.6 V		±10		µA
	B port		0 to 3.6 V	0 V		±10		

† All typical values are at T_A = 25°C.

‡ The bus-hold circuit can sink at least the minimum low sustaining current at V_{IL} max. I_{BHL} should be measured after lowering V_{IN} to GND and then raising it to V_{IL} max.

§ The bus-hold circuit can source at least the minimum high sustaining current at V_{IH} min. I_{BHH} should be measured after raising V_{IN} to V_{CC} and then lowering it to V_{IH} min.

¶ An external driver must source at least I_{BHLO} to switch this node from low to high.

An external driver must sink at least I_{BHHO} to switch this node from high to low.

NOTE 7: V_{CCO} is the V_{CC} associated with the output port.

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**electrical characteristics over recommended operating free-air temperature range (continued)
(unless otherwise noted) (see Notes 8 and 9)**

PARAMETER		TEST CONDITIONS		V _{CCA}	V _{CCB}	MIN	TYP†	MAX	UNIT	
I _{OZ} ‡	A or B ports	V _O = V _{CCO} or GND, V _I = V _{CCI} or GND	OE = V _{IH}	3.6 V	3.6 V			±12.5	µA	
	B port		OE = don't care	0 V	3.6 V			±12.5		
	A port			3.6 V	0 V			±12.5		
I _{CCA}		V _I = V _{CCI} or GND, I _O = 0		1.6 V	1.6 V			20	µA	
				1.95 V	1.95 V			20		
				2.7 V	2.7 V			30		
				0 V	3.6 V			-40		
				3.6 V	0 V			40		
				3.6 V	3.6 V			40		
I _{CCB}		V _I = V _{CCI} or GND, I _O = 0		1.6 V	1.6 V			20	µA	
				1.95 V	1.95 V			20		
				2.7 V	2.7 V			30		
				0 V	3.6 V			40		
				3.6 V	0 V			-40		
				3.6 V	3.6 V			40		
C _i	Control inputs	V _I = 3.3 V or GND		3.3 V	3.3 V			4	pF	
C _{io}	A or B ports	V _O = 3.3 V or GND		3.3 V	3.3 V			5	pF	

† All typical values are at T_A = 25°C.‡ For I/O ports, the parameter I_{OZ} includes the input leakage current.NOTES: 8. V_{CCO} is the V_{CC} associated with the output port.9. V_{CCI} is the V_{CC} associated with the input port.

**switching characteristics over recommended operating free-air temperature range,
V_{CCA} = 1.5 V ± 0.1 V (see Figure 2)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CCB} = 1.5 V ± 0.1 V		V _{CCB} = 1.8 V ± 0.15 V		V _{CCB} = 2.5 V ± 0.2 V		V _{CCB} = 3.3 V ± 0.3 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t _{pd}	A	B	1.7	6.7	1.9	6.3	1.8	5.5	1.7	5.8	ns
	B	A	1.8	6.8	2.2	7.4	2.1	7.6	2.1	7.3	
t _{en}	OE	A	2.5	8.4	2.4	7.4	2.1	5.2	1.9	4.2	ns
	OE	B	2.1	9	2.9	9.8	3.2	10	3	9.8	
t _{dis}	OE	A	2.2	6.9	2.3	6.1	1.3	3.6	1.3	3	ns
	OE	B	2.1	7.1	2.3	6.4	1.7	5.1	1.6	4.8	

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switching characteristics over recommended operating free-air temperature range,
 $V_{CCA} = 1.8 \text{ V} \pm 0.15 \text{ V}$ (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CCB} = 1.5 \text{ V} \pm 0.1 \text{ V}$		$V_{CCB} = 1.8 \text{ V} \pm 0.15 \text{ V}$		$V_{CCB} = 2.5 \text{ V} \pm 0.2 \text{ V}$		$V_{CCB} = 3.3 \text{ V} \pm 0.3 \text{ V}$		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A	B	1.7	6.4	1.8	6	1.7	4.7	1.6	4.3	ns
	B	A	1.4	5.5	1.8	6	1.8	5.8	1.8	5.5	
t_{en}	\overline{OE}	A	2.6	8.5	2.5	7.5	2.2	5.3	1.9	4.2	ns
	\overline{OE}	B	1.8	7.6	2.6	7.7	2.6	7.6	2.6	7.4	
t_{dis}	\overline{OE}	A	2.3	7	2.3	6.1	1.3	3.6	1.3	3	ns
	\overline{OE}	B	1.8	7	2.5	6.3	1.8	4.7	1.7	4.4	

switching characteristics over recommended operating free-air temperature range,
 $V_{CCA} = 2.5 \text{ V} \pm 0.2 \text{ V}$ (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CCB} = 1.5 \text{ V} \pm 0.1 \text{ V}$		$V_{CCB} = 1.8 \text{ V} \pm 0.15 \text{ V}$		$V_{CCB} = 2.5 \text{ V} \pm 0.2 \text{ V}$		$V_{CCB} = 3.3 \text{ V} \pm 0.3 \text{ V}$		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A	B	1.6	6	1.8	5.6	1.5	4	1.4	3.4	ns
	B	A	1.3	4.6	1.7	4.4	1.5	4	1.4	3.7	
t_{en}	\overline{OE}	A	3.1	8.5	2.5	7.5	2.2	5.3	1.9	4.2	ns
	\overline{OE}	B	1.7	5.7	2.2	5.5	2.2	5.3	2.2	5.1	
t_{dis}	\overline{OE}	A	2.4	7	3	6.1	1.4	3.6	1.2	3	ns
	\overline{OE}	B	1.2	5.8	1.9	5	1.4	3.6	1.3	3.3	

switching characteristics over recommended operating free-air temperature range,
 $V_{CCA} = 3.3 \text{ V} \pm 0.3 \text{ V}$ (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CCB} = 1.5 \text{ V} \pm 0.1 \text{ V}$		$V_{CCB} = 1.8 \text{ V} \pm 0.15 \text{ V}$		$V_{CCB} = 2.5 \text{ V} \pm 0.2 \text{ V}$		$V_{CCB} = 3.3 \text{ V} \pm 0.3 \text{ V}$		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A	B	1.5	5.9	1.7	5.4	1.5	3.7	1.4	3.1	ns
	B	A	1.3	4.5	1.6	3.8	1.5	3.3	1.4	3.1	
t_{en}	\overline{OE}	A	2.6	8.3	2.5	7.4	2.2	5.2	1.9	4.1	ns
	\overline{OE}	B	1.6	4.9	2	4.5	2	4.3	1.9	4.1	
t_{dis}	\overline{OE}	A	2.3	7	3	6	1.3	3.5	1.2	3.5	ns
	\overline{OE}	B	1.3	6.9	2.1	5.5	1.6	3.8	1.5	3.5	

operating characteristics, V_{CCA} and $V_{CCB} = 3.3$ V, $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pdA} (V_{CCA})	Power dissipation capacitance per transceiver, A port input, B port output	Outputs enabled	14 7 20 7	pF
		Outputs disabled		
	Power dissipation capacitance per transceiver, B port input, A port output	Outputs enabled		
		Outputs disabled		
C_{pdB} (V_{CCB})	Power dissipation capacitance per transceiver, A port input, B port output	Outputs enabled	20 7 14 7	pF
		Outputs disabled		
	Power dissipation capacitance per transceiver, B port input, A port output	Outputs enabled		
		Outputs disabled		

output description

The DOC™ circuitry is implemented, which, during the transition, initially lowers the output impedance to effectively drive the load and, subsequently, raises the impedance to reduce noise. Figure 1 shows typical V_{OL} vs I_{OL} and V_{OH} vs I_{OH} curves to illustrate the output impedance and drive capability of the circuit. At the beginning of the signal transition, the DOC circuit provides a maximum dynamic drive that is equivalent to a high-drive standard-output device. For more information, refer to the TI application reports, *AVC Logic Family Technology and Applications*, literature number SCEA006, and *Dynamic Output Control (DOC™) Circuitry Technology and Applications*, literature number SCEA009.

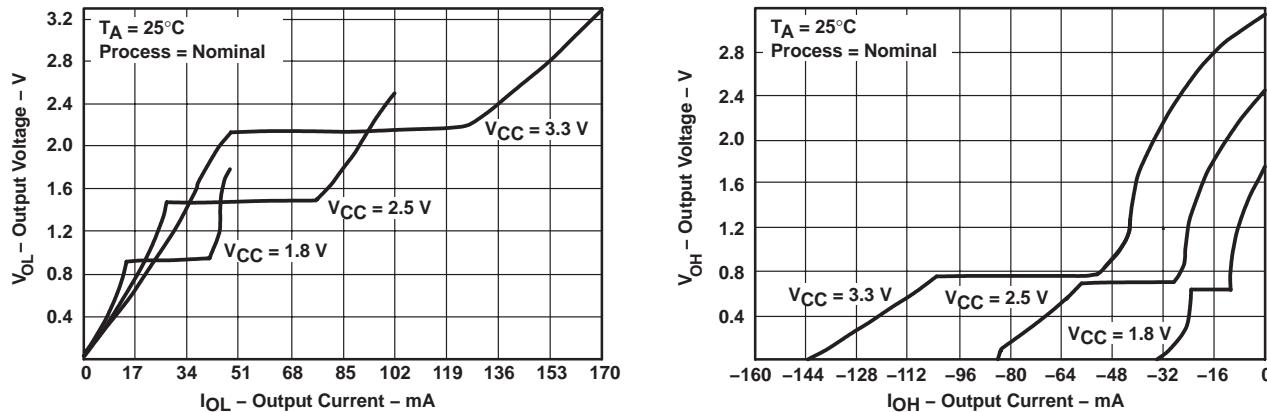
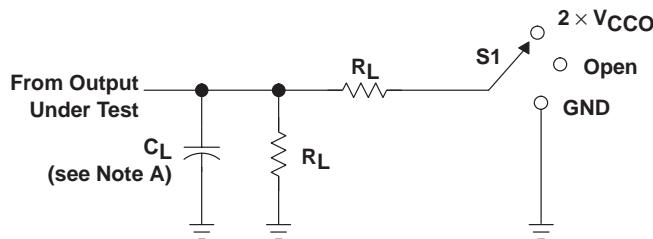


Figure 1. Typical Output Voltage vs Output Current

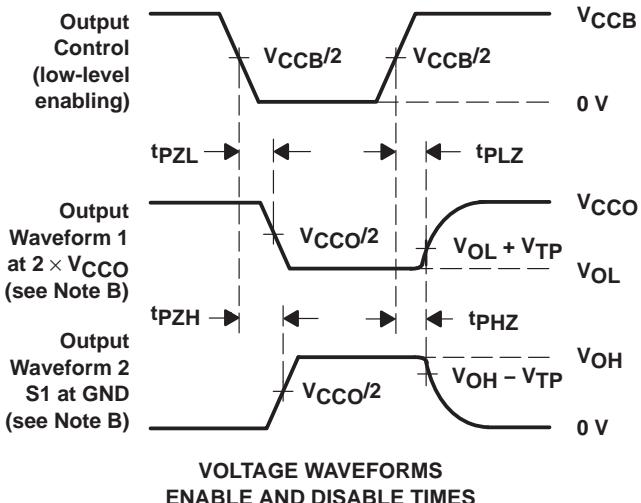
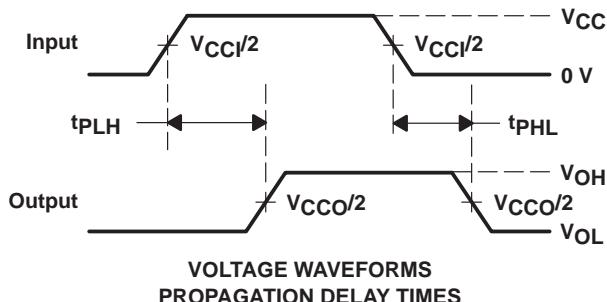
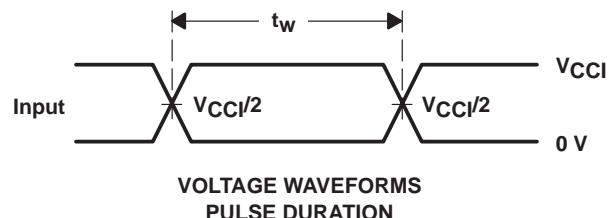
PARAMETER MEASUREMENT INFORMATION



TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	$2 \times V_{CCO}$
t_{PHZ}/t_{PZH}	GND

LOAD CIRCUIT

V_{CCO}	C_L	R_L	V_{TP}
$1.5 \text{ V} \pm 0.1 \text{ V}$	15 pF	2 k Ω	0.1 V
$1.8 \text{ V} \pm 0.15 \text{ V}$	30 pF	1 k Ω	0.15 V
$2.5 \text{ V} \pm 0.2 \text{ V}$	30 pF	500 Ω	0.15 V
$3.3 \text{ V} \pm 0.3 \text{ V}$	30 pF	500 Ω	0.3 V



NOTES:

- A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $dv/dt \geq 1 \text{ V/ns}$, $dv/dt \geq 1 \text{ V/ns}$.
- D. The outputs are measured one at a time, with one transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
- F. t_{PZL} and t_{PZH} are the same as t_{en} .
- G. t_{PLH} and t_{PHL} are the same as t_{pd} .
- H. V_{CCI} is the V_{CC} associated with the input port.
- I. V_{CCO} is the V_{CC} associated with the output port.

Figure 2. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
SN74AVCBH164245G	PREVIEW	TSSOP	DGG	48	40	Pb-Free (RoHS)	CU NIPDAU	Level-1-250C-UNLIM
SN74AVCBH164245GR	ACTIVE	TSSOP	DGG	48	2000	Pb-Free (RoHS)	CU NIPDAU	Level-1-250C-UNLIM
SN74AVCBH164245KR	ACTIVE	VFBGA	GQL	56	1000	None	SNPB	Level-1-240C-UNLIM
SN74AVCBH164245VR	ACTIVE	TVSOP	DGV	48	2000	Pb-Free (RoHS)	CU NIPDAU	Level-1-250C-UNLIM

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - May not be currently available - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

None: Not yet available Lead (Pb-Free).

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Green (RoHS & no Sb/Br): TI defines "Green" to mean "Pb-Free" and in addition, uses package materials that do not contain halogens, including bromine (Br) or antimony (Sb) above 0.1% of total product weight.

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDECindustry standard classifications, and peak solder temperature.

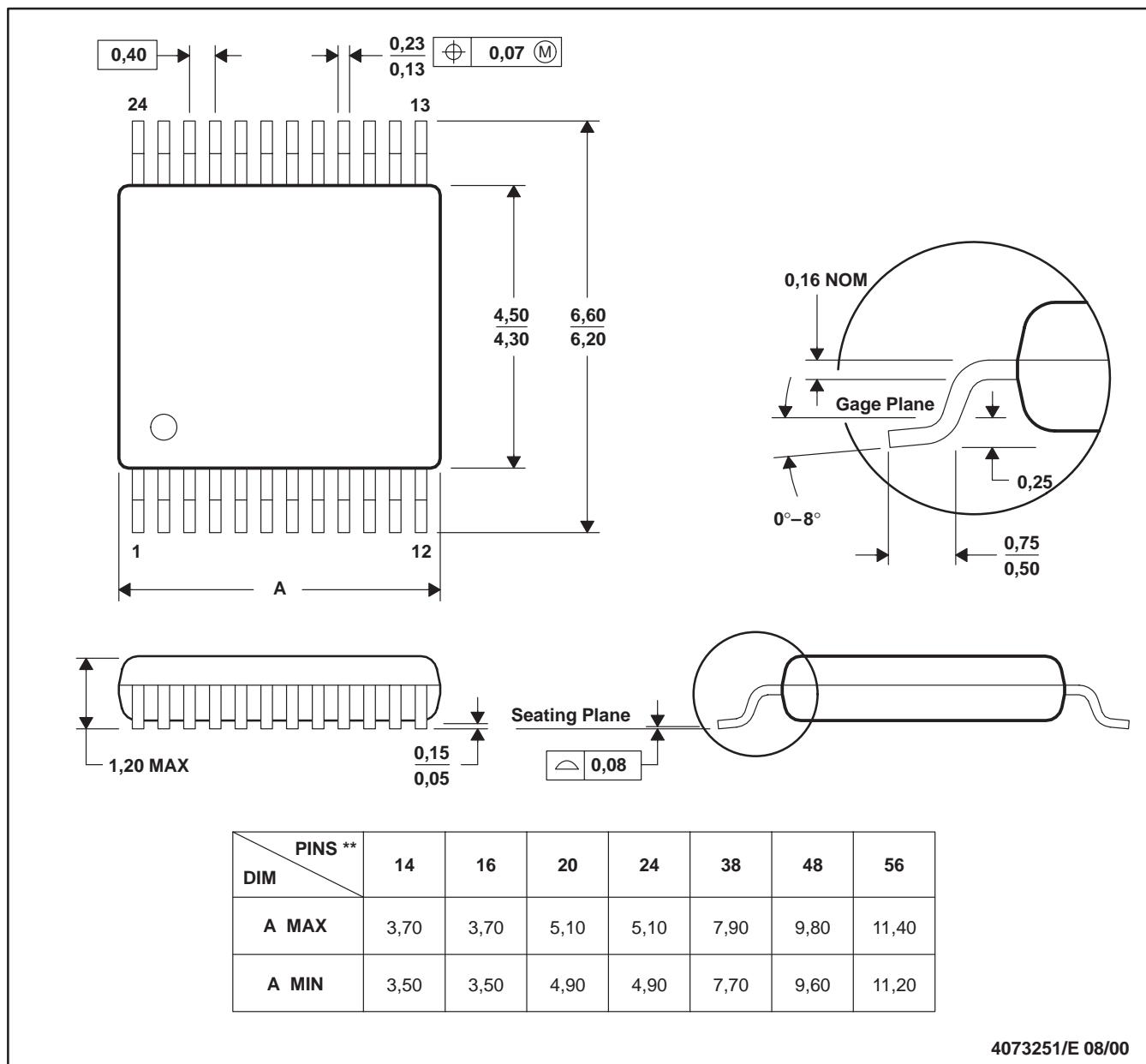
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DGV (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

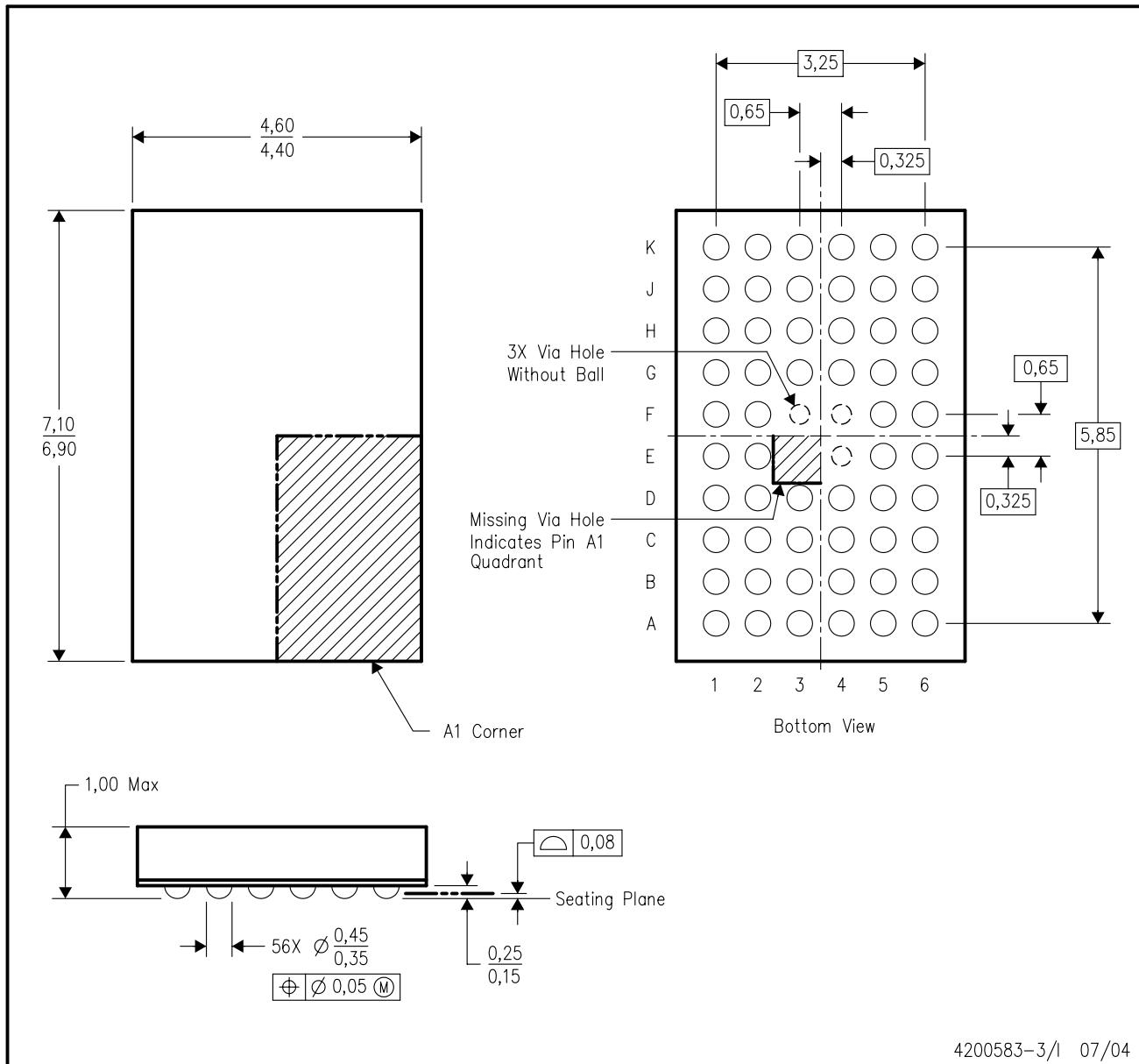
24 PINS SHOWN



NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
 D. Falls within JEDEC: 24/48 Pins – MO-153
 14/16/20/56 Pins – MO-194

GQL (R-PBGA-N56)

PLASTIC BALL GRID ARRAY



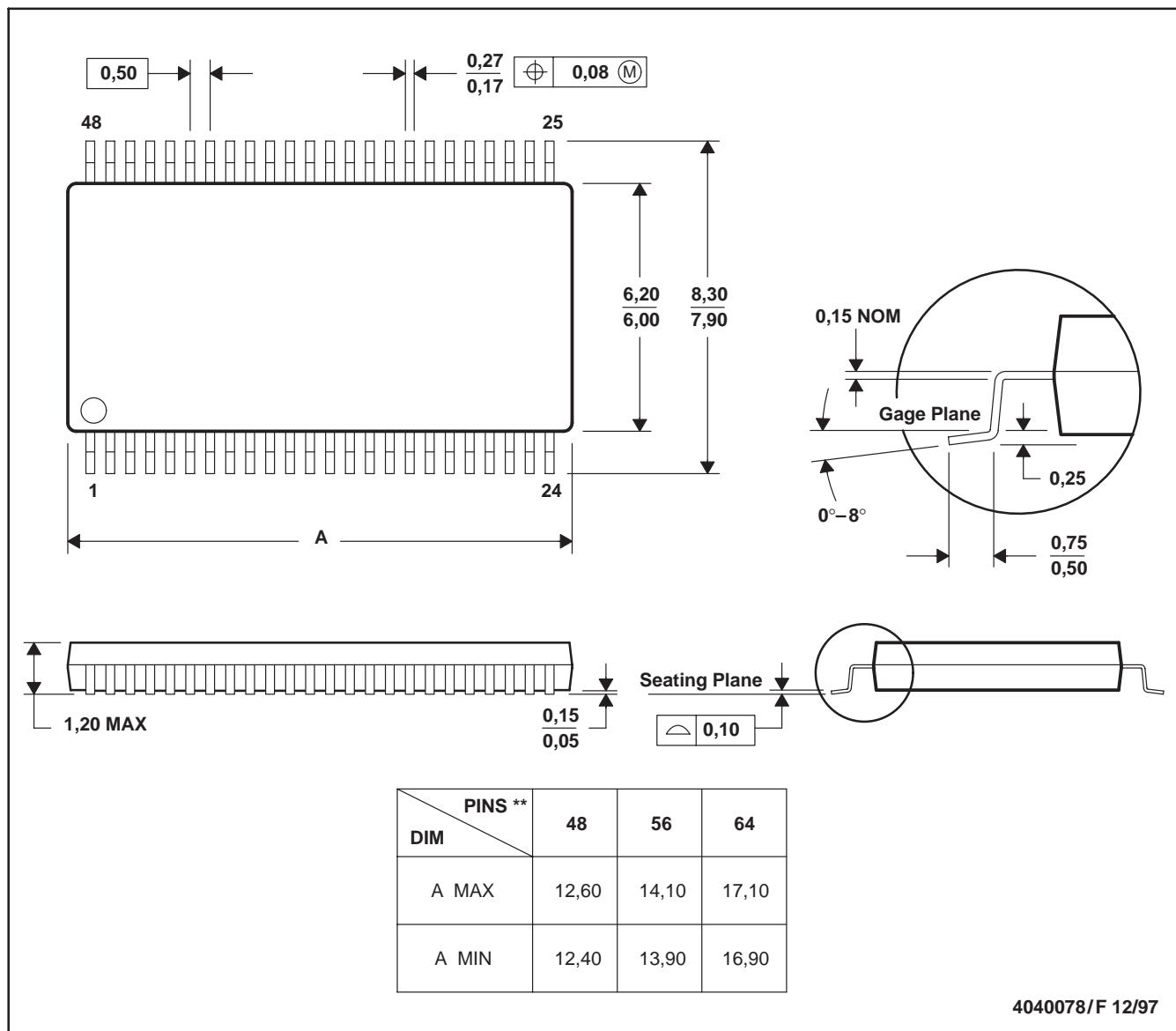
NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MO-225 variation BA.
D. This package is tin-lead (SnPb). Refer to the 56 ZQL package (drawing 4204437) for lead-free.

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DGG (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

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