LINEAR IMAGE SENSOR IC FOR CONTACT IMAGE SENSOR

S-8660AWI

The S-8660AWI is a linear image sensor IC suitable for multichip-type contact color image sensors that use an RGB LED light source and have a scanning density of 600 dpi.
The scanning length of this IC is 12.2 mm. The S-8660AWI outputs image signals one after another as analog signals that are received by a 288-dot photoreceptor. The signals pass through an amplifier and synchronized with clock signals.

■ Features

- Resolution: 600 dpi (DS: = N.C. or = VDD)
  ... The resolution can be changed to 300 dpi (DS: = GND)
- Scanning length: 12.2 mm
  ... Various sizes of paper can be scanned by simply changing the number of chips aligned in line.
- High frequency: fck = 2 MHz
- Two input signals: SI (FS) and CLK
  ... Only two input signals, start and clock, make scanning easy.
- High picture quality: Photodiode photoreceptor (picture element)
- Low power consumption: 5 V single power supply and CMOS scanning circuit

■ Pin Description

Table 1

Pin No.	Symbol	Name	Function
1	SI	Start signal input pin	Inputs the start signal for the scanning circuit. →Outputs analog image signals at the 64th and later clock pulses after SI is input. CMOS input (Logic level is TTL-level)
2	FS	Image scanning signal input pin	Inputs the same signal as SI for the first chip to all chips. →Outputs quasi-dark signals only for the first chip from the 32nd to 63rd clock pulses after SI is input. CMOS input (Logic level is TTL-level)
3	CLK	Clock pulse input pin	Inputs clock pulses for the scanning circuit. CMOS input (Logic level is TTL-level)
4	DS	Resolution selection pin	● Connected to VDD or not connected →Scanning at 600 dpi Outputs signals of all pixels one after another in synchronization with 288 clock pulses. ● Connected to GND →Scanning at 300 dpi Outputs signals of odd-number pixels one after another in synchronization with 144 clock pulses. CMOS input (Logic level is TTL-level) Built-in Pull-up resistor
5	GND	Ground pin	Usually connected to 0 V
6	VDD	Power supply pin	Usually connected to 5 V. A 47 μF capacitor is connected between the VDD and GND pins.
7	SIG	Analog image signal output pin	Load capacitance ≤ 50 pF
8	VREF	Reference voltage output pin	A 47 μF capacitor is connected between the VREF and GND pins.
9	GND	Ground pin	Usually connected to 0 V
10	LS	Quasi-dark signal output selection pin	● GND → Outputs quasi-dark signals for 12 pixels after the SIG signal for the last pixel is output. ● Not connected → No quasi-dark signals are output. CMOS input (Logic level is TTL-level) Built-in Pull-up resistor
11	SO	Start signal output pin	Usually connected to the SI pin of the next chip.

■ Block Diagram

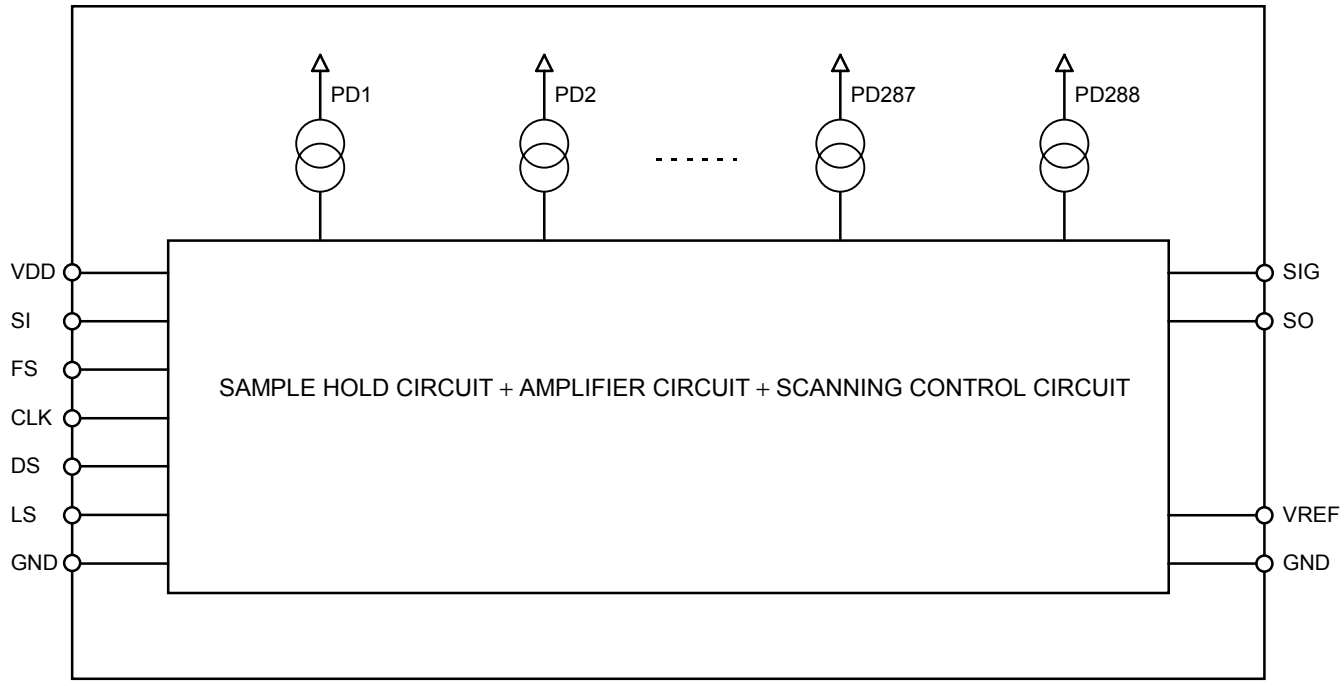

Figure 1

■ Timing Chart

(a) 600 dpi (DS: = N.C. or VDD)

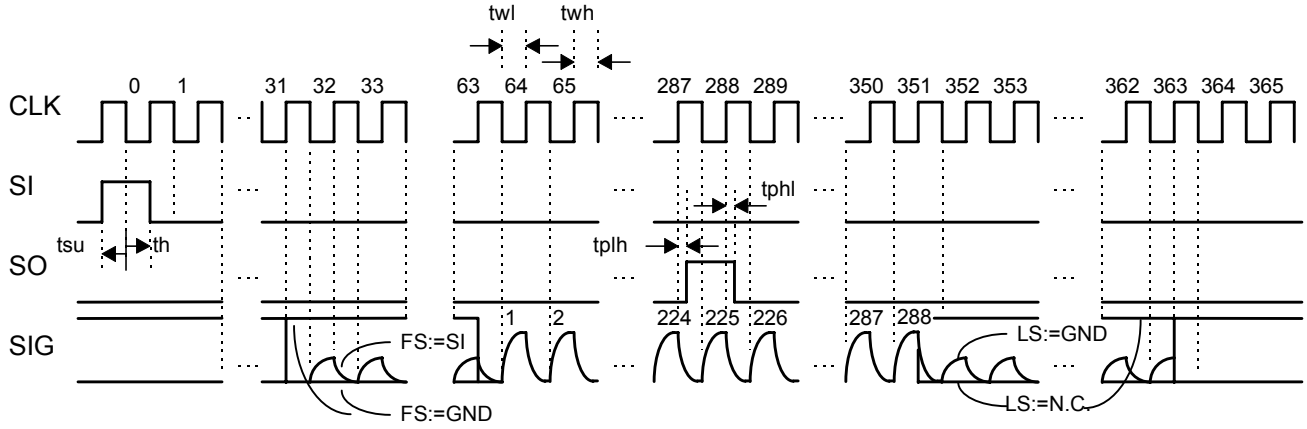

Figure 2a

(b) 300 dpi (DS: = GND)

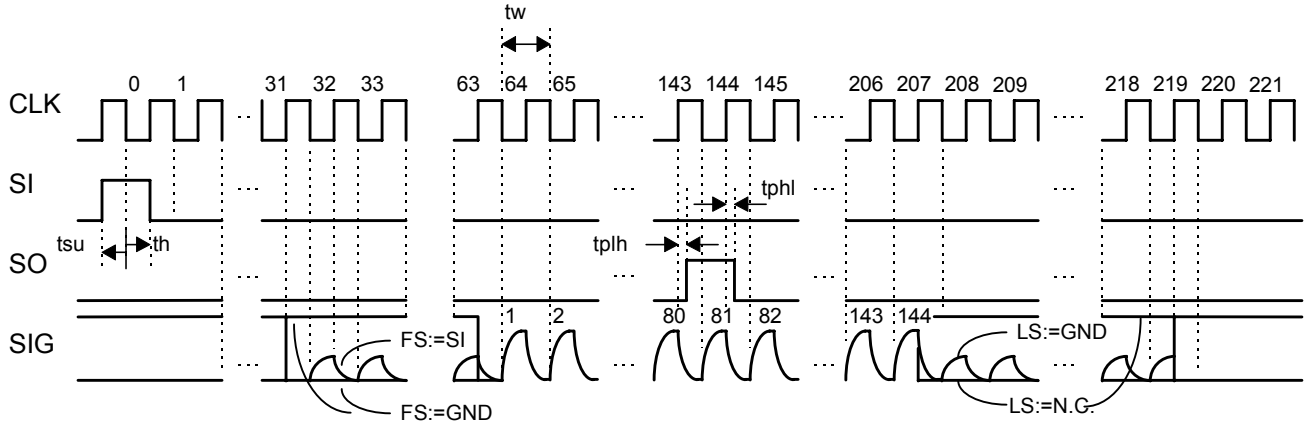

Figure 2b

(c) LED

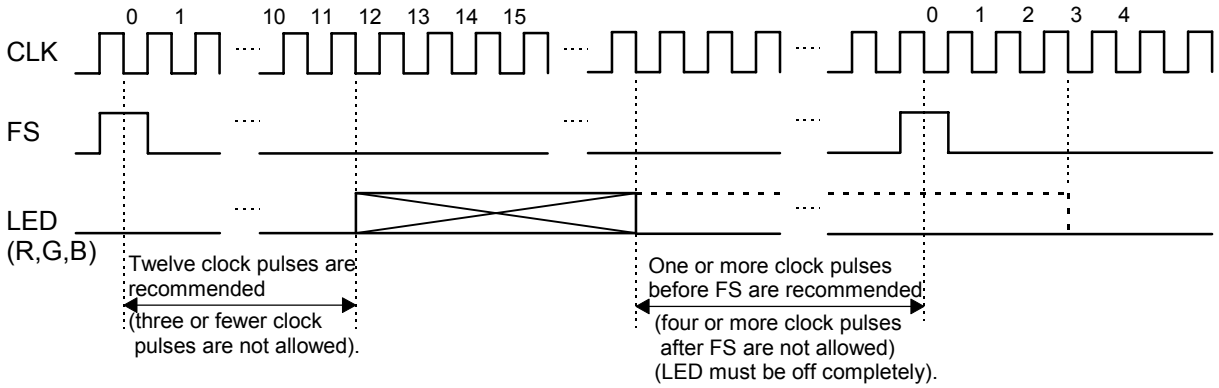

Figure 2c

(d) Color SIG

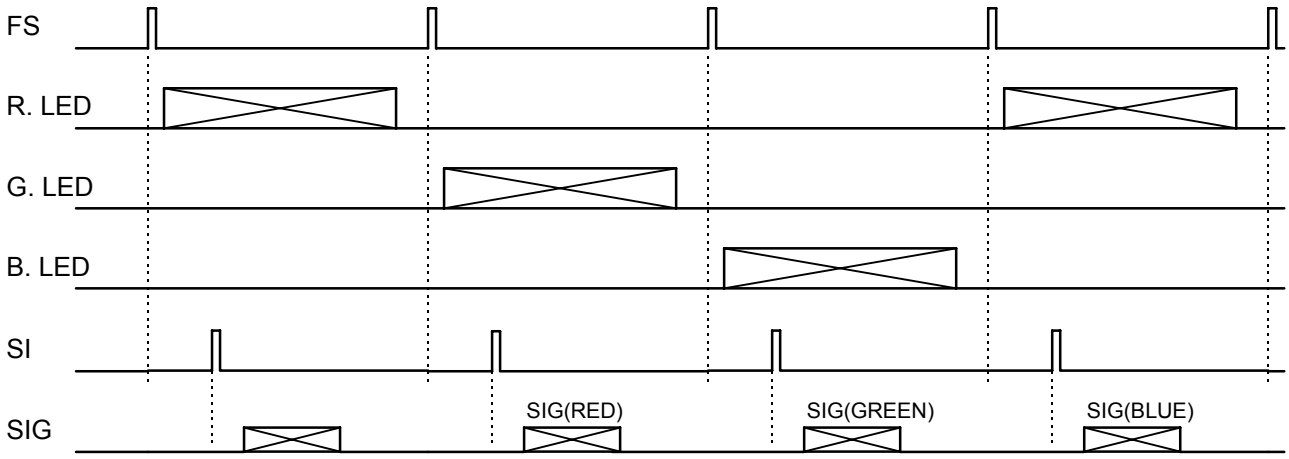

Figure 2d

(e) Vdummy, FS

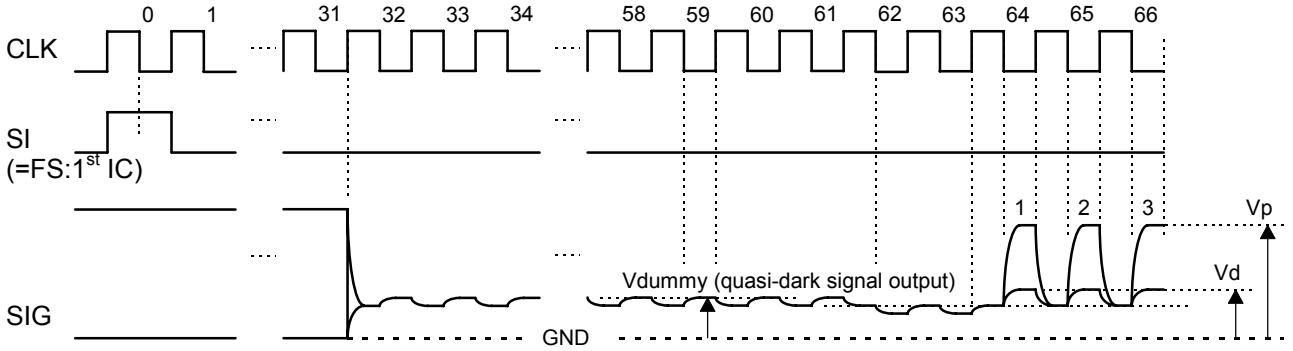

Figure 2e

Notes:
1. Vdummy signals are provided between the 32nd and the 61st clock pulses of the 1st IC. Do not use the dummy signals of the 62nd and 63rd clock pulses because the difference from Vd is large.
2. Vdummy signals are also provided during the 12 clock signals just after the output of image signal of the last bit of the last IC. (LS: GND)
3. The FS signal should be entered at the 24th or later clock signal after the output of the image signal of the last bit of the last IC. The FS signal input before the 23rd clock pulse is prohibited.

■ Absolute Maximum Ratings

Table 2

Parameter	Symbol	Condition	Rating	Unit
Power supply voltage	V_{DD}	VDD-GND	-0.4 to +7.0	V
Input voltage	V_{IN}	SI,FS,CLK,DS,LS	-0.4 to V_{DD}+0.4	V
Output voltage	V_{OUT}	SIG,VREF,SO	-0.4 to V_{DD}+0.4	V
Operating temperature	T_{OPR}	—	-5 to +85	°C
Storage temperature	T_{STR}	—	-40 to +125	°C

Caution The absolute maximum ratings are rated values exceeding which the product could suffer physical damage. These values must therefore not be exceeded under any conditions.

■ Electric Characteristics

(1) DC characteristics

Table 3

V_{DD}=5 V±10%, T_{OPR}=55°C

Parameter	Symbol	Condition	Rating			Unit
			min.	typ.	max.	
Input voltage	V_{IH}	SI, FS, CLK, DS, LS	2.4	—	—	V
	V_{IL}		—	—	0.8	
Input current	I_{IH}	SI, FS, CLK, DS, LS	—	—	0.5	μA
	I_{IL}	SI, FS, CLK	-0.5	—	—	
		DS, LS	-40.0	—	—	
Output voltage	V_{OH}	SO, I_{OH} = -100 μA	3.8	—	—	V
	V_{OL}	SO, I_{OL} = 100 μA	—	—	0.4	
Reference voltage	V_{REF}	V_{DD} = 5 V	990.	—	1390.	mV
Current consumption at operating 1	I_{DD1}	fck = 2.0 MHz amplifier stops	—	1.0	2.0	mA
Current consumption at operating 2	I_{DD2}	VDD-GND amplifier operates	—	27.0	43.0	mA
Current consumption at operating 3	I_{DD3}	VDD-GND supplying FS, 14-clock period	—	8.5	17.0	mA
Current consumption at standby	I_S	VDD-GND amplifier stops	—	0.7	1.0	mA

Note: When the power is turned on, current equal to the total of I_{DD2} and I_{DD3} may flow, and analog image signals are undetermined. If clock signals and start signals for two or more lines are input, the normal scanning mode is set.

(2) Switching characteristics

Table 4

V_{DD}=5 V±10%, T_{OPR}=55°C

Parameter	Symbol	Condition		Rating			Unit
				min.	typ.	max.	
Clock pulse width	t_{wl}	Scanning circuit operation guaranteed		225	—	—	ns
	t_{wh}	Scanning circuit operation guaranteed	300 dpi	225	—	—	
			600 dpi	135	—	—	
Data setup time	t_{su}	SI, FS		75	—	(1/fck)-120	ns
Data hold time	t_h	SI, FS		125	—	(1/fck)-120	ns
Clock frequency	fck	Low duty=50 % SIG and SO output guaranteed		0.5	—	2.0	MHz
CLK-SO L-H delay time	t_{plh}	fck = 2.0 MHz C_L = 10 pF	300 dpi	—	—	100	ns
			600 dpi	—	—	50	
CLK-SO H-L delay time	t_{phl}	fck = 2.0 MHz C_L = 10 pF	300 dpi	—	—	90	ns
			600 dpi	—	—	50	

(3) Photoelectric conversion characteristics

Condition: V_{DD} = 5 V, T_{OPR} = 55°C, fck = 1.0 MHz (low duty = 50%)
Scanning period RT = 1 msec, 1st IC mode (SI = FS)
Load capacitor CL = 50 pF, load resistor RL = 100 kΩ
Light source: LED (λ = 570 nm, half-width Δλ ≅ 30 nm, illuminance 10.0 lx)
Connect a 1 μF capacitor between VDD and GND and between VREF and GND, and check the output value Vp of the external measurement circuit shown in Figure 3.

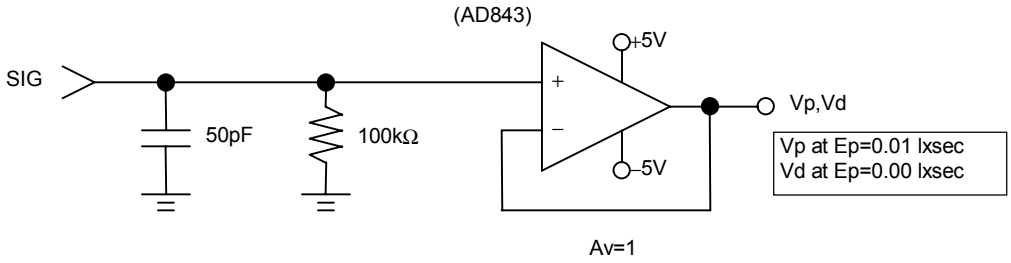

Figure 3 Measurement Circuit

Table 5

Parameter	Symbol	Condition		Rating min.	Rating typ.	Rating max.	Unit	Note
Effective bright signal	Vpave	Exposure value Ep = 0.01 lx · s		500	750	1000	mV	Vp
Bright signal deviation	dV3	Scanning period R_T = 1 ms	300dpi	0	—	+14	%	Vp See 3)-1
			600dpi	0	—	+18	%	
	dV4	R_T = 1 ms i= 2 to 142	300dpi	0	—	+7	%	
		R_T = 1 ms i= 2 to 286	600dpi	0	—	+15	%	
		R_T = 1 ms i= 1, 143	300dpi	0	—	+10	%	
		R_T = 1 ms i= 1, 287	600dpi	0	—	+16	%	
Dark signal	Vd	R_T = 1 ms		1000	—	1400	mV	Vd
Dark signal deviation 1	Δ Vd1	R_T = 1 ms	300dpi	—	—	45	mV	Vd(max.) - Vd(min.)
			600dpi	—	—	70		
Quasi-dark signal output	Vdmmy	R_T = 1 ms		980	—	1380	mV	See Figure 2e
Dark signal deviation 2	Δ Vd2	R_T = 1 ms	300dpi	-90	—	110	mV	Vd(i) - V_{REF}
			600dpi	-85	—	150		
Dark signal deviation 3	Δ Vd3	R_T = 1 ms	300dpi	-80	—	120	mV	Vd(i) - Vdummy
			600dpi	-75	—	160		
Linearity	Rγ 20%	At Vpave check	Average	0.15	—	0.23		See 3)-2
			All pixels	0.13	—	0.25		
	Rγ 80%		Average	0.76	—	0.84		
			All pixels	0.74	—	0.85		
Image lag rate	R_{IL}	At Vpave check	Average	-3	—	+3	%	See 3)-1
			All pixels	-5	—	+5		
Light response rate	R_{IR}	At Vpave check	Average	85	—	101	%	
			All pixels	80	—	105		

3)-1 Definitions

The definitions of parameters are as follows:

· Vp(i): Output of bright signal of i-th pixel

· Vd(i): Output of dark signal of i-th pixel

· Vpe(i)=: Vp(i) - Vd(i): Output of effective bright signal of i-th pixel

· Vp_ave: Average of Vpe(i) of all pixels

· Vp_max.: Maximum Vpe(i) (i = 2 to 287 for 600 dpi, i = 2 to 143 for 300 dpi)

· Vp_min.: Minimum Vpe(i) (i = 2 to 287 for 600 dpi, i = 2 to 143 for 300 dpi)

$$\cdot\ dV3 = \frac{Vp\_max - Vp\_min}{Vp\_ave} \times 100$$

$$dV4 = \text{maximum} \left| \frac{Vpe(i) - Vpe(i+1)}{Vp\_ave} \right| \times 100$$

· Vdummy: Average of output values of 32nd to 61st clock pulses in first IC mode (see Figure 2e)

· RIL: Average of image lag ratios of all pixels (see Figure 4)

· RIR: Average of light response ratios of all pixels (see Figure 4)

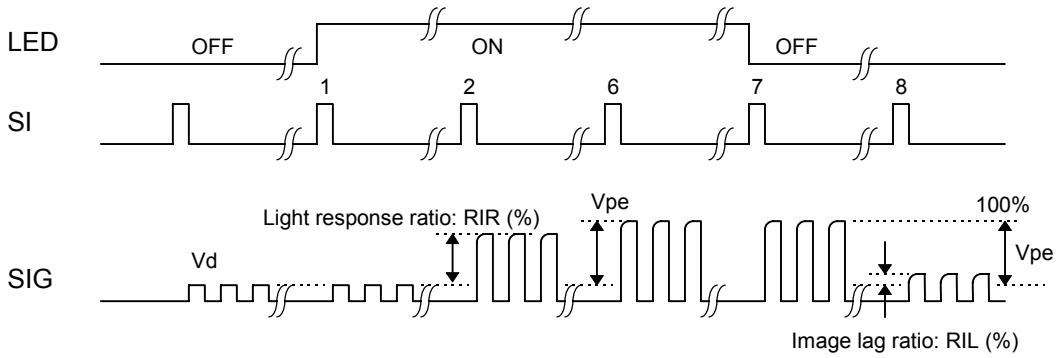

Figure 4

3)-2 Linearity

Check $R\gamma$ as follows (the illuminance is 5.0 lx for scanning at Vp04, Vp16, and Vp20 below):

· Vd: Average of dark signal output Vd(i) at RT = 1.0 ms

· Vp04: Average of bright signal output Vp(i) at RT = 0.4 ms

· Vp16P: Average of bright signal output Vp(i) at RT = 1.6 ms

· Vp20: Average of bright signal output Vp(i) at RT = 2.0 ms

· i : 1 to 288

·

$$R\gamma(20\%) = \frac{Vp04 - Vd}{Vp20 - Vd}$$

$$R\gamma(80\%) = \frac{Vp16 - Vd}{Vp20 - Vd}$$

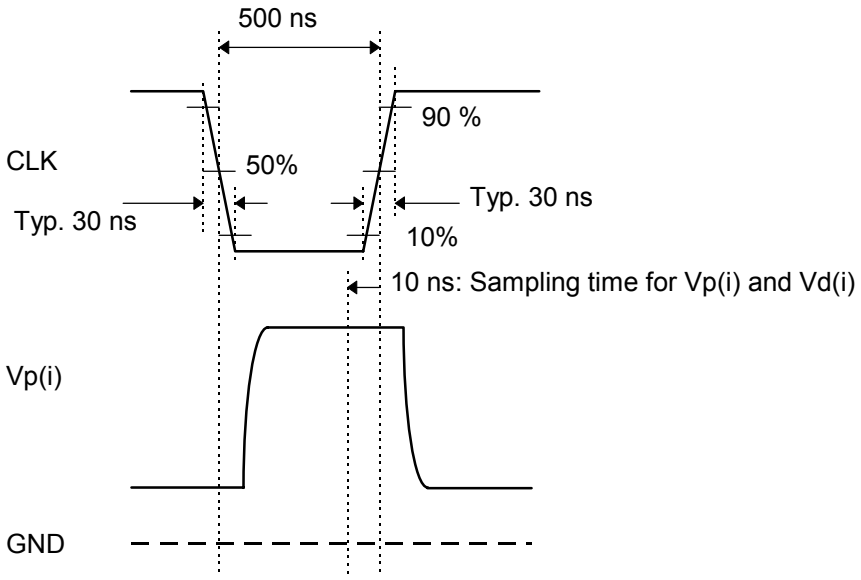

Figure 5

■ Pad Configuration

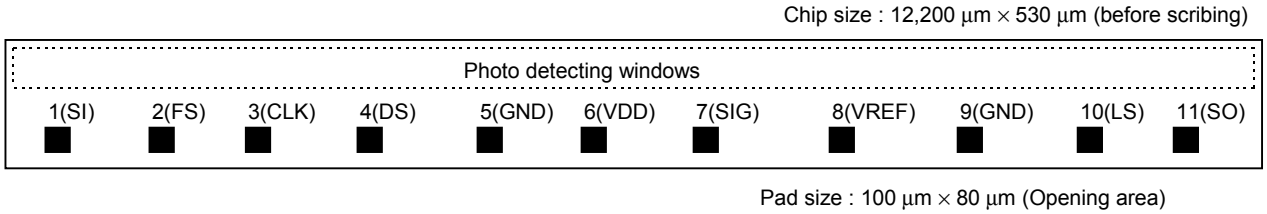

Figure 6

Table 7

Unit : μm

PAD No.	Name	Coordinate		PAD No.	Name	Coordinate	
		X	Y			X	Y
1	SI	1,843	102	7	SIG	5,813	102
2	FS	2,257	102	8	VREF	7,755	102
3	CLK	2,671	102	9	GND	10,316	102
4	DS	3,662	102	10	LS	10,749	102
5	GND	4,970	102	11	SO	11,487	102
6	VDD	5,352	102	—	—	—	—

Note: The coordinate origin is the lower left corner of the IC, and the pad coordinate in the above table is the coordinate value of the center of the pad.

■ Chip Size and Sensor Arrangement Diagram

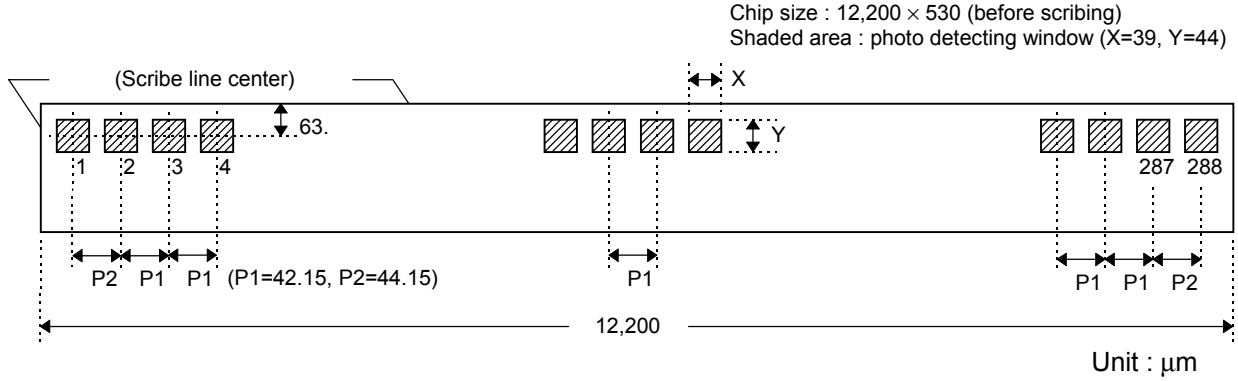

Figure 7

■ Wafer Form

Note: IC arrangement is subject to change without notes.

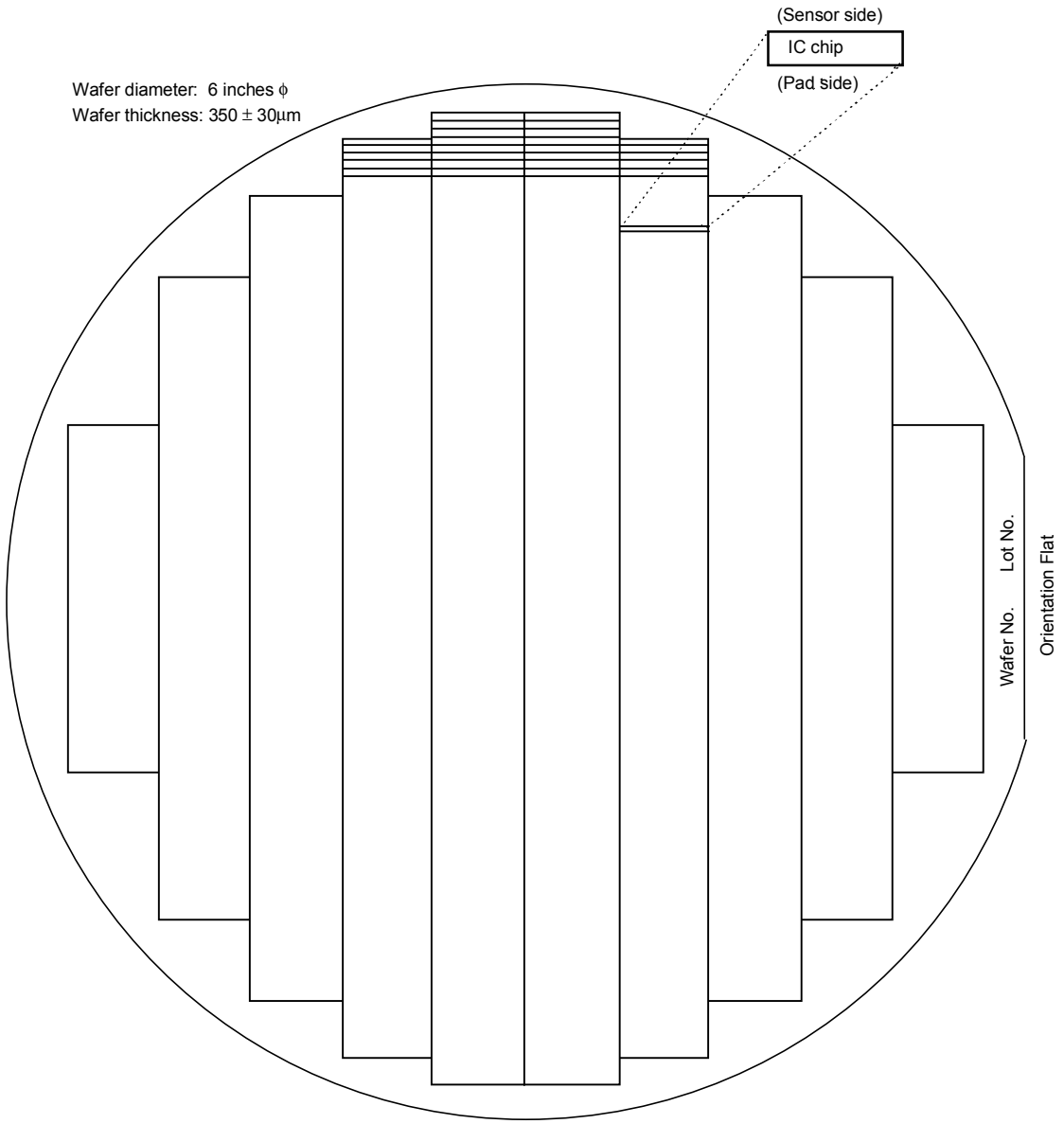

Figure 8

■ Scribe Line

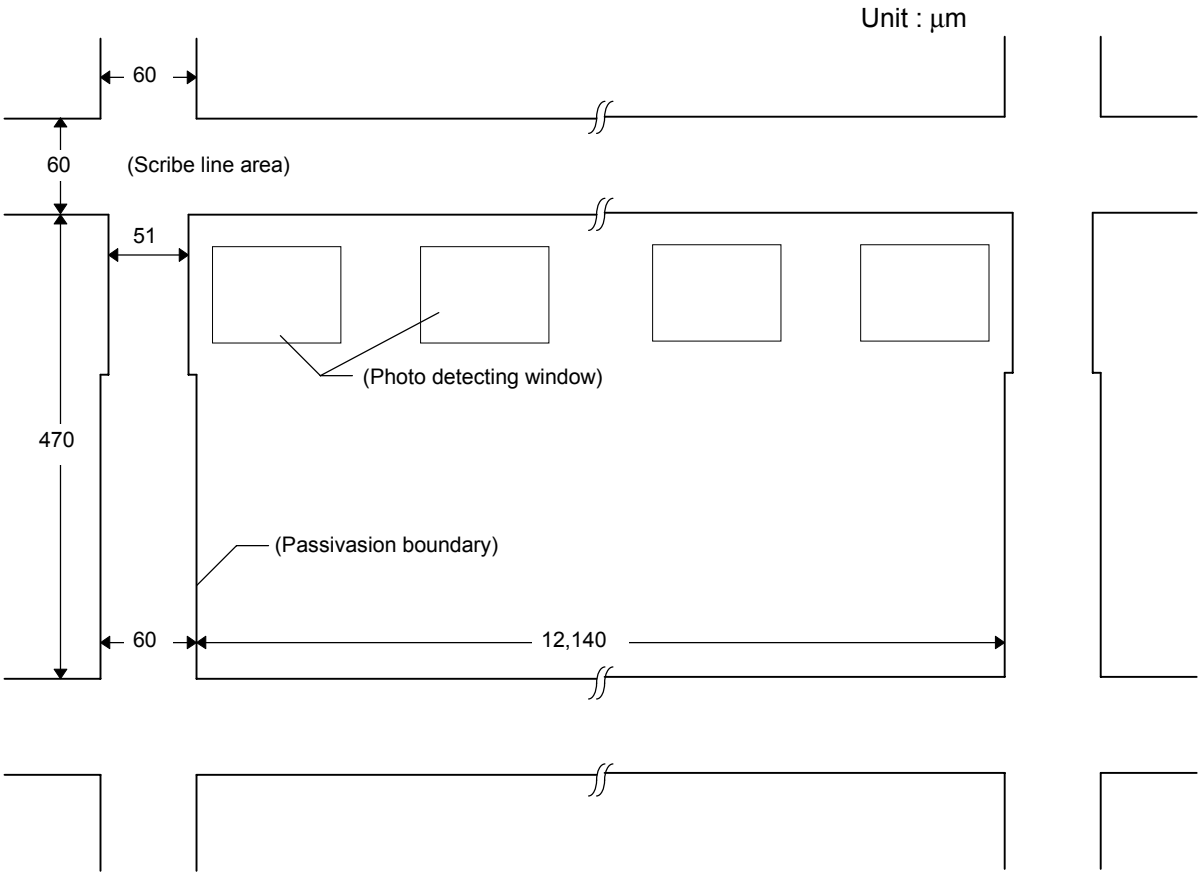

Figure 9

■ Connection Diagram

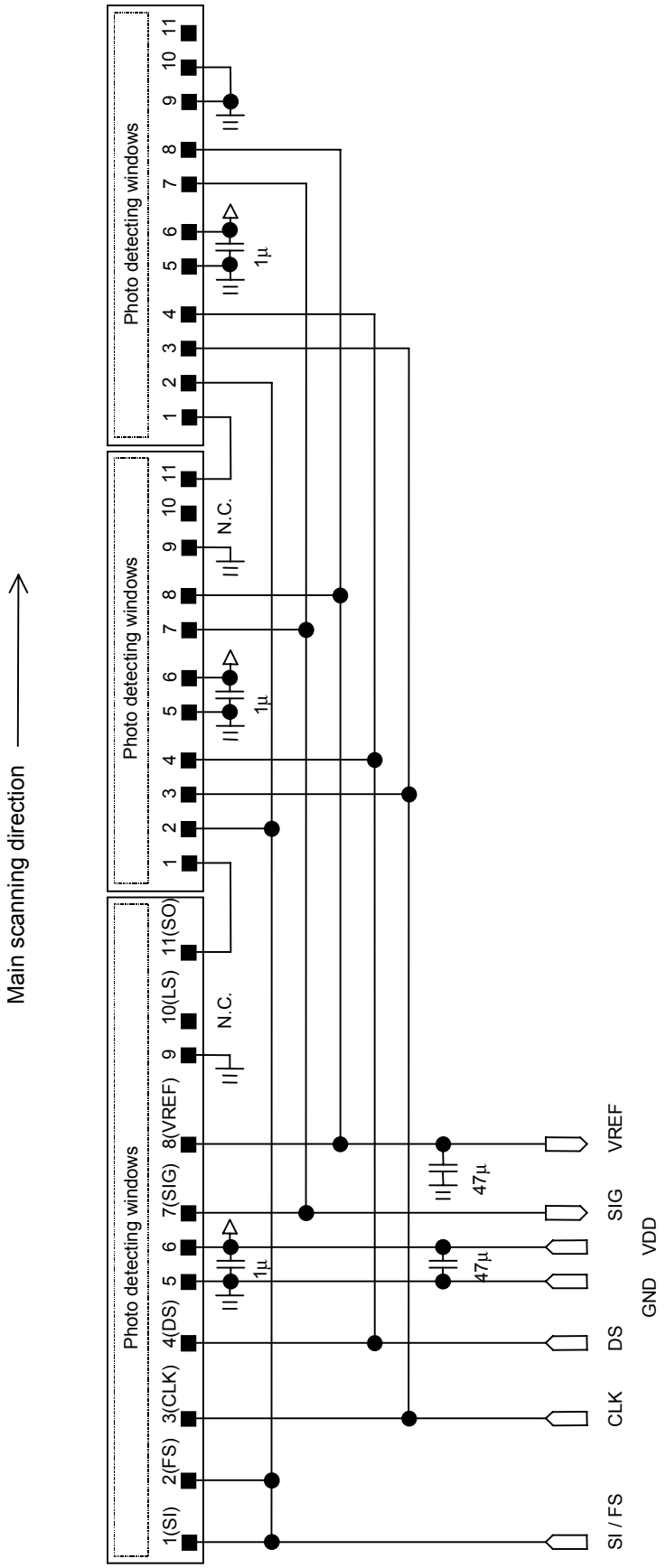

Figure 10

■ Notes on Handling

Products are shipped in wafer or bare chip form. Follow these points when handling the products.

1. Protect against static electricity damage when mounting a on a sawing or dicing machine.
   - Wear charge-proof clothing and discharge all static electricity from body.
   - Work on a grounded conductive mat.
   - Ground all soldering irons and machines.
   - Maintain room humidity from 50 to 60%RH.

2. Prevent malfunctions due to corrosion of electrode pads.
   - Do not store products in a high temperature and humidity, dusty environment or one that where there is any corrosive gas.
   - Coat surface of IC with silicon resin to keep surface clean.
   - Use clear and non-static packing material.
   - Store products in a dry box filled with dry N2 gas at a temperature of –30°C or less when storing products for 3 months or more.

3. Protect the internal wires and protective film of the IC when mounting products.
   - Do not damage the surface of the IC when mounting a die or bonding wires.
   - Do not touch the surface of the IC with a pair of tweezers.

4. Maintain the stability of the IC.
   - The IC uses an n-type substrate.
   - Send the null data until the Vsig signal becomes stable at power on.
   - Coat the IC with a transparent resin like silicon resin or enclose the IC with glass.
   - Decrease the wiring resistance of GND and VDD of the circuit board on which the IC is mounted.
   - Decrease the wiring capacitance between CLK and SIG of the circuit board on which the IC is mounted.
   - Fix the cycle and duty of the input signal while operating.
   - Mount a low inductance, high frequency ceramic capacitor of 1.0 μF or more between VDD and GND close to each IC chip to prevent influence of voltage fluctuation due to the response current of IC. Mount a electrolytic capacitor of 2.5 μF or more for one IC chip between the VDD and GND pins close to the board input. (e.g. 45 μF or more for 18 chips: 2.5 μF x 18 = 45 μF) Decide mounting method and capacitance of capacitor based on evaluation of the product in an actual application.

- The information described herein is subject to change without notice.
- Seiko Instruments Inc. is not responsible for any problems caused by circuits or diagrams described herein whose related industrial properties, patents, or other rights belong to third parties. The application circuit examples explain typical applications of the products, and do not guarantee the success of any specific mass-production design.
- When the products described herein are regulated products subject to the Wassenaar Arrangement or other agreements, they may not be exported without authorization from the appropriate governmental authority.
- Use of the information described herein for other purposes and/or reproduction or copying without the express permission of Seiko Instruments Inc. is strictly prohibited.
- The products described herein cannot be used as part of any device or equipment affecting the human body, such as exercise equipment, medical equipment, security systems, gas equipment, or any apparatus installed in airplanes and other vehicles, without prior written permission of Seiko Instruments Inc.
- Although Seiko Instruments Inc. exerts the greatest possible effort to ensure high quality and reliability, the failure or malfunction of semiconductor products may occur. The user of these products should therefore give thorough consideration to safety design, including redundancy, fire-prevention measures, and malfunction prevention, to prevent any accidents, fires, or community damage that may ensue.