

TPIC2701

7-CHANNEL COMMON-SOURCE POWER DMOS ARRAY

SLIS019A – SEPTEMBER 1992 – REVISED SEPTEMBER 1996

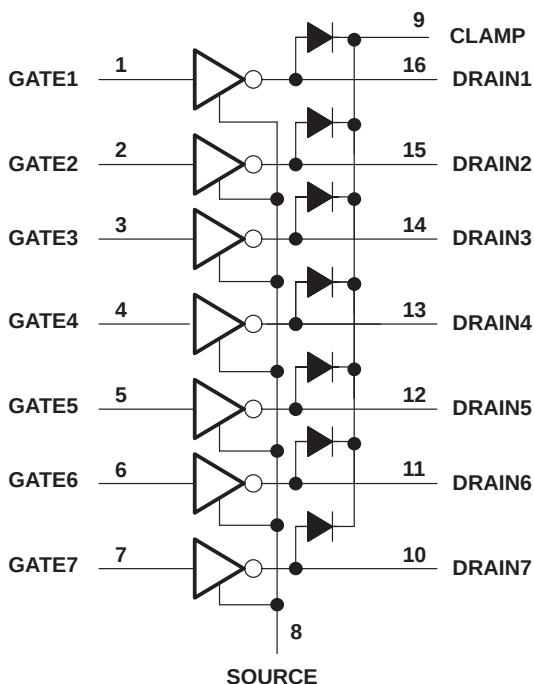
- Seven 0.5-A Independent Output Channels
- Integrated Clamp Diode With Each Output
- Low $r_{DS(on)}$. . . 0.5 Ω Typical
- Output Voltage . . . 60 V
- Pulsed Current . . . 3 A Per Channel
- Avalanche Energy . . . 22 mJ

description

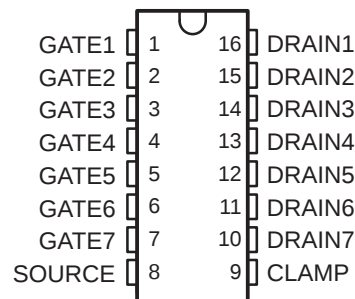
The TPIC2701 is a monolithic power DMOS transistor array that consists of seven independent N-channel enhancement-mode DMOS transistors connected in a common-source configuration with open drains. The TPIC2701 is pin-for-pin functionally compatible with the Texas Instruments ULN2001A through ULN2004A.

The TPIC2701 is characterized for operation over a temperature range of 0°C to 125°C. The TPIC2701M is characterized for operation over the full military temperature range of –55°C to 125°C.

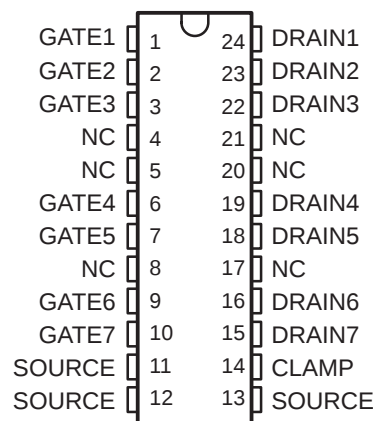
logic diagram



TPIC2701
N PACKAGE
(TOP VIEW)



TPIC2701M
J PACKAGE†
(TOP VIEW)



NC – No internal connection

† Refer to the mechanical data for the JW package.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS
INSTRUMENTS**

POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

Copyright © 1996, Texas Instruments Incorporated

TPIC2701

7-CHANNEL COMMON-SOURCE POWER DMOS ARRAY

SLIS019A – SEPTEMBER 1992 – REVISED SEPTEMBER 1996

absolute maximum ratings over operating case temperature range (unless otherwise noted)

Drain-source voltage, V_{DS}	60 V
Gate-source voltage, V_{GS}	± 20 V
Clamp-drain voltage, V_{CD}	60 V
Continuous source-drain diode current	0.5 A
Pulsed drain current, each output, I_D (see Note 1 and Figure 17)	3 A
Pulsed clamp current, I_{CL} (see Note 1 and Figure 18)	3 A
Continuous drain current, each output, all outputs on	0.5 A
Single-pulse avalanche energy, E_{AS} (see Figure 4)	22 mJ
Continuous total power dissipation	See Dissipation Rating Table
Operating virtual junction temperature range, T_J : TPIC2701	-40°C to 150°C
TPIC2701M	-55°C to 150°C
Operating case temperature range, T_C : TPIC2701	-40°C to 125°C
TPIC2701M	-55°C to 125°C
Storage temperature range, T_{stg}	-65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: N Package	260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: J Package	300°C

NOTE 1: Pulse duration = 10 ms, duty cycle = 6%.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25^\circ\text{C}$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25^\circ\text{C}$	$T_A = 70^\circ\text{C}$ POWER RATING	$T_A = 85^\circ\text{C}$ POWER RATING	$T_A = 125^\circ\text{C}$ POWER RATING
J	2660 mW	21.3 mW/ $^\circ\text{C}$	1701 mW	1382 mW	530 mW
N	1400 mW	11.0 mW/ $^\circ\text{C}$	905 mW	740 mW	300 mW

electrical characteristics, $T_C = 25^\circ\text{C}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	TPIC2701			UNIT
		MIN	TYP	MAX	
$V_{(BR)DS}$ Drain-source breakdown voltage	$I_D = 1 \mu\text{A}$, $V_{GS} = 0$	60			V
V_{TGS} Gate-source threshold voltage	$I_D = 1 \text{ mA}$, $V_{DS} = V_{GS}$	1.2	1.75	2.4	V
$V_{DS(on)}$ Drain-source on-state voltage	$I_D = 0.5 \text{ A}$, $V_{GS} = 15 \text{ V}$, See Notes 2 and 3		0.25	0.4	V
I_{DSS} Zero-gate-voltage drain current	$V_{DS} = 48 \text{ V}$, $V_{GS} = 0$	$T_C = 25^\circ\text{C}$	0.05	1	μA
		$T_C = 125^\circ\text{C}$	0.5	10	
I_{GSSF} Forward gate current, drain short circuited to source	$V_{GS} = 20 \text{ V}$, $V_{DS} = 0$		10	100	nA
I_{GSSR} Reverse gate current, drain short circuited to source	$V_{GS} = -20 \text{ V}$, $V_{DS} = 0$		10	100	nA
$r_{DS(on)}$ Forward drain-source on-state resistance	$V_{GS} = 15 \text{ V}$, $I_D = 0.5 \text{ A}$, See Notes 2 and 3 and Figures 5 and 6	$T_C = 25^\circ\text{C}$	0.5	0.8	Ω
		$T_C = 125^\circ\text{C}$	0.8	1.3	
g_{fs} Forward transconductance	$V_{DS} = 15 \text{ V}$, $I_D = 0.5 \text{ A}$, See Notes 2 and 3	0.5	0.8		S
C_{iss} Short-circuit input capacitance, common source	$V_{DS} = 25 \text{ V}$, $V_{GS} = 0$, $f = 300 \text{ kHz}$		105		pF
C_{oss} Short-circuit output capacitance, common source			65		
C_{rss} Short-circuit reverse transfer capacitance, common source			15		

NOTES: 2. Technique should limit $T_J - T_C$ to 10°C maximum.

3. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts with a single output transistor conducting.



POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

TPIC2701

7-CHANNEL COMMON-SOURCE POWER DMOS ARRAY

SLIS019A – SEPTEMBER 1992 – REVISED SEPTEMBER 1996

**electrical characteristics over case temperature operating range (unless otherwise noted)
(see Note 4)**

PARAMETER		TEST CONDITIONS	T _C [†]	TPIC2701M			UNIT
				MIN	TYP	MAX	
V _{(BR)DS}	Drain-to-source breakdown voltage	I _D = 1 μA, V _{GS} = 0	25°C	60			V
		I _D = 1 mA, V _{GS} = 0	Full range				
V _{TGS}	Gate-to-source input threshold voltage	I _D = 1 mA, V _{DS} = V _{GS}	Full range	1.2	1.75	2.4	V
V _{DS(on)}	Drain-to-source on-state voltage	I _D = 0.5 A, V _{GS} = 15 V	25°C	0.25	0.45	V	
			Full range	0.65			
I _{DSS}	Zero-gate-voltage drain current	V _{DS} = 48 V, V _{GS} = 0	25°C	0.05	1	μA	
			Full range	10			
I _{GSSF}	Forward gate current, drain short-circuited to source	V _{GS} = 20 V, V _{DS} = 0	25°C	10	100	nA	
			Full range	10		μA	
I _{GSSR}	Reverse gate current, drain short-circuited to source	V _{GS} = −20 V, V _{DS} = 0	25°C	10	100	nA	
			Full range	10		μA	
r _{DS(on)}	Forward drain-source on-state resistance	V _{GS} = 15 V, I _D = 0.5 A	25°C	0.5	0.9	Ω	
			Full range	1.3			
g _{fs}	Forward transconductance	V _{DS} = 15 V, I _D = 0.5 A	25°C	0.8		S	
C _{iSS}	Short-circuit input capacitance, common source	V _{DS} = 25 V, V _{GS} = 0, f = 300 kHz	Full range	105		pF	
C _{OSS}	Short-circuit output capacitance, common source			65			
C _{rSS}	Short-circuit reverse transfer capacitance, common source			15			

[†] Full range is -55°C to 125°C.

NOTE 4: Pulse testing techniques are used to maintain the virtual junction temperature as close to the case temperature as possible. Thermal effects must be taken into account separately.

source-drain diode characteristics, T_C = 25°C

PARAMETER	TEST CONDITIONS	TPIC2701			UNIT
		MIN	TYP	MAX	
V _{SD} Forward On voltage	I _S = 0.5 A, V _{GS} = 0	0.9 1.4			V
t _{rr(SD)} Reverse-recovery time	I _S = 0.5 A, V _{GS} = 0, V _{DS} = 48 V, di/dt = 25 A/μs, See Figure 1	165			ns
QRR Total source-drain diode charge		250			nC

source-to-drain diode characteristics over operating case temperature range (unless otherwise noted) (see Note 4)

PARAMETER	TEST CONDITIONS	TPIC2701M			UNIT
		MIN	TYP	MAX	
V _{SD} Forward On voltage	I _S = 0.5 A, V _{GS} = 0	0.9 1.4			V
t _{rr} Reverse recovery time	I _S = 0.5 A, V _{GS} = 0, V _{DS} = 48 V, di/dt = 25 A/μs, T _C = 25°C, See Figure 1	165			ns
QRR Total source-to-drain diode charge		250			nC

NOTE 4: Pulse testing techniques are used to maintain the virtual junction temperature as close to the case temperature as possible. Thermal effects must be taken into account separately.



TPIC2701

7-CHANNEL COMMON-SOURCE POWER DMOS ARRAY

SLIS019A – SEPTEMBER 1992 – REVISED SEPTEMBER 1996

clamp diode characteristics, $T_C = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	TPIC2701			UNIT
		MIN	TYP	MAX	
V_F Forward on-voltage	$I_F = 0.5\text{ A}$		1	1.5	V
V_{BR} Breakdown voltage	$I_R = 1\text{ }\mu\text{A}$	60			V
I_R Reverse leakage current	$V_R = 48\text{ V}$		0.05	1	μA
$t_{rr}(\text{CD})$ Reverse-recovery time	$I_F = 0.1\text{ A}$, $di/dt = 25\text{ A}/\mu\text{s}$, $V_{CD} = 48\text{ V}$, See Figure 1		90		ns
Q_{RR} Total source-drain diode charge			100		nC

clamp diode characteristics over operating case temperature range (unless otherwise noted) (see Note 4)

PARAMETER	TEST CONDITIONS	TPIC2701M			UNIT
		MIN	TYP	MAX	
V_F Forward voltage	$I_F = 0.5\text{ A}$		1	1.5	V
$V_{(BR)}$ Breakdown voltage	$I_R = 1\text{ }\mu\text{A}$, $T_C = 25^\circ\text{C}$	60			V
	$I_R = 1\text{ mA}$				
I_R Reverse leakage current	$V_R = 48\text{ V}$, $T_C = 25^\circ\text{C}$		0.05	1	μA
				10	
$t_{rr}(\text{SD})$ Reverse recovery time, source-to-drain	$I_F = 0.1\text{ A}$, $di/dt = 25\text{ A}/\mu\text{s}$, $T_C = 25^\circ\text{C}$ $V_{CD} = 48\text{ V}$, See Figure 1		90		ns
Q_{RR} Total source-to-drain diode charge			100		nC

NOTE 4: Pulse testing techniques are used to maintain the virtual junction temperature as close to the case temperature as possible. Thermal effects must be taken into account separately.

resistive-load switching characteristics, $T_C = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS			TPIC2701			UNIT
					MIN	TYP	MAX	
t _{d(on)}	Turn-on delay time	V _{DD} = 25 V, t _{dis} = 10 ns, See Figure 2	R _L = 100 Ω, See Figure 2	t _{en} = 10 ns,	10		ns	
t _{d(off)}	Turn-off delay time				30			
t _r	Rise time				15			
t _f	Fall time				5			
Q _g	Total gate charge	V _{DS} = 48 V, See Figure 3	I _D = 0.25 A, See Figure 3	V _{GS} = 10 V,	2.8	3.6	nC	
Q _{gs}	Gate-source charge				1.6	2		
Q _{gd}	Gate-drain charge				1.2	1.6		

TPIC2701

7-CHANNEL COMMON-SOURCE POWER DMOS ARRAY

SLIS019A – SEPTEMBER 1992 – REVISED SEPTEMBER 1996

resistive-load switching characteristics over operating case temperature range (unless otherwise noted) (see Note 4)

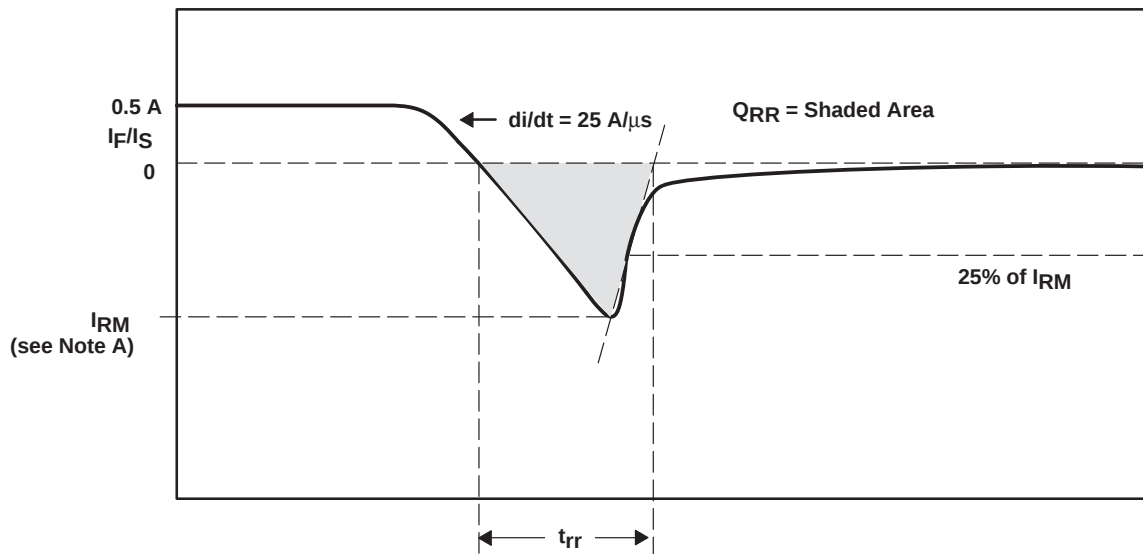
PARAMETER	TEST CONDITIONS	TPIC2701M			UNIT
		MIN	TYP	MAX	
$t_{d(on)}$ Turn-on delay time	$V_{DD} = 25\text{ V}$, $R_L = 100\ \Omega$, $t_{en} = 10\text{ ns}$, $t_{dis} = 10\text{ ns}$, See Figure 2		10		ns
$t_{d(off)}$ Turn-off delay time			30		
t_r Rise time			15		
t_f Fall time			5		
Q_g Total gate charge	$V_{DS} = 48\text{ V}$, $I_D = 0.25\text{ A}$, $V_{GS} = 10\text{ V}$, See Figure 3		2.8		nC
Q_{gs} Gate-to-source charge			1.6		
Q_{gd} Gate-to-drain charge			1.2		

NOTE 4: Pulse testing techniques are used to maintain the virtual junction temperature as close to the case temperature as possible. Thermal effects must be taken into account separately.

thermal resistance

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$R_{\theta JA}$ Junction-to-ambient thermal resistance	N package with all outputs at equal power			90	$^{\circ}\text{C/W}$
	J package with all outputs at equal power			66	

PARAMETER MEASUREMENT INFORMATION



NOTE A: I_{RM} = maximum recovery current

Figure 1. Reverse-Recovery-Current Waveforms of Source-Drain and Clamp Diodes

TPIC2701
7-CHANNEL COMMON-SOURCE POWER DMOS ARRAY

SLIS019A – SEPTEMBER 1992 – REVISED SEPTEMBER 1996

PARAMETER MEASUREMENT INFORMATION

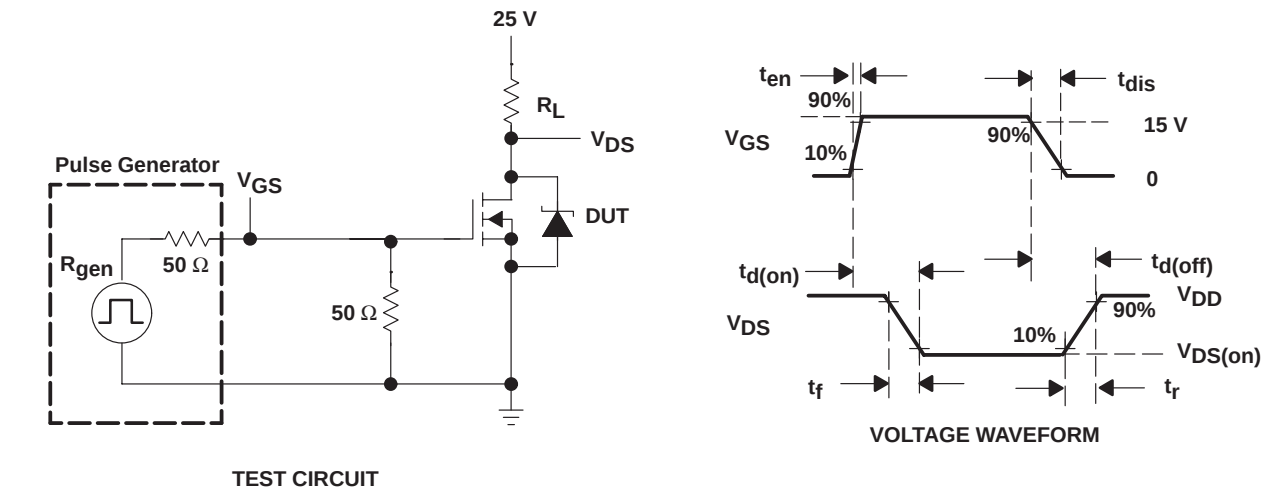


Figure 2. Resistive Switching

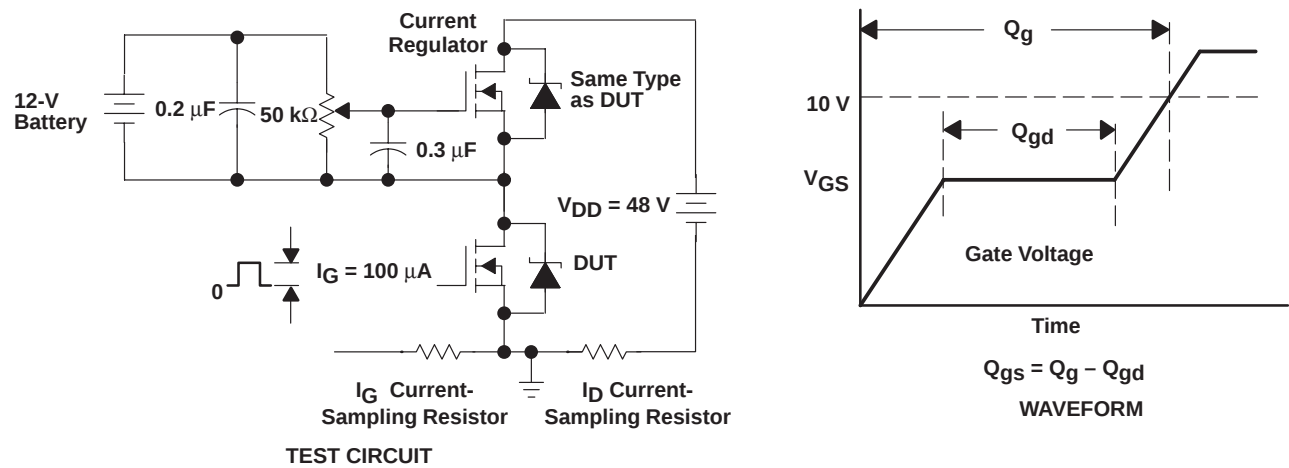
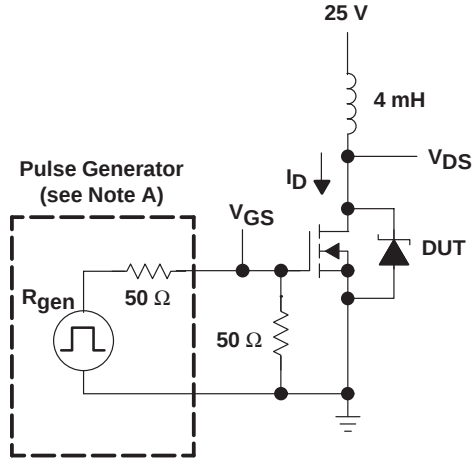
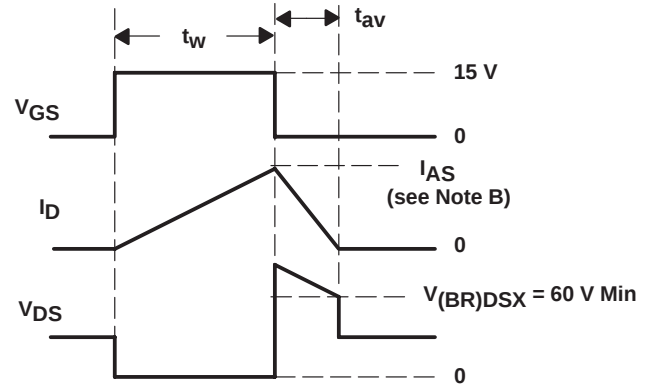


Figure 3. Gate Charge Test Circuit and Waveform

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE AND CURRENT WAVEFORMS

- NOTES: A. The pulse generator has the following characteristics: $t_r \leq 10\text{ ns}$, $t_f \leq 10\text{ ns}$, $Z_O = 50\ \Omega$.
B. Input pulse duration (t_w) is increased until peak current $I_{AS} = 2.5\text{ A}$.

$$\text{Energy test level is defined as } E_{AS} = \frac{I_{AS} \times V_{(BR)DSX} \times t_{av}}{2} = 22\text{ mJ min.}$$

Figure 4. Single-Pulse Avalanche Energy Test Circuit and Waveforms

TYPICAL CHARACTERISTICS

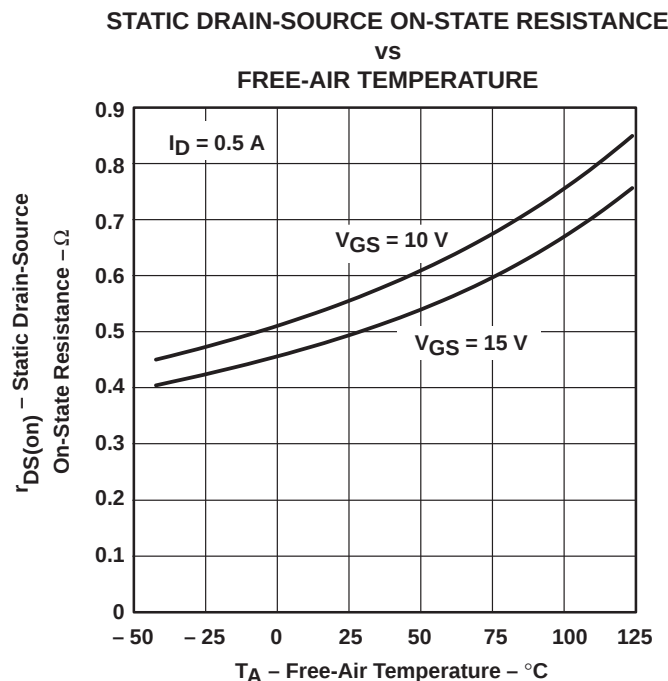


Figure 5

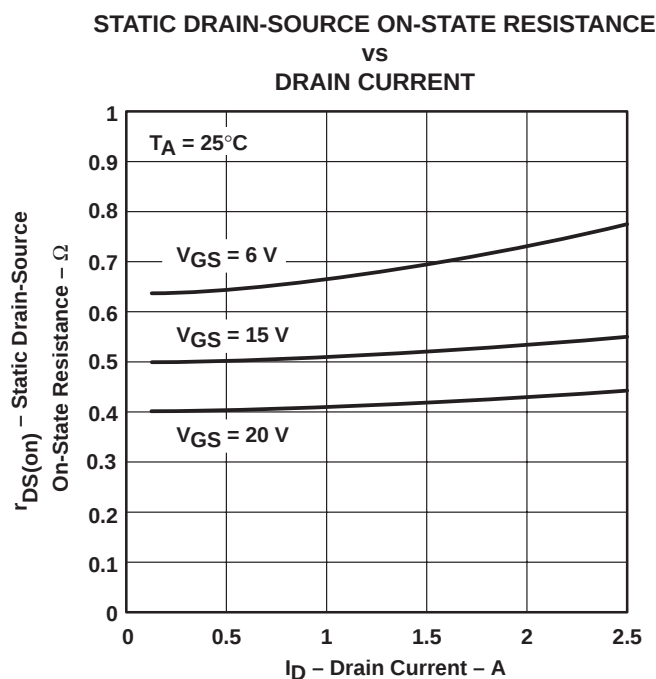


Figure 6

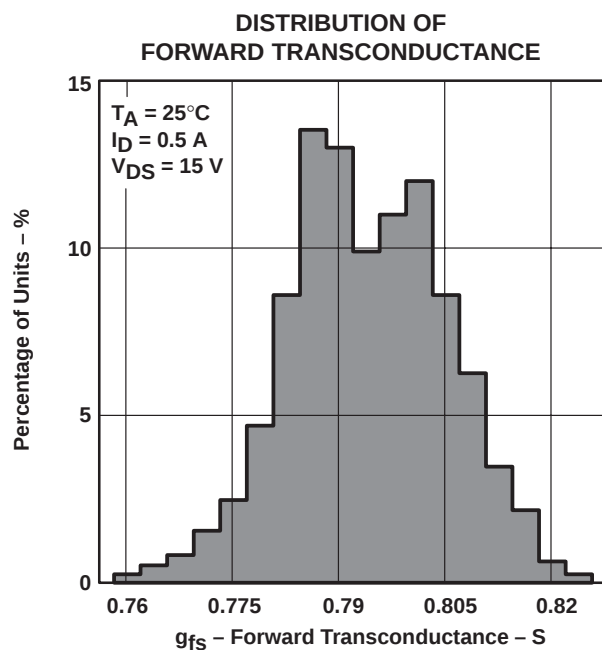


Figure 7

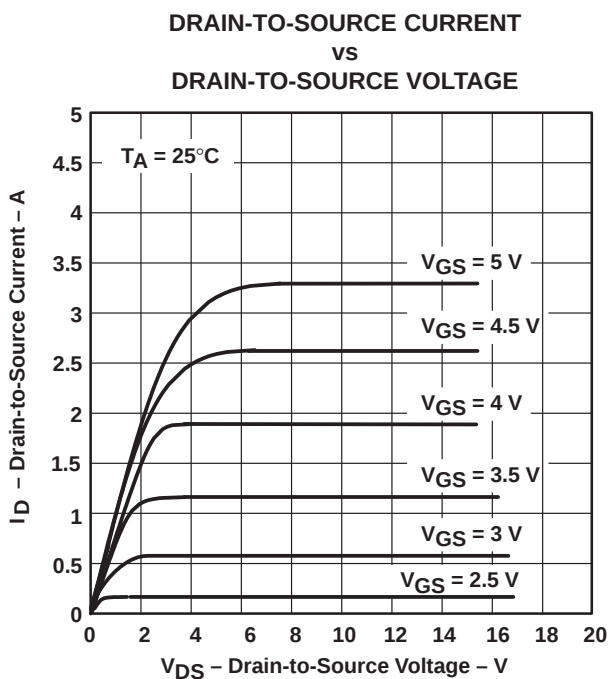


Figure 8

TYPICAL CHARACTERISTICS

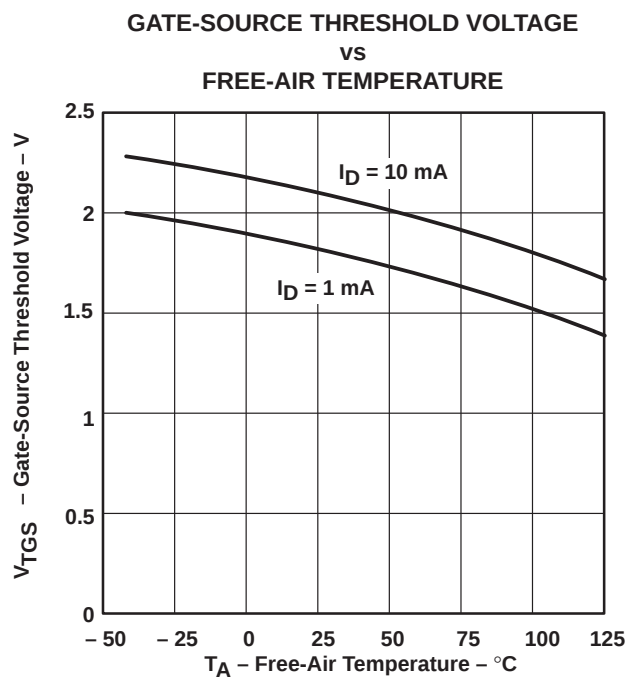


Figure 9

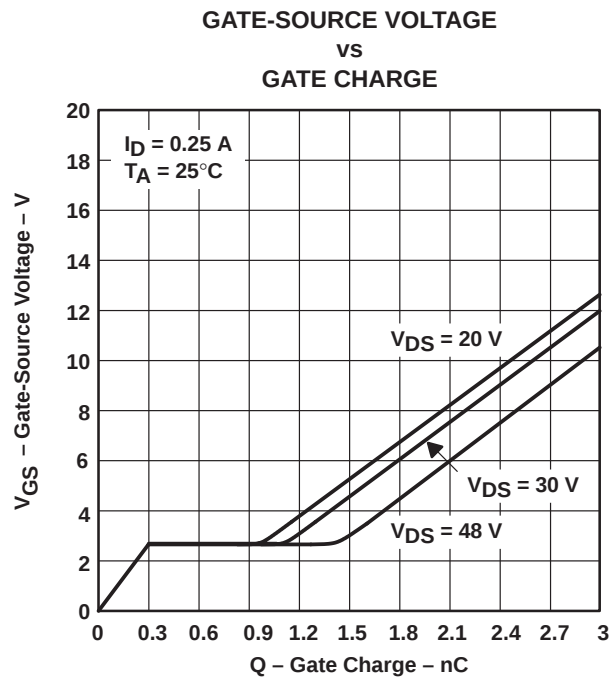


Figure 10

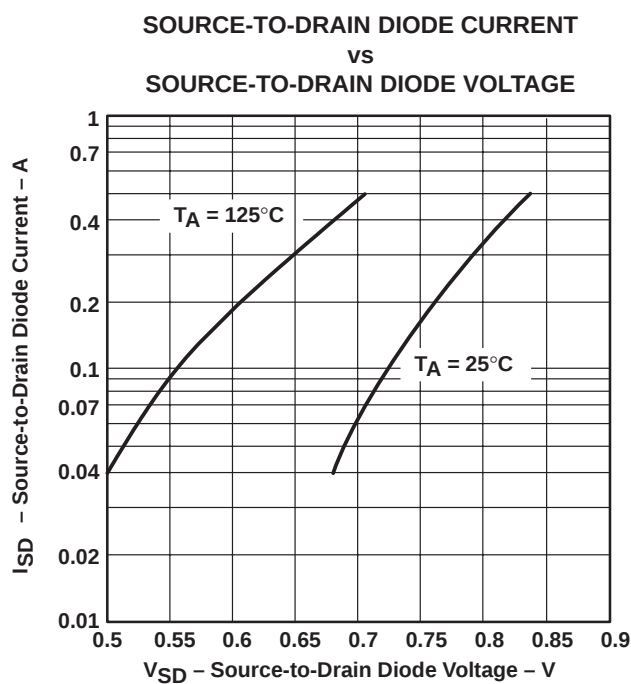


Figure 11

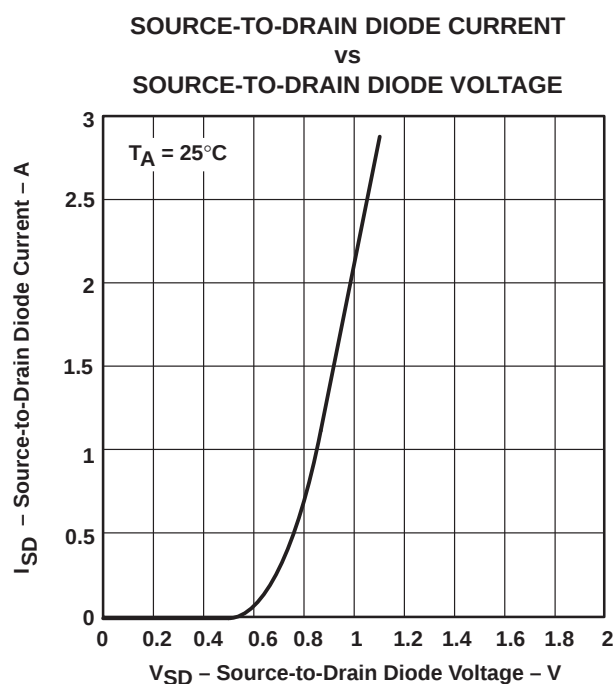


Figure 12

TPIC2701

7-CHANNEL COMMON-SOURCE POWER DMOS ARRAY

SLIS019A – SEPTEMBER 1992 – REVISED SEPTEMBER 1996

TYPICAL CHARACTERISTICS

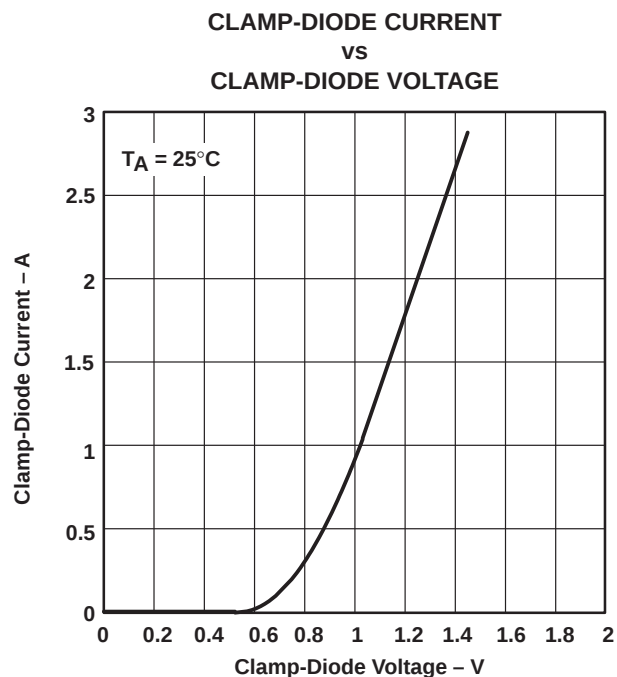


Figure 13

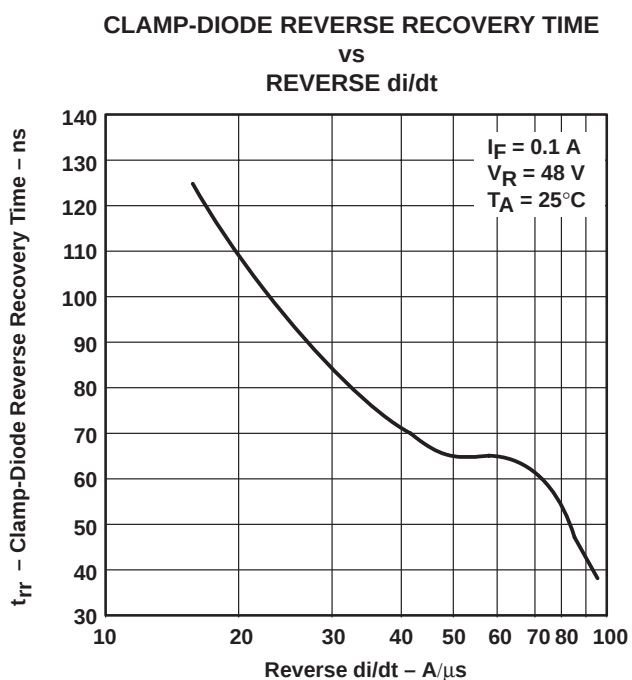


Figure 14

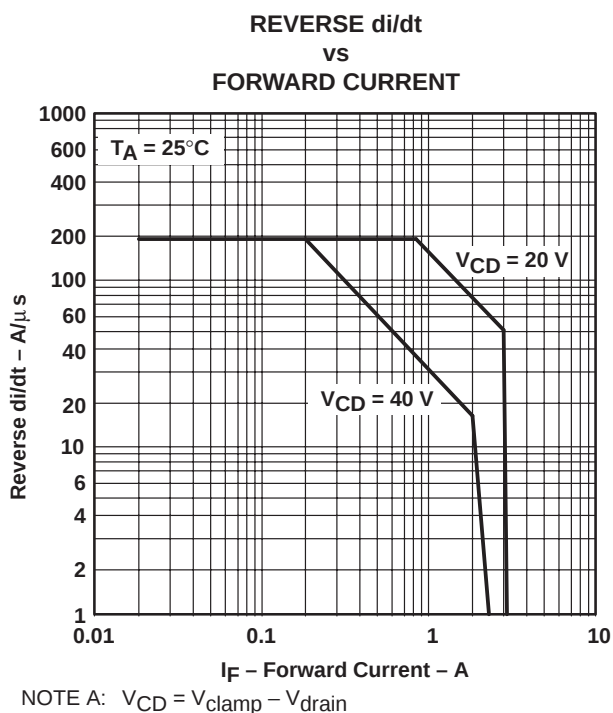


Figure 15

TYPICAL CHARACTERISTICS

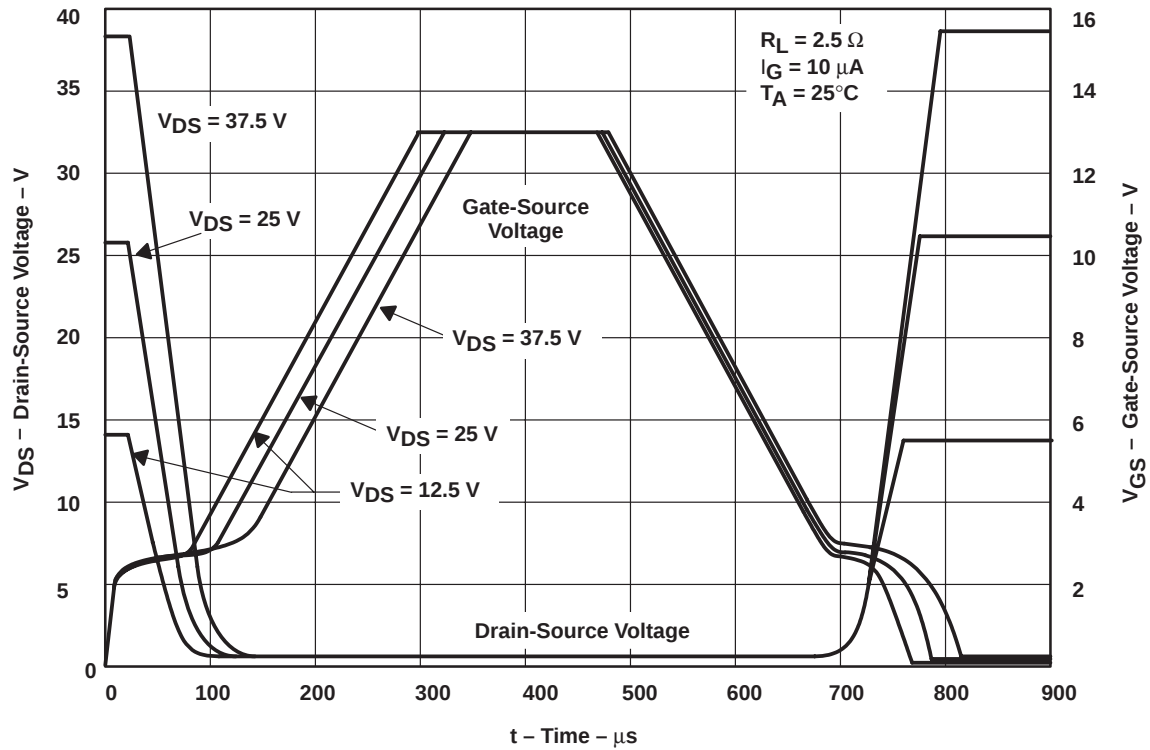


Figure 16. Resistive Switching Waveforms

TPIC2701

7-CHANNEL COMMON-SOURCE POWER DMOS ARRAY

SLIS019A – SEPTEMBER 1992 – REVISED SEPTEMBER 1996

THERMAL INFORMATION

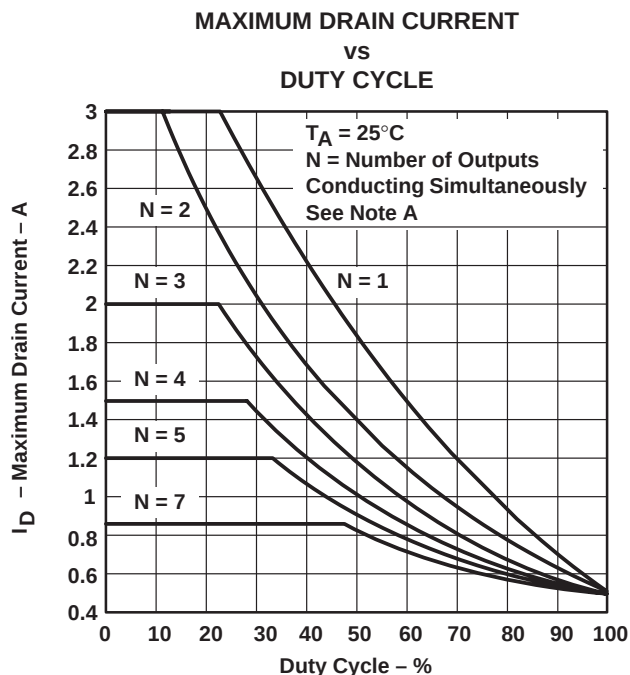


Figure 17

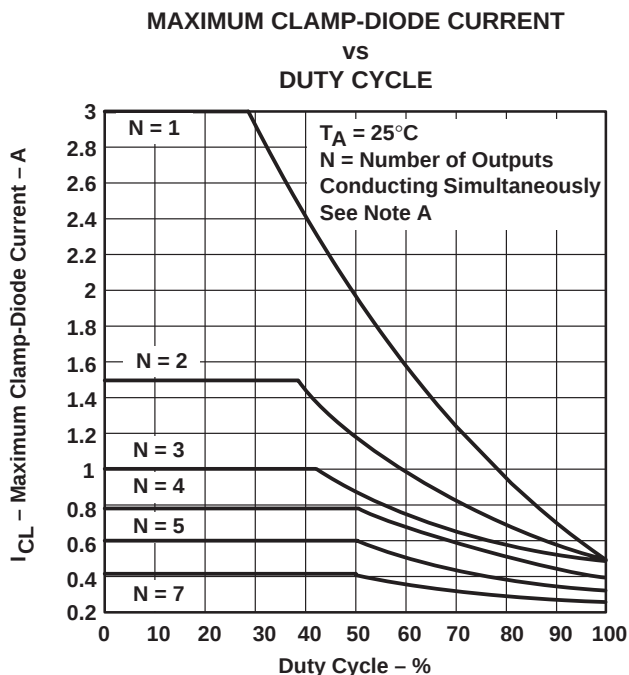


Figure 18

NOTE A: For Figures 17 and 18, $d = t_W/t_C = 10 \text{ ms} / t_C$, where t_W and t_C are defined by the following:

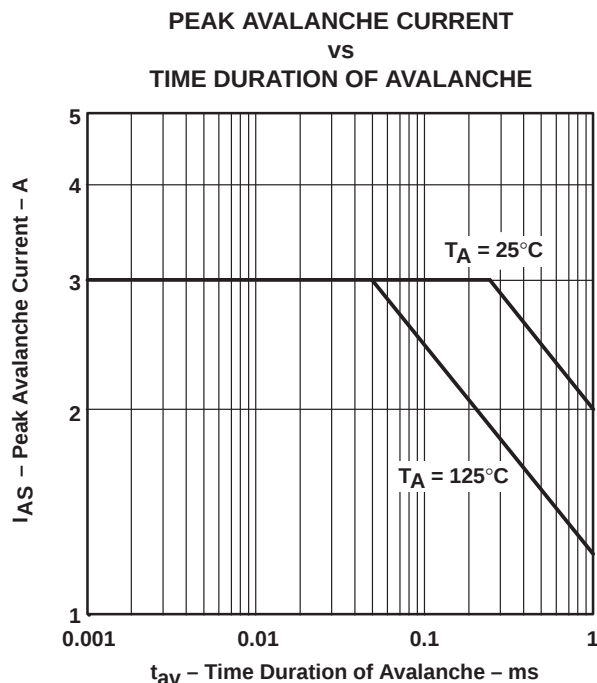
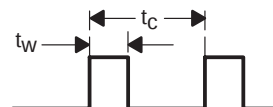


Figure 19

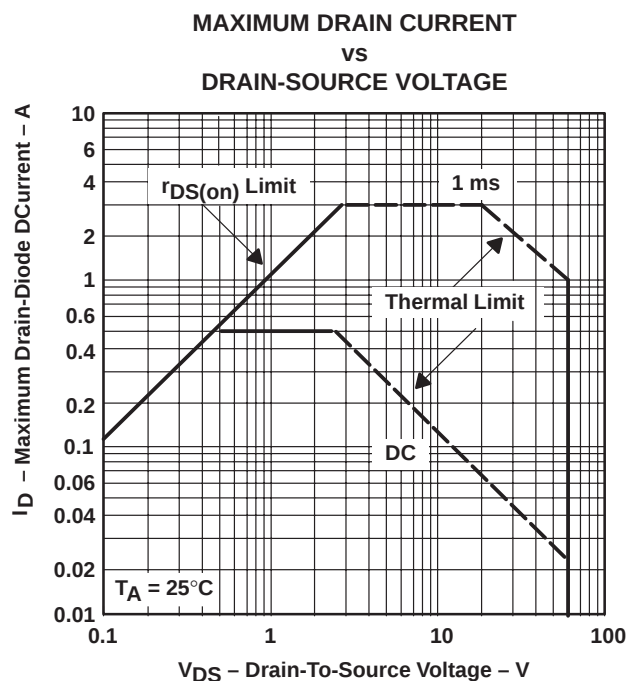


Figure 20

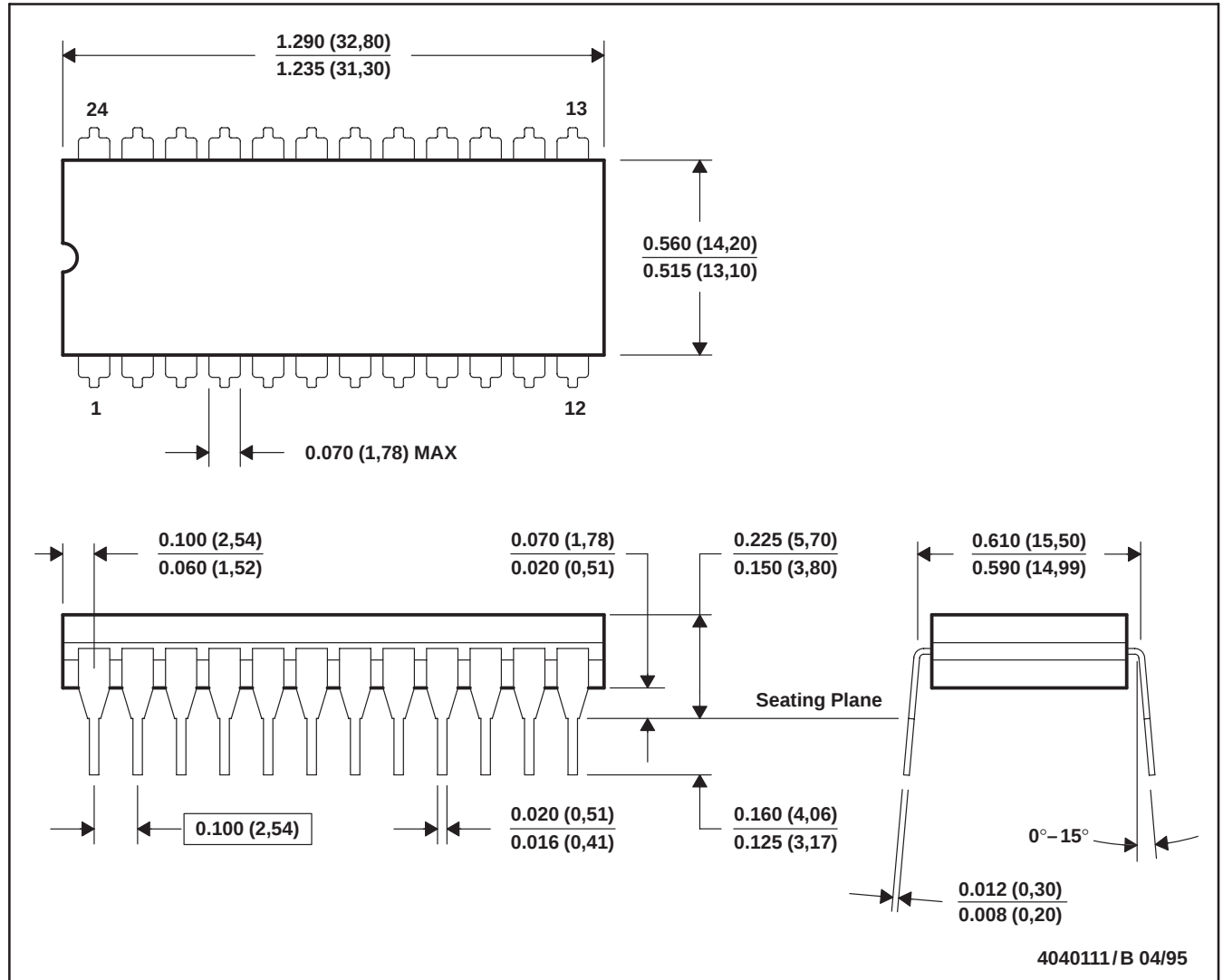
TPIC2701
7-CHANNEL COMMON-SOURCE POWER DMOS ARRAY

SLIS019A – SEPTEMBER 1992 – REVISED SEPTEMBER 1996

MECHANICAL INFORMATION

JW (R-GDIP-T24)

CERAMIC DUAL-IN-LINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only
 - E. Falls within MIL-STD-1835 GDIP5-T24

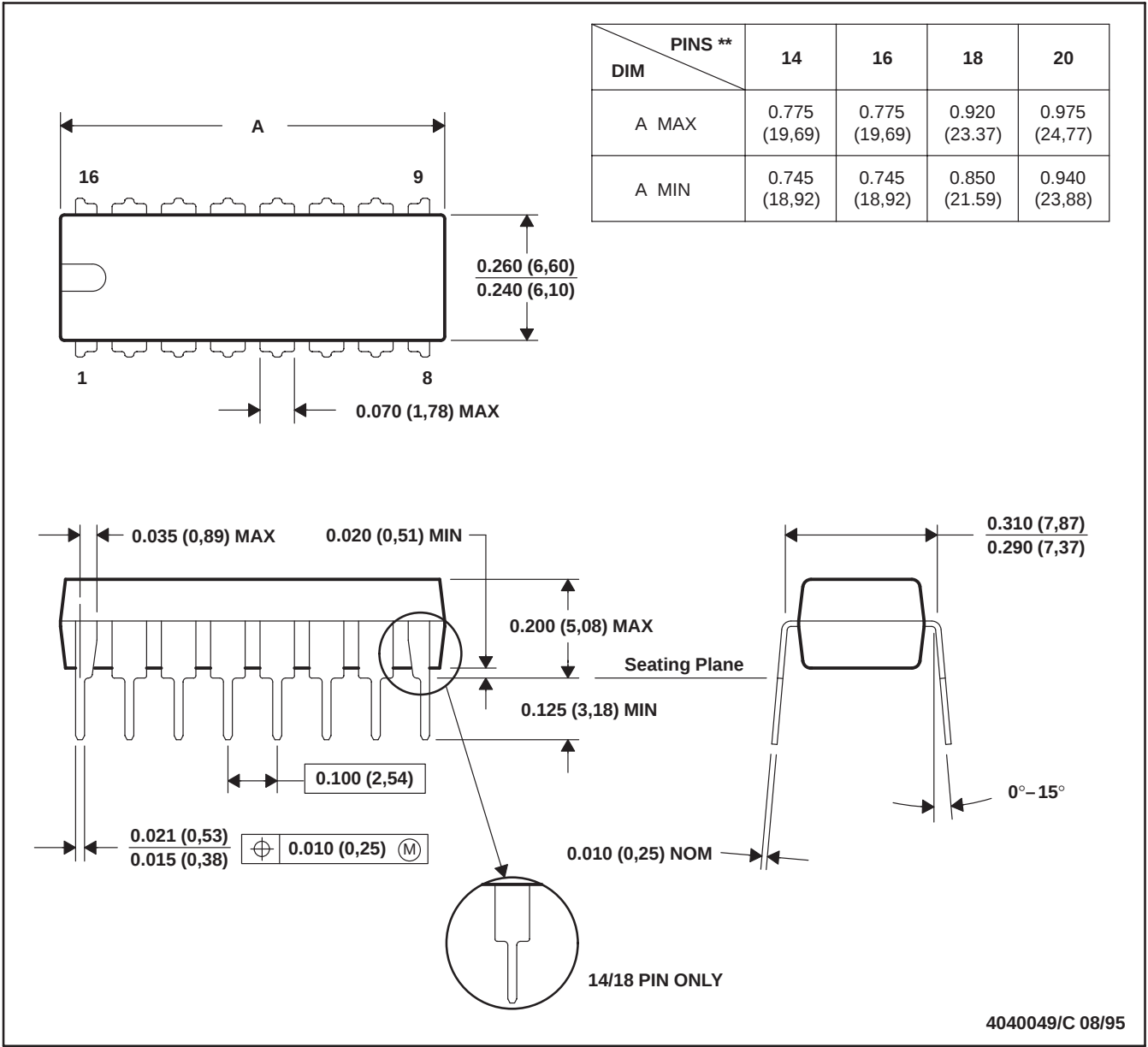
TPIC2701
7-CHANNEL COMMON-SOURCE POWER DMOS ARRAY

SLIS019A – SEPTEMBER 1992 – REVISED SEPTEMBER 1996

MECHANICAL INFORMATION

N (R-PDIP-T**)
16 PIN SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



- NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-001 (20 pin package is shorter than MS-001.)

IMPORTANT NOTICE

Texas Instruments and its subsidiaries (TI) reserve the right to make changes to their products or to discontinue any product or service without notice, and advise customers to obtain the latest version of relevant information to verify, before placing orders, that information being relied on is current and complete. All products are sold subject to the terms and conditions of sale supplied at the time of order acknowledgement, including those pertaining to warranty, patent infringement, and limitation of liability.

TI warrants performance of its semiconductor products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

CERTAIN APPLICATIONS USING SEMICONDUCTOR PRODUCTS MAY INVOLVE POTENTIAL RISKS OF DEATH, PERSONAL INJURY, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE ("CRITICAL APPLICATIONS"). TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS. INCLUSION OF TI PRODUCTS IN SUCH APPLICATIONS IS UNDERSTOOD TO BE FULLY AT THE CUSTOMER'S RISK.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards must be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance or customer product design. TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used. TI's publication of information regarding any third party's products or services does not constitute TI's approval, warranty or endorsement thereof.