Versatile EMI Reduction IC

Features

- FCC approved method of EMI attenuation
- Provides up to 20 dB of EMI suppression
- Generates a low EMI spread spectrum clock of the input frequency
- Optimized for 25 MHz to 60MHz input frequency range
- Internal loop filter minimizes external components and board space
- 4 selectable spread ranges
- SSON control pin for spread spectrum enable and disable options
- Characterizes to work with EMI-Lator®, EMC simulation program.
- Low cycle-to-cycle jitter
- 3.3 V or 5.0 V operating range
- 16 mA output drives
- TTL or CMOS compatible outputs
- Low power CMOS design
- Available in 8 pin SOIC and TSSOP

Product Description

The P2041 is a selectable spread spectrum frequency modulator designed specifically for PC peripheral and embedded controller markets .The P2041 reduces electromagnetic interference (EMI) at the clock source which provides system wide reduction of EMI of all clock dependent signals. The P2041 allows significant system cost savings by reducing the number of circuit board layers and shielding that are traditionally required to pass EMI regulations.

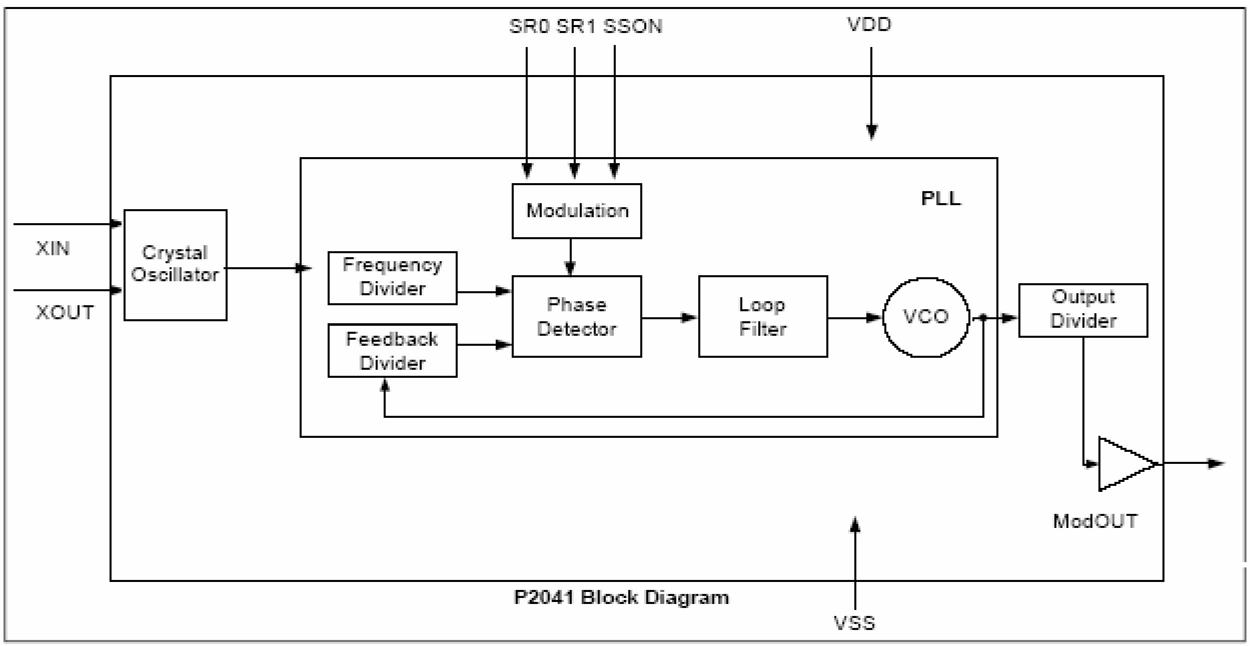
The P2041 uses the most efficient and optimized modulation profile approved by the FCC and is implemented in a proprietary all-digital method.

The P2041 modulates the output of a single PLL in order to “spread” the bandwidth of a synthesized clock and, more importantly, decreases the peak amplitudes of its harmonics. This results in significantly lower system EMI compared to the typical narrow band signal produced by oscillators and most frequency generators. Lowering EMI by increasing a signal’s bandwidth is called “spread spectrum clock generation”.

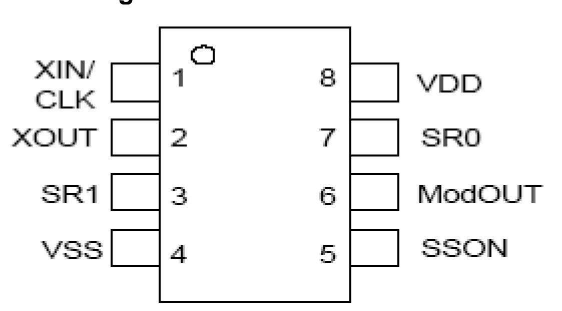
Applications

The P2041 is targeted towards the embedded controller market and PC peripheral markets including scanners, MFP’s, printers, PDA, IA , and GPS devices.

Block Diagram



Pin Configuration



Pin Description

Pin#	Pin Name	Type	Description
1	XIN/CLK	I	Connect to crystal or externally generated clock signal.
2	XOUT	I	Connect to crystal. No connect if externally generated clock signal is used.
3	SR1	I	Digital logic input used to select Spreading Range (see Table 1). This pin has an internal pull-up resistor.
4	VSS	P	Ground Connection. Connect to system ground.
5	SSON	I	Digital logic input used to enable Spread Spectrum function (Active Low). Spread Spectrum function enable when low. This pin has an internal pull-low resistor.
6	ModOUT	O	Spread Spectrum Clock Output.
7	SR0	I	Digital logic input used to select Spreading Range (see Table 1). This pin has an internal pull-up resistor.
8	VDD	P	Connect to +3.3V or +5.0V

Table 1 - Spread Range Selection

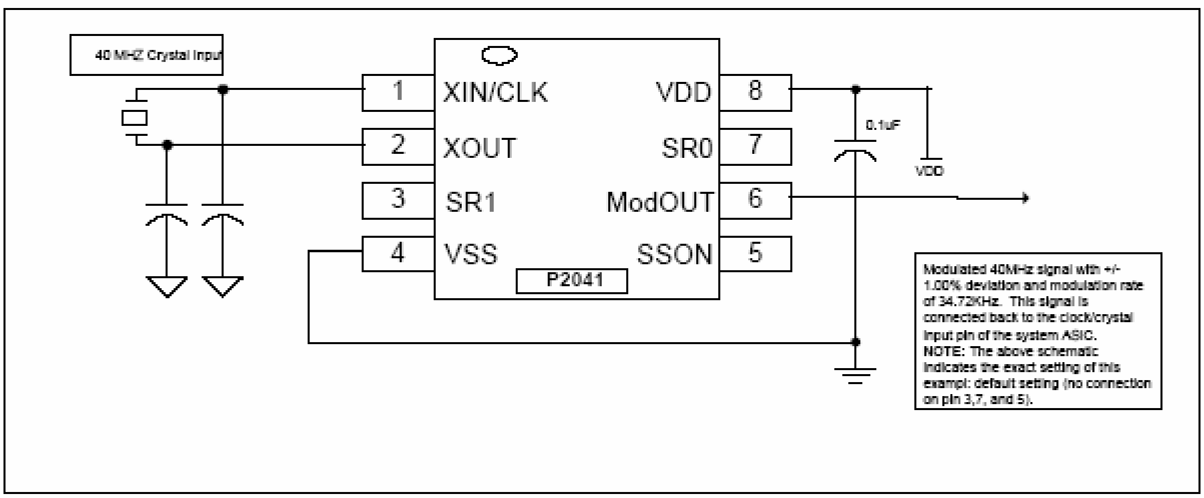
FS0	SR0	Spreading Range	Input Frequency	Modulation rate
0	0	+/- 1.50%	(Fin/40)*34.72 KHz	0
0	1	+/- 2.50%	(Fin/40)*34.72 KHz	0
1	0	+/- 0.50%	(Fin/40)*34.72 KHz**	1
1	1	+/- 1.00%	(Fin/40)*34.72 KHz**	1

Spread spectrum selection
Table 1 illustrates the possible spread spectrum options. The optimal setting should minimize system EMI to the fullest without affecting system performance. The spreading is described as a percentage deviation of the center frequency (Note: the center frequency is the frequency of the external reference input on CLKIN, Pin 1).

Example of a typical printer or scanner application that operates on a clock frequency of 40 MHz:
A spreading selection of SR1=1 and SR0=1 provides a percentage deviation of +/-1.00%* (see Table 1) of F_{cen}. This results in the frequency on ModOUT being swept from 40.40 MHz to 39.60 MHz at a modulation rate of 40/40*34.72=34.72 KHz (see Table 1). This particular example (see Figure below) given here is a common EMI reduction method for scanners and has already been implemented by most of the leading manufacturers.

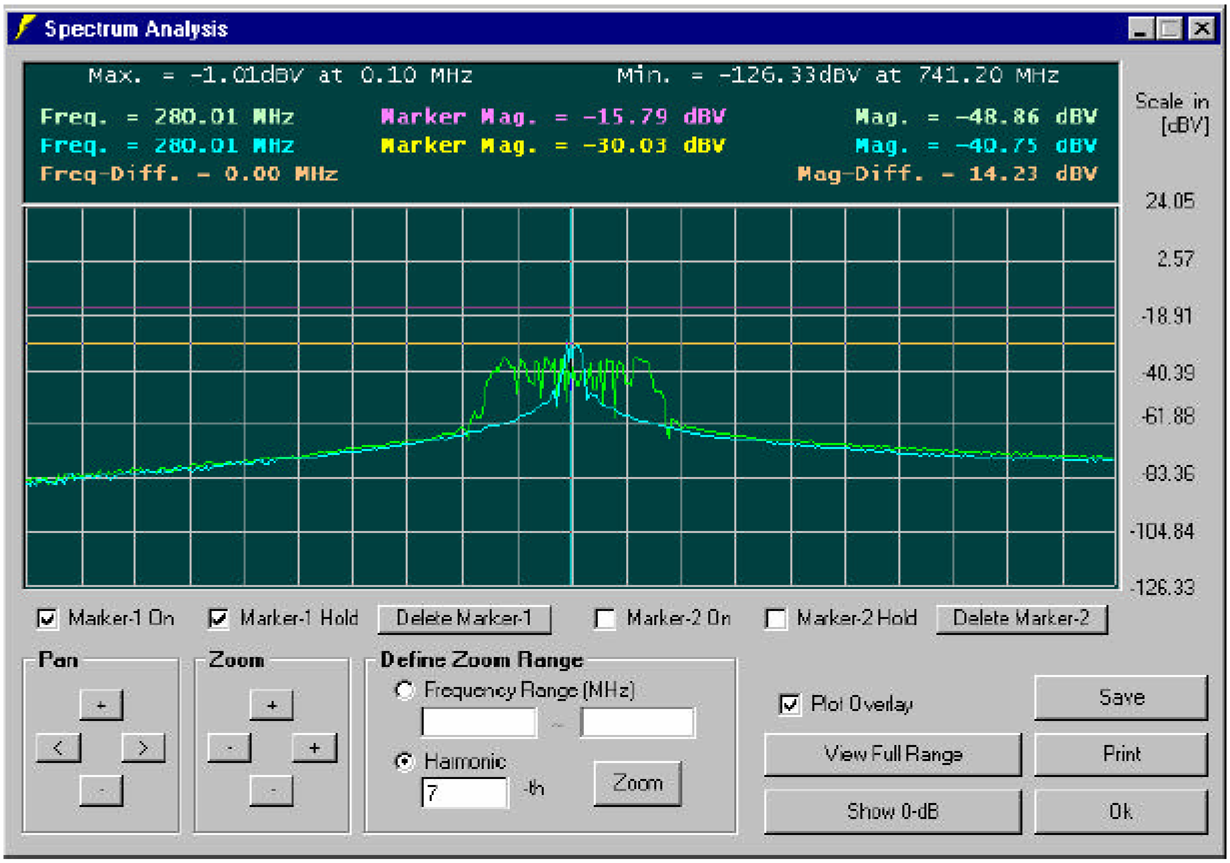
NOTE: Spreading range selection varies from different system manufacturers and their designs. The spreading range of P2041 can be set to +/-2.5% when working with certain scanner model.

P2041 Application Schematic for Flat-Bed Scanner



EMC Software Simulation
By using Alliance Semiconductor's proprietary EMC simulation software – EMI-lator®, radiated system level EMI analysis can be made easier to allow a quantitative assessment on Alliance's EMI reduction products. The simulation engine of this EMC software has already been characterized to correlate with the electrical characteristics of Alliance EMI reduction IC's. The figure below is an example of the simulation result. Please visit our web site at www.alsc.comfor information on how to obtain a free copy and demonstration of EMI-lator®.

Simulation Result from EMI-lator®



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Absolute Maximum Ratings

Symbol	Parameter	Rating	Unit
V_{DD}, V_{IN}	Voltage on any pin with respect to GND	-0.5 to + 7.0	V
T_{STG}	Storage temperature	-65 to +125	°C
T_A	Operating temperature	0 to +70	°C

DC Electrical Characteristics

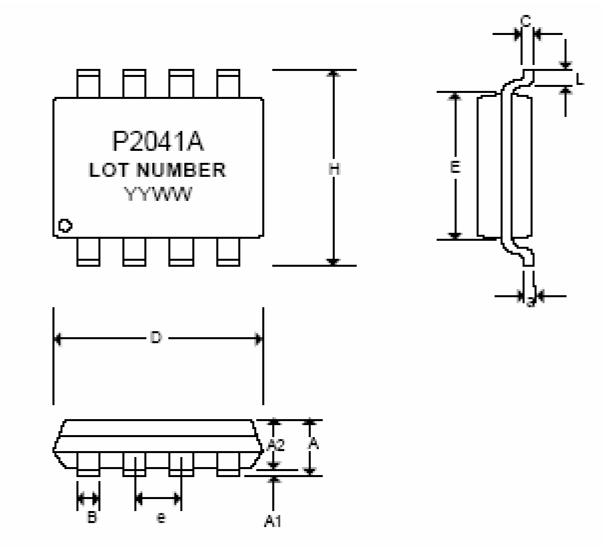
Symbol	Parameter	Min	Typ	Max	Unit
V_{IL}	Input Low Voltage	GND – 0.3	-	0.8	V
V_{IH}	Input High Voltage	2.0	-	V_{DD} + 0.3	V
I_{IL}	Input Low Current (pull-up resistor on inputs SR0, 1)	-	-	-35	µA
I_{IH}	Input High Current (pull-down resistor on input SSON)	-	-	35	µA
I_{XOL}	XOUT Output Low Current (@ 0.4V, V_{DD} = 3.3V)	-	3	-	mA
I_{XOH}	XOUT Output High Current (@ 2.5V, V_{DD} = 3.3V)	-	3	-	mA
V_{OL}	Output Low Voltage (V_{DD}=3.3V, I_{OL} = 20 mA)	-	-	0.4	V
V_{OH}	Output High Voltage (V_{DD}=3.3V, I_{OH} = 20 mA)	2.5	-	-	V
I_{DD}	Static Supply Current	-	0.6	-	mA
I_{CC}	Dynamic Supply Current (3.3V and 15 pF loading)	7	8.6	10	mA
V_{DD}	Operating Voltage	2.7	3.3	5.5	V

AC Electrical Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
f_{IN}	Input Frequency when	25	40	60	MHz
t_{LH}*	Output rise time (Measured at 0.8V to 2.0V)	0.7	0.9	1.1	ns
t_{HL}*	Output fall time (Measured at 0.8V to 2.0V)	0.6	0.8	1.0	ns
t_{JC}	Jitter (cycle to cycle)	-	-	360	ps
t_D	Output duty cycle	45	50	55	%
*t_{LH} and t_{HL} are measured into a capacitive load of 15pF					

Package Information

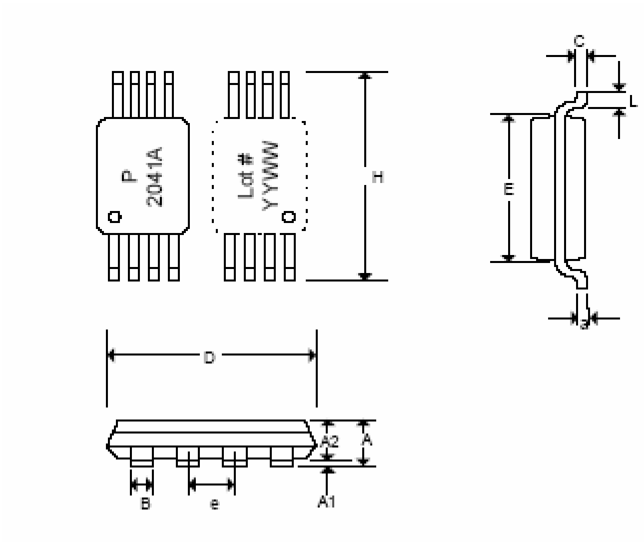
Mechanical Package Outline 8-Pin SOIC



Symbol	Dimensions in inches			Dimensions in millimeters		
	Min	Nor	Max	Min	Nor	Max
A	0.057	0.064	0.071	1.45	1.63	1.80
A1	0.004	0.007	0.010	0.10	0.18	0.25
A2	0.053	0.061	0.069	1.35	1.55	1.75
B	0.012	0.016	0.020	0.31	0.41	0.51
C	0.004	0.006	0.01	0.10	0.15	0.25
D	0.186	0.194	0.202	4.72	4.92	5.12
E	0.148	0.156	0.164	3.75	3.95	4.15
e	0.050 BSC			1.27 BSC		
H	0.224	0.236	0.248	5.70	6.00	6.30
L	0.012	0.020	0.028	0.30	0.50	0.70
a	0°	5°	8°	0°	5°	8°

Note: Controlling dimensions are millimeters

Mechanical Package Outline 8-Pin TSSOP



	Dimensions in inches			Dimensions in millimeters		
Symbol	**Min**	**Nor**	**Max**	**Min**	**Nor**	**Max**
A			0.047			1.10
A1	0.002		0.006	0.05		0.15
A2	0.031	0.039	0.041	0.80	1.00	1.05
B	0.007		0.012	0.19		0.30
C	0.004		0.008	0.09		0.20
D	0.114	0.118	0.122	2.90	3.00	3.10
E	0.169	0.173	0.177	4.30	4.40	4.50
e	0.026 BSC			0.65 BSC		
H	0.244	0.252	0.260	6.20	6.40	6.60
L	0.018	0.024	0.030	0.45	0.60	0.75
a	0°	5°	8°	0°	5°	8°

Note: Controlling dimensions are millimeters

Ordering Codes

Part Number	Marking	Package Type	Qty per reel	Temperature (°C)
P2041A-08ST	P2041A	8 PIN SOIC, TUBE		0 TO 70
P2041A-08SR	P2041A	8 PIN SOIC, TAPE & REEL	2,500	0 TO 70
P2041A-08TT	P2041A	8 PIN TSSOP, TUBE		0 TO 70
P2041A-08TR	P2041A	8 PIN TSSOP, TAPE & REEL	2,500	0 TO 70

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Preliminary datasheet. Specification subject to change without notice.

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