

- **Read Access Time - 200 ns**
- **Automatic Page Write Operation**
 - Internal Address and Data Latches for 256 Bytes
 - Internal Control Timer
- **Fast Write Cycle Time**
 - Page Write Cycle Time - 10 ms Maximum
 - 1 to 256 Byte Page Write Operation
- **Low Power Dissipation**
 - 80 mA Active Current
- **Hardware and Software Data Protection**
- **DATA Polling for End of Write Detection**
- **High Reliability CMOS Technology**
 - Endurance: 10,000 Cycles
 - Data Retention: 10 Years
- **Single 5V $\pm$ 10% Supply**
- **CMOS and TTL Compatible Inputs and Outputs**
- **JEDEC Approved Byte-Wide Pinout**

The AT28C040 is a high-performance electrically erasable and programmable read only memory (EEPROM). Its 4 megabits of memory is organized as 524,288 words by 8 bits. Manufactured with Atmel's advanced nonvolatile CMOS technology, the device offers access times to 200 ns with power dissipation of just 440 mW.

Pin Configurations

Pin Name	Function
A0 - A18	Addresses
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
I/O0 - I/O7	Data Inputs/Outputs
NC	No Connect

Pinout diagram of the 74VHC04 hex inverters. The chip has 14 pins. Pin 1 is ground (GND), pin 14 is VCC, and pin 7 is VCC. The inverters are located between pins 1-6, 6-14, and 14-7. The output of each inverter is indicated by a bubble at the output pin.

Pin	Function
1	GND
2	Input of Inverter 1
3	Input of Inverter 2
4	Input of Inverter 3
5	Input of Inverter 4
6	VCC
7	VCC
8	Output of Inverter 1
9	Output of Inverter 2
10	Output of Inverter 3
11	Output of Inverter 4
12	Input of Inverter 5
13	Input of Inverter 6
14	VCC
15	Output of Inverter 5
16	Output of Inverter 6
17	Output of Inverter 7
18	Output of Inverter 8
19	Output of Inverter 9
20	Output of Inverter 10
21	Output of Inverter 11
22	Output of Inverter 12
23	Output of Inverter 13
24	Output of Inverter 14
25	Output of Inverter 15
26	Output of Inverter 16
27	Output of Inverter 17
28	Output of Inverter 18
29	Output of Inverter 19
30	Output of Inverter 20
31	Output of Inverter 21
32	Output of Inverter 22
33	Output of Inverter 23
34	Output of Inverter 24
35	Output of Inverter 25
36	Output of Inverter 26
37	Output of Inverter 27
38	Output of Inverter 28
39	Output of Inverter 29
40	Output of Inverter 30
41	Output of Inverter 31
42	Output of Inverter 32
43	Output of Inverter 33
44	Output of Inverter 34
45	Output of Inverter 35
46	Output of Inverter 36
47	Output of Inverter 37
48	Output of Inverter 38
49	Output of Inverter 39
50	Output of Inverter 40
51	Output of Inverter 41
52	Output of Inverter 42
53	Output of Inverter 43
54	Output of Inverter 44
55	Output of Inverter 45
56	Output of Inverter 46
57	Output of Inverter 47
58	Output of Inverter 48
59	Output of Inverter 49
60	Output of Inverter 50
61	Output of Inverter 51
62	Output of Inverter 52
63	Output of Inverter 53
64	Output of Inverter 54
65	Output of Inverter 55
66	Output of Inverter 56
67	Output of Inverter 57
68	Output of Inverter 58
69	Output of Inverter 59
70	Output of Inverter 60
71	Output of Inverter 61
72	Output of Inverter 62
73	Output of Inverter 63
74	Output of Inverter 64
75	Output of Inverter 65
76	Output of Inverter 66
77	Output of Inverter 67
78	Output of Inverter 68
79	Output of Inverter 69
80	Output of Inverter 70
81	Output of Inverter 71
82	Output of Inverter 72
83	Output of Inverter 73
84	Output of Inverter 74
85	Output of Inverter 75
86	Output of Inverter 76
87	Output of Inverter 77
88	Output of Inverter 78
89	Output of Inverter 79
90	Output of Inverter 80
91	Output of Inverter 81
92	Output of Inverter 82
93	Output of Inverter 83
94	Output of Inverter 84
95	Output of Inverter 85
96	Output of Inverter 86
97	Output of Inverter 87
98	Output of Inverter 88
99	Output of Inverter 89
100	Output of Inverter 90

A18	1	32	VCC
A16	2	31	$\overline{\text{WE}}$
A15	3	30	A17
A12	4	29	A14
A7	5	28	A13
A6	6	27	A8
A5	7	26	A9
A4	8	25	A11
A3	9	24	$\overline{\text{OE}}$
A2	10	23	A10
A1	11	22	$\overline{\text{CE}}$
A0	12	21	I/O7
I/O0	13	20	I/O6
I/O1	14	19	I/O5
I/O2	15	18	I/O4
GND	16	17	I/O3



4-Megabit (512K x 8) Paged Parallel EEPROMs

AT28C040

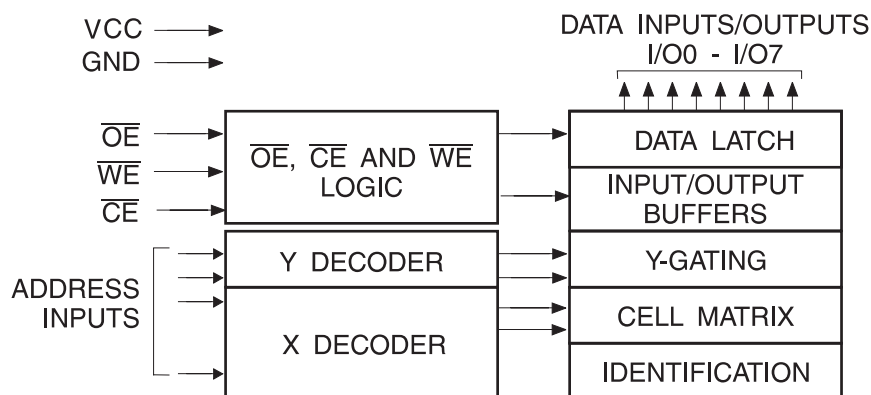
Rev. 0542B-10/98



The AT28C040 is accessed like a static RAM for the read or write cycle without the need for external components. The device contains a 256-byte page register to allow writing of up to 256 bytes simultaneously. During a write cycle, the address and 1 to 256 bytes of data are internally latched, freeing the address and data bus for other operations. Following the initiation of a write cycle, the device will automatically write the latched data using an internal control timer. The end of a write cycle can be detected by

$\overline{\text{DATA POLLING}}$ of I/O7. Once the end of a write cycle has been detected, a new access for a read or write can begin. Atmel's AT28C040 has additional features to ensure high quality and manufacturability. The device utilizes internal error correction for extended endurance and improved data retention characteristics. An optional software data protection mechanism is available to guard against inadvertent writes. The device also includes an extra 256 bytes of EEPROM for device identification or tracking.

Block Diagram



Absolute Maximum Ratings*

Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
All Input Voltages (including NC pins) with Respect to Ground	-0.6V to +6.25V
All Output Voltages with Respect to Ground	-0.6V to $V_{CC} + 0.6V$
Voltage on $\overline{\text{OE}}$ and A9 with Respect to Ground	-0.6V to +13.5V

***NOTICE:** Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Device Operation

READ: The AT28C040 is accessed like a static RAM. When $\overline{CE}$ and $\overline{OE}$ are low and $\overline{WE}$ is high, the data stored at the memory location determined by the address pins is asserted on the outputs. The outputs are put in the high impedance state when either $\overline{CE}$ or $\overline{OE}$ is high. This dual-line control gives designers flexibility in preventing bus contention in their systems.

BYTE WRITE: A low pulse on the $\overline{WE}$ or $\overline{CE}$ input with $\overline{CE}$ or $\overline{WE}$ low (respectively) and $\overline{OE}$ high initiates a write cycle. The address is latched on the falling edge of $\overline{CE}$ or $\overline{WE}$, whichever occurs last. The data is latched by the first rising edge of $\overline{CE}$ or $\overline{WE}$. Once a byte write has been started, it will automatically time itself to completion. Once a programming operation has been initiated and for the duration of t_{WC} , a read operation will effectively be a polling operation.

PAGE WRITE: The page write operation of the AT28C040 allows 1 to 256 bytes of data to be written into the device during a single internal programming period. A page write operation is initiated in the same manner as a byte write; the first byte written can then be followed by 1 to 255 additional bytes. Each successive byte must be written within 150 μs (t_{BLC}) of the previous byte. If the t_{BLC} limit is exceeded, the AT28C040 will cease accepting data and commence the internal programming operation. All bytes during a page write operation must reside on the same page as defined by the state of the A8 - A18 inputs. For each $\overline{WE}$ high to low transition during the page write operation, A8 - A18 must be the same.

The A0 to A7 inputs specify which bytes within the page are to be written. The bytes may be loaded in any order and may be altered within the same load period. Only bytes which are specified for writing will be written; unnecessary cycling of other bytes within the page does not occur.

DATA POLLING: The AT28C040 features $\overline{DATA}$ Polling to indicate the end of a write cycle. During a byte or page write cycle an attempted read of the last byte written will result in the complement of the written data to be presented on I/O7. Once the write cycle has been completed, true data is valid on all outputs, and the next write cycle may begin. $\overline{DATA}$ Polling may begin at anytime during the write cycle.

TOGGLE BIT: In addition to $\overline{DATA}$ Polling, the AT28C040 provides another method for determining the end of a write cycle. During the write operation, successive attempts to read data from the device will result in I/O6 toggling between one and zero. Once the write has completed, I/O6 will stop toggling and valid data will be read. Reading the toggle bit may begin at any time during the write cycle.

DATA PROTECTION: If precautions are not taken, inadvertent writes may occur during transitions of the host system power supply. Atmel has incorporated both hardware

and software features that will protect the memory against inadvertent writes.

HARDWARE PROTECTION: Hardware features protect against inadvertent writes to the AT28C040 in the following ways: (a) V_{CC} sense - if V_{CC} is below 3.8V (typical) the write function is inhibited; (b) V_{CC} power-on delay - once V_{CC} has reached 3.8V the device will automatically time out 5 ms (typical) before allowing a write; (c) write inhibit - holding any one of $\overline{OE}$ low, $\overline{CE}$ high or $\overline{WE}$ high inhibits write cycles; (d) noise filter - pulses of less than 15 ns (typical) on the $\overline{WE}$ or $\overline{CE}$ inputs will not initiate a write cycle.

SOFTWARE DATA PROTECTION: A software controlled data protection feature has been implemented on the AT28C040. When enabled, the software data protection (SDP), will prevent inadvertent writes. The SDP feature may be enabled or disabled by the user; the AT28C040 is shipped from Atmel with SDP disabled.

SDP is enabled when the host system issues a series of three write commands; three specific bytes of data are written to three specific addresses (refer to Software Data Protection Algorithm). After writing the 3-byte command sequence and after t_{WC} , the entire AT28C040 will be protected against inadvertent write operations. It should be noted that once protected, the host can still perform a byte or page write to the AT28C040. To do so, the same 3-byte command sequence used to enable SDP must precede the data to be written.

Once set, SDP will remain active unless the disable command sequence is issued. Power transitions do not disable SDP, and SDP will protect the AT28C040 during power-up and power-down conditions. All command sequences must conform to the page write timing specifications. The data in the enable and disable command sequences is not written to the device, and the memory addresses used in the sequence may be written with data in either a byte or page write operation.

After setting SDP, any attempt to write to the device without the 3-byte command sequence will start the internal write timers. No data will be written to the device; however, for the duration of t_{WC} , read operations will effectively be polling operations.

DEVICE IDENTIFICATION: An extra 256 bytes of EEPROM memory are available to the user for device identification. By raising A9 to 12V $\pm$ 0.5V and using address locations 7FF80H to 7FFFFH, the bytes may be written to or read from in the same manner as the regular memory array.

OPTIONAL CHIP ERASE MODE: The entire device can be erased using a 6-byte software erase code. Please see Software Chip Erase application note for details.

DC and AC Operating Range

		AT28C040-20		AT28C040-25	
		Operation		Operation	
		Read	Program	Read	Program
Operating Temperature (Case)	Commercial	0°C - 70°C	0°C - 70°C	0°C - 70°C	0°C - 70°C
	Industrial	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C
	Extended	-55°C - 125°C	-40°C - 85°C	-55°C - 125°C	-40°C - 85°C
V _{CC} Power Supply		5V ± 10%	5V ± 10%	5V ± 10%	5V ± 10%

Operating Modes

Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O
Read	V _{IL}	V _{IL}	V _{IH}	D _{OUT}
Write ⁽²⁾	V _{IL}	V _{IH}	V _{IL}	D _{IN}
Standby/Write Inhibit	V _{IH}	X ⁽¹⁾	X	High Z
Write Inhibit	X	X	V _{IH}	
Write Inhibit	X	V _{IL}	X	
Output Disable	X	V _{IH}	X	High Z

Notes: 1. X can be V_{IL} or V_{IH}.
2. Refer to AC Programming Waveforms.

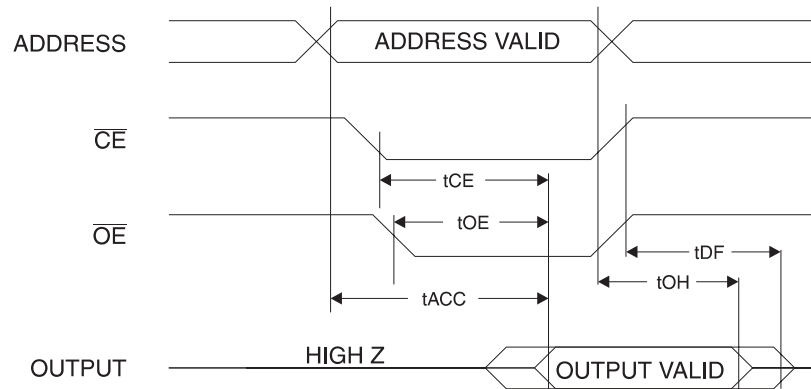
DC Characteristics

Symbol	Parameter	Condition	Min	Max	Units
I _{LI}	Input Load Current	V _{IN} = 0V to V _{CC} + 1V		10	μA
I _{LO}	Output Leakage Current	V _{I/O} = 0V to V _{CC}		10	μA
I _{SB1}	V _{CC} Standby Current CMOS	$\overline{CE} = V_{CC} - 0.3V$ to V _{CC} + 1V		3	mA
I _{SB2}	V _{CC} Standby Current TTL	$\overline{CE} = 2.0V$ to V _{CC} + 1V		3	mA
I _{CC}	V _{CC} Active Current	f = 5 MHz; I _{OUT} = 0 mA		80	mA
V _{IL}	Input Low Voltage			0.8	V
V _{IH}	Input High Voltage		2.0		V
V _{OL}	Output Low Voltage	I _{OL} = 2.1 mA		0.45	V
V _{OH1}	Output High Voltage	I _{OH} = -400 μA	2.4		V
V _{OH2}	Output High Voltage CMOS	I _{OH} = -100 μA; V _{CC} = 4.5V	4.2		V

AC Read Characteristics

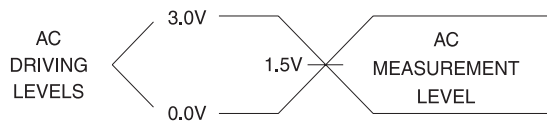
Symbol	Parameter	AT28C040-20		AT28C040-25		Units
		Min	Max	Min	Max	
t_{ACC}	Address to Output Delay		200		250	ns
$t_{CE}^{(1)}$	$\overline{CE}$ to Output Delay		200		250	ns
$t_{OE}^{(2)}$	$\overline{OE}$ to Output Delay	0	55	0	55	ns
$t_{DF}^{(3)(4)}$	$\overline{CE}$ or $\overline{OE}$ to Output Float	0	55	0	55	ns
t_{OH}	Output Hold from $\overline{OE}$, $\overline{CE}$ or Address, whichever occurred first	0		0		ns

AC Read Waveforms⁽¹⁾⁽²⁾⁽³⁾⁽⁴⁾



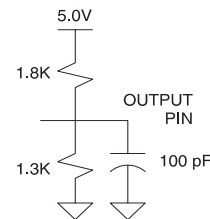
- Note:
- $\overline{CE}$ May be delayed up to $t_{ACC} - t_{CE}$ after the address transition without impact on t_{ACC} .
 - $\overline{OE}$ may be delayed up to $t_{CE} - t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{CE} or by $t_{ACC} - t_{OE}$ after an address change without impact on t_{ACC} .
 - t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first ($C_L = 5$ pF).
 - This parameter is characterized and is not 100% tested.

Input Test Waveforms and Measurement Level



$t_R, t_F < 5$ ns

Output Test Load



Pin Capacitance

$f = 1$ MHz, $T = 25^\circ\text{C}^{(1)}$

Symbol	Typ	Max	Units	Conditions
C_{IN}	4	10	pF	$V_{IN} = 0V$
C_{OUT}	8	12	pF	$V_{OUT} = 0V$

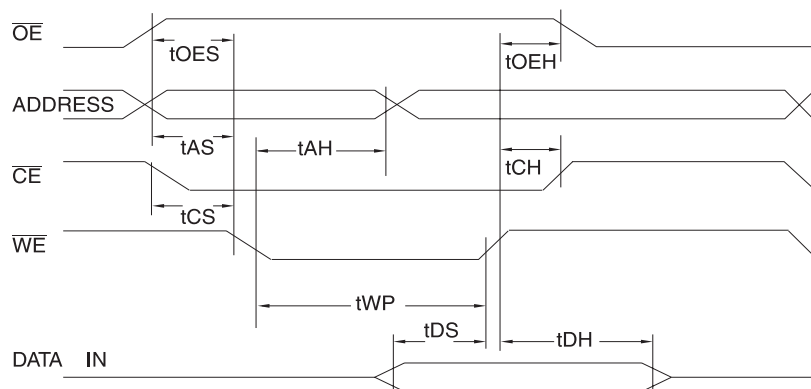
- Note:
- This parameter is characterized and is not 100% tested.

AC Write Characteristics

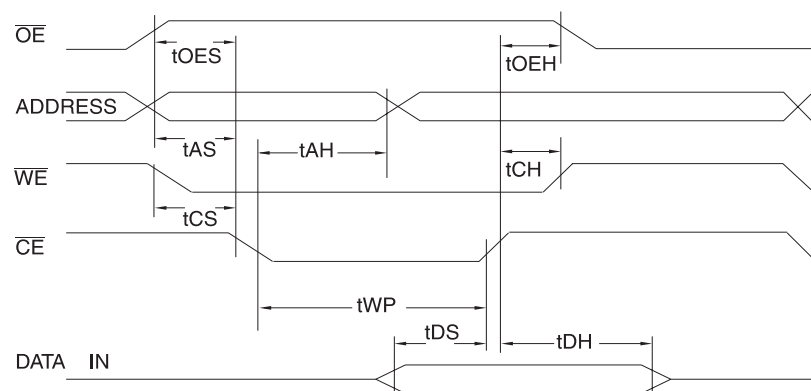
Symbol	Parameter	Min	Max	Units
t_{AS}, t_{OES}	Address, $\overline{OE}$ Set-up Time	0		ns
t_{AH}	Address Hold Time	50		ns
t_{CS}	Chip Select Set-up Time	0		ns
t_{CH}	Chip Select Hold Time	0		ns
t_{WP}	Write Pulse Width ($\overline{WE}$ or $\overline{CE}$)	100		ns
t_{DS}	Data Set-up Time	50		ns
t_{DH}, t_{OEH}	Data, $\overline{OE}$ Hold Time	0		ns

AC Write Waveforms

$\overline{WE}$ Controlled



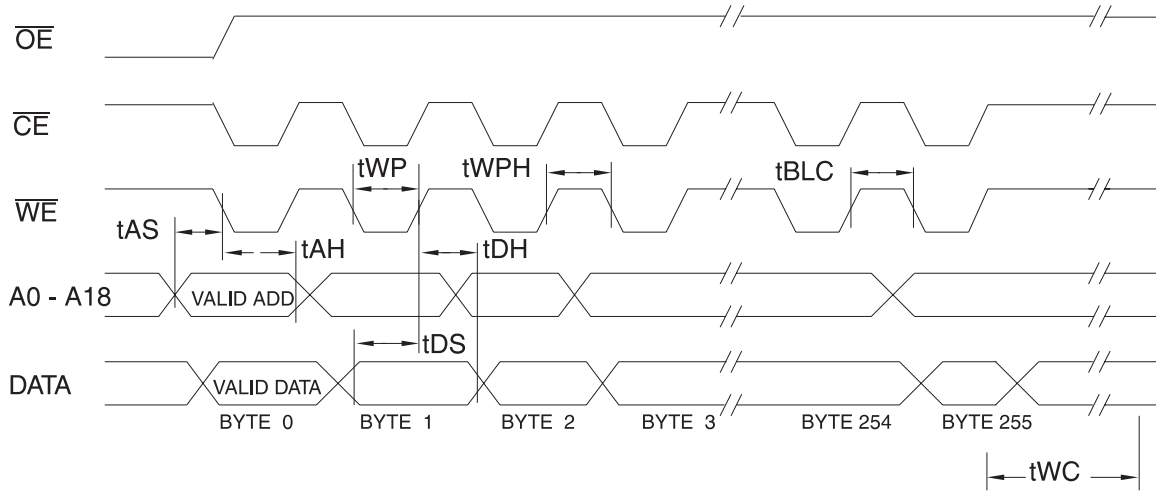
$\overline{CE}$ Controlled



Page Mode Characteristics

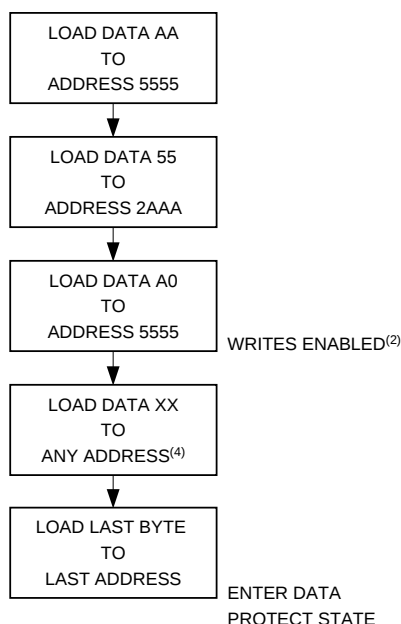
Symbol	Parameter	Min	Max	Units
t_{WC}	Write Cycle Time		10	ms
t_{AS}	Address Set-up Time	0		ns
t_{AH}	Address Hold Time	50		ns
t_{DS}	Data Set-up Time	50		ns
t_{DH}	Data Hold Time	0		ns
t_{WP}	Write Pulse Width	100		ns
t_{BLC}	Byte Load Cycle Time		150	μ s
t_{WPH}	Write Pulse Width High	50		ns

Page Mode Write Waveforms⁽¹⁾⁽²⁾



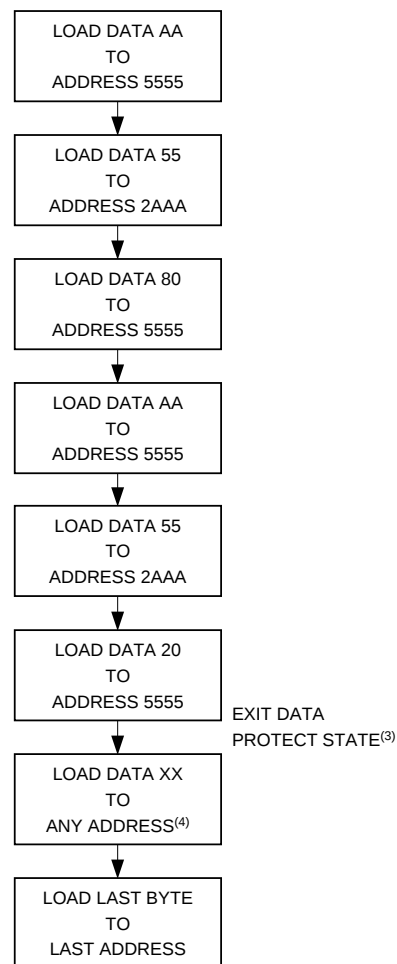
- Notes:
1. A8 through A18 must specify the page address during each high to low transition of $\overline{WE}$ (or $\overline{CE}$).
 2. $\overline{OE}$ must be high only when $\overline{WE}$ and $\overline{CE}$ are both low.

Software Data Protection Enable Algorithm⁽¹⁾

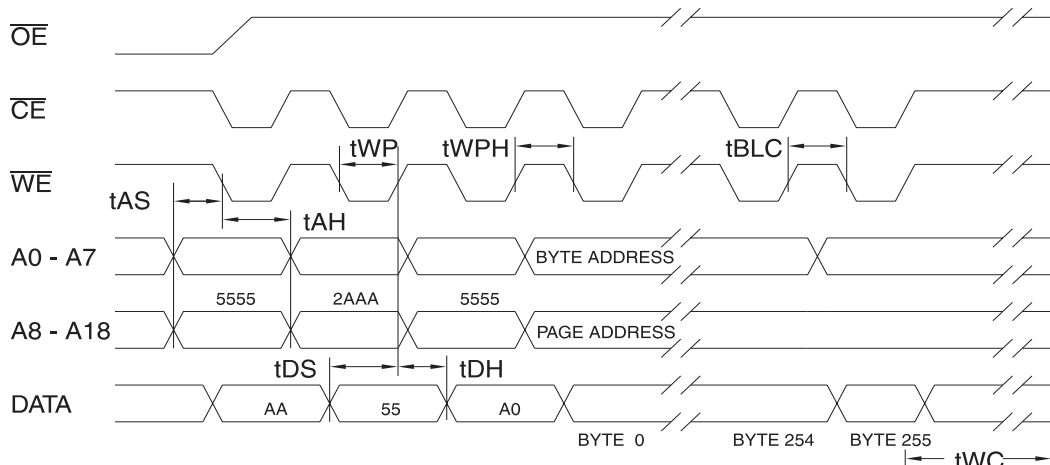


- Notes:
1. Data Format: I/O7 - I/O0 (Hex);
Address Format: A14 - A0 (Hex).
 2. Write Protect state will be activated at end of write even if no other data is loaded.
 3. Write Protect state will be deactivated at end of write period even if no other data is loaded.
 4. 1 to 256 bytes of data are loaded.

Software Data Protection Disable Algorithm⁽¹⁾



Software Protected Program Cycle Waveform⁽¹⁾⁽²⁾⁽³⁾



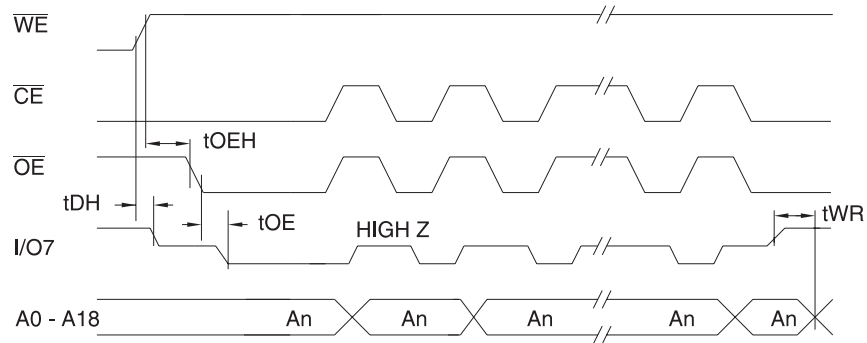
- Notes:
1. A0 - A14 must conform to the addressing sequence for the first 3 bytes as shown above.
 2. After the command sequence has been issued and a page write operation follows, the page address inputs (A8 - A18) must be the same for each high to low transition of $\overline{WE}$ (or $\overline{CE}$).
 3. $\overline{OE}$ must be high only when $\overline{WE}$ and $\overline{CE}$ are both low.

Data Polling Characteristics⁽¹⁾

Symbol	Parameter	Min	Typ	Max	Units
t_{DH}	Data Hold Time	10			ns
$t_{OE\overline{H}}$	$\overline{OE}$ Hold Time	10			ns
t_{OE}	$\overline{OE}$ to Output Delay ⁽²⁾				ns
t_{WR}	Write Recovery Time	0			ns

Notes: 1. These parameters are characterized and not 100% tested.
2. See AC Read Characteristics.

Data Polling Waveforms

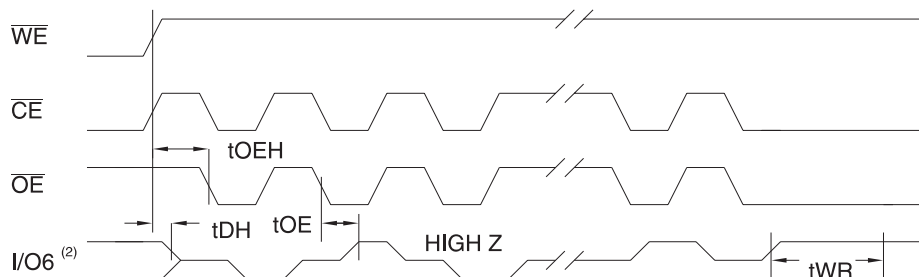


Toggle Bit Characteristics⁽¹⁾

Symbol	Parameter	Min	Typ	Max	Units
t_{DH}	Data Hold Time	10			ns
$t_{OE\overline{H}}$	$\overline{OE}$ Hold Time	10			ns
t_{OE}	$\overline{OE}$ to Output Delay ⁽²⁾				ns
t_{OEHP}	$\overline{OE}$ High Pulse	150			ns
t_{WR}	Write Recovery Time	0			ns

Notes: 1. These parameters are characterized and not 100% tested.
2. See AC Read Characteristics.

Toggle Bit Waveforms⁽¹⁾⁽²⁾⁽³⁾



Notes: 1. Toggling either OE or CE or both OE and CE will operate toggle bit.
2. Beginning and ending state of I/O6 will vary.
3. Any address location may be used but the address should not vary.



Ordering Information⁽¹⁾

t _{ACC} (ns)	I _{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
200	80	3	AT28C040-20BC	32B	Commercial (0° to 70°C)
			AT28C040-20FC	32F	
			AT28C040-20LC	44L	
	80	3	AT28C040-20BI	32B	Industrial (-40° to 85°C)
			AT28C040-20FI	32F	
			AT28C040-20LI	44L	
	80	3	AT28C040-20BI SL703	32B	Extended (See DC and AC Operating Range Table)
			AT28C040-20FI SL703	32F	
			AT28C040-20LI SL703	44L	
250	80	3	AT28C040-25BC	32B	Commercial (0° to 70°C)
			AT28C040-25FC	32F	
			AT28C040-25LC	44L	
	80	3	AT28C040-25BI	32B	Industrial (-40° to 85°C)
			AT28C040-25FI	32F	
			AT28C040-25LI	44L	
	80	3	AT28C040-25BI SL703	32B	Extended (See DC and AC Operating Range Table)
			AT28C040-25FI SL703	32F	
			AT28C040-25LI SL703	44L	

Note: 1. See Valid Part Numbers.

Valid Part Numbers

The following table lists standard Atmel products that can be ordered.

Device Numbers	Speed	Package and Temperature Combinations
AT28C040	20	BC, BI, FC, FI, LC, LI, BI SL703, FI SL703, LI SL703
AT28C040	25	BC, BI, FC, FI, LC, LI, BI SL703, FI SL703, LI SL703

Die Products

Reference Section: Parallel EEPROM Die Products

Package Type	
32B	32-Lead, 0.600" Wide, Ceramic Side Braze Dual Inline (Side Braze)
32F	32-Lead, Non-Windowed, Ceramic Bottom-Brazed Flat Package (Flatpack)
44L	44-Pad, Non-Windowed, Ceramic Leadless Chip Carrier (LCC)
Options	
Blank	Standard Device: Endurance = 10K Write Cycles; Write Time = 10 ms



Atmel Headquarters

Corporate Headquarters

2325 Orchard Parkway
San Jose, CA 95131
TEL (408) 441-0311
FAX (408) 487-2600

Europe

Atmel U.K., Ltd.
Coliseum Business Centre
Riverside Way
Camberley, Surrey GU15 3YL
England
TEL (44) 1276-686677
FAX (44) 1276-686697

Asia

Atmel Asia, Ltd.
Room 1219
Chinachem Golden Plaza
77 Mody Road
Tsimshatsui East
Kowloon, Hong Kong
TEL (852) 27219778
FAX (852) 27221369

Japan

Atmel Japan K.K.
Tonetsu Shinkawa Bldg., 9F
1-24-8 Shinkawa
Chuo-ku, Tokyo 104-0033
Japan
TEL (81) 3-3523-3551
FAX (81) 3-3523-7581

Atmel Operations

Atmel Colorado Springs

1150 E. Cheyenne Mtn. Blvd.
Colorado Springs, CO 80906
TEL (719) 576-3300
FAX (719) 540-1759

Atmel Rousset

Zone Industrielle
13106 Rousset Cedex, France
TEL (33) 4 42 53 60 00
FAX (33) 4 42 53 60 01

Fax-on-Demand

North America:
1-(800) 292-8635
International:
1-(408) 441-0732

e-mail

literature@atmel.com

Web Site

<http://www.atmel.com>

BBS

1-(408) 436-4309

© Atmel Corporation 1998.

Atmel Corporation makes no warranty for the use of its products, other than those expressly contained in the Company's standard warranty which is detailed in Atmel's Terms and Conditions located on the Company's website. The Company assumes no responsibility for any errors which may appear in this document, reserves the right to change devices or specifications detailed herein at any time without notice, and does not make any commitment to update the information contained herein. No licenses to patents or other intellectual property of Atmel are granted by the Company in connection with the sale of Atmel products, expressly or by implication. Atmel's products are not authorized for use as critical components in life support devices or systems.

Marks bearing ® and/or ™ are registered trademarks and trademarks of Atmel Corporation.

Terms and product names in this document may be trademarks of others.



Printed on recycled paper.

0542B-10/98/xM