

ADS42xx Dual-Channel, 14-Bit, 12-Bit, 160, 125, 65 MSPS Ultralow-Power ADC

1 Features

- Ultralow power with single 1.8-V Supply, CMOS output:
 - 183 mW Total power at 65 MSPS
 - 277 mW Total power at 125 MSPS
 - 332 mW Total power at 160 MSPS
- High dynamic performance:
 - 88-dBc SFDR at 170 MHz
 - 71.4-dBFS SNR at 170 MHz
- Crosstalk: > 90 dB at 185 MHz
- Programmable gain up to 6 dB for SNR/SFDR trade-off
- DC offset correction
- Output interface options:
 - 1.8-V parallel CMOS interface
 - Double data rate (DDR) LVDS with programmable swing:
 - Standard swing: 350 mV
 - Low swing: 200 mV
- Supports low input clock amplitude down to 200 mV_{PP}
- Package: VQFN-64 (9.00 mm × 9.00 mm)

2 Applications

- Wireless communications infrastructure
- Software-defined radio
- Power amplifier linearization

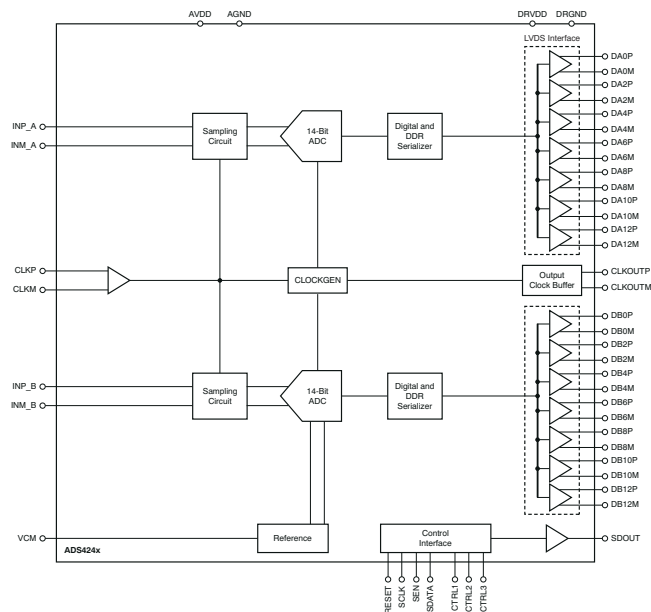
3 Description

The ADS424x and ADS422x family of devices are low-speed variants of the ADS42xx ultralow-power family of dual-channel, 14-bit or 12-bit analog-to-digital converters (ADCs). Innovative design techniques are used to achieve high-dynamic performance, while consuming extremely low power with 1.8-V supply. This topology makes the ADS424x/422x well-suited for multi-carrier, wide-bandwidth communications applications.

Package Information

| PART NUMBER | PACKAGE ⁽¹⁾ | BODY SIZE (NOM) |
|-------------|------------------------|-------------------|
| ADS4222 | VQFN (64) | 9.00 mm × 9.00 mm |
| ADS4225 | | |
| ADS4226 | | |
| ADS4242 | | |
| ADS4245 | | |
| ADS4246 | | |

(1) For all available packages, see the orderable addendum at the end of the data sheet.



ADS4222, 25, 26, 42, 45, 46 Block Diagram



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| Changes from Revision D (December 2015) to Revision E (February 2023) | Page |
|--|-------------|
| • Changed the Device Information table to the <i>Package Information</i> table..... | 1 |
| • Changed VQFN (48) to VQFN (64) in the <i>Package Information</i> table..... | 1 |
| • Changed the <i>Pin Configuration and Functions</i> . Updated the Pin Functions tables and pinout images..... | 5 |

| Changes from Revision C (March 2011) to Revision D (December 2015) | Page |
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| • Added <i>ESD Ratings</i> table, <i>Feature Description</i> section, <i>Device Functional Modes</i> , <i>Application and Implementation</i> section, <i>Power Supply Recommendations</i> section, <i>Layout</i> section, <i>Device and Documentation Support</i> section, and <i>Mechanical, Packaging, and Orderable Information</i> section. | 1 |

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| • Changed device status from Mixed Status to Production Data..... | 1 |
| • Changed 125MSPS sub-bullet of first Features bullet..... | 1 |
| • Changed sub-bullets of second Features bullet..... | 1 |
| • Changed description of pin 64 in Pin Descriptions: LVDS Mode table..... | 5 |
| • Changed description of pin 64 in Pin Descriptions: CMOS Mode table..... | 7 |
| • Changed ADS4246 $f_{IN} = 170$ MHz <i>Worst spur</i> typical specification in the ADS4246/ADS4245/ADS4242 Electrical Characteristics table..... | 11 |
| • Added ADS4225/ADS4222 $f_{IN} = 70$ MHz <i>SNR</i> , <i>SINAD</i> , <i>SFDR</i> , <i>THD</i> , <i>HD2</i> , <i>HD3</i> , and <i>Worst spur</i> minimum and typical specifications in the ADS4226/ADS4225/ADS4222 Electrical Characteristics table..... | 14 |
| • Added ADS4225/ADS4222 <i>DNL</i> minimum and maximum specifications in the ADS4226/ADS4225/ADS4222 Electrical Characteristics table..... | 14 |
| • Added ADS4225/ADS4222 <i>INL</i> maximum specifications in the ADS4226/ADS4225/ADS4222 Electrical Characteristics table..... | 14 |

| | |
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| • Changed ADS4242/ADS4222 Power Supply, <i>Digital power LVDS interface</i> typical specification in Electrical Characteristics: General table..... | 17 |
| • Changed ADS4245/ADS4225 Power Supply, <i>Digital power CMOS interface</i> typical specification in Electrical Characteristics: General table..... | 17 |
| • Moved High-Performance Modes into separate table..... | 20 |
| • Changed description of READOUT disabled in <i>Serial Register Readout</i> section..... | 61 |
| • Updated Figure 8-18 | 61 |
| • Changed READOUT description in <i>Register Address 00h</i> section..... | 69 |
| • Changed CLKOUT FALL POSN and CLKOUT RISE POSN description in <i>Register Address 42h</i> section..... | 69 |

Changes from Revision A (May 2011) to Revision B (May 2011)

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| | |
|--|----|
| • Changed sub-bullets of first Features bullet..... | 1 |
| • Updated description of NC pin in LVDS Pin Descriptions table..... | 5 |
| • Updated description of NC pin in CMOS Pin Descriptions table..... | 7 |
| • Changed <i>ENOB</i> , <i>DNL</i> , and <i>INL</i> test conditions in the Electrical Characteristics: ADS4246/ADS4245/ADS4242 table | 11 |
| • Deleted <i>INL</i> minimum specifications from Electrical Characteristics: ADS4246/ADS4245/ADS4242 table..... | 11 |
| • Changed <i>INL</i> maximum specifications in the Electrical Characteristics: ADS4246/ADS4245/ADS4242 table.... | 11 |
| • Changed <i>ENOB</i> , <i>DNL</i> , and <i>INL</i> test conditions in the Electrical Characteristics: ADS4226/ADS4225/ADS4222 table | 14 |
| • Changed ADS4226 <i>INL</i> maximum specification in the Electrical Characteristics: ADS4226/ADS4225/ADS4222 table..... | 14 |
| • Changed Power Supply, <i>IDRVDD</i> and <i>Digital power CMOS interface</i> rows in the Electrical Characteristics: General table..... | 17 |
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5 Description (continued)

The ADS424x/422x have gain options that can be used to improve SFDR performance at lower full-scale input ranges. These devices include a dc offset correction loop that can be used to cancel the ADC offset. Both DDR (double data rate) LVDS and parallel CMOS digital output interfaces are available in a compact VQFN-64 package.

The devices include internal references while the traditional reference pins and associated decoupling capacitors have been eliminated. All devices are specified over the industrial temperature range (–40°C to 85°C).

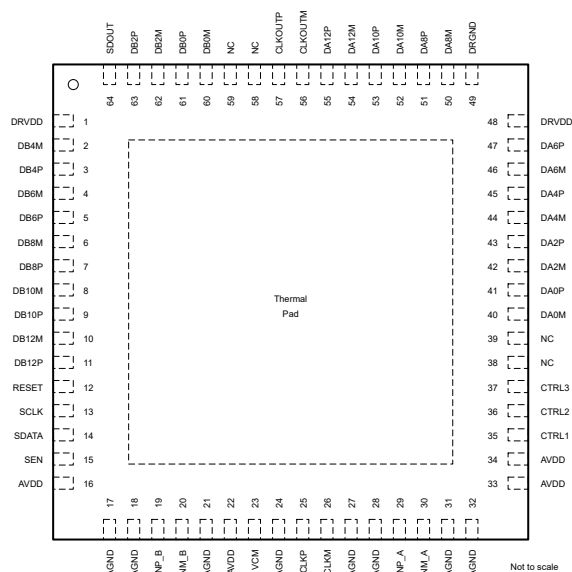
Table 5-1. ADS424x, 422x Family Comparison

| DEVICE FAMILY ⁽¹⁾ | 250 MSPS | 160 MSPS | 125 MSPS | 65 MSPS |
|------------------------------|-------------------------|-------------------------|-------------------------|-------------------------|
| ADS424x 14-bit family | ADS4249 | ADS4246 | ADS4245 | ADS4242 |
| ADS422x 12-bit family | ADS4229 | ADS4226 | ADS4225 | ADS4222 |

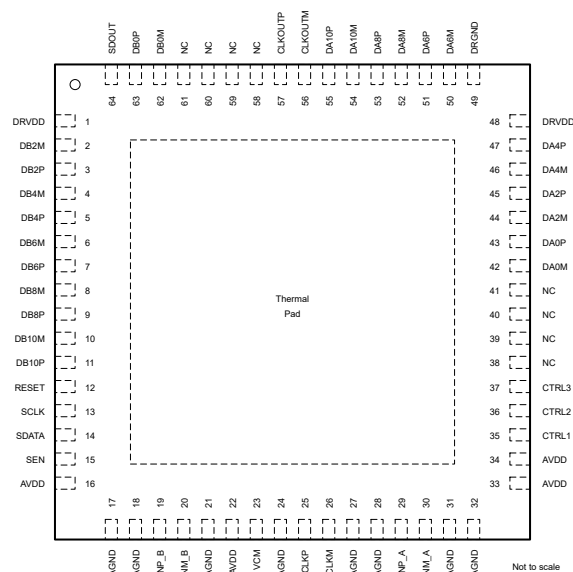
(1) See [Table 8-1](#) for details on migrating from the ADS62P49 family.

6 Pin Configuration and Functions

Pin Functions – LVDS Mode



**Figure 6-1. ADS4246, ADS4245, and ADS4242
RGC Package
64-Pin VQFN With Exposed Thermal Pad
LVDS Mode (Top View)**



**Figure 6-2. ADS4226, ADS4225, and ADS4222
RGC Package
64-Pin VQFN With Exposed Thermal Pad
LVDS Mode (Top View)**

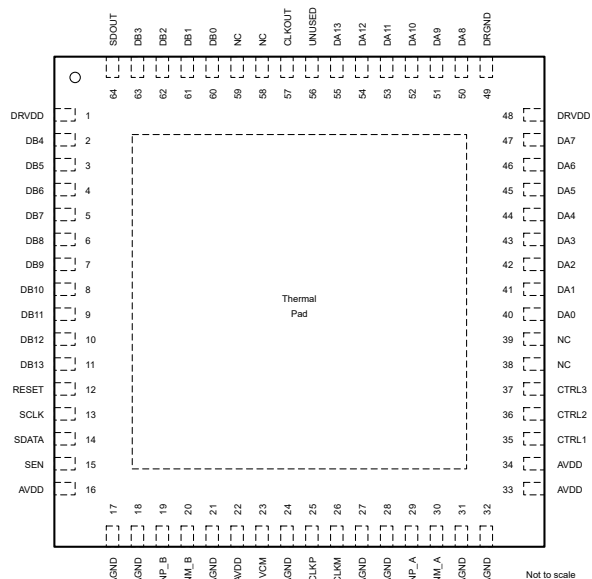
Table 6-1. Pin Functions

| NAME | PIN | | TYPE | DESCRIPTION |
|---------|--------------------------------|--------------------------------|--------|--|
| | ADS4246, 45, 42 | ADS4226, 25, 22 | | |
| AGND | 17, 18, 21, 24, 27, 28, 31, 32 | 17, 18, 21, 24, 27, 28, 31, 32 | Input | Analog ground |
| AVDD | 16, 22, 33, 34 | 16, 22, 33, 34 | Input | Analog power supply |
| CLKM | 26 | 26 | Input | Differential clock negative input |
| CLKOUTM | 56 | 56 | Output | Differential output clock, complement |
| CLKOUTP | 57 | 57 | Output | Differential output clock, true |
| CLKP | 25 | 25 | Input | Differential clock positive input |
| CTRL1 | 35 | 35 | Input | Digital control input pins. Together, they control the various power-down modes. |
| CTRL2 | 36 | 36 | Input | Digital control input pins. Together, they control the various power-down modes. |
| CTRL3 | 37 | 37 | Input | Digital control input pins. Together, they control the various power-down modes. |
| DA0P | 41 | 43 | Output | Channel A differential output data pair, D0 and D1 multiplexed |
| DA0M | 40 | 42 | Output | Channel A differential output data pair, D0 and D1 multiplexed |
| DA2P | 43 | 45 | Output | Channel A differential output data D2 and D3 multiplexed |
| DA2M | 42 | 44 | Output | Channel A differential output data D2 and D3 multiplexed |
| DA4P | 45 | 47 | Output | Channel A differential output data D4 and D5 multiplexed |
| DA4M | 44 | 46 | Output | Channel A differential output data D4 and D5 multiplexed |
| DA6P | 47 | 51 | Output | Channel A differential output data D6 and D7 multiplexed |
| DA6M | 46 | 50 | Output | Channel A differential output data D6 and D7 multiplexed |
| DA8P | 51 | 53 | Output | Channel A differential output data D8 and D9 multiplexed |
| DA8M | 50 | 52 | Output | Channel A differential output data D8 and D9 multiplexed |
| DA10P | 53 | 55 | Output | Channel A differential output data D10 and D11 multiplexed |
| DA10M | 52 | 54 | Output | Channel A differential output data D10 and D11 multiplexed |

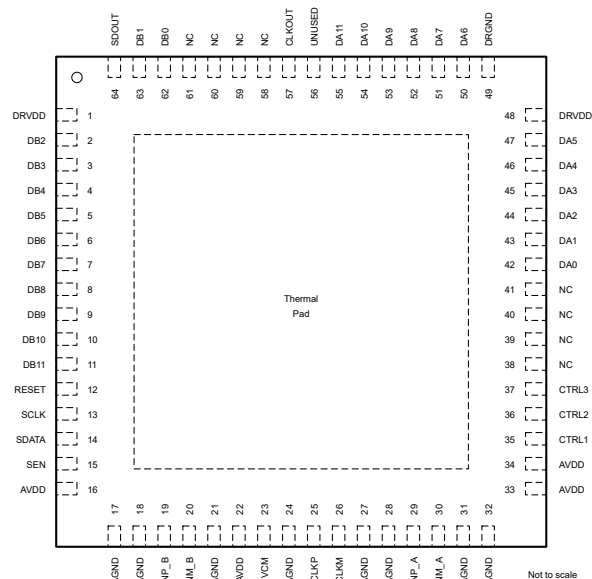
Table 6-1. Pin Functions (continued)

| NAME | PIN | | TYPE | DESCRIPTION |
|-------|--|--------------------------------|--------|--|
| | ADS4246, 45, 42 | ADS4226, 25, 22 | | |
| DA12M | 54 | -- | Output | Channel A differential output data D12 and D13 multiplexed (ADS424x only) |
| DA12P | 55 | -- | Output | Channel A differential output data D12 and D13 multiplexed (ADS424x only) |
| DB0P | 61 | 63 | Output | Channel B differential output data pair, D0 and D1 multiplexed |
| DB0M | 60 | 62 | Output | Channel B differential output data pair, D0 and D1 multiplexed |
| DB2P | 63 | 3 | Output | Channel B differential output data D2 and D3 multiplexed |
| DB2M | 62 | 2 | Output | Channel B differential output data D2 and D3 multiplexed |
| DB4P | 3 | 5 | Output | Channel B differential output data D4 and D5 multiplexed |
| DB4M | 2 | 4 | Output | Channel B differential output data D4 and D5 multiplexed |
| DB6P | 5 | 7 | Output | Channel B differential output data D6 and D7 multiplexed |
| DB6M | 4 | 6 | Output | Channel B differential output data D6 and D7 multiplexed |
| DB8P | 7 | 9 | Output | Channel B differential output data D8 and D9 multiplexed |
| DB8M | 6 | 8 | Output | Channel B differential output data D8 and D9 multiplexed |
| DB10P | 9 | 11 | Output | Channel B differential output data D10 and D11 multiplexed |
| DB10M | 8 | 10 | Output | Channel B differential output data D10 and D11 multiplexed |
| DB12P | 11 | -- | Output | Channel B differential output data D12 and D13 multiplexed (ADS424x only) |
| DB12M | 10 | -- | Output | Channel B differential output data D12 and D13 multiplexed (ADS424x only) |
| DRGND | 49, PAD | 49, PAD | Input | Output buffer ground. The Thermal PAD is connected to DRGND |
| DRVDD | 1, 48 | 1, 48 | Input | Output buffer supply |
| INM_A | 30 | 30 | Input | Differential analog negative input, channel A |
| INM_B | 20 | 20 | Input | Differential analog negative input, channel B |
| INP_A | 29 | 29 | Input | Differential analog positive input, channel A |
| INP_B | 19 | 19 | Input | Differential analog positive input, channel B |
| NC | 38, 39, 58, 59 Refer to Figure 7-28 , Figure 7-29 , and Figure 7-45 | 38, 39, 40, 41, 58, 59, 60, 61 | — | Do not connect, must be floated |
| RESET | 12 | 12 | Input | Serial interface RESET input. When using the serial interface mode, the internal registers must be initialized through a hardware RESET by applying a high pulse on this pin or by using the software reset option; refer to the Section 8.5.3 section. In parallel interface mode, the RESET pin must be permanently tied high. SCLK and SEN are used as parallel control pins in this mode. This pin has an internal 150-kΩ pulldown resistor. |
| SCLK | 13 | 13 | Input | This pin functions as a serial interface clock input when RESET is low. It controls the low-speed mode selection when RESET is tied high; see Table 8-6 for detailed information. This pin has an internal 150-kΩ pulldown resistor. |
| SDATA | 14 | 14 | Input | Serial interface data input; this pin has an internal 150-kΩ pulldown resistor. |
| SDOUT | 64 | 64 | Output | This pin functions as a serial interface register readout when the READOUT bit is enabled. When READOUT = 0, this pin is in high-impedance state. |
| SEN | 15 | 15 | Input | This pin functions as a serial interface enable input when RESET is low. It controls the output interface and data format selection when RESET is tied high; see Table 8-7 for detailed information. This pin has an internal 150-kΩ pullup resistor to AVDD. |
| VCM | 23 | 23 | Output | This pin outputs the common-mode voltage (0.95 V) that can be used externally to bias the analog input pins |

Pin Functions – CMOS Mode



**Figure 6-3. ADS4246, ADS4245, and ADS4242
RGC Package
64-Pin VQFN With Exposed Thermal Pad
CMOS Mode (Top View)**



**Figure 6-4. ADS4226, ADS4225, and ADS4222
RGC Package
64-Pin VQFN With Exposed Thermal Pad
CMOS Mode (Top View)**

Table 6-2. Pin Functions

| NAME | PIN | | TYPE | DESCRIPTION |
|--------|--------------------------------|--------------------------------|--------|--|
| | ADS4246, 45, 42 | ADS4226, 25, 22 | | |
| AGND | 17, 18, 21, 24, 27, 28, 31, 32 | 17, 18, 21, 24, 27, 28, 31, 32 | Input | Analog ground |
| AVDD | 16, 22, 33, 34 | 16, 22, 33, 34 | Input | Analog power supply |
| CLKM | 26 | 26 | Input | Differential clock negative input |
| CLKOUT | 57 | 57 | Output | CMOS output clock |
| CLKP | 25 | 25 | Input | Differential clock positive input |
| CTRL1 | 35 | 35 | Input | Digital control input pins. Together, they control various power-down modes. |
| CTRL2 | 36 | 36 | Input | Digital control input pins. Together, they control various power-down modes. |
| CTRL3 | 37 | 37 | Input | Digital control input pins. Together, they control various power-down modes. |
| DA0 | 40 | 42 | Output | Channel A ADC output data bits, CMOS levels |
| DA1 | 41 | 43 | Output | Channel A ADC output data bits, CMOS levels |
| DA2 | 42 | 44 | Output | Channel A ADC output data bits, CMOS levels |
| DA3 | 43 | 45 | Output | Channel A ADC output data bits, CMOS levels |
| DA4 | 44 | 46 | Output | Channel A ADC output data bits, CMOS levels |
| DA5 | 45 | 47 | Output | Channel A ADC output data bits, CMOS levels |
| DA6 | 46 | 50 | Output | Channel A ADC output data bits, CMOS levels |
| DA7 | 47 | 51 | Output | Channel A ADC output data bits, CMOS levels |
| DA8 | 50 | 52 | Output | Channel A ADC output data bits, CMOS levels |
| DA9 | 51 | 53 | Output | Channel A ADC output data bits, CMOS levels |
| DA10 | 52 | 54 | Output | Channel A ADC output data bits, CMOS levels |
| DA11 | 53 | 55 | Output | Channel A ADC output data bits, CMOS levels |
| DA12 | 54 | -- | Output | Channel A ADC output data bits, CMOS levels (ADS424x only) |
| DA13 | 55 | -- | Output | Channel A ADC output data bits, CMOS levels (ADS424x only) |
| DB0 | 60 | 62 | Output | Channel B ADC output data bits, CMOS levels |

Table 6-2. Pin Functions (continued)

| NAME | PIN | | TYPE | DESCRIPTION |
|--------|-----------------|--------------------------------|--------|---|
| | ADS4246, 45, 42 | ADS4226, 25, 22 | | |
| DB1 | 61 | 63 | Output | Channel B ADC output data bits, CMOS levels |
| DB2 | 62 | 2 | Output | Channel B ADC output data bits, CMOS levels |
| DB3 | 63 | 3 | Output | Channel B ADC output data bits, CMOS levels |
| DB4 | 2 | 4 | Output | Channel B ADC output data bits, CMOS levels |
| DB5 | 3 | 5 | Output | Channel B ADC output data bits, CMOS levels |
| DB6 | 4 | 6 | Output | Channel B ADC output data bits, CMOS levels |
| DB7 | 5 | 7 | Output | Channel B ADC output data bits, CMOS levels |
| DB8 | 6 | 8 | Output | Channel B ADC output data bits, CMOS levels |
| DB9 | 7 | 9 | Output | Channel B ADC output data bits, CMOS levels |
| DB10 | 8 | 10 | Output | Channel B ADC output data bits, CMOS levels |
| DB11 | 9 | 11 | Output | Channel B ADC output data bits, CMOS levels |
| DB12 | 10 | -- | Output | Channel B ADC output data bits, CMOS levels (ADS424x only) |
| DB13 | 11 | -- | Output | Channel B ADC output data bits, CMOS levels (ADS424x only) |
| DRGND | 49, PAD | 49, PAD | Input | Output buffer ground. The Thermal PAD is connected to DRGND |
| DRVDD | 1, 48 | 1, 48 | Input | Output buffer supply |
| INM_A | 30 | 30 | Input | Differential analog negative input, channel A |
| INM_B | 20 | 20 | Input | Differential analog negative input, channel B |
| INP_A | 29 | 29 | Input | Differential analog positive input, channel A |
| INP_B | 19 | 19 | Input | Differential analog positive input, channel B |
| NC | 38, 39, 58, 59 | 38, 39, 40, 41, 58, 59, 60, 61 | — | Do not connect, must be floated |
| RESET | 12 | 12 | Input | Serial interface RESET input. When using the serial interface mode, the internal registers must be initialized through a hardware RESET by applying a high pulse on this pin or by using the software reset option; refer to the Serial Interface Configuration section. In parallel interface mode, the RESET pin must be permanently tied high. SDATA and SEN are used as parallel control pins in this mode. This pin has an internal 150-kΩ pulldown resistor. |
| SCLK | 13 | 13 | Input | This pin functions as a serial interface clock input when RESET is low. It controls the low-speed mode when RESET is tied high; see Table 8-6 for detailed information. This pin has an internal 150-kΩ pulldown resistor. |
| SDATA | 14 | 14 | Input | Serial interface data input; this pin has an internal 150-kΩ pulldown resistor. |
| SDOUT | 64 | 64 | Output | This pin functions as a serial interface register readout when the READOUT bit is enabled. When READOUT = 0, this pin is in high-impedance state. |
| SEN | 15 | 15 | Input | This pin functions as a serial interface enable input when RESET is low. It controls the output interface and data format selection when RESET is tied high; see Table 8-7 for detailed information. This pin has an internal 150-kΩ pullup resistor to AVDD. |
| UNUSED | 56 | 56 | — | This pin is not used in the CMOS interface |
| VCM | 23 | 23 | Output | This pin outputs the common-mode voltage (0.95 V) that can be used externally to bias the analog input pins |

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

| | | MIN | MAX | UNIT |
|---|---|------|------------------------------|------|
| Supply voltage range, AVDD | | –0.3 | 2.1 | V |
| Supply voltage range, DRVDD | | –0.3 | 2.1 | V |
| Voltage between AGND and DRGND | | –0.3 | 0.3 | V |
| Voltage between AVDD to DRVDD (when AVDD leads DRVDD) | | –2.4 | 2.4 | V |
| Voltage between DRVDD to AVDD (when DRVDD leads AVDD) | | –2.4 | 2.4 | V |
| Voltage applied to input pins | INP_A, INM_A, INP_B, INM_B | –0.3 | Minimum (1.9, AVDD + 0.3) | V |
| | CLKP, CLKM ⁽²⁾ | –0.3 | AVDD + 0.3 | V |
| | RESET, SCLK, SDATA, SEN, CTRL1, CTRL2, CTRL3 | –0.3 | 3.9 | V |
| Operating free-air temperature range, T _A | | –40 | 85 | °C |
| Operating junction temperature range, T _J | | | 125 | °C |
| Storage temperature range, T _{stg} | | –65 | 150 | °C |

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) When AVDD is turned off, it is recommended to switch off the input clock (or ensure the voltage on CLKP, CLKM is less than |0.3 V|). This configuration prevents the ESD protection diodes at the clock input pins from turning on.

7.2 ESD Ratings

| | | VALUE | UNIT |
|--|--|-------|------|
| V _(ESD) Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾ | ±2000 | V |
| | Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾ | ±500 | |

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

Over operating free-air temperature range, unless otherwise noted.

| | | MIN | NOM | MAX | UNIT |
|--|---|------------|-----|------|-----------------|
| SUPPLIES | | | | | |
| Analog supply voltage, AVDD | | 1.7 | 1.8 | 1.9 | V |
| Digital supply voltage, DRVDD | | 1.7 | 1.8 | 1.9 | V |
| ANALOG INPUTS | | | | | |
| Differential input voltage range | | 2 | | | V _{PP} |
| Input common-mode voltage | | VCM ± 0.05 | | | V |
| Maximum analog input frequency with 2 V _{PP} input amplitude ⁽¹⁾ | | 400 | | | MHz |
| Maximum analog input frequency with 1 V _{PP} input amplitude ⁽¹⁾ | | 600 | | | MHz |
| CLOCK INPUT | | | | | |
| Input clock sample rate (ADS4242/ADS4222) | Low-speed mode enabled (by default after reset) | 1 | 65 | MSPS | |
| Input clock sample rate (ADS4245/ADS4225) | Low-speed mode enabled ⁽²⁾ | 1 | 80 | MSPS | |
| | Low-speed mode disabled ⁽²⁾ (by default after reset) | 80 | 125 | | |
| Input clock sample rate (ADS4246/ADS4226) | Low-speed mode enabled ⁽²⁾ | 1 | 80 | MSPS | |
| | Low-speed mode disabled ⁽²⁾ (by default after reset) | 80 | 160 | MSPS | |

7.3 Recommended Operating Conditions (continued)

Over operating free-air temperature range, unless otherwise noted.

| | | MIN | NOM | MAX | UNIT |
|--|-----------------------------------|-----|-----|-----|--------------------|
| Input clock amplitude differential ($V_{CLKP} - V_{CLKM}$) | Sine wave, ac-coupled | 0.2 | 1.5 | | V_{PP} |
| | LVPECL, ac-coupled | | 1.6 | | V_{PP} |
| | LVDS, ac-coupled | | 0.7 | | V_{PP} |
| | LVC MOS, single-ended, ac-coupled | | 1.5 | | V |
| INPUT CLOCK DUTY CYCLE | | | | | |
| Low-speed mode disabled | | 35% | 50% | 65% | |
| Low-speed mode enabled | | 40% | 50% | 60% | |
| DIGITAL OUTPUTS | | | | | |
| Maximum external load capacitance from each output pin to DRGND, C_{LOAD} | | | 5 | | pF |
| Differential load resistance between the LVDS output pairs (LVDS mode), R_{LOAD} | | | 100 | | Ω |
| Operating free-air temperature, T_A | | –40 | | 85 | $^{\circ}\text{C}$ |

(1) See the [Application Information](#) section.

(2) See the [Serial Interface Configuration](#) section for details on programming the low-speed mode.

7.4 Thermal Information

| THERMAL METRIC | | ADS42xx | UNIT |
|----------------------|--|------------|----------------------|
| | | RGC (VQFN) | |
| | | 64 PINS | |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 23.9 | $^{\circ}\text{C/W}$ |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 10.9 | $^{\circ}\text{C/W}$ |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 4.3 | $^{\circ}\text{C/W}$ |
| Ψ_{JT} | Junction-to-top characterization parameter | 0.1 | $^{\circ}\text{C/W}$ |
| Ψ_{JB} | Junction-to-board characterization parameter | 4.4 | $^{\circ}\text{C/W}$ |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | 0.6 | $^{\circ}\text{C/W}$ |

7.5 Electrical Characteristics: ADS4246, ADS4245, ADS4242

Typical values are at 25°C, AVDD = 1.8 V, DRVDD = 1.8 V, 50% clock duty cycle, –1 dBFS differential analog input, LVDS interface, and 0-dB gain, unless otherwise noted. Minimum and maximum values are across the full temperature range: T_{MIN} = –40°C to T_{MAX} = 85°C, AVDD = 1.8 V, and DRVDD = 1.8 V.

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|--------------------------------------|-------|---------------------------|--------------------|------|------|-----|------|
| Resolution | | | | | | 14 | Bits |
| Signal-to-noise ratio | SNR | f _{IN} = 20 MHz | ADS4246 (160 MSPS) | | 72.8 | | dBFS |
| | | | ADS4245 (125 MSPS) | | 73.4 | | |
| | | | ADS4242 (65 MSPS) | | 73.6 | | |
| | | f _{IN} = 70 MHz | ADS4246 (160 MSPS) | | 72.5 | | dBFS |
| | | | ADS4245 (125 MSPS) | 70 | 72.9 | | |
| | | | ADS4242 (65 MSPS) | 69.5 | 72.5 | | |
| | | f _{IN} = 100 MHz | ADS4246 (160 MSPS) | | 72.2 | | dBFS |
| | | | ADS4245 (125 MSPS) | | 72.6 | | |
| | | | ADS4242 (65 MSPS) | | 72.3 | | |
| | | f _{IN} = 170 MHz | ADS4246 (160 MSPS) | 69 | 71.2 | | dBFS |
| | | | ADS4245 (125 MSPS) | | 71.4 | | |
| | | | ADS4242 (65 MSPS) | | 70.4 | | |
| | | f _{IN} = 300 MHz | ADS4246 (160 MSPS) | | 69.4 | | dBFS |
| | | | ADS4245 (125 MSPS) | | 69.3 | | |
| | | | ADS4242 (65 MSPS) | | 69.4 | | |
| Signal-to-noise and distortion ratio | SINAD | f _{IN} = 20 MHz | ADS4246 (160 MSPS) | | 72.6 | | dBFS |
| | | | ADS4245 (125 MSPS) | | 73.2 | | |
| | | | ADS4242 (65 MSPS) | | 73.5 | | |
| | | f _{IN} = 70 MHz | ADS4246 (160 MSPS) | | 72.1 | | dBFS |
| | | | ADS4245 (125 MSPS) | 69 | 72.6 | | |
| | | | ADS4242 (65 MSPS) | 68.5 | 72.3 | | |
| | | f _{IN} = 100 MHz | ADS4246 (160 MSPS) | | 71.7 | | dBFS |
| | | | ADS4245 (125 MSPS) | | 72.3 | | |
| | | | ADS4242 (65 MSPS) | | 72.1 | | |
| | | f _{IN} = 170 MHz | ADS4246 (160 MSPS) | 67.5 | 70.8 | | dBFS |
| | | | ADS4245 (125 MSPS) | | 71.2 | | |
| | | | ADS4242 (65 MSPS) | | 70.2 | | |
| | | f _{IN} = 300 MHz | ADS4246 (160 MSPS) | | 68 | | dBFS |
| | | | ADS4245 (125 MSPS) | | 68.5 | | |
| | | | ADS4242 (65 MSPS) | | 68.2 | | |
| Spurious-free dynamic range | SFDR | f _{IN} = 20 MHz | ADS4246 (160 MSPS) | | 86 | | dBc |
| | | | ADS4245 (125 MSPS) | | 88 | | |
| | | | ADS4242 (65 MSPS) | | 91 | | |
| | | f _{IN} = 70 MHz | ADS4246 (160 MSPS) | | 84 | | dBc |
| | | | ADS4245 (125 MSPS) | 73.5 | 86 | | |
| | | | ADS4242 (65 MSPS) | 73.5 | 88 | | |
| | | f _{IN} = 100 MHz | ADS4246 (160 MSPS) | | 82 | | dBc |
| | | | ADS4245 (125 MSPS) | | 85 | | |
| | | | ADS4242 (65 MSPS) | | 87 | | |
| | | f _{IN} = 170 MHz | ADS4246 (160 MSPS) | 72 | 82 | | dBc |
| | | | ADS4245 (125 MSPS) | | 88 | | |
| | | | ADS4242 (65 MSPS) | | 85 | | |
| | | f _{IN} = 300 MHz | ADS4246 (160 MSPS) | | 78 | | dBc |
| | | | ADS4245 (125 MSPS) | | 78 | | |
| | | | ADS4242 (65 MSPS) | | 74 | | |

7.5 Electrical Characteristics: ADS4246, ADS4245, ADS4242 (continued)

Typical values are at 25°C, AVDD = 1.8 V, DRVDD = 1.8 V, 50% clock duty cycle, –1 dBFS differential analog input, LVDS interface, and 0-dB gain, unless otherwise noted. Minimum and maximum values are across the full temperature range: T_{MIN} = –40°C to T_{MAX} = 85°C, AVDD = 1.8 V, and DRVDD = 1.8 V.

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|----------------------------|---------------------------|--------------------------|--------------------|------|-----|-----|------|
| Total harmonic distortion | THD | f _{IN} = 20 MHz | ADS4246 (160 MSPS) | | 84 | | dBc |
| | | | ADS4245 (125 MSPS) | | 86 | | |
| | | | ADS4242 (65 MSPS) | | 88 | | |
| | f _{IN} = 70 MHz | | ADS4246 (160 MSPS) | | 81 | | dBc |
| | | | ADS4245 (125 MSPS) | 72 | 84 | | |
| | | | ADS4242 (65 MSPS) | 72 | 85 | | |
| | f _{IN} = 100 MHz | | ADS4246 (160 MSPS) | | 81 | | dBc |
| | | | ADS4245 (125 MSPS) | | 83 | | |
| | | | ADS4242 (65 MSPS) | | 85 | | |
| | f _{IN} = 170 MHz | | ADS4246 (160 MSPS) | 70 | 80 | | dBc |
| | | | ADS4245 (125 MSPS) | | 84 | | |
| | | | ADS4242 (65 MSPS) | | 82 | | |
| | f _{IN} = 300 MHz | | ADS4246 (160 MSPS) | | 76 | | dBc |
| | | | ADS4245 (125 MSPS) | | 75 | | |
| | | | ADS4242 (65 MSPS) | | 73 | | |
| Second-harmonic distortion | HD2 | f _{IN} = 20 MHz | ADS4246 (160 MSPS) | | 86 | | dBc |
| | | | ADS4245 (125 MSPS) | | 88 | | |
| | | | ADS4242 (65 MSPS) | | 91 | | |
| | f _{IN} = 70 MHz | | ADS4246 (160 MSPS) | | 84 | | dBc |
| | | | ADS4245 (125 MSPS) | 73.5 | 86 | | |
| | | | ADS4242 (65 MSPS) | 73.5 | 88 | | |
| | f _{IN} = 100 MHz | | ADS4246 (160 MSPS) | | 82 | | dBc |
| | | | ADS4245 (125 MSPS) | | 85 | | |
| | | | ADS4242 (65 MSPS) | | 87 | | |
| | f _{IN} = 170 MHz | | ADS4246 (160 MSPS) | 72 | 82 | | dBc |
| | | | ADS4245 (125 MSPS) | | 88 | | |
| | | | ADS4242 (65 MSPS) | | 85 | | |
| | f _{IN} = 300 MHz | | ADS4246 (160 MSPS) | | 78 | | dBc |
| | | | ADS4245 (125 MSPS) | | 78 | | |
| | | | ADS4242 (65 MSPS) | | 74 | | |
| Third-harmonic distortion | HD3 | f _{IN} = 20 MHz | ADS4246 (160 MSPS) | | 92 | | dBc |
| | | | ADS4245 (125 MSPS) | | 93 | | |
| | | | ADS4242 (65 MSPS) | | 95 | | |
| | f _{IN} = 70 MHz | | ADS4246 (160 MSPS) | | 86 | | dBc |
| | | | ADS4245 (125 MSPS) | 73.5 | 89 | | |
| | | | ADS4242 (65 MSPS) | 73.5 | 90 | | |
| | f _{IN} = 100 MHz | | ADS4246 (160 MSPS) | | 93 | | dBc |
| | | | ADS4245 (125 MSPS) | | 89 | | |
| | | | ADS4242 (65 MSPS) | | 96 | | |
| | f _{IN} = 170 MHz | | ADS4246 (160 MSPS) | 72 | 94 | | dBc |
| | | | ADS4245 (125 MSPS) | | 90 | | |
| | | | ADS4242 (65 MSPS) | | 87 | | |
| | f _{IN} = 300 MHz | | ADS4246 (160 MSPS) | | 80 | | dBc |
| | | | ADS4245 (125 MSPS) | | 81 | | |
| | | | ADS4242 (65 MSPS) | | 81 | | |

7.5 Electrical Characteristics: ADS4246, ADS4245, ADS4242 (continued)

Typical values are at 25°C, AVDD = 1.8 V, DRVDD = 1.8 V, 50% clock duty cycle, –1 dBFS differential analog input, LVDS interface, and 0-dB gain, unless otherwise noted. Minimum and maximum values are across the full temperature range: T_{MIN} = –40°C to T_{MAX} = 85°C, AVDD = 1.8 V, and DRVDD = 1.8 V.

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---------------------------|---|--------------------|-------|------|------|-------------|
| Worst spur (other than second and third harmonics) | f _{IN} = 20 MHz | ADS4246 (160 MSPS) | | | 90 | | dBc |
| | | ADS4245 (125 MSPS) | | | 95 | | |
| | | ADS4242 (65 MSPS) | | | 98 | | |
| | f _{IN} = 70 MHz | ADS4246 (160 MSPS) | | | 92 | | dBc |
| | | ADS4245 (125 MSPS) | | 78 | 94 | | |
| | | ADS4242 (65 MSPS) | | 79 | 97 | | |
| | f _{IN} = 100 MHz | ADS4246 (160 MSPS) | | | 89 | | dBc |
| | | ADS4245 (125 MSPS) | | | 93 | | |
| | | ADS4242 (65 MSPS) | | | 95 | | |
| | f _{IN} = 170 MHz | ADS4246 (160 MSPS) | | 77 | 89 | | dBc |
| | | ADS4245 (125 MSPS) | | | 91 | | |
| | | ADS4242 (65 MSPS) | | | 93 | | |
| | f _{IN} = 300 MHz | ADS4246 (160 MSPS) | | | 91 | | dBc |
| | | ADS4245 (125 MSPS) | | | 89 | | |
| | | ADS4242 (65 MSPS) | | | 92 | | |
| Two-tone intermodulation distortion | IMD | f ₁ = 46 MHz, f ₂ = 50 MHz, each tone at –7 dBFS | ADS4246 (160 MSPS) | | 96 | | dBFS |
| | | | ADS4245 (125 MSPS) | | 96 | | |
| | | | ADS4242 (65 MSPS) | | 98 | | |
| | | f ₁ = 185 MHz, f ₂ = 190 MHz, each tone at –7 dBFS | ADS4246 (160 MSPS) | | 83 | | dBFS |
| | | | ADS4245 (125 MSPS) | | 92 | | |
| | | | ADS4242 (65 MSPS) | | 92 | | |
| Crosstalk | | 20-MHz full-scale signal on channel under observation; 170-MHz full-scale signal on other channel | | | 95 | | dB |
| Input overload recovery | | Recovery to within 1% (of full-scale) for 6-dB overload with sine-wave input | | | 1 | | Clock cycle |
| AC power-supply rejection ratio | PSRR | For 100-mV _{pp} signal on AVDD supply, up to 10 MHz | | | > 30 | | dB |
| Effective number of bits | ENOB | f _{IN} = 70 MHz (ADS4245, ADS4242) f _{IN} = 170 MHz (ADS4246) | | | 11.5 | | LSBs |
| Differential nonlinearity | DNL | f _{IN} = 70 MHz (ADS4245, ADS4242) f _{IN} = 170 MHz (ADS4246) | | –0.97 | ±0.5 | +1.7 | LSBs |
| Integrated nonlinearity | INL | f _{IN} = 70 MHz (ADS4245, ADS4242) f _{IN} = 170 MHz (ADS4246) | | | ±2 | ±5 | LSBs |

7.6 Electrical Characteristics: ADS4226, ADS4225, ADS4222

Typical values are at 25°C, AVDD = 1.8 V, DRVDD = 1.8 V, 50% clock duty cycle, –1 dBFS differential analog input, LVDS interface, and 0-dB gain, unless otherwise noted. Minimum and maximum values are across the full temperature range:

T_{MIN} = –40°C to T_{MAX} = 85°C, AVDD = 1.8 V, and DRVDD = 1.8 V.

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|--------------------------------------|---------------------------|--------------------|--|------|------|-----|------|
| Resolution | | | | | | 12 | Bits |
| Signal-to-noise ratio | f _{IN} = 20 MHz | ADS4226 (160 MSPS) | | | 70.5 | | dBFS |
| | | ADS4225 (125 MSPS) | | | 70.8 | | |
| | | ADS4222 (65 MSPS) | | | 70.9 | | |
| | f _{IN} = 70 MHz | ADS4226 (160 MSPS) | | | 70.3 | | dBFS |
| | | ADS4225 (125 MSPS) | | 68 | 70.5 | | |
| | | ADS4222 (65 MSPS) | | 68 | 70.3 | | |
| | f _{IN} = 100 MHz | ADS4226 (160 MSPS) | | | 70.1 | | dBFS |
| | | ADS4225 (125 MSPS) | | | 70.3 | | |
| | | ADS4222 (65 MSPS) | | | 70.2 | | |
| | f _{IN} = 170 MHz | ADS4226 (160 MSPS) | | 67.5 | 69.5 | | dBFS |
| | | ADS4225 (125 MSPS) | | | 69.9 | | |
| | | ADS4222 (65 MSPS) | | | 69.9 | | |
| | f _{IN} = 300 MHz | ADS4226 (160 MSPS) | | | 68.2 | | dBFS |
| | | ADS4225 (125 MSPS) | | | 68.1 | | |
| | | ADS4222 (65 MSPS) | | | 68.2 | | |
| Signal-to-noise and distortion ratio | f _{IN} = 20 MHz | ADS4226 (160 MSPS) | | | 70.4 | | dBFS |
| | | ADS4225 (125 MSPS) | | | 70.7 | | |
| | | ADS4222 (65 MSPS) | | | 70.8 | | |
| | f _{IN} = 70 MHz | ADS4226 (160 MSPS) | | | 70.1 | | dBFS |
| | | ADS4225 (125 MSPS) | | 67 | 70.3 | | |
| | | ADS4222 (65 MSPS) | | 67 | 70.2 | | |
| | f _{IN} = 100 MHz | ADS4226 (160 MSPS) | | | 69.8 | | dBFS |
| | | ADS4225 (125 MSPS) | | | 70.1 | | |
| | | ADS4222 (65 MSPS) | | | 70.1 | | |
| | f _{IN} = 170 MHz | ADS4226 (160 MSPS) | | 66.5 | 69.3 | | dBFS |
| | | ADS4225 (125 MSPS) | | | 69.5 | | |
| | | ADS4222 (65 MSPS) | | | 68.7 | | |
| | f _{IN} = 300 MHz | ADS4226 (160 MSPS) | | | 67.6 | | dBFS |
| | | ADS4225 (125 MSPS) | | | 67.5 | | |
| | | ADS4222 (65 MSPS) | | | 67.2 | | |
| Spurious-free dynamic range | f _{IN} = 20 MHz | ADS4226 (160 MSPS) | | | 86 | | dBc |
| | | ADS4225 (125 MSPS) | | | 88 | | |
| | | ADS4222 (65 MSPS) | | | 91 | | |
| | f _{IN} = 70 MHz | ADS4226 (160 MSPS) | | | 84 | | dBc |
| | | ADS4225 (125 MSPS) | | 72.5 | 86 | | |
| | | ADS4222 (65 MSPS) | | 72.5 | 88 | | |
| | f _{IN} = 100 MHz | ADS4226 (160 MSPS) | | | 82 | | dBc |
| | | ADS4225 (125 MSPS) | | | 85 | | |
| | | ADS4222 (65 MSPS) | | | 87 | | |
| | f _{IN} = 170 MHz | ADS4226 (160 MSPS) | | 70 | 82 | | dBc |
| | | ADS4225 (125 MSPS) | | | 88 | | |
| | | ADS4222 (65 MSPS) | | | 85 | | |
| | f _{IN} = 300 MHz | ADS4226 (160 MSPS) | | | 78 | | dBc |
| | | ADS4225 (125 MSPS) | | | 78 | | |
| | | ADS4222 (65 MSPS) | | | 74 | | |

7.6 Electrical Characteristics: ADS4226, ADS4225, ADS4222 (continued)

Typical values are at 25°C, AVDD = 1.8 V, DRVDD = 1.8 V, 50% clock duty cycle, –1 dBFS differential analog input, LVDS interface, and 0-dB gain, unless otherwise noted. Minimum and maximum values are across the full temperature range: T_{MIN} = –40°C to T_{MAX} = 85°C, AVDD = 1.8 V, and DRVDD = 1.8 V.

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|----------------------------|---------------------------|--------------------------|--------------------|------|-----|-----|------|
| Total harmonic distortion | THD | f _{IN} = 20 MHz | ADS4226 (160 MSPS) | | 84 | | dBc |
| | | | ADS4225 (125 MSPS) | | 86 | | |
| | | | ADS4222 (65 MSPS) | | 88 | | |
| | f _{IN} = 70 MHz | | ADS4226 (160 MSPS) | | 81 | | dBc |
| | | | ADS4225 (125 MSPS) | 70 | 84 | | |
| | | | ADS4222 (65 MSPS) | 71 | 85 | | |
| | f _{IN} = 100 MHz | | ADS4226 (160 MSPS) | | 81 | | dBc |
| | | | ADS4225 (125 MSPS) | | 83 | | |
| | | | ADS4222 (65 MSPS) | | 85 | | |
| | f _{IN} = 170 MHz | | ADS4226 (160 MSPS) | 68 | 80 | | dBc |
| | | | ADS4225 (125 MSPS) | | 84 | | |
| | | | ADS4222 (65 MSPS) | | 82 | | |
| | f _{IN} = 300 MHz | | ADS4226 (160 MSPS) | | 76 | | dBc |
| | | | ADS4225 (125 MSPS) | | 75 | | |
| | | | ADS4222 (65 MSPS) | | 73 | | |
| Second-harmonic distortion | HD2 | f _{IN} = 20 MHz | ADS4226 (160 MSPS) | | 86 | | dBc |
| | | | ADS4225 (125 MSPS) | | 88 | | |
| | | | ADS4222 (65 MSPS) | | 91 | | |
| | f _{IN} = 70 MHz | | ADS4226 (160 MSPS) | | 84 | | dBc |
| | | | ADS4225 (125 MSPS) | 72.5 | 86 | | |
| | | | ADS4222 (65 MSPS) | 72.5 | 88 | | |
| | f _{IN} = 100 MHz | | ADS4226 (160 MSPS) | | 82 | | dBc |
| | | | ADS4225 (125 MSPS) | | 85 | | |
| | | | ADS4222 (65 MSPS) | | 87 | | |
| | f _{IN} = 170 MHz | | ADS4226 (160 MSPS) | 70 | 82 | | dBc |
| | | | ADS4225 (125 MSPS) | | 88 | | |
| | | | ADS4222 (65 MSPS) | | 85 | | |
| | f _{IN} = 300 MHz | | ADS4226 (160 MSPS) | | 78 | | dBc |
| | | | ADS4225 (125 MSPS) | | 78 | | |
| | | | ADS4222 (65 MSPS) | | 74 | | |
| Third-harmonic distortion | HD3 | f _{IN} = 20 MHz | ADS4226 (160 MSPS) | | 92 | | dBc |
| | | | ADS4225 (125 MSPS) | | 93 | | |
| | | | ADS4222 (65 MSPS) | | 95 | | |
| | f _{IN} = 70 MHz | | ADS4226 (160 MSPS) | | 86 | | dBc |
| | | | ADS4225 (125 MSPS) | 72.5 | 89 | | |
| | | | ADS4222 (65 MSPS) | 72.5 | 90 | | |
| | f _{IN} = 100 MHz | | ADS4226 (160 MSPS) | | 93 | | dBc |
| | | | ADS4225 (125 MSPS) | | 89 | | |
| | | | ADS4222 (65 MSPS) | | 96 | | |
| | f _{IN} = 170 MHz | | ADS4226 (160 MSPS) | 70 | 94 | | dBc |
| | | | ADS4225 (125 MSPS) | | 90 | | |
| | | | ADS4222 (65 MSPS) | | 87 | | |
| | f _{IN} = 300 MHz | | ADS4226 (160 MSPS) | | 80 | | dBc |
| | | | ADS4225 (125 MSPS) | | 81 | | |
| | | | ADS4222 (65 MSPS) | | 81 | | |

7.6 Electrical Characteristics: ADS4226, ADS4225, ADS4222 (continued)

Typical values are at 25°C, AVDD = 1.8 V, DRVDD = 1.8 V, 50% clock duty cycle, –1 dBFS differential analog input, LVDS interface, and 0-dB gain, unless otherwise noted. Minimum and maximum values are across the full temperature range: T_{MIN} = –40°C to T_{MAX} = 85°C, AVDD = 1.8 V, and DRVDD = 1.8 V.

| PARAMETER | | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|--------------------|------|-------|------|-------------|------|
| Worst spur (other than second and third harmonics) | f _{IN} = 20 MHz | ADS4226 (160 MSPS) | | | 90 | | dBc | |
| | | ADS4225 (125 MSPS) | | | 95 | | | |
| | | ADS4222 (65 MSPS) | | | 98 | | | |
| | f _{IN} = 70 MHz | ADS4226 (160 MSPS) | | | 92 | | dBc | |
| | | ADS4225 (125 MSPS) | 76 | 94 | | | | |
| | | ADS4222 (65 MSPS) | 77 | 97 | | | | |
| | f _{IN} = 100 MHz | ADS4226 (160 MSPS) | | | 89 | | dBc | |
| | | ADS4225 (125 MSPS) | | | 93 | | | |
| | | ADS4222 (65 MSPS) | | | 95 | | | |
| | f _{IN} = 170 MHz | ADS4226 (160 MSPS) | 75 | 89 | | dBc | | |
| | | ADS4225 (125 MSPS) | | | 91 | | | |
| | | ADS4222 (65 MSPS) | | | 93 | | | |
| | f _{IN} = 300 MHz | ADS4226 (160 MSPS) | | | 91 | | dBc | |
| | | ADS4225 (125 MSPS) | | | 89 | | | |
| | | ADS4222 (65 MSPS) | | | 92 | | | |
| Two-tone intermodulation distortion | IMD | f ₁ = 46 MHz, f ₂ = 50 MHz, each tone at –7 dBFS | ADS4226 (160 MSPS) | | | 96 | | dBFS |
| | | | ADS4225 (125 MSPS) | | | 96 | | |
| | | | ADS4222 (65 MSPS) | | | 98 | | |
| | | f ₁ = 185 MHz, f ₂ = 190 MHz, each tone at –7 dBFS | ADS4226 (160 MSPS) | | | 83 | | dBFS |
| | | | ADS4225 (125 MSPS) | | | 92 | | |
| | | | ADS4222 (65 MSPS) | | | 92 | | |
| Crosstalk | 20-MHz full-scale signal on channel under observation; 170-MHz full-scale signal on other channel | | | | 95 | | dB | |
| Input overload recovery | Recovery to within 1% (of full-scale) for 6-dB overload with sine-wave input | | | | 1 | | Clock cycle | |
| AC power-supply rejection ratio | PSRR | For 100-mV _{PP} signal on AVDD supply, up to 10 MHz | | | | 30 | | dB |
| Effective number of bits | ENOB | f _{IN} = 70 MHz (ADS4225, ADS4222) f _{IN} = 170 MHz (ADS4226) | ADS4226 (160 MSPS) | | | 11.2 | | LSBs |
| | | | ADS4225 (125 MSPS) | | | 11.3 | | |
| | | | ADS4222 (65 MSPS) | | | 11.1 | | |
| Differential nonlinearity | DNL | f _{IN} = 70 MHz (ADS4225, ADS4222) f _{IN} = 170 MHz (ADS4226) | ADS4226 (160 MSPS) | –0.8 | ±0.13 | +1.5 | LSBs | |
| | | | ADS4225 (125 MSPS) | –0.8 | ±0.13 | +1.5 | | |
| | | | ADS4222 (65 MSPS) | –0.8 | ±0.13 | +1.2 | | |
| Integrated nonlinearity | INL | f _{IN} = 70 MHz (ADS4225, ADS4222) f _{IN} = 170 MHz (ADS4226) | ADS4226 (160 MSPS) | | | ±0.5 | | LSBs |
| | | | ADS4225 (125 MSPS) | | | ±0.5 | | |
| | | | ADS4222 (65 MSPS) | | | ±0.5 | | |
| | | | | | | | | |

7.7 Electrical Characteristics: General

Typical values are at 25°C, AVDD = 1.8 V, DRVDD = 1.8 V, 50% clock duty cycle, and –1 dBFS differential analog input, unless otherwise noted. Minimum and maximum values are across the full temperature range: T_{MIN} = –40°C to T_{MAX} = 85°C, AVDD = 1.8 V, and DRVDD = 1.8 V.

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|----------------------------|-------|-----|-----------------|
| ANALOG INPUTS | | | | | |
| Differential input voltage range | 0 dB gain | | 2 | | V _{PP} |
| Differential input resistance | At 200 MHz | | 0.75 | | kΩ |
| Differential input capacitance | At 200 MHz | | 3.7 | | pF |
| Analog input bandwidth | With 50-Ω source impedance, and 50-Ω termination | | 550 | | MHz |
| Analog input common-mode current | Per input pin of each channel | | 1.5 | | μA/MSPS |
| Common-mode output voltage | VCM | | 0.95 | | V |
| VCM output current capability | | | 4 | | mA |
| DC ACCURACY | | | | | |
| Offset error | | –15 | 2.5 | 15 | mV |
| Temperature coefficient of offset error | | | 0.003 | | mV/°C |
| Gain error as a result of internal reference inaccuracy alone | E _{GREF} | –2 | | 2 | %FS |
| Gain error of channel alone | E _{GCHAN} | ADS4246/ADS4226 (160 MSPS) | ±0.1 | –1 | %FS |
| | | ADS4245/ADS4225 (125 MSPS) | ±0.1 | | |
| | | ADS4242/ADS4222 (65 MSPS) | ±0.1 | –1 | |
| Temperature coefficient of E _{GCHAN} | | | 0.002 | | Δ%/°C |
| POWER SUPPLY | | | | | |
| IAVDD Analog supply current | ADS4246/ADS4226 (160 MSPS) | | 123 | 150 | mA |
| | ADS4245/ADS4225 (125 MSPS) | | 105 | 130 | |
| | ADS4242/ADS4222 (65 MSPS) | | 73 | 85 | |
| IDRVDD Output buffer supply current | LVDS interface, 350-mV swing with 100-Ω external termination, f _{IN} = 2.5 MHz | ADS4246/ADS4226 (160 MSPS) | 111 | 135 | mA |
| | | ADS4245/ADS4225 (125 MSPS) | 99 | 120 | |
| | | ADS4242/ADS4222 (65 MSPS) | 78 | 95 | |
| IDRVDD Output buffer supply current | CMOS interface, no load capacitance ⁽¹⁾ f _{IN} = 2.5 MHz | ADS4246/ADS4226 (160 MSPS) | 61 | | mA |
| | | ADS4245/ADS4225 (125 MSPS) | 49 | | |
| | | ADS4242/ADS4222 (65 MSPS) | 28 | | |
| Analog power | ADS4246/ADS4226 (160 MSPS) | | 222 | | mW |
| | ADS4245/ADS4225 (125 MSPS) | | 189 | | |
| | ADS4242/ADS4222 (65 MSPS) | | 133 | | |
| Digital power | LVDS interface, 350-mV swing with 100-Ω external termination, f _{IN} = 2.5 MHz | ADS4246/ADS4226 (160 MSPS) | 199 | | mW |
| | | ADS4245/ADS4225 (125 MSPS) | 179 | | |
| | | ADS4242/ADS4222 (65 MSPS) | 131 | | |
| Digital power | CMOS interface, no load capacitance ⁽¹⁾ f _{IN} = 2.5 MHz | ADS4246/ADS4226 (160 MSPS) | 109 | | mW |
| | | ADS4245/ADS4225 (125 MSPS) | 88 | | |
| | | ADS4242/ADS4222 (65 MSPS) | 50 | | |
| Global power-down | | | | 25 | mW |

- (1) In CMOS mode, the DRVDD current scales with the sampling frequency, the load capacitance on output pins, input frequency, and the supply voltage (see the [CMOS Interface Power Dissipation](#) section in the [Application Information](#)).

7.8 Digital Characteristics

At AVDD = 1.8 V and DRVDD = 1.8 V, unless otherwise noted. DC specifications refer to the condition where the digital outputs do not switch, but are permanently at a valid logic level 0 or 1.

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--|----------------------------|--|-------------|-------|------|------|
| DIGITAL INPUTS (RESET, SCLK, SDATA, SEN, CTRL1, CTRL2, CTRL3)⁽¹⁾ | | | | | | |
| High-level input voltage | | All digital inputs support 1.8-V and 3.3-V CMOS logic levels | 1.3 | | | V |
| Low-level input voltage | | All digital inputs support 1.8-V and 3.3-V CMOS logic levels | | | 0.4 | V |
| High-level input current | SDATA, SCLK ⁽²⁾ | V _{HIGH} = 1.8 V | | 10 | | μA |
| | SEN ⁽³⁾ | V _{HIGH} = 1.8 V | | 0 | | μA |
| Low-level input current | SDATA, SCLK | V _{LOW} = 0 V | | 0 | | μA |
| | SEN | V _{LOW} = 0 V | | 10 | | μA |
| DIGITAL OUTPUTS, CMOS INTERFACE (DA[13:0], DB[13:0], CLKOUT, SDOUT) | | | | | | |
| High-level output voltage | | | DRVDD – 0.1 | DRVDD | | V |
| Low-level output voltage | | | | 0 | 0.1 | V |
| Output capacitance (internal to device) | | | | | | pF |
| DIGITAL OUTPUTS, LVDS INTERFACE | | | | | | |
| High-level output differential voltage | V _{ODH} | With an external 100-Ω termination | 270 | 350 | 430 | mV |
| Low-level output differential voltage | V _{ODL} | With an external 100-Ω termination | –430 | –350 | –270 | mV |
| Output common-mode voltage | | V _{OCM} | 0.9 | 1.05 | 1.25 | V |

(1) SCLK, SDATA, and SEN function as digital input pins in serial configuration mode.

(2) SDATA, SCLK have internal 150-kΩ pull-down resistor.

(3) SEN has an internal 150-kΩ pull-up resistor to AVDD. Because the pull-up is weak, SEN can also be driven by 1.8-V or 3.3-V CMOS buffers.

7.9 Timing Requirements: LVDS and CMOS Modes⁽¹⁾

Typical values are at 25°C, AVDD = 1.8 V, DRVDD = 1.8 V, sampling frequency = 160MSPS, sine wave input clock, 1.5 V_{pp} clock amplitude, C_{LOAD} = 5 pF⁽²⁾, and R_{LOAD} = 100 Ω⁽³⁾, unless otherwise noted. Minimum and maximum values are across the full temperature range: T_{MIN} = –40°C to T_{MAX} = 85°C, AVDD = 1.8 V, and DRVDD = 1.7 V to 1.9 V.

| | | | MIN | NOM | MAX | UNIT |
|------------------------------|-----------------------------|---|------|-----|-----|--------------------|
| t _A | Aperture delay | | 0.5 | 0.8 | 1.1 | ns |
| | Aperture delay matching | Between the two channels of the same device | ±70 | | | ps |
| | Variation of aperture delay | Between two devices at the same temperature and DRVDD supply | ±150 | | | ps |
| t _J | Aperture jitter | | 140 | | | f _S rms |
| | Wakeup time | Time to valid data after coming out of STANDBY mode | 50 | | 100 | μs |
| | | Time to valid data after coming out of GLOBAL power-down mode | 100 | | 500 | μs |
| | ADC latency ⁽⁷⁾ | Default latency after reset | 16 | | | Clock cycles |
| | | Digital functions enabled (EN DIGITAL = 1) | 24 | | | Clock cycles |
| DDR LVDS MODE ⁽⁴⁾ | | | | | | |
| t _{SU} | Data setup time | Data valid ⁽⁵⁾ to zero-crossing of CLKOUTP | 1.5 | 2 | | ns |
| t _H | Data hold time | Zero-crossing of CLKOUTP to data becoming invalid ⁽⁵⁾ | 0.35 | 0.6 | | ns |
| t _{PDI} | Clock propagation delay | Input clock rising edge cross-over to output clock rising edge cross-over | 5 | 6.1 | 7.5 | ns |

7.9 Timing Requirements: LVDS and CMOS Modes⁽¹⁾ (continued)

Typical values are at 25°C, AVDD = 1.8 V, DRVDD = 1.8 V, sampling frequency = 160MSPS, sine wave input clock, 1.5 V_{pp} clock amplitude, C_{LOAD} = 5 pF⁽²⁾, and R_{LOAD} = 100 Ω⁽³⁾, unless otherwise noted. Minimum and maximum values are across the full temperature range: T_{MIN} = –40°C to T_{MAX} = 85°C, AVDD = 1.8 V, and DRVDD = 1.7 V to 1.9 V.

| | | | MIN | NOM | MAX | UNIT |
|--|---|--|-----|------|-----|------|
| | LVDS bit clock duty cycle | Duty cycle of differential clock, (CLKOUTP-CLKOUTM) | | 49% | | |
| t _{RISE} , t _{FALL} | Data rise time, Data fall time | Rise time measured from –100 mV to +100 mV Fall time measured from +100 mV to –100 mV 1MSPS ≤ Sampling frequency ≤ 160MSPS | | 0.13 | | ns |
| t _{CLKRISE} , t _{CLKFALL} | Output clock rise time, Output clock fall time | Rise time measured from –100 mV to +100 mV Fall time measured from +100 mV to –100 mV 1MSPS ≤ Sampling frequency ≤ 160MSPS | | 0.13 | | ns |

PARALLEL CMOS MODE

| | | | | | | |
|--|--|--|-----|-----|-----|----|
| t _{SU} | Data setup time | Data valid ⁽⁶⁾ to zero-crossing of CLKOUT | 1.6 | 2.5 | | ns |
| t _H | Data hold time | Zero-crossing of CLKOUT to data becoming invalid ⁽⁶⁾ | 2.3 | 2.7 | | ns |
| t _{PDI} | Clock propagation delay | Input clock rising edge cross-over to output clock rising edge cross-over | 4.5 | 6.4 | 8.5 | ns |
| | Output clock duty cycle | Duty cycle of output clock, CLKOUT 1MSPS ≤ Sampling frequency ≤ 160MSPS | | 46% | | |
| t _{RISE} , t _{FALL} | Data rise time, Data fall time | Rise time measured from 20% to 80% of DRVDD Fall time measured from 80% to 20% of DRVDD 1MSPS ≤ Sampling frequency ≤ 160MSPS | | 1 | | ns |
| t _{CLKRISE} , t _{CLKFALL} | Output clock rise time Output clock fall time | Rise time measured from 20% to 80% of DRVDD Fall time measured from 80% to 20% of DRVDD 1MSPS ≤ Sampling frequency ≤ 160MSPS | | 1 | | ns |

- (1) Timing parameters are ensured by design and characterization and not tested in production.
- (2) C_{LOAD} is the effective external single-ended load capacitance between each output pin and ground
- (3) R_{LOAD} is the differential load resistance between the LVDS output pair.
- (4) Measurements are done with a transmission line of 100Ω characteristic impedance between the device and the load. Setup and hold time specifications take into account the effect of jitter on the output data and clock.
- (5) Data valid refers to a logic high of +100 mV and a logic low of –100 mV.
- (6) Data valid refers to a logic high of 1.26 V and a logic low of 0.54 V
- (7) At higher frequencies, t_{PDI} is greater than one clock period and overall latency = ADC latency + 1.

7.10 Serial Interface Timing Characteristics⁽¹⁾

See the [Section 8.5.6.1](#) section.

| PARAMETER | | MIN | TYP | MAX | UNIT |
|---------------------|--|------|-----|-----|------|
| f _{SCLK} | SCLK frequency (equal to 1/t _{SCLK}) | > DC | | 20 | MHz |
| t _{SLOADS} | SEN to SCLK setup time | 25 | | | ns |
| t _{SLOADH} | SCLK to SEN hold time | 25 | | | ns |
| t _{DSU} | SDATA setup time | 25 | | | ns |
| t _{DH} | SDATA hold time | 25 | | | ns |

- (1) Typical values at 25°C; minimum and maximum values across the full temperature range: T_{MIN} = –40°C to T_{MAX} = 85°C, AVDD = 1.8 V, and DRVDD = 1.8 V, unless otherwise noted.

7.11 Reset Timing (Only When Serial Interface Is Used)

See the [Section 8.5.6.2](#) section.

| PARAMETER | CONDITIONS | MIN | TYP ⁽¹⁾ | MAX | UNIT |
|-------------------------------------|--|-----|--------------------|-----|------|
| t ₁ Power-on delay | Delay from AVDD and DRVDD power-up to active RESET pulse | 1 | | | ms |
| t ₂ Reset pulse width | Active RESET signal pulse width | 10 | | | ns |
| | | | | 1 | μs |
| t ₃ Register write delay | Delay from RESET disable to SEN active | 100 | | | ns |

(1) Typical values at 25°C; minimum and maximum values across the full temperature range: T_{MIN} = –40°C to T_{MAX} = 85°C, unless otherwise noted.

Table 7-1. LVDS Timings at Lower Sampling Frequencies

| SAMPLING FREQUENCY (MSPS) | SETUP TIME (ns) | | | HOLD TIME (ns) | | | t _{PDI} , CLOCK PROPAGATION DELAY (ns) | | |
|---------------------------------|-----------------|-----|-----|----------------|-----|-----|--|-----|-----|
| | MIN | TYP | MAX | MIN | TYP | MAX | MIN | TYP | MAX |
| 65 | 5.9 | 6.6 | | 0.35 | 0.6 | | 5 | 6.1 | 7.5 |
| 80 | 4.5 | 5.2 | | 0.35 | 0.6 | | 5 | 6.1 | 7.5 |
| 105 | 3.1 | 3.6 | | 0.35 | 0.6 | | 5 | 6.1 | 7.5 |
| 125 | 2.3 | 2.9 | | 0.35 | 0.6 | | 5 | 6.1 | 7.5 |
| 150 | 1.7 | 2.2 | | 0.35 | 0.6 | | 5 | 6.1 | 7.5 |

Table 7-2. CMOS Timings at Lower Sampling Frequencies

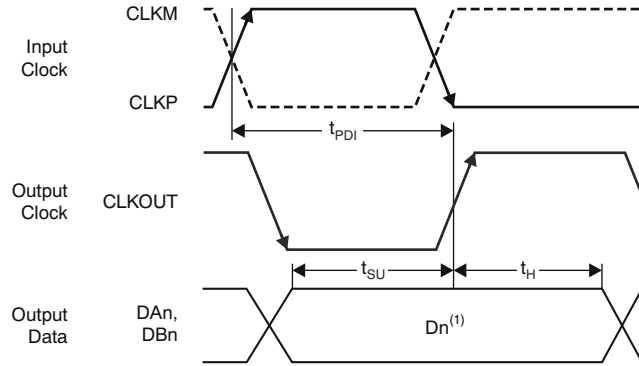
| SAMPLING FREQUENCY (MSPS) | TIMINGS SPECIFIED WITH RESPECT TO CLKOUT | | | | | | | | |
|---------------------------------|--|-----|-----|----------------|-----|-----|--|-----|-----|
| | SETUP TIME (ns) | | | HOLD TIME (ns) | | | t _{PDI} , CLOCK PROPAGATION DELAY (ns) | | |
| | MIN | TYP | MAX | MIN | TYP | MAX | MIN | TYP | MAX |
| 65 | 6.1 | 7.2 | | 6.7 | 7.1 | | 4.5 | 6.4 | 8.5 |
| 80 | 4.7 | 5.8 | | 5.3 | 5.8 | | 4.5 | 6.4 | 8.5 |
| 105 | 3.4 | 4.3 | | 3.8 | 4.3 | | 4.5 | 6.4 | 8.5 |
| 125 | 2.7 | 3.6 | | 3.1 | 3.6 | | 4.5 | 6.4 | 8.5 |
| 150 | 1.9 | 2.8 | | 2.5 | 2.9 | | 4.5 | 6.4 | 8.5 |

Table 7-3. High-Performance Modes

| PARAMETER ^{(1) (2)} | DESCRIPTION |
|------------------------------|--|
| High-performance mode | Set the HIGH PERF MODE register bit to obtain best performance across sample clock and input signal frequencies. See Figure 7-5 . Register address = 03h, data = 03h |
| High-frequency mode | Set the HIGH FREQ MODE CH A and HIGH FREQ MODE CH B register bits for high input signal frequencies greater than 200 MHz. See Figure 7-5 . Register address = 4Ah, data = 01h Register address = 58h, data = 01h |

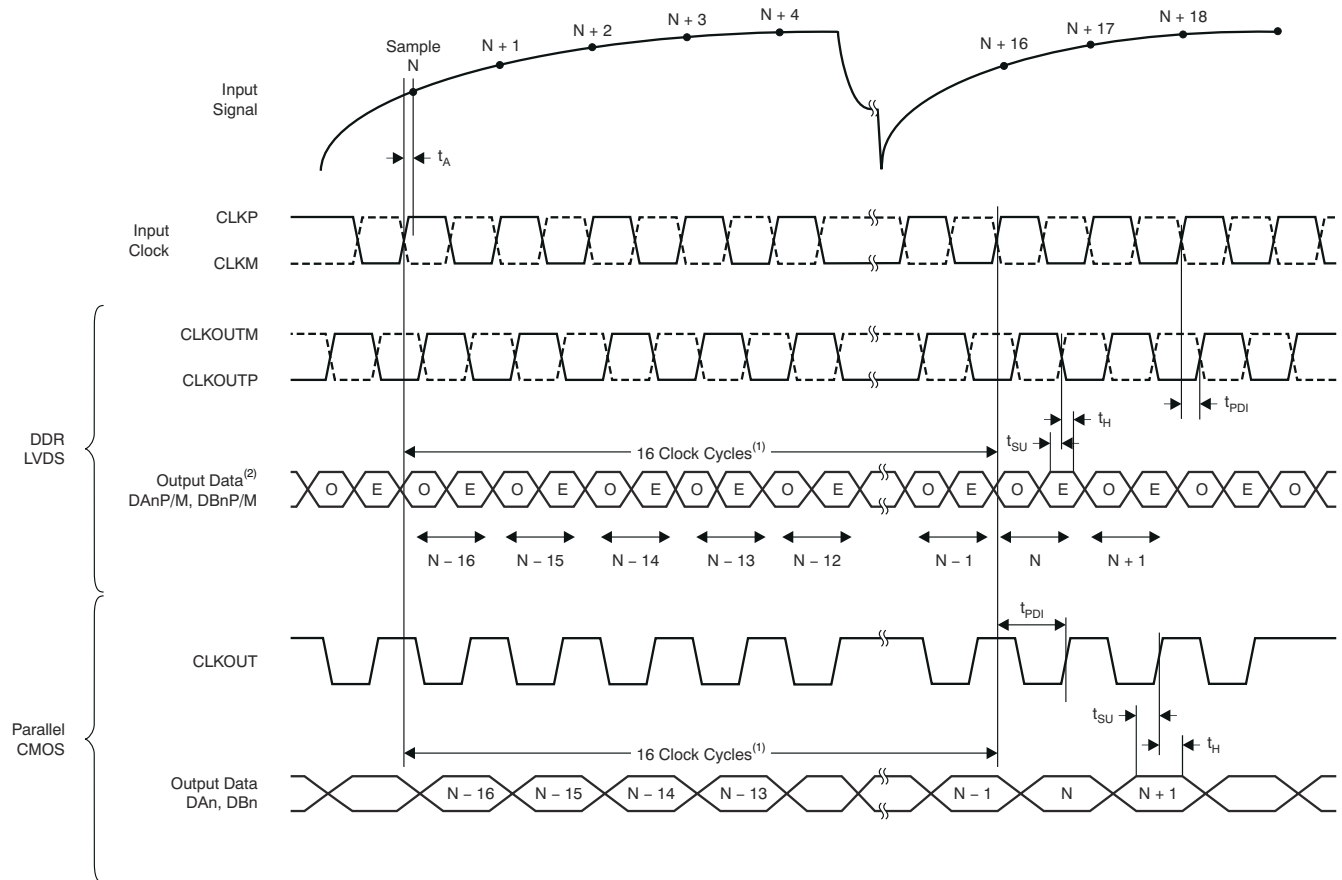
(1) It is recommended to use these modes to obtain best performance.

(2) See the [Section 8.5.3](#) section for details on register programming.



A. D_n = bits D0, D1, D2, etc. of channels A and B.

Figure 7-1. CMOS Interface Timing Diagram



A. ADC latency after reset. At higher sampling frequencies, t_{PDI} is greater than one clock cycle, which then makes the overall latency = ADC latency + 1.

B. E = even bits (D0, D2, D4, etc.); O = odd bits (D1, D3, D5, etc.).

Figure 7-2. Latency Timing Diagram

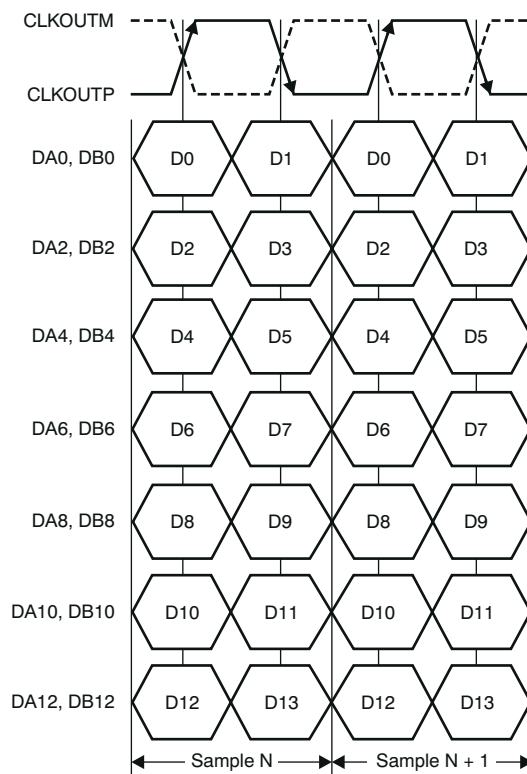


Figure 7-3. ADS4246/45/42 LVDS Interface Timing Diagram

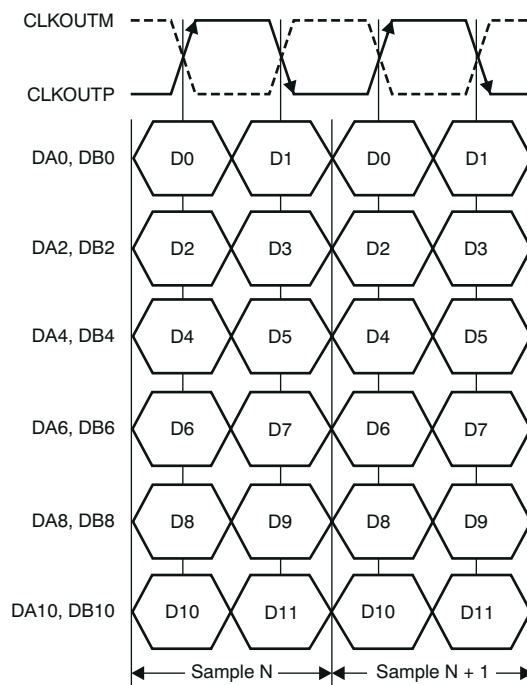
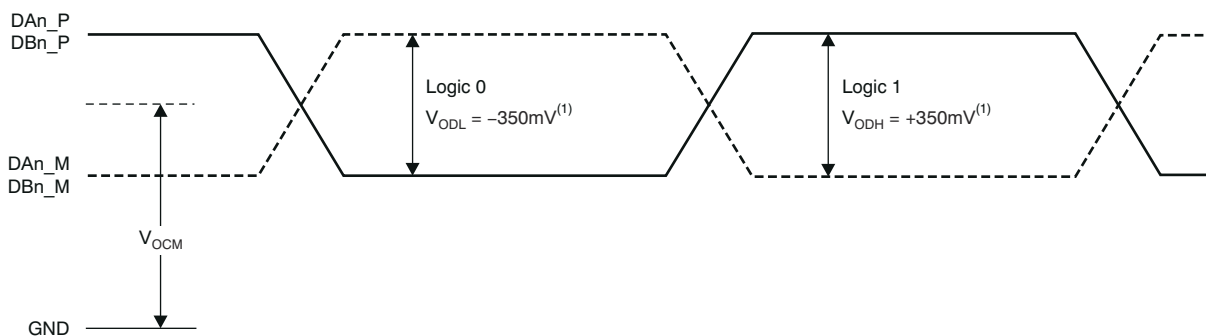


Figure 7-4. ADS4226/25/22 LVDS Interface Timing Diagram



A. With external 100- Ω termination.

Figure 7-5. LVDS Output Voltage Levels

7.12 Typical Characteristics

7.12.1 ADS4246

At $T_A = 25^\circ\text{C}$, $AV_{DD} = 1.8\text{ V}$, $DRV_{DD} = 1.8\text{ V}$, maximum rated sampling frequency, sine wave input clock, $1.5\text{-}V_{PP}$ differential clock amplitude, 50% clock duty cycle, -1 dBFS differential analog input, High-Performance Mode disabled, 0-dB gain, DDR LVDS output interface, and 32k point FFT, unless otherwise noted.

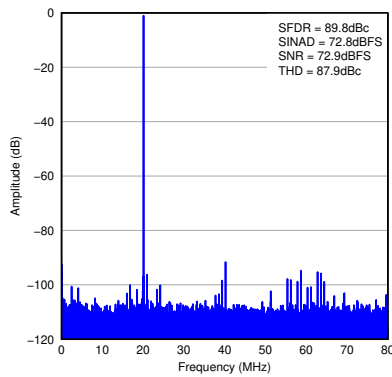


Figure 7-6. FFT for 20-MHz Input Signal

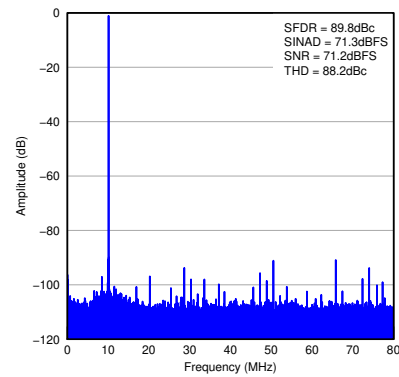


Figure 7-7. FFT for 170-MHz Input Signal

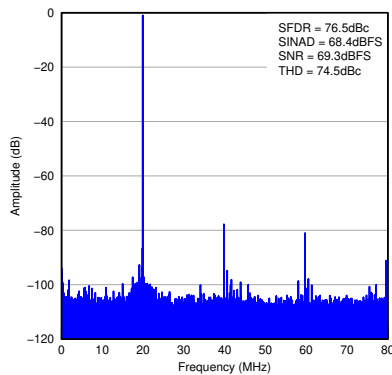


Figure 7-8. FFT for 300-MHz Input Signal

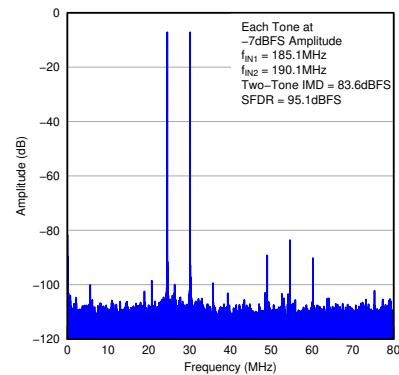


Figure 7-9. FFT for Two-tone Input Signal

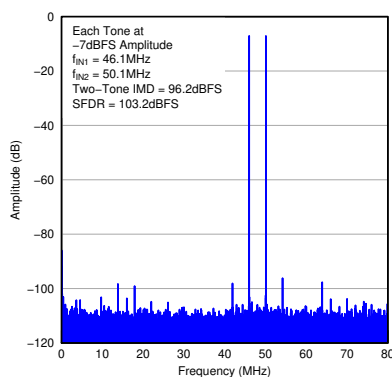


Figure 7-10. FFT for Two-Tone Input Signal

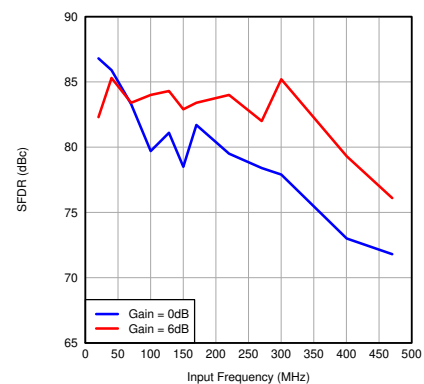


Figure 7-11. SFDR vs Input Frequency

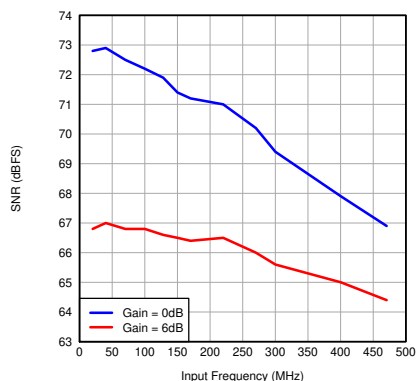


Figure 7-12. SNR vs Input Frequency

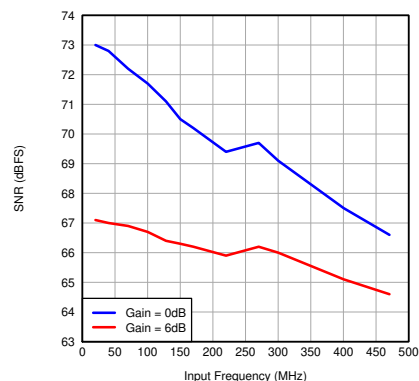


Figure 7-13. SNR vs Input Frequency (CMOS)

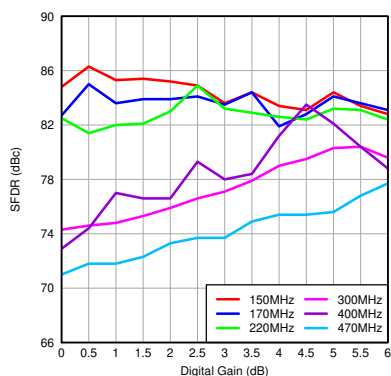


Figure 7-14. SFDR vs Gain and Input Frequency

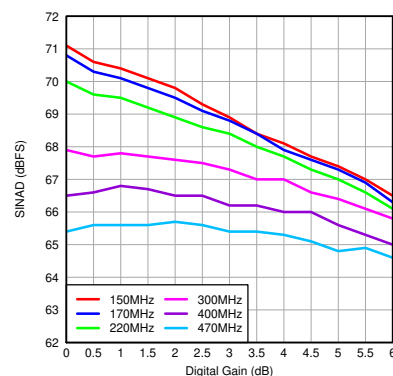


Figure 7-15. SINAD vs Gain and Input Frequency

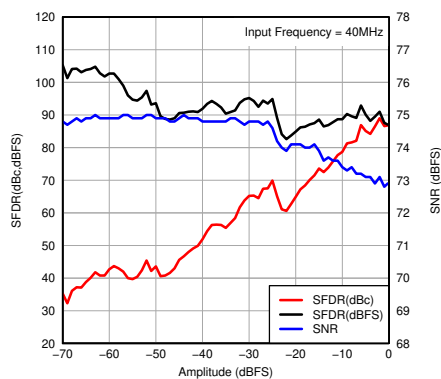


Figure 7-16. Performance vs Input Amplitude

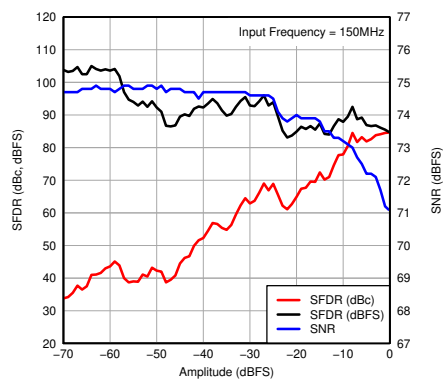


Figure 7-17. Performance vs Input Amplitude

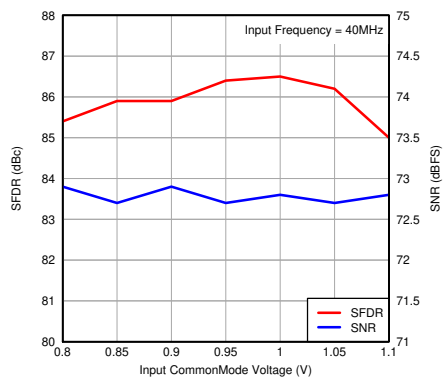


Figure 7-18. Performance vs Input Common-Mode Voltage

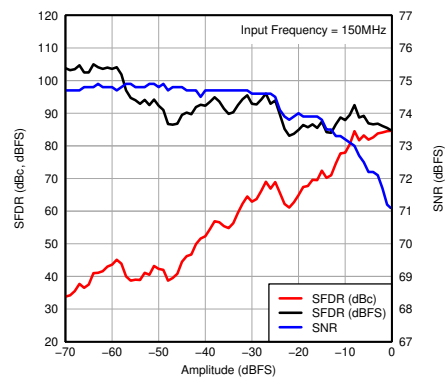


Figure 7-19. Performance vs Input Common-Mode Voltage

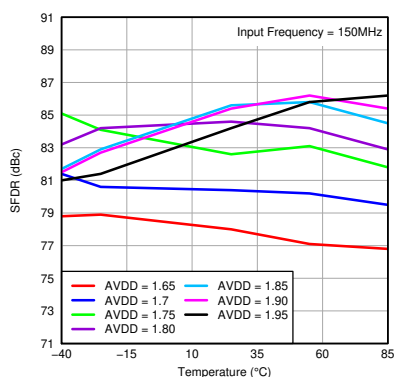


Figure 7-20. SFDR vs Temperature and AVDD Supply

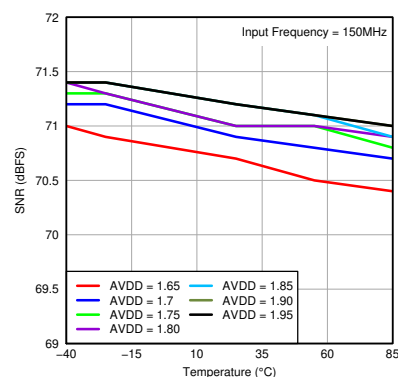


Figure 7-21. SNR vs Temperature and AVDD Supply

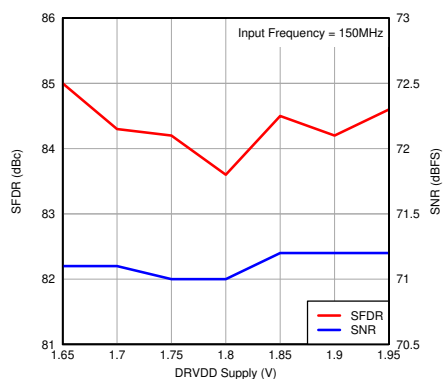


Figure 7-22. Performance vs DRVDD Supply Voltage

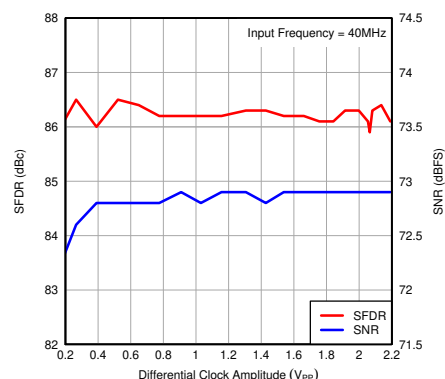


Figure 7-23. Performance vs Input Clock Amplitude

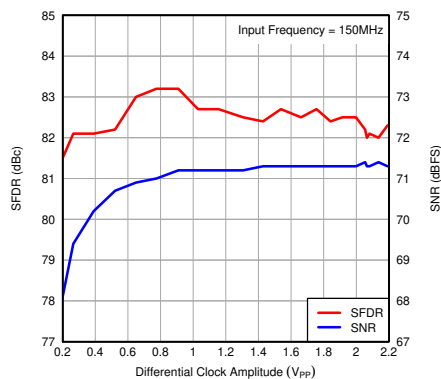


Figure 7-24. Performance vs Input Clock Amplitude

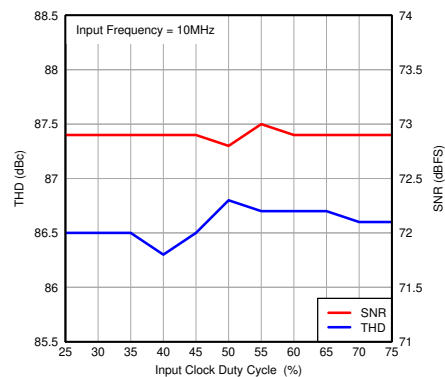


Figure 7-25. Performance vs Input Clock Duty Cycle

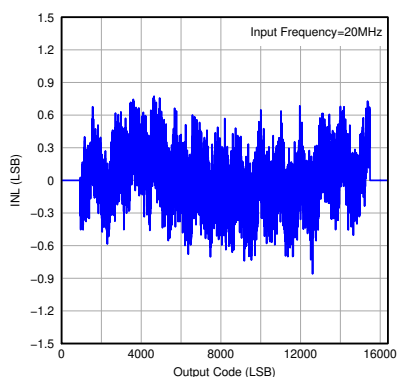


Figure 7-26. Integrated Nonlinearity

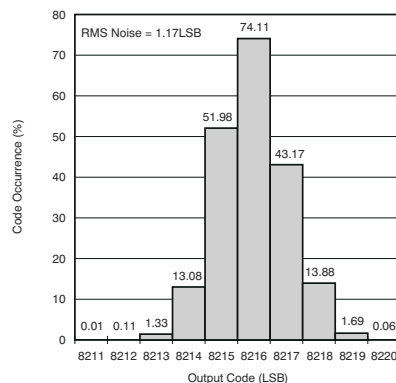


Figure 7-27. Output Noise Histogram (With Inputs Shorted to VCM)

7.12.2 ADS4245

At $T_A = 25^\circ\text{C}$, $AV_{DD} = 1.8\text{ V}$, $DRV_{DD} = 1.8\text{ V}$, maximum rated sampling frequency, sine wave input clock, $1.5\text{-}V_{PP}$ differential clock amplitude, 50% clock duty cycle, -1 dBFS differential analog input, High-Performance Mode disabled, 0-dB gain, DDR LVDS output interface, and 32k point FFT, unless otherwise noted.

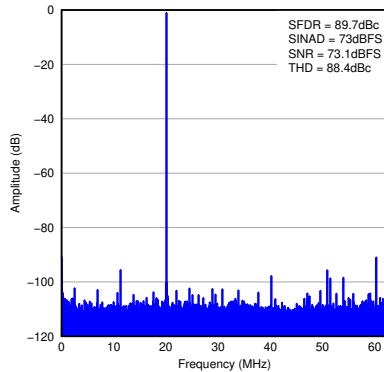


Figure 7-28. FFT for 20-MHz Input Signal

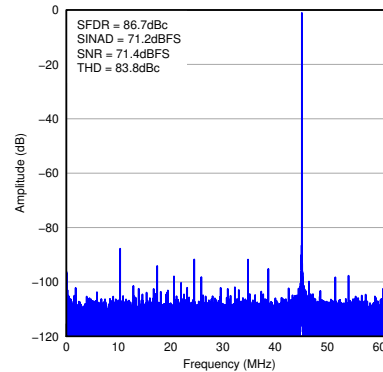


Figure 7-29. FFT for 170-MHz Input Signal

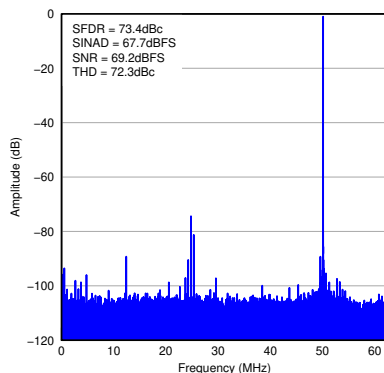


Figure 7-30. FFT for 300-MHz Input Signal

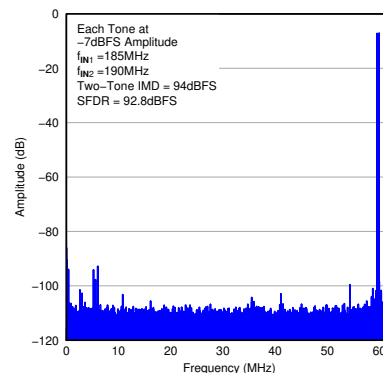


Figure 7-31. FFT for Two-Tone Input Signal

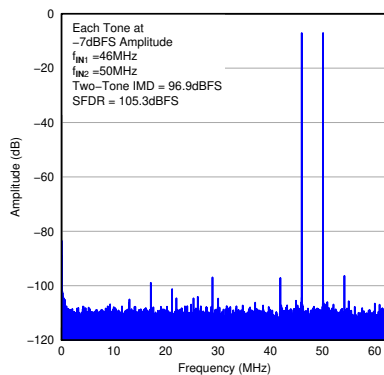


Figure 7-32. FFT for Two-Tone Input Signal

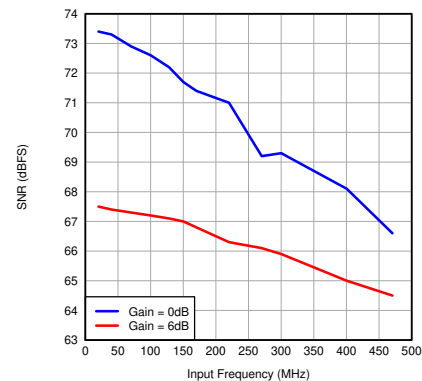


Figure 7-33. SNR vs Input Frequency

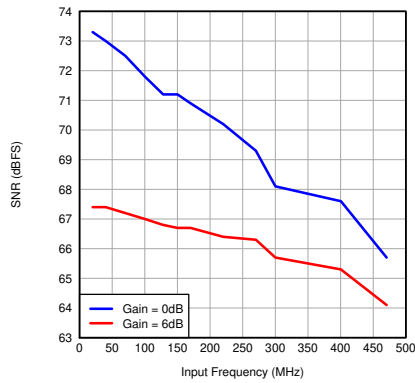


Figure 7-34. SNR vs Input Frequency (CMOS)

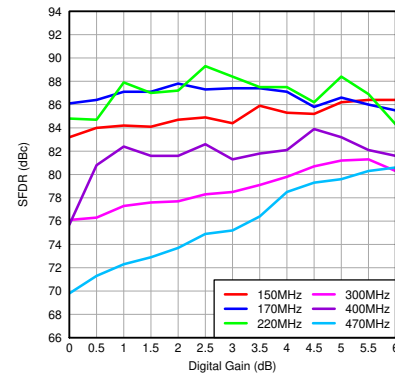


Figure 7-35. SFDR vs Gain and Input Frequency

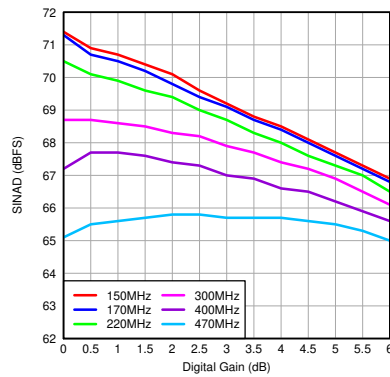


Figure 7-36. SINAD vs Gain and Input Frequency

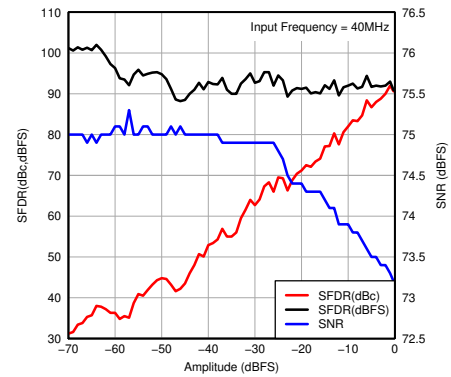


Figure 7-37. Performance vs Input Amplitude

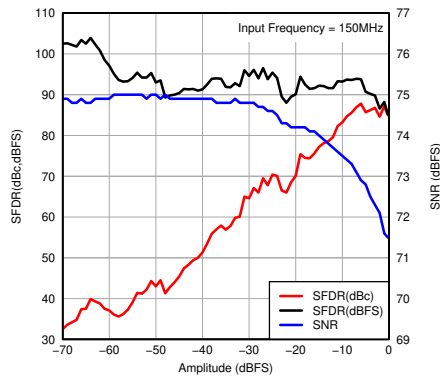


Figure 7-38. Performance vs Input Amplitude

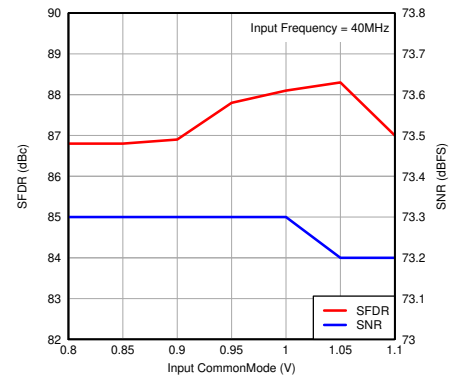


Figure 7-39. Performance vs Input Common-Mode Voltage

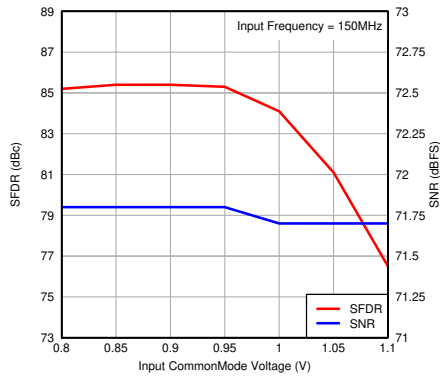


Figure 7-40. Performance vs Input Common-Mode Voltage

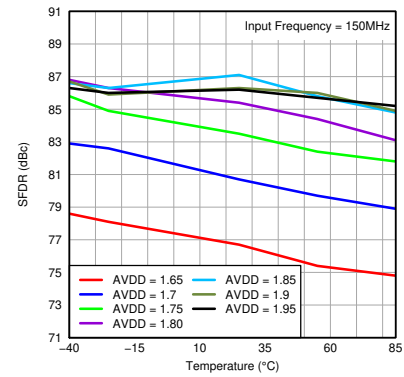


Figure 7-41. SFDR vs Temperature and AVDD Supply

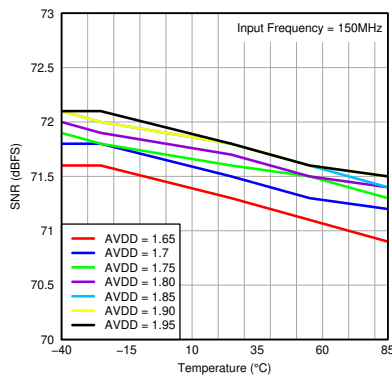


Figure 7-42. SNR vs Temperature and AVDD Supply

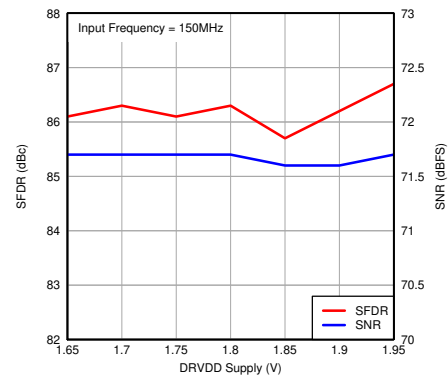


Figure 7-43. Performance vs DRVDD Supply Voltage

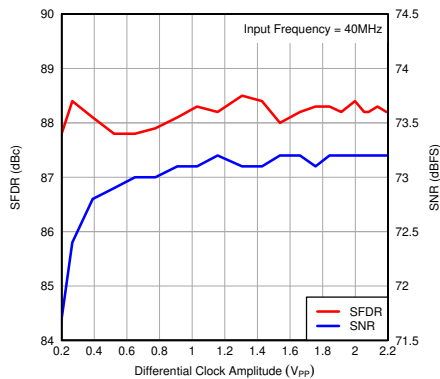


Figure 7-44. Performance vs Input Clock Amplitude

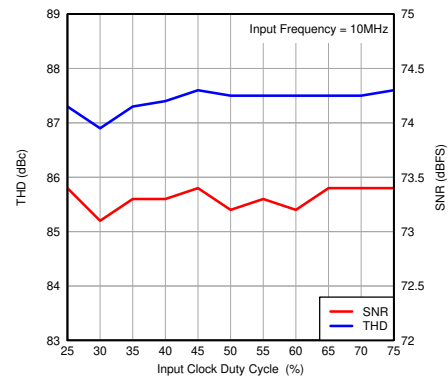


Figure 7-45. Performance vs Input Clock Duty Cycle

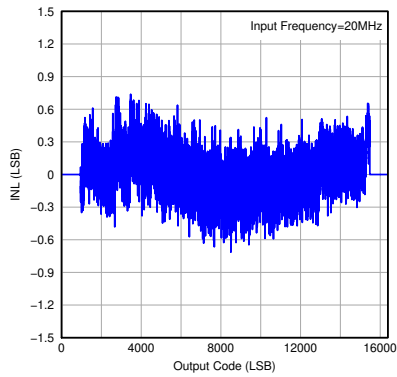


Figure 7-46. Integrated Nonlinearity

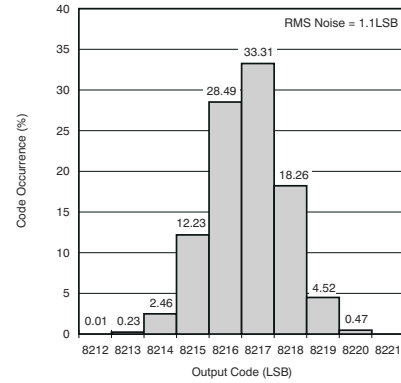


Figure 7-47. Output Noise Histogram (With Inputs Shorted to VCM)

7.12.3 ADS4242

At $T_A = 25^\circ\text{C}$, $AV_{DD} = 1.8\text{ V}$, $DRV_{DD} = 1.8\text{ V}$, maximum rated sampling frequency, sine wave input clock, $1.5\text{-}V_{PP}$ differential clock amplitude, 50% clock duty cycle, -1 dBFS differential analog input, High-Performance Mode disabled, 0-dB gain, DDR LVDS output interface, and 32k point FFT, unless otherwise noted.

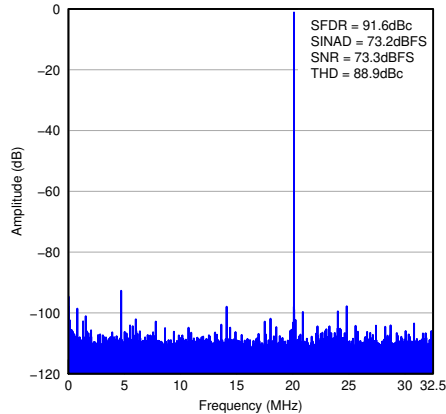


Figure 7-48. FFT for 20-MHz Input Signal

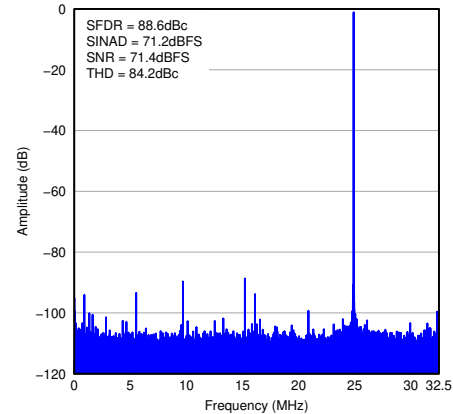


Figure 7-49. FFT for 170-MHz Input Signal

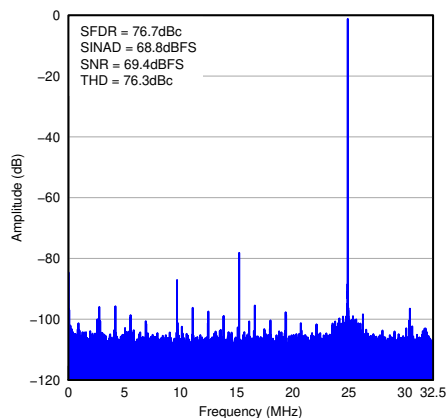


Figure 7-50. FFT for 300-MHz Input Signal

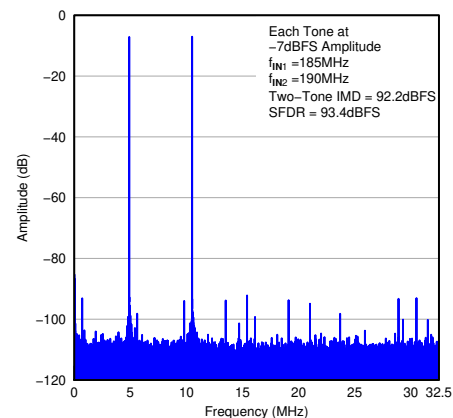


Figure 7-51. FFT for Two-Tone Input Signal

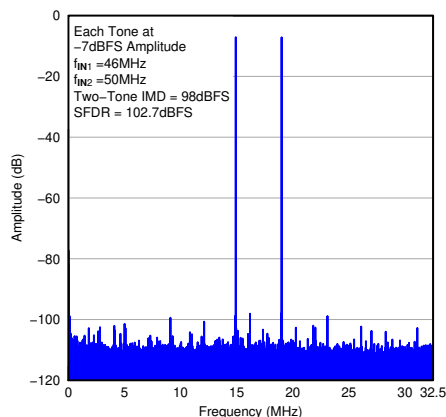


Figure 7-52. FFT for Two-Tone Input Signal

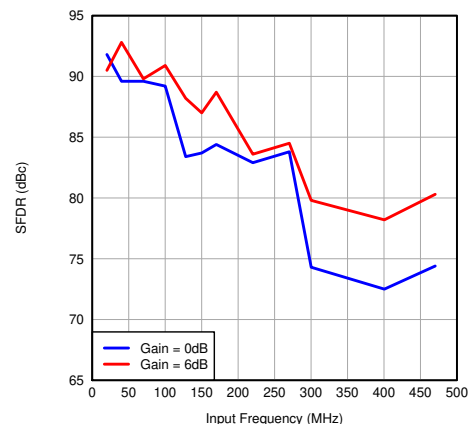


Figure 7-53. SFDR vs Input Frequency

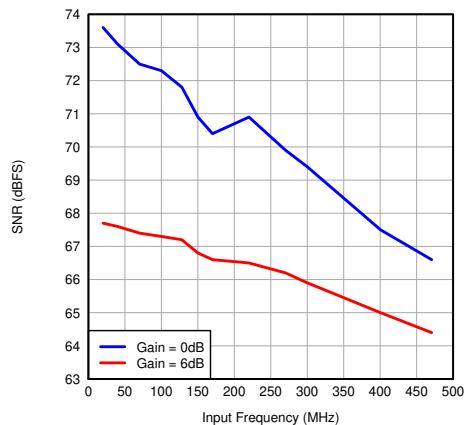


Figure 7-54. SNR vs Input Frequency

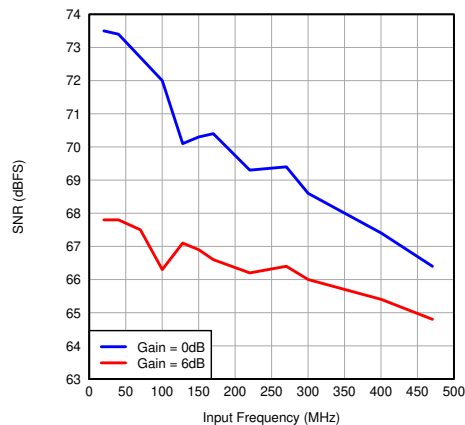


Figure 7-55. SNR vs Input Frequency (CMOS)

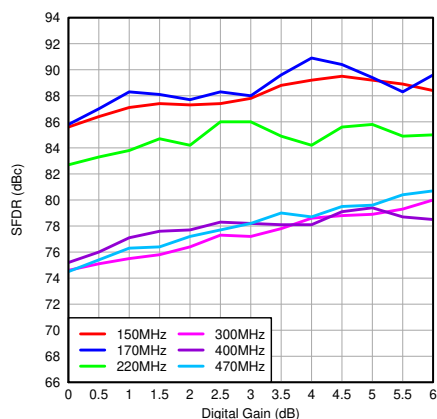


Figure 7-56. SFDR vs Gain and Input Frequency

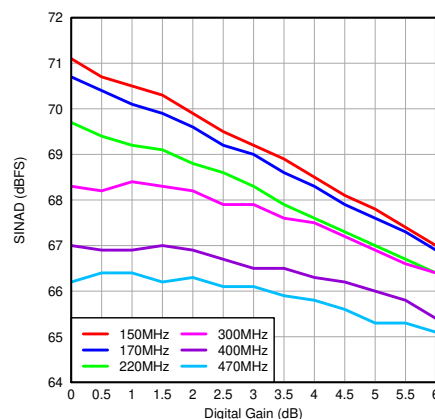


Figure 7-57. SINAD vs Gain and Input Frequency

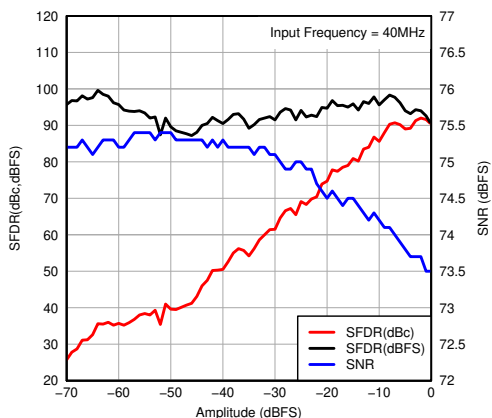


Figure 7-58. Performance vs Input Amplitude

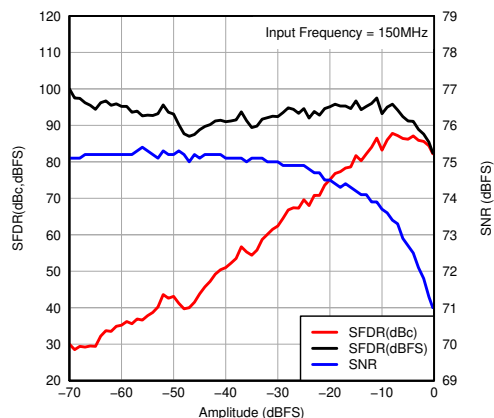


Figure 7-59. Performance vs Input Amplitude

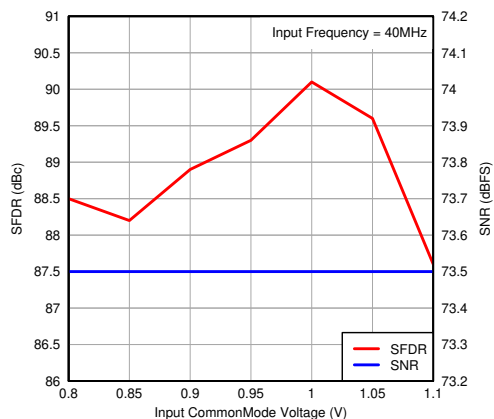


Figure 7-60. Performance vs Input Common-Mode Voltage

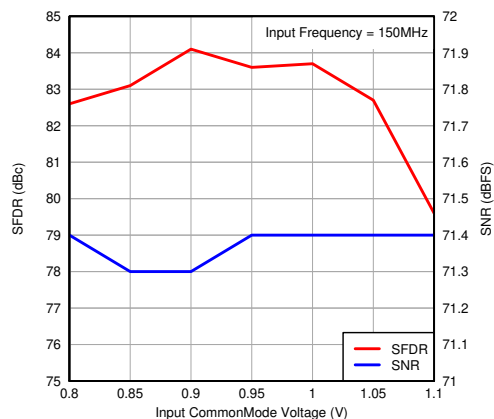


Figure 7-61. Performance vs Input Common-Mode Voltage

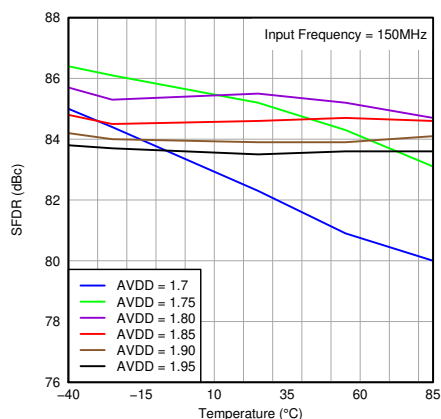


Figure 7-62. SFDR vs Temperature and AVDD Supply

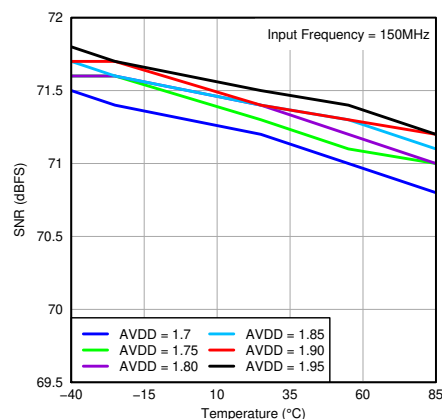


Figure 7-63. SNR vs Temperature and AVDD Supply

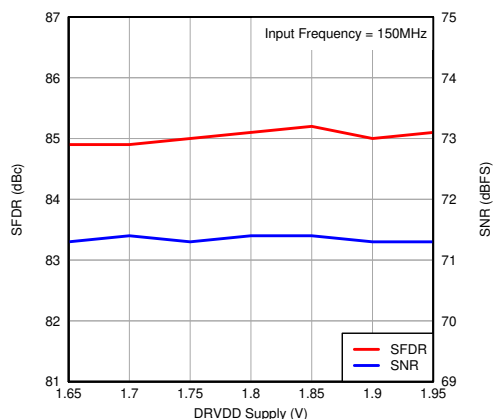


Figure 7-64. Performance vs DRVDD Supply Voltage

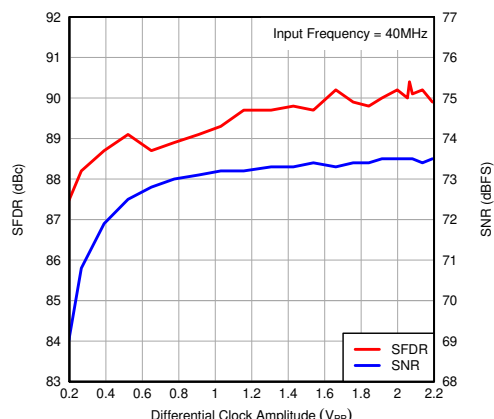


Figure 7-65. Performance vs Input Clock Amplitude

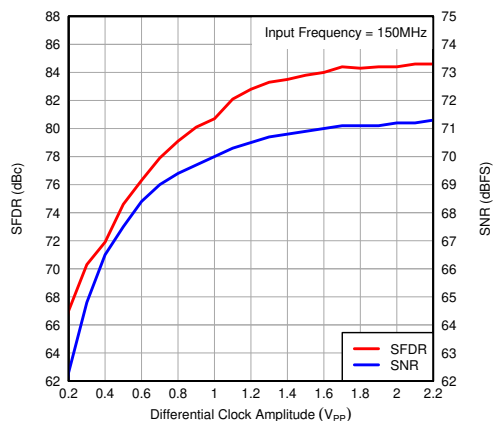


Figure 7-66. Performance vs Input Clock Amplitude

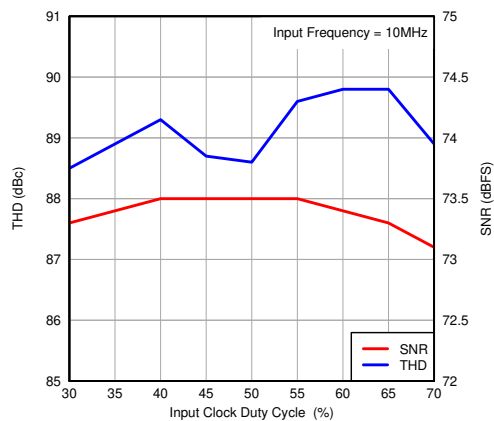


Figure 7-67. Performance Across Input Clock Duty Cycle

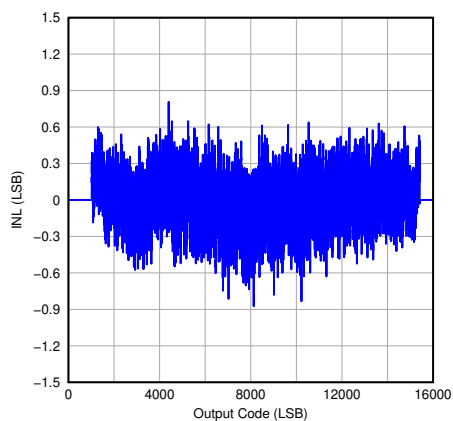


Figure 7-68. Integrated Nonlinearity

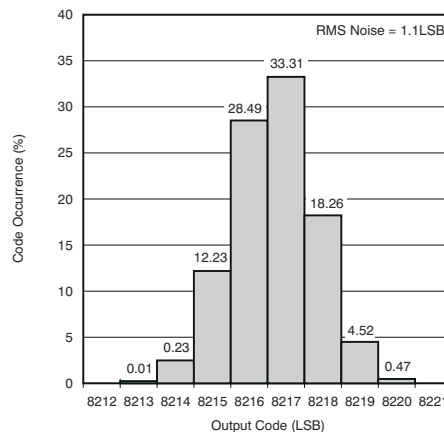


Figure 7-69. Output Noise Histogram (With Inputs Shorted to VCM)

7.12.4 ADS4226

At $T_A = 25^\circ\text{C}$, $AV_{DD} = 1.8\text{ V}$, $DRV_{DD} = 1.8\text{ V}$, maximum rated sampling frequency, sine wave input clock, $1.5\text{-}V_{PP}$ differential clock amplitude, 50% clock duty cycle, -1 dBFS differential analog input, High-Performance Mode disabled, 0-dB gain, DDR LVDS output interface, and 32k point FFT, unless otherwise noted.

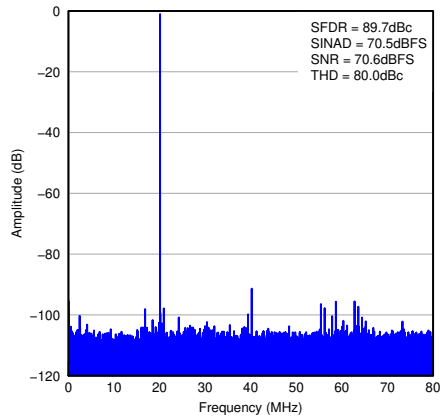


Figure 7-70. FFT for 20-MHz Input Signal

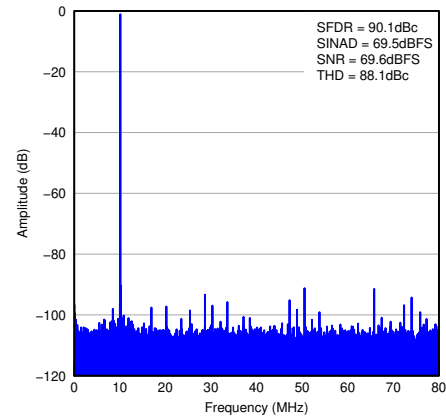


Figure 7-71. FFT for 170-MHz Input Signal

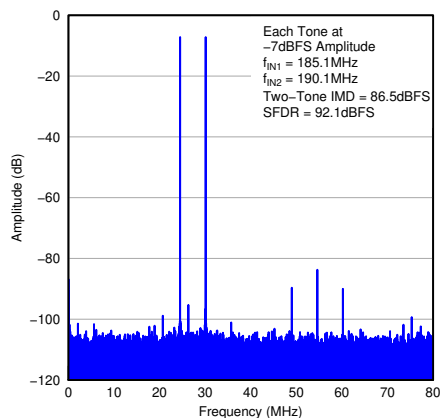


Figure 7-72. FFT for Two-Tone Input Signal

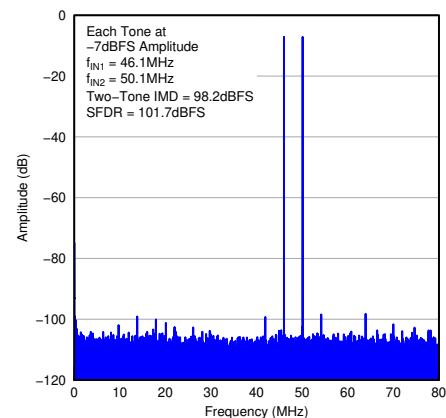


Figure 7-73. FFT for Two-Tone Input Signal

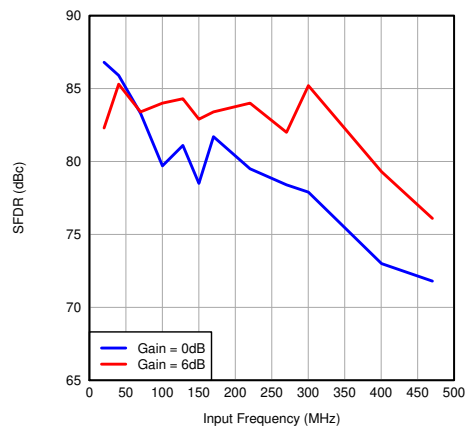


Figure 7-74. SFDR vs Input Frequency

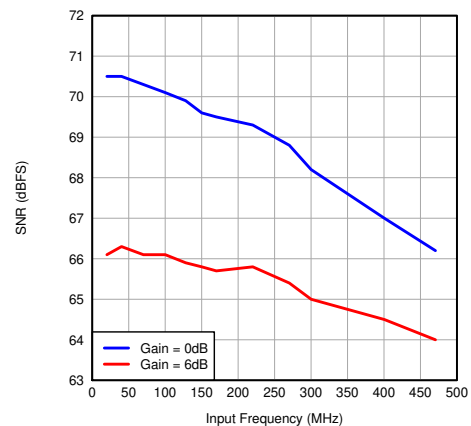


Figure 7-75. SNR vs Input Frequency

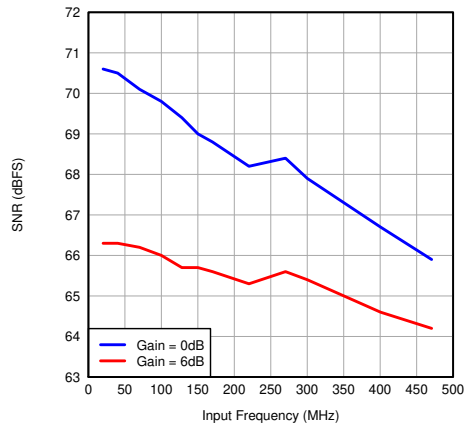


Figure 7-76. SNR vs Input Frequency (CMOS)

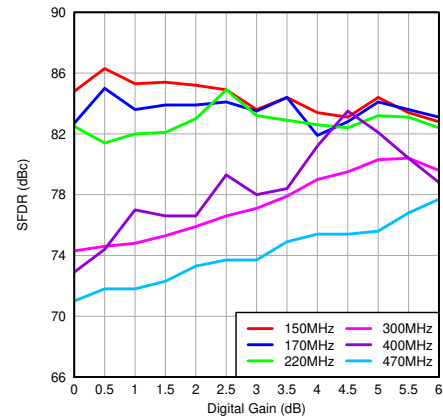


Figure 7-77. SFDR vs Gain and Input Frequency

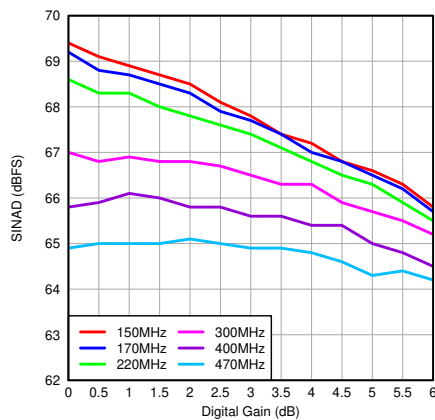


Figure 7-78. SINAD vs Gain and Input Frequency

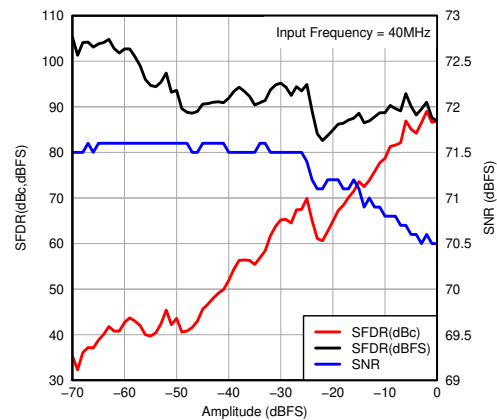


Figure 7-79. Performance vs Input Amplitude

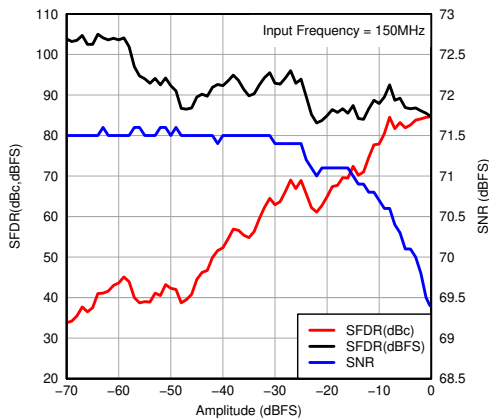


Figure 7-80. Performance vs Input Amplitude

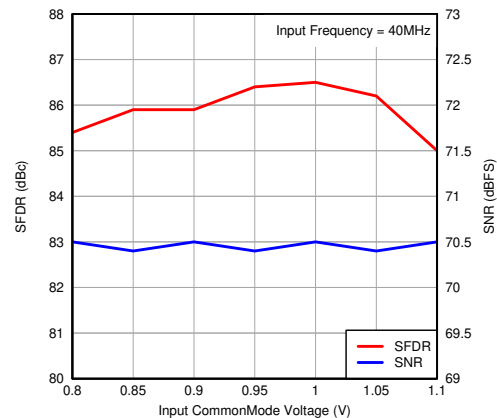


Figure 7-81. Performance vs Input Common-Mode Voltage

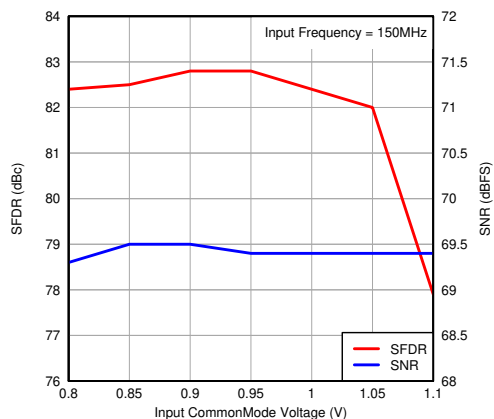


Figure 7-82. Performance vs Input Common-Mode Voltage

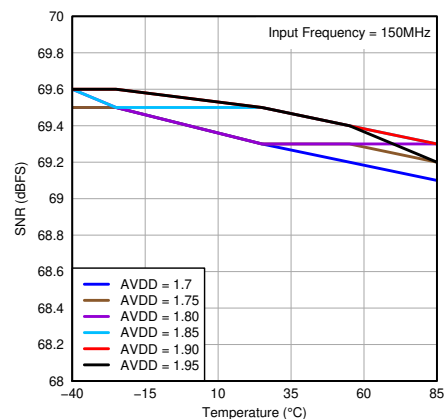


Figure 7-83. SNR vs Temperature and AVDD Supply

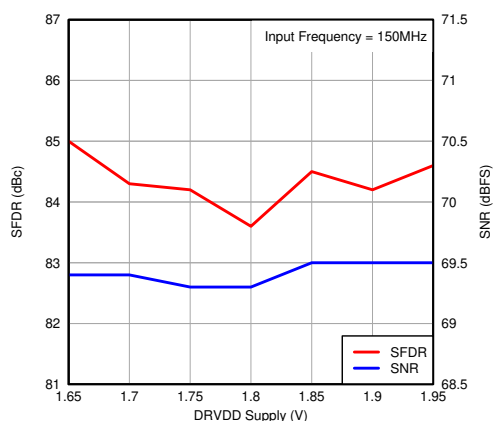


Figure 7-84. Performance vs DRVDD Supply Voltage

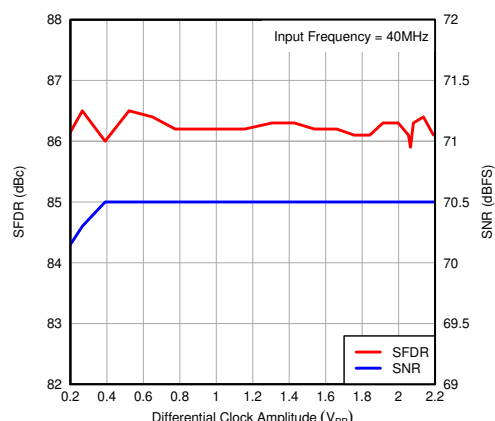


Figure 7-85. Performance vs Input Clock Amplitude

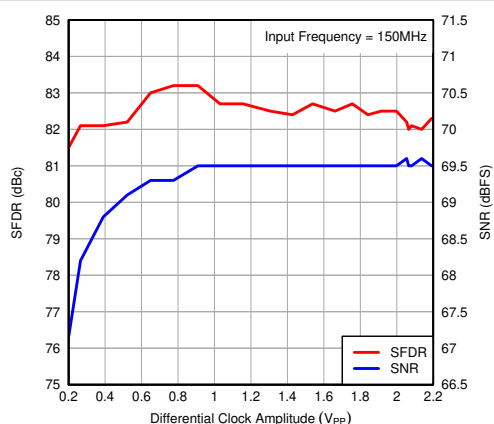


Figure 7-86. Performance vs Input Clock Amplitude

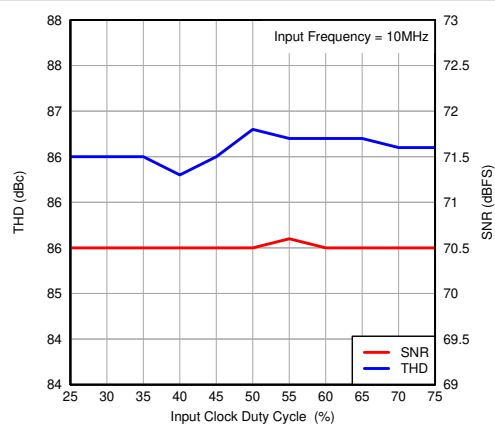


Figure 7-87. Performance vs Input Clock Duty Cycle

7.12.5 ADS4225

At $T_A = 25^\circ\text{C}$, $AV_{DD} = 1.8\text{ V}$, $DRV_{DD} = 1.8\text{ V}$, maximum rated sampling frequency, sine wave input clock, $1.5\text{-}V_{PP}$ differential clock amplitude, 50% clock duty cycle, -1 dBFS differential analog input, High-Performance Mode disabled, 0-dB gain, DDR LVDS output interface, and 32k point FFT, unless otherwise noted.

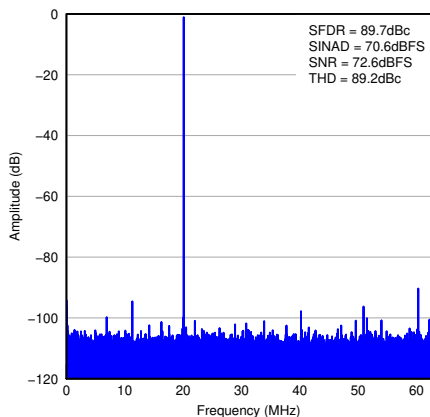


Figure 7-88. FFT for 20-MHz Input Signal

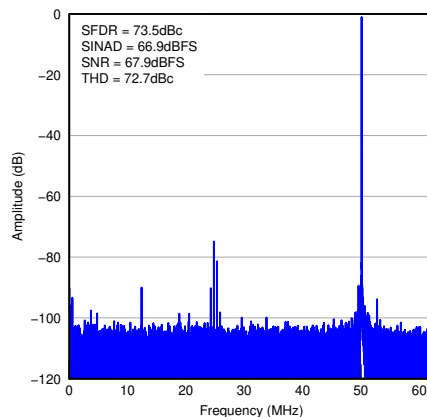


Figure 7-89. FFT for 300-MHz Input Signal

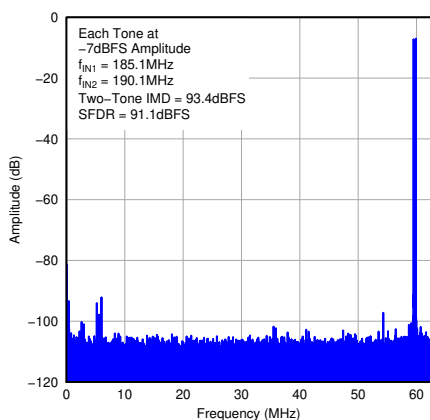


Figure 7-90. FFT for Two-Tone Input Signal

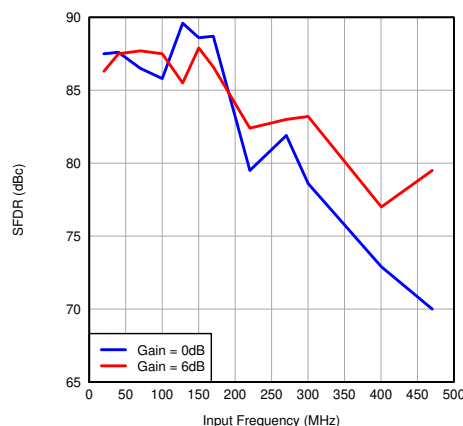


Figure 7-91. SFDR vs Input Frequency

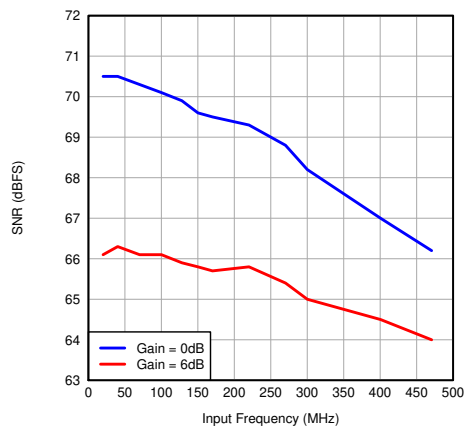


Figure 7-92. SNR vs Input Frequency

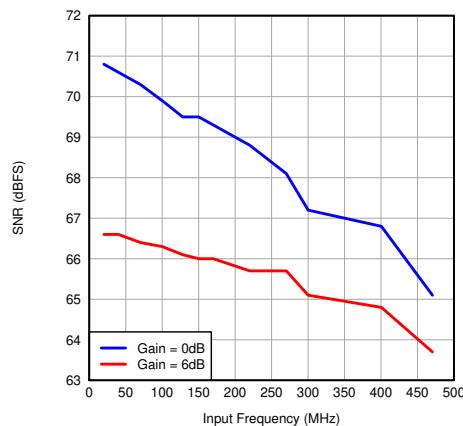


Figure 7-93. SNR vs Input Frequency (CMOS)

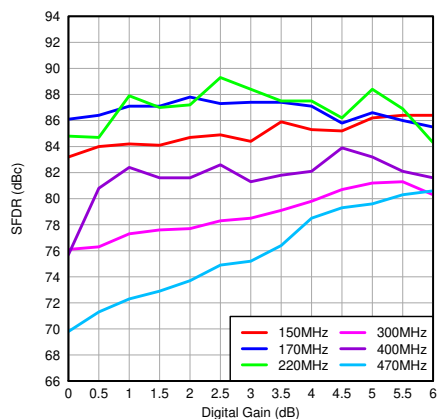


Figure 7-94. SFDR vs Gain and Input Frequency

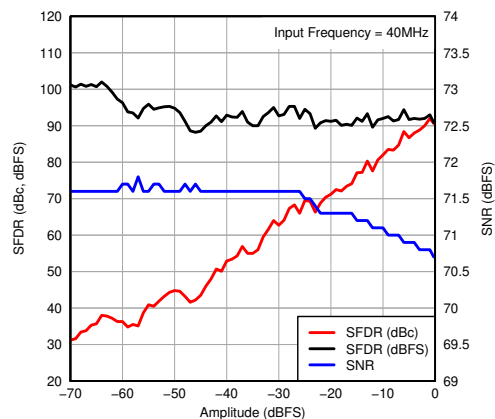


Figure 7-95. Performance vs Input Amplitude

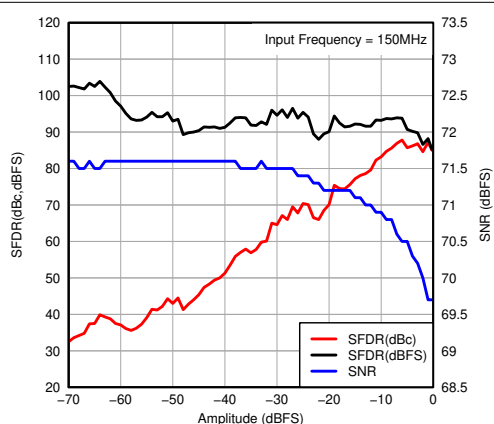


Figure 7-96. Performance vs Input Amplitude

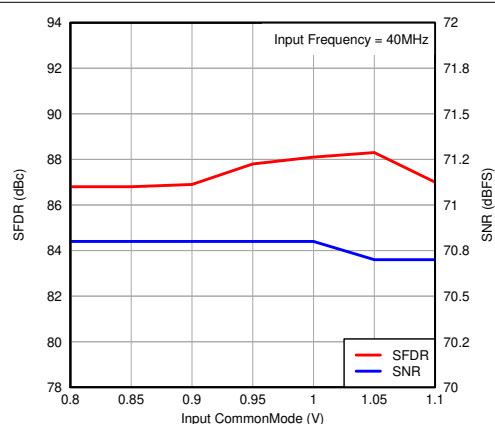


Figure 7-97. Performance vs Input Common-Mode Voltage

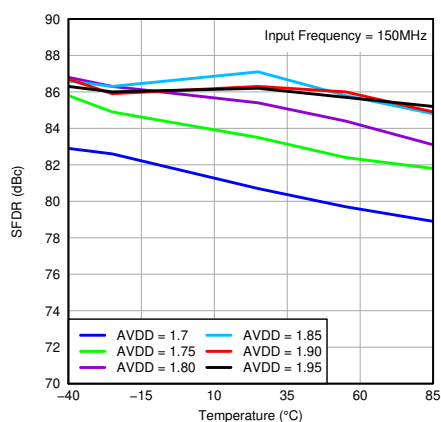


Figure 7-98. SFDR vs Temperature and AVDD Supply

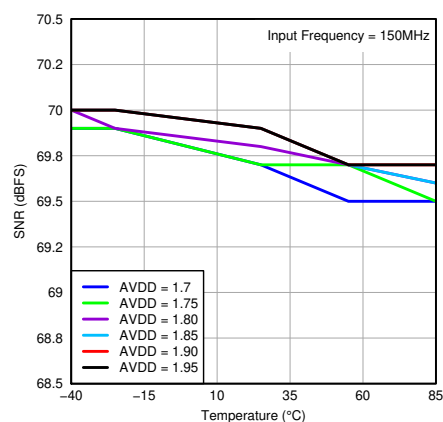


Figure 7-99. SNR vs Temperature and AVDD Supply

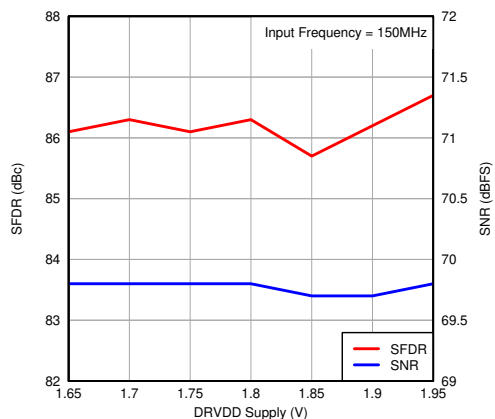


Figure 7-100. Performance vs DRVDD Supply Voltage

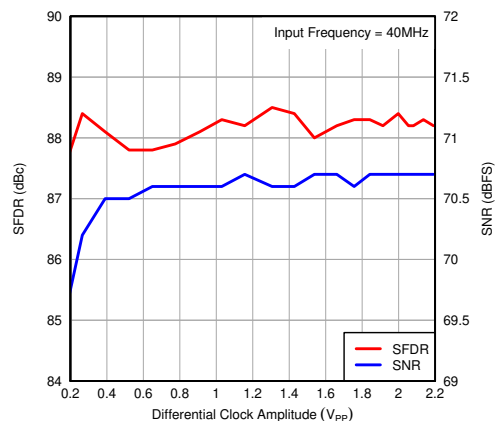


Figure 7-101. Performance vs Input Clock Amplitude

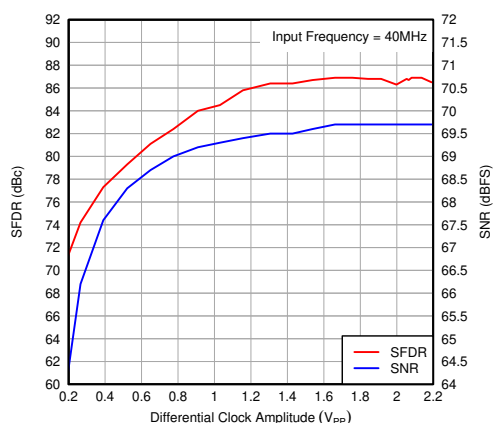


Figure 7-102. Performance vs Input Clock Amplitude

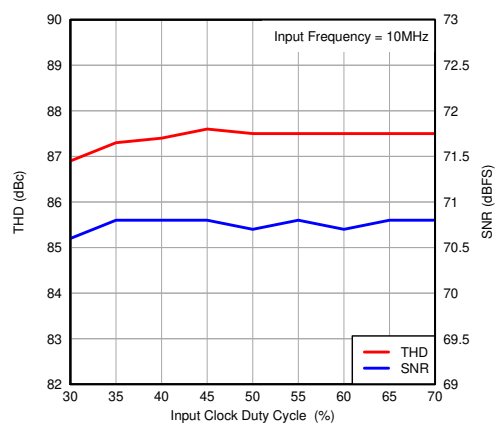


Figure 7-103. Performance vs Input Clock Duty Cycle

7.12.6 ADS4222

At $T_A = 25^\circ\text{C}$, $AV_{DD} = 1.8\text{ V}$, $DRV_{DD} = 1.8\text{ V}$, maximum rated sampling frequency, sine wave input clock, $1.5\text{-}V_{PP}$ differential clock amplitude, 50% clock duty cycle, -1 dBFS differential analog input, High-Performance Mode disabled, 0-dB gain, DDR LVDS output interface, and 32k point FFT, unless otherwise noted.

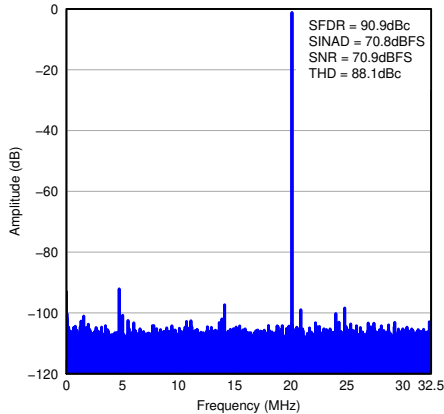


Figure 7-104. FFT for 20-MHz Input Signal

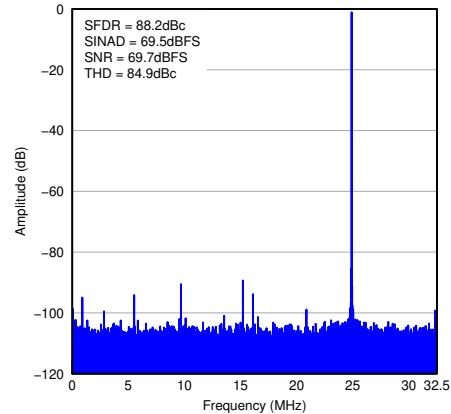


Figure 7-105. FFT for 170-MHz Input Signal

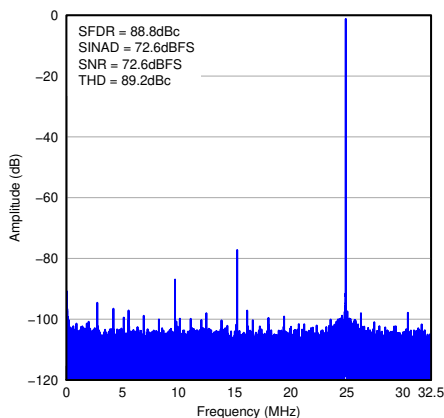


Figure 7-106. FFT for 300-MHz Input Signal

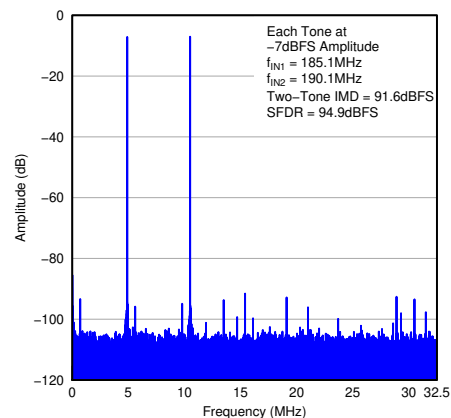


Figure 7-107. FFT for Two-Tone Input Signal

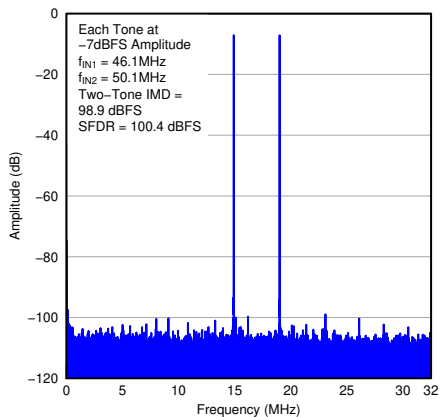


Figure 7-108. FFT for Two-Tone Input Signal

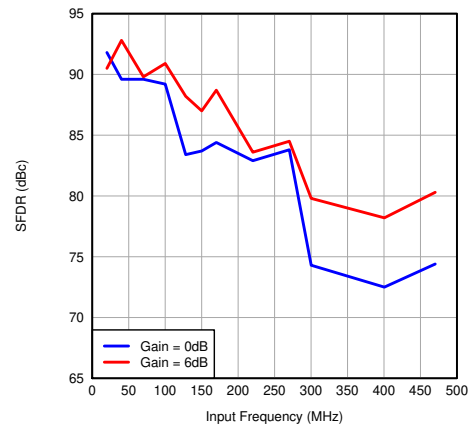


Figure 7-109. SFDR vs Input Frequency

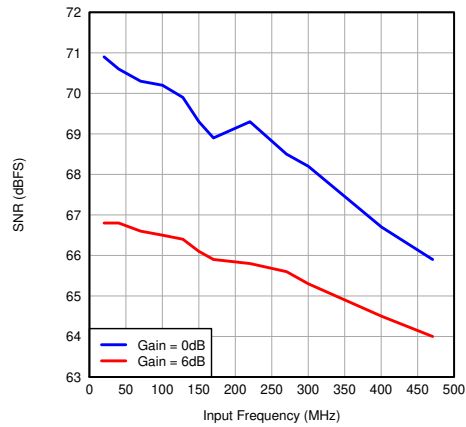


Figure 7-110. SNR vs Input Frequency

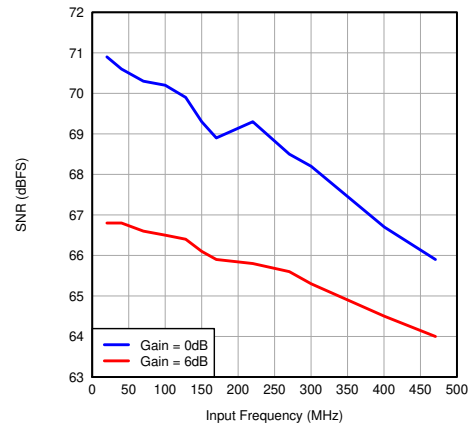


Figure 7-111. SNR vs Input Frequency (CMOS)

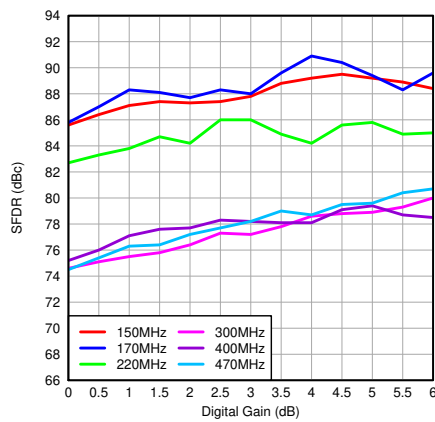


Figure 7-112. SFDR vs Gain and Input Frequency

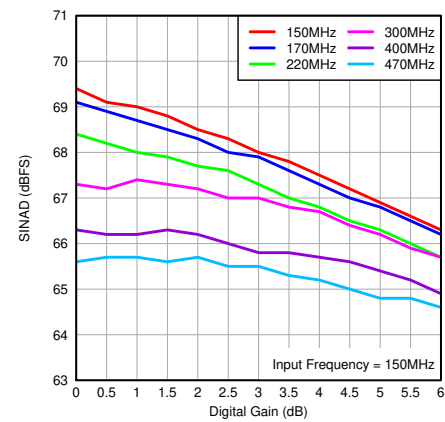


Figure 7-113. SINAD vs Gain and Input Frequency

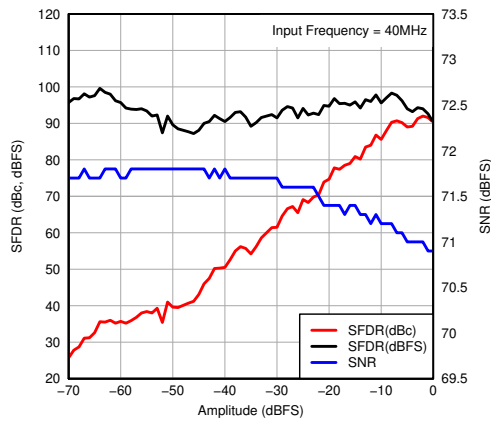


Figure 7-114. Performance vs Input Amplitude

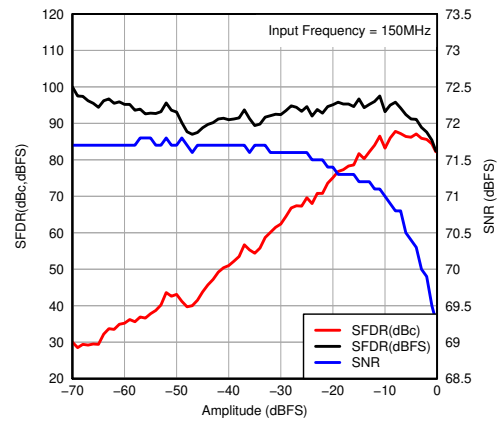


Figure 7-115. Performance vs Input Amplitude

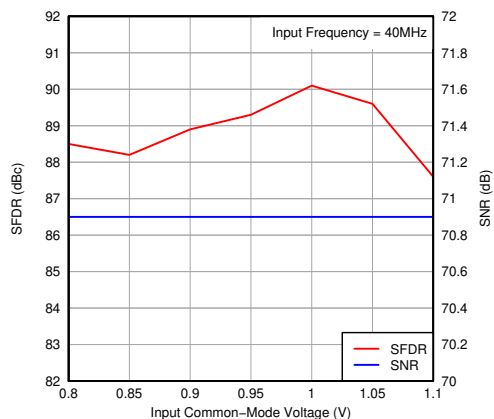


Figure 7-116. Performance vs Input Common-Mode Voltage

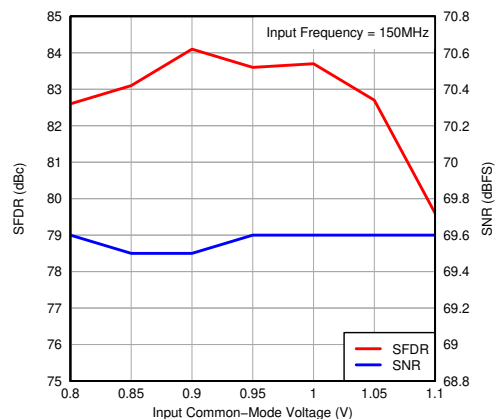


Figure 7-117. Performance vs Input Common-Mode Voltage

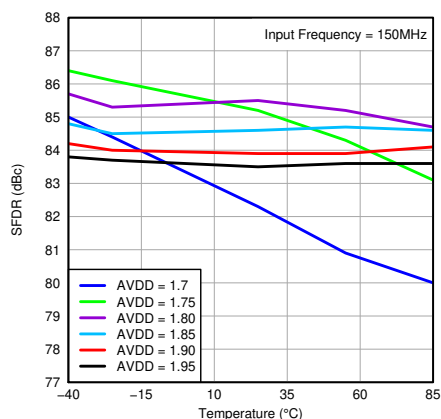


Figure 7-118. SFDR vs Temperature and AVDD Supply

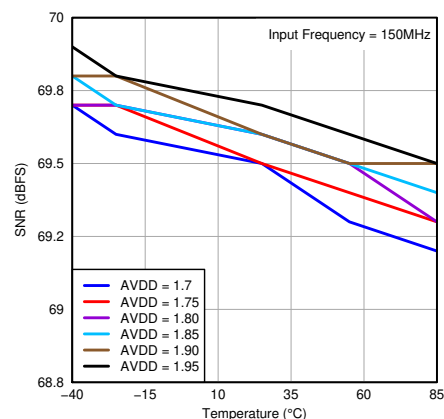


Figure 7-119. SNR vs Temperature and AVDD Supply

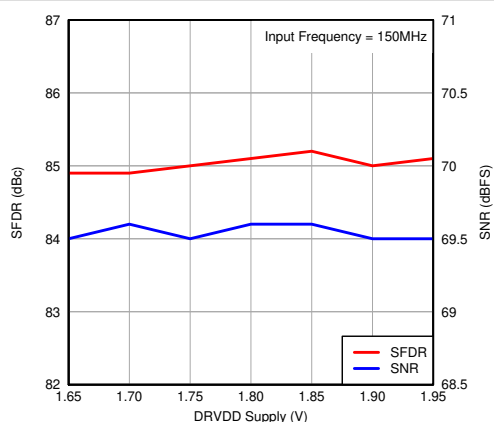


Figure 7-120. Performance vs DRVDD Supply Voltage

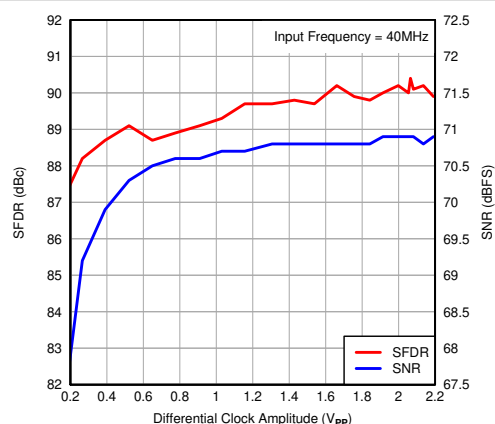


Figure 7-121. Performance vs Input Clock Amplitude

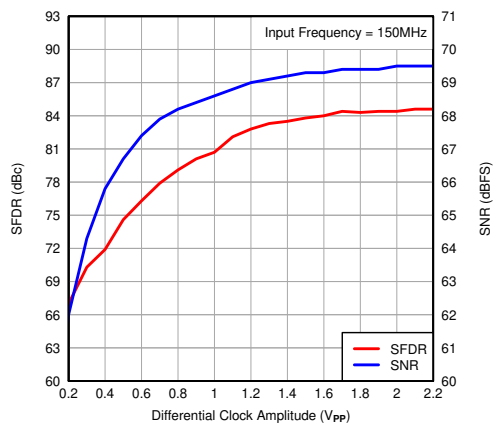


Figure 7-122. Performance vs Input Clock Amplitude

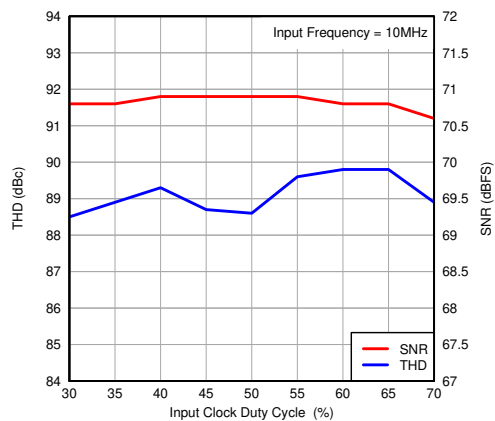


Figure 7-123. Performance vs Input Clock Duty Cycle

7.12.7 General

At $T_A = 25^\circ\text{C}$, $AV_{DD} = 1.8\text{ V}$, $DRV_{DD} = 1.8\text{ V}$, maximum rated sampling frequency, sine wave input clock, $1.5\text{-}V_{PP}$ differential clock amplitude, 50% clock duty cycle, -1 dBFS differential analog input, High-Performance Mode disabled, 0-dB gain, DDR LVDS output interface, and 32k point FFT, unless otherwise noted.

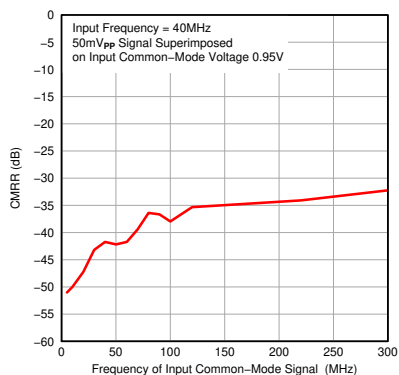


Figure 7-124. CMRR vs Test Signal Frequency

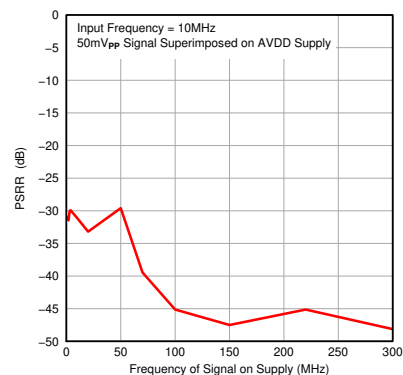


Figure 7-125. PSRR vs Test Signal Frequency

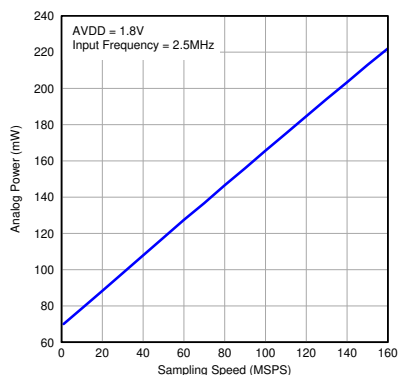


Figure 7-126. Analog Power vs Sampling Frequency

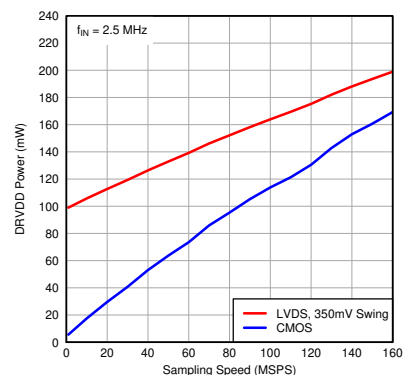


Figure 7-127. Digital Power LVDS CMOS

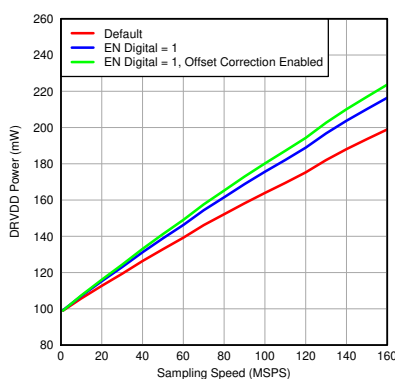


Figure 7-128. Digital Power in Various Modes (LVDS)

7.12.8 Contour

All graphs are at 25°C, AVDD = 1.8 V, DRVDD = 1.8 V, maximum rated sampling frequency, sine wave input clock. 1.5-V_{PP} differential clock amplitude, 50% clock duty cycle, –1 dBFS differential analog input, High-Performance Mode disabled, 0-dB gain, DDR LVDS output interface, and 32k point FFT, unless otherwise noted.

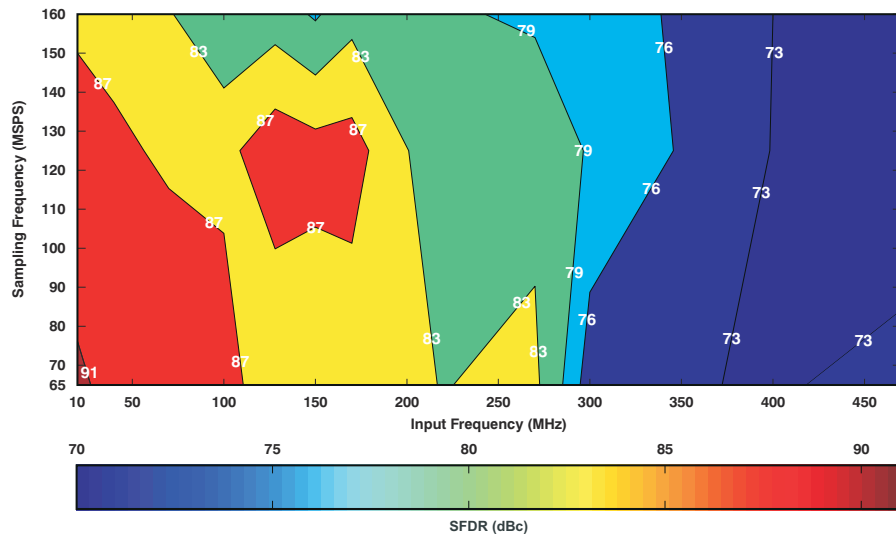


Figure 7-129. Spurious-Free Dynamic Range (0-dB Gain)

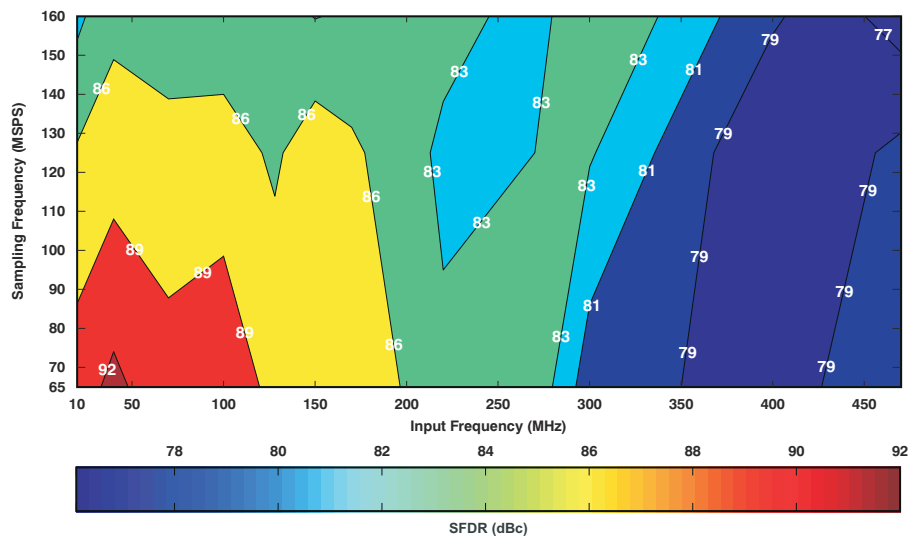


Figure 7-130. Spurious-Free Dynamic Range (6-dB Gain)

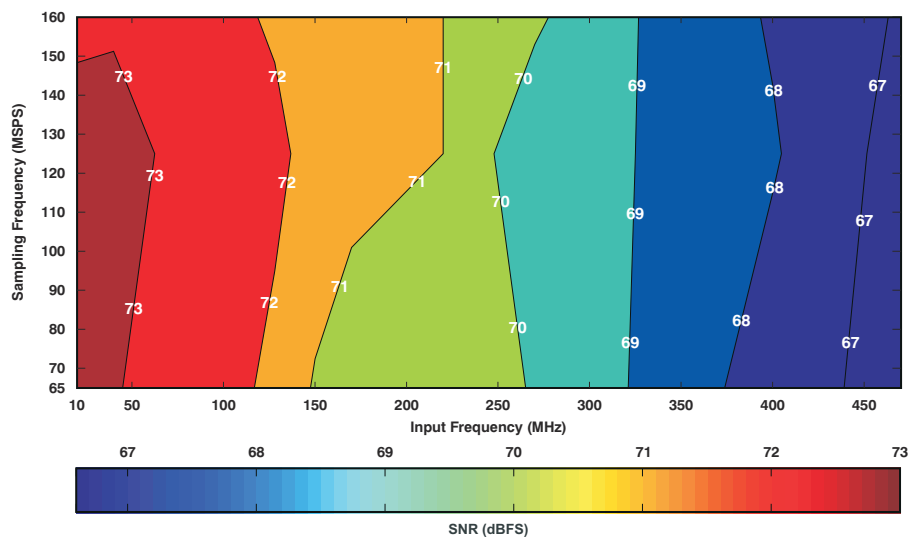


Figure 7-131. ADS424x Signal-to-Noise Ratio (0-dB Gain)

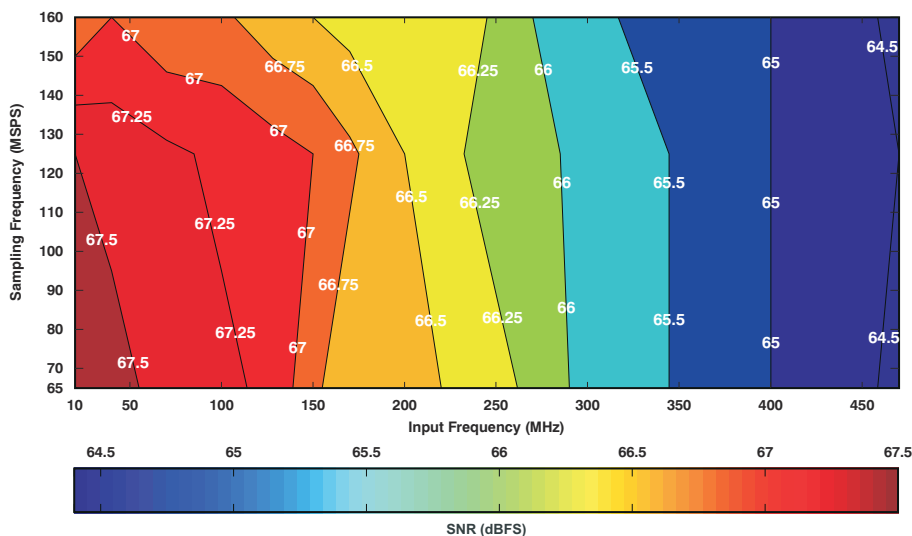


Figure 7-132. ADS424x Signal-to-Noise Ratio (6-dB Gain)

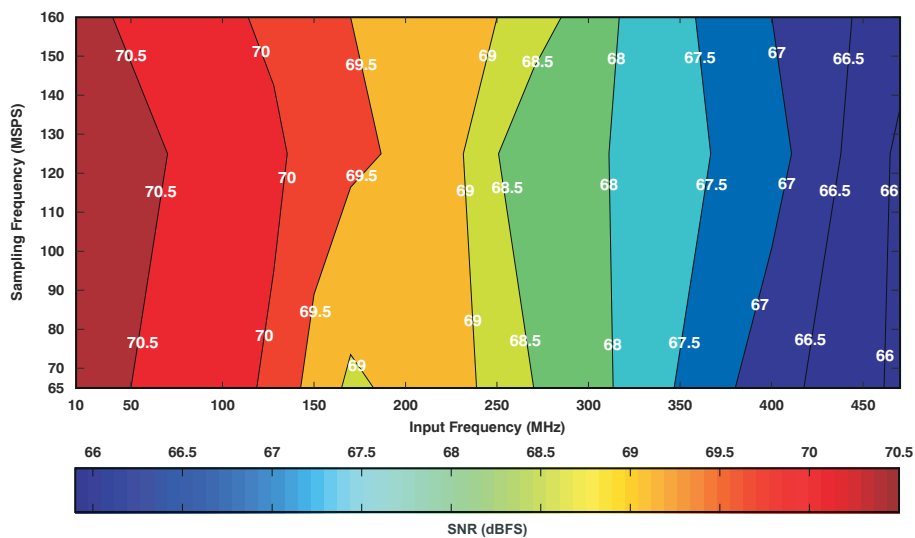


Figure 7-133. ADS422x Signal-to-Noise Ratio (0-dB Gain)

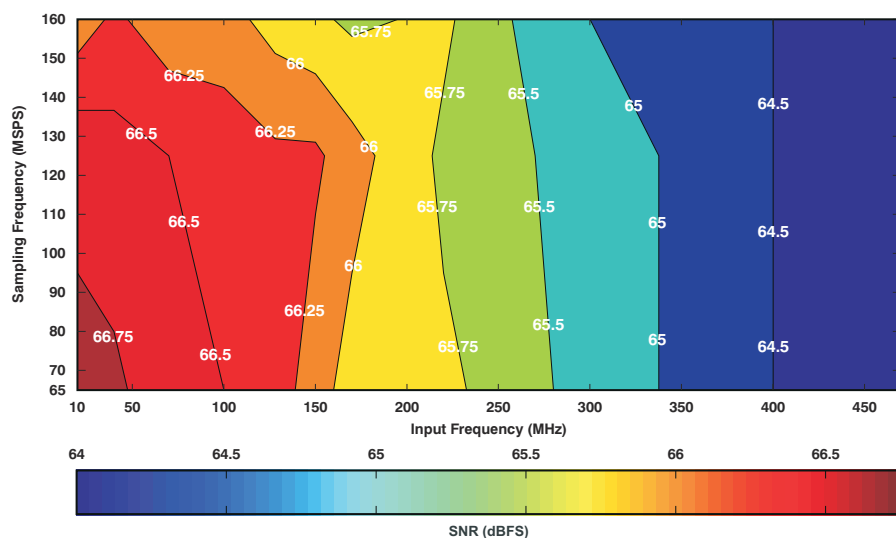


Figure 7-134. ADS422x Signal-to-Noise Ratio (6-dB Gain)

8 Detailed Description

8.1 Overview

The ADS424x/422x belong to TI's ultralow power family of dual-channel, 14-bit/12-bit, analog-to-digital converters (ADCs). High performance is maintained, while power is reduced for power-sensitive applications. In addition to its low power and high performance, the ADS424x/422x has a number of digital features and operating modes to enable design flexibility.

8.2 Functional Block Diagrams

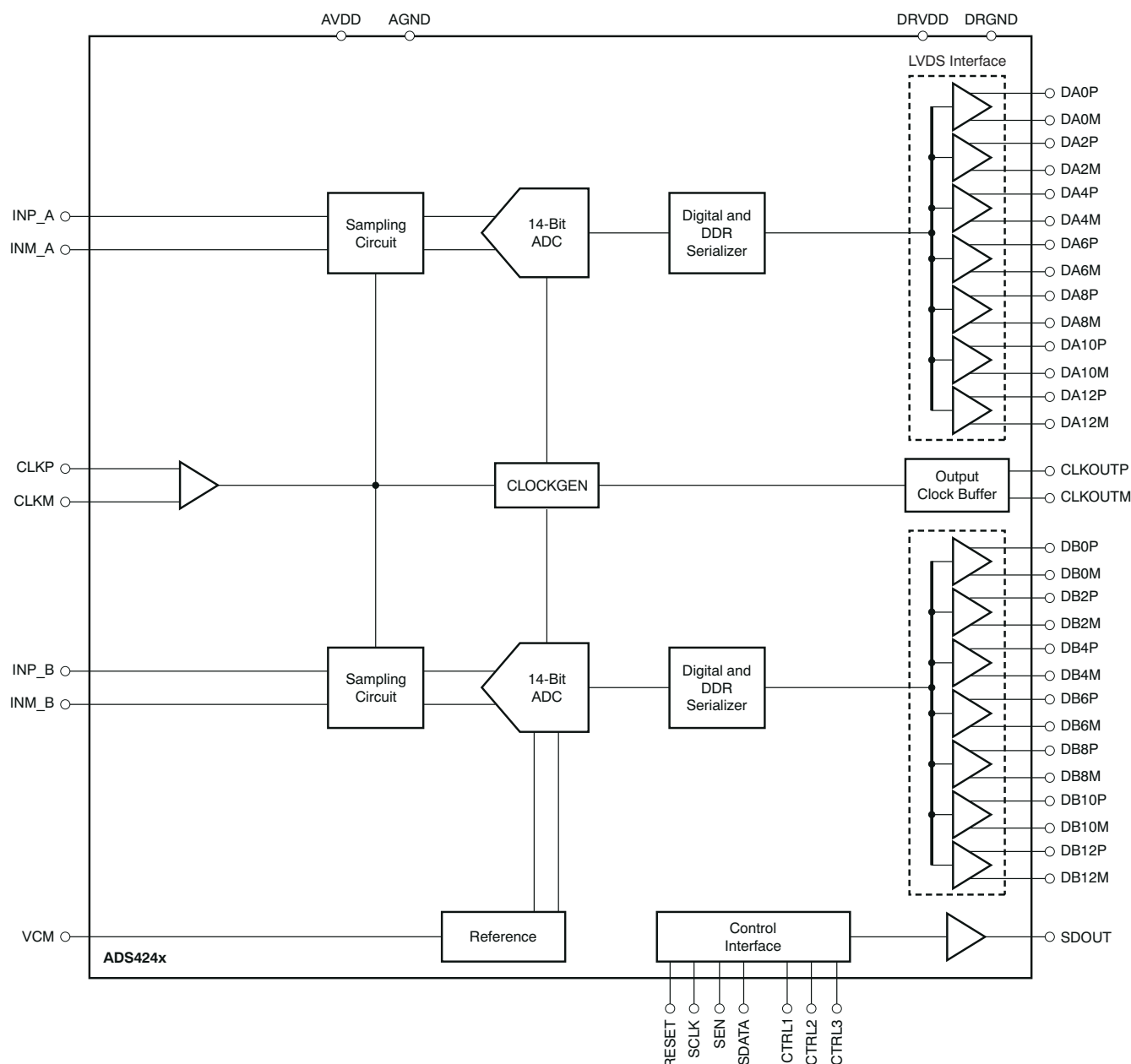


Figure 8-1. ADS4246, 45, 42 Block Diagram

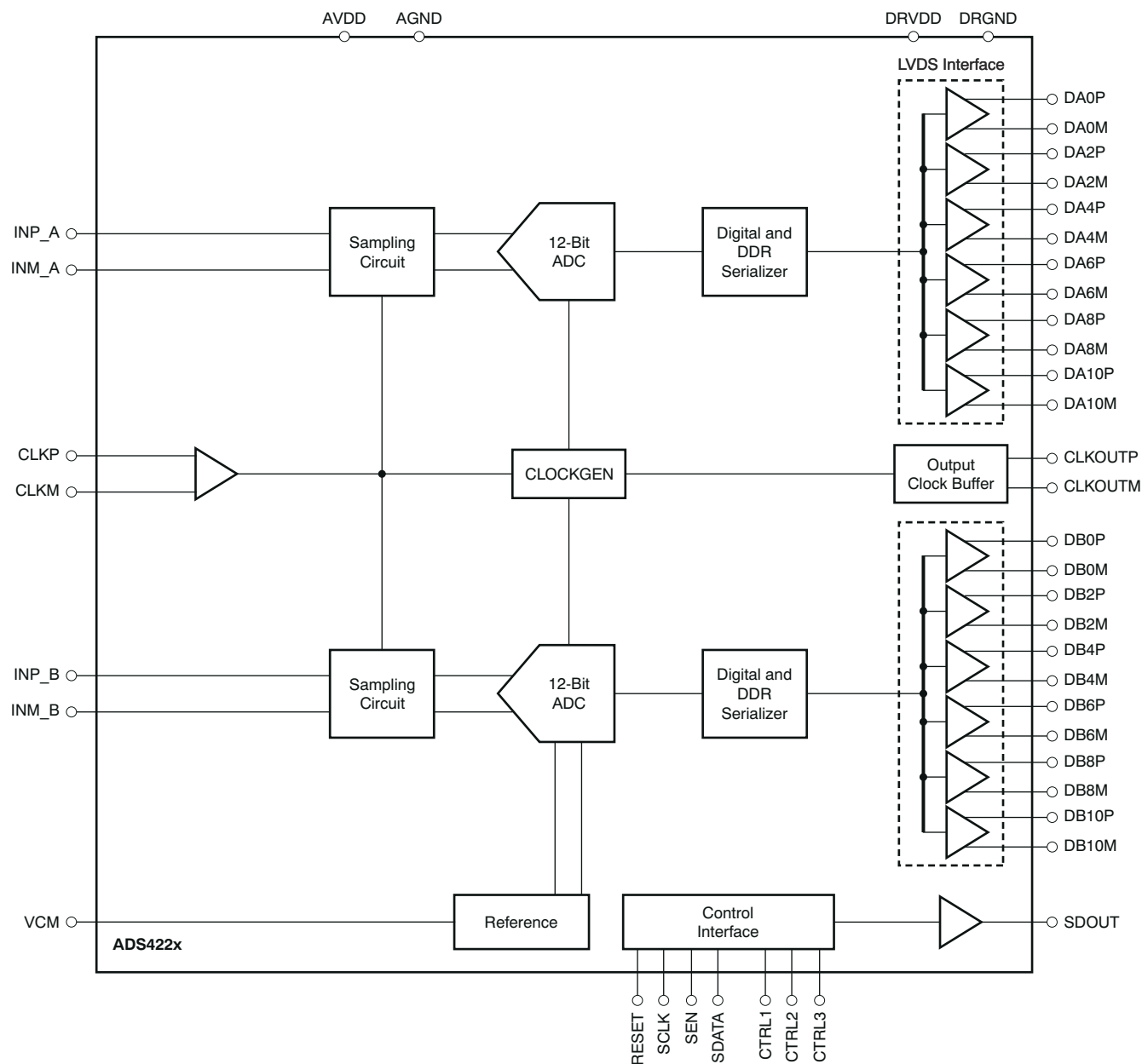


Figure 8-2. ADS4226, 25, 22 Block Diagram

8.3 Feature Description

The ADS424x/422x are pin-compatible with the previous generation ADS62P49 family of data converters; this architecture enables easy migration. However, there are some important differences between the two device generations, summarized in [Table 8-1](#).

Table 8-1. Migrating from the ADS62P49

| ADS62P49 FAMILY | ADS424x/422x FAMILY |
|--|---|
| PINS | |
| Pin 22 is NC (not connected) | Pin 22 is AVDD |
| Pins 38 and 58 are DRVDD | Pins 38 and 58 are NC (do not connect, must be floated) |
| Pins 39 and 59 are DRGND | Pins 39 and 59 are NC (do not connect, must be floated) |
| SUPPLY | |
| AVDD is 3.3 V | AVDD is 1.8 V |
| DRVDD is 1.8 V | No change |
| INPUT COMMON-MODE VOLTAGE | |
| VCM is 1.5 V | VCM is 0.95 V |
| SERIAL INTERFACE | |
| Protocol: 8-bit register address and 8-bit register data | No change in protocol New serial register map |
| EXTERNAL REFERENCE | |
| Supported | Not supported |

8.3.1 Analog Input

The analog input consists of a switched-capacitor based, differential sample-and-hold (S/H) architecture. This differential topology results in very good ac performance even for high input frequencies at high sampling rates. The INP and INM pins must be externally biased around a common-mode voltage of 0.95 V, available on the VCM pin. For a full-scale differential input, each input pin (INP and INM) must swing symmetrically between $V_{CM} + 0.5\text{ V}$ and $V_{CM} - 0.5\text{ V}$, resulting in a $2\text{-}V_{PP}$ differential input swing. The input sampling circuit has a high 3 dB bandwidth that extends up to 550 MHz (measured from the input pins to the sampled voltage). [Figure 8-3](#) shows an equivalent circuit for the analog input.

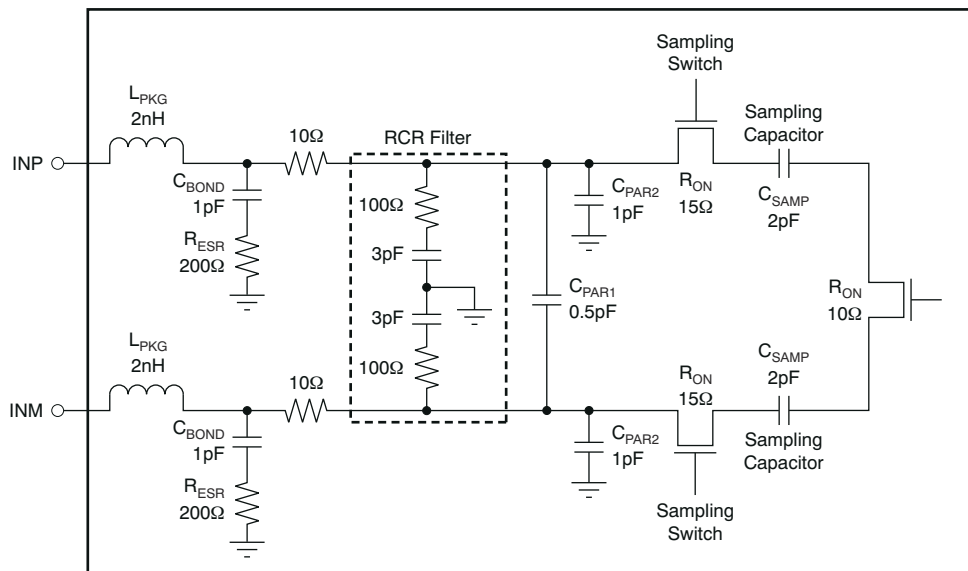


Figure 8-3. Analog Input Equivalent Circuit

8.3.1.1 Drive Circuit Requirements

For optimum performance, the analog inputs must be driven differentially. This operation improves the common-mode noise immunity and even-order harmonic rejection. A 5Ω to 15Ω resistor in series with each input pin is recommended to damp out ringing caused by package parasitics.

SFDR performance can be limited as a result of several reasons, including the effects of sampling glitches, nonlinearity of the sampling circuit, and nonlinearity of the quantizer that follows the sampling circuit. Depending on the input frequency, sample rate, and input amplitude, one of these factors plays a dominant part in limiting performance. At very high input frequencies (greater than approximately 300 MHz), SFDR is determined largely by the device sampling circuit nonlinearity. At low input amplitudes, the quantizer nonlinearity usually limits performance.

Glitches are caused by the opening and closing of the sampling switches. The driving circuit should present a low source impedance to absorb these glitches. Otherwise, glitches could limit performance, primarily at low input frequencies (up to approximately 200 MHz). It is also necessary to present low impedance (less than 50Ω) for the common-mode switching currents. This configuration can be achieved by using two resistors from each input terminated to the common-mode voltage (VCM).

The device includes an internal R-C filter from each input to ground. The purpose of this filter is to absorb the sampling glitches inside the device itself. The cutoff frequency of the R-C filter involves a trade-off. A lower cutoff frequency (larger C) absorbs glitches better, but it reduces the input bandwidth. On the other hand, with a higher cutoff frequency (smaller C), bandwidth support is maximized. However, the sampling glitches now must be supplied by the external drive circuit. This tradeoff has limitations as a result of the presence of the package bond-wire inductance.

In the ADS424x/422x, the R-C component values have been optimized while supporting high input bandwidth (up to 550 MHz). However, in applications with input frequencies up to 200 MHz to 300 MHz, the filtering of the glitches can be improved further using an external R-C-R filter; see [Figure 8-6](#) and [Figure 8-7](#).

In addition, the drive circuit may have to be designed to provide a low insertion loss over the desired frequency range and matched impedance to the source. Furthermore, the ADC input impedance must be considered. [Figure 8-4](#) and [Figure 8-5](#) show the impedance ($Z_{IN} = R_{IN} \parallel C_{IN}$) looking into the ADC input pins.

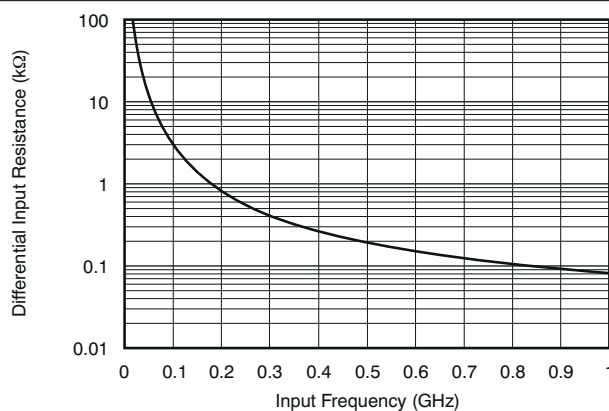


Figure 8-4. ADC Analog Input Resistance (R_{IN}) Across Frequency

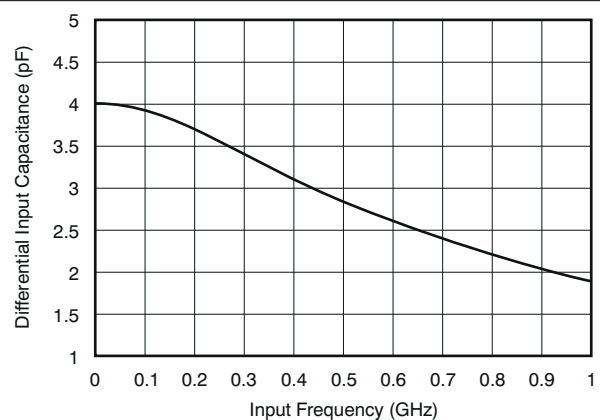


Figure 8-5. ADC Analog Input Capacitance (C_{IN}) Across Frequency

8.3.1.2 Driving Circuit

Two example driving circuit configurations are shown in [Figure 8-6](#) and [Figure 8-7](#)—one optimized for low bandwidth (low input frequencies) and the other one for high bandwidth to support higher input frequencies. Note that both of the drive circuits have been terminated by 50Ω near the ADC side. The termination is accomplished by a 25Ω resistor from each input to the 1.5-V common-mode (VCM) from the device. This architecture allows the analog inputs to be biased around the required common-mode voltage.

The mismatch in the transformer parasitic capacitance (between the windings) results in degraded even-order harmonic performance. Connecting two identical RF transformers back-to-back helps minimize this mismatch; good performance is obtained for high-frequency input signals. An additional termination resistor pair may be required between the two transformers, as shown in [Figure 8-6](#), [Figure 8-7](#), and [Figure 8-8](#). The center point of this termination is connected to ground to improve the balance between the P and M sides. The values of the terminations between the transformers and on the secondary side must be chosen to obtain an effective 50Ω (in the case of 50Ω source impedance).

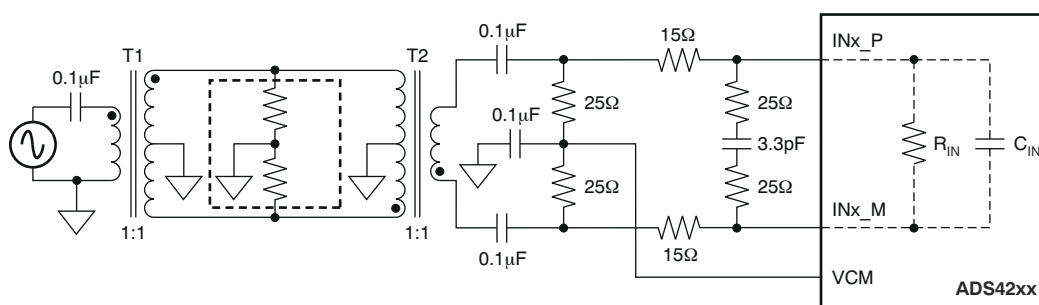


Figure 8-6. Drive Circuit with Low Bandwidth (for Low Input Frequencies Less Than 150 MHz)

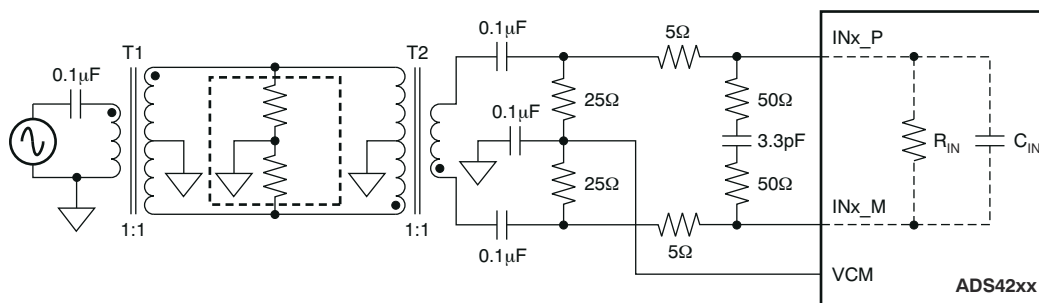


Figure 8-7. Drive Circuit with High Bandwidth (for High Input Frequencies Greater Than 150 MHz and Less Than 270 MHz)

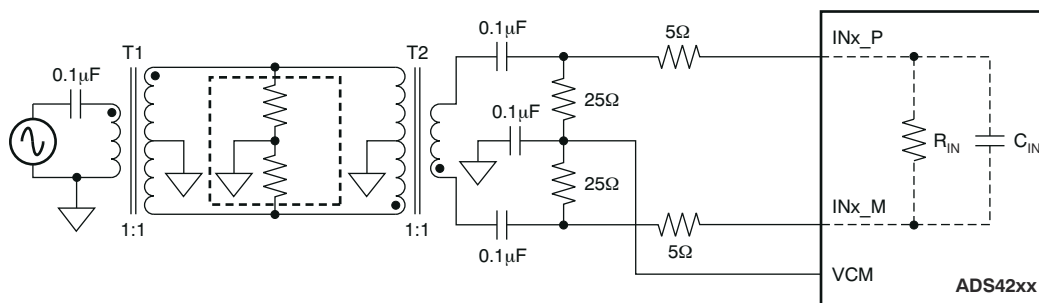


Figure 8-8. Drive Circuit with Very High Bandwidth (Greater than 270 MHz)

All of these examples show 1:1 transformers being used with a 50-Ω source. As explained in the [Section 8.3.1.1](#) section, this configuration helps to present a low source impedance to absorb the sampling glitches. With a 1:4 transformer, the source impedance is 200 Ω. The higher source impedance is unable to absorb the sampling glitches effectively and can lead to degradation in performance (compared to using 1:1 transformers).

In almost all cases, either a band-pass or low-pass filter is required to obtain the desired dynamic performance, as shown in [Figure 8-9](#). Such filters present low source impedance at the high frequencies corresponding to the sampling glitch and help avoid the performance loss with the high source impedance.

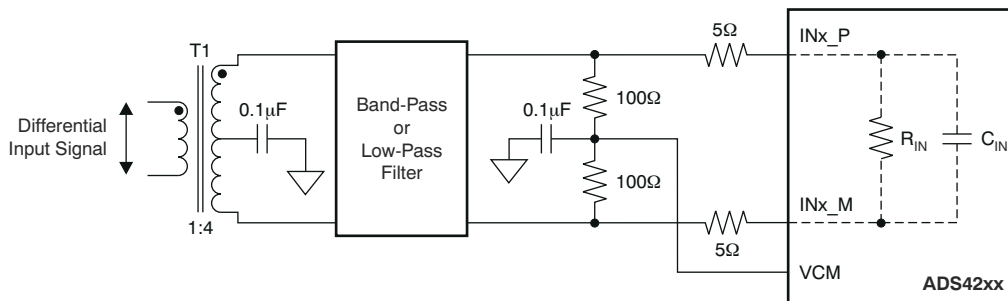
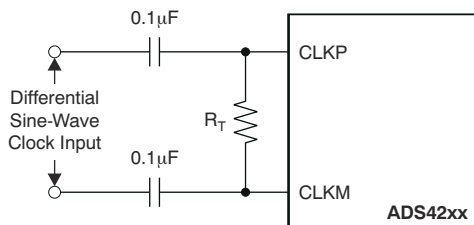


Figure 8-9. Drive Circuit with a 1:4 Transformer

8.3.2 Clock Input

The ADS424x/422x clock inputs can be driven differentially (sine, LVPECL, or LVDS) or single-ended (LVCMOS), with little or no difference in performance between them. The common-mode voltage of the clock inputs is set to VCM using internal 5-kΩ resistors. This setting allows the use of transformer-coupled drive circuits for sine-wave clock or ac-coupling for LVPECL and LVDS clock sources are shown in [Figure 8-10](#), [Figure 8-11](#) and [Figure 8-12](#). The internal clock buffer is shown in [Figure 8-13](#).



R_T = termination resistor, if necessary.

Figure 8-10. Differential Sine-Wave Clock Driving Circuit

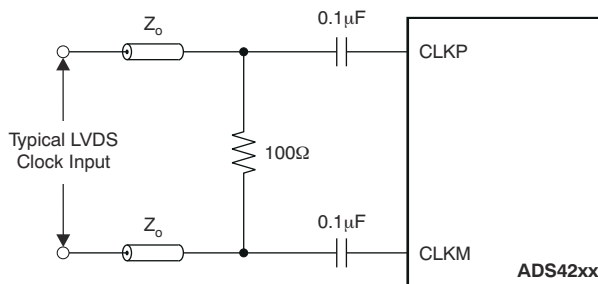


Figure 8-11. LVDS Clock Driving Circuit

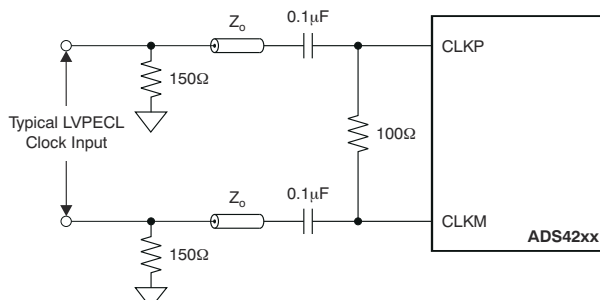
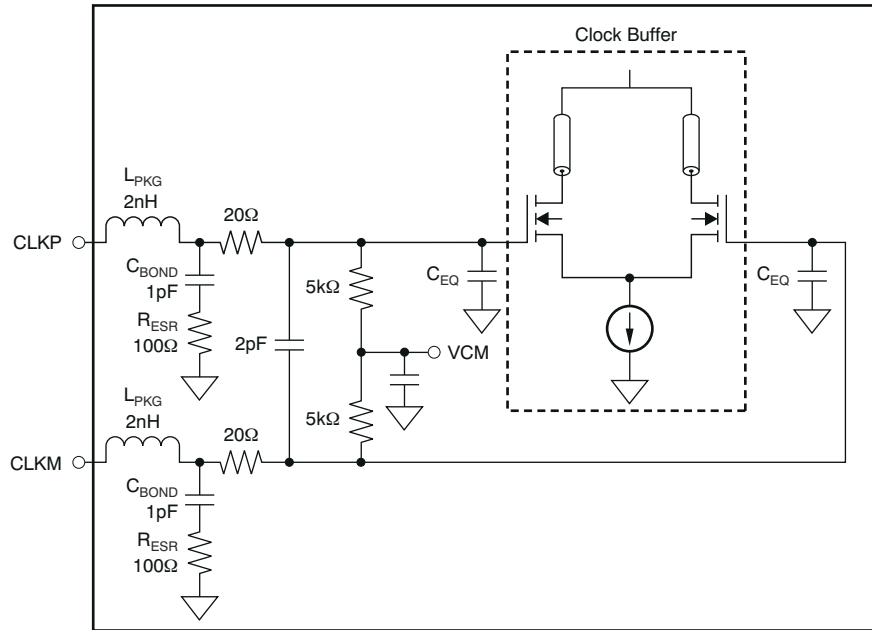


Figure 8-12. LVPECL Clock Driving Circuit



C_{EQ} is 1 pF to 3 pF, and is the equivalent input capacitance of the clock buffer.

Figure 8-13. Internal Clock Buffer

A single-ended CMOS clock can be ac-coupled to the CLKP input, with CLKM connected to ground with a 0.1-μF capacitor, as shown in Figure 8-14. For best performance, the clock inputs must be driven differentially, thereby reducing susceptibility to common-mode noise. For high input frequency sampling, it is recommended to use a clock source with very low jitter. Band-pass filtering of the clock source can help reduce the effects of jitter. There is no change in performance with a non-50% duty cycle clock input.

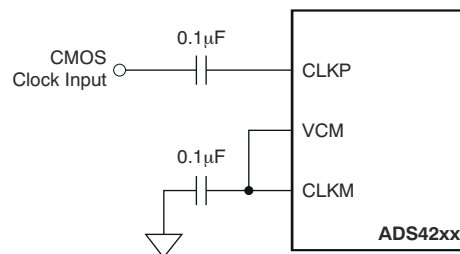


Figure 8-14. Single-Ended Clock Driving Circuit

8.3.3 Digital Functions

The device has several useful digital functions (such as test patterns, gain, and offset correction). These functions require extra clock cycles for operation and increase the overall latency and power of the device. These digital functions are disabled by default after reset and the raw ADC output is routed to the output data pins with a latency of 16 clock cycles. [Figure 8-15](#) shows more details of the processing after the ADC. In order to use any of the digital functions, the EN DIGITAL bit must be set to 1. After this, the respective register bits must be programmed as described in the following sections and in the [Section 8.6](#) section.

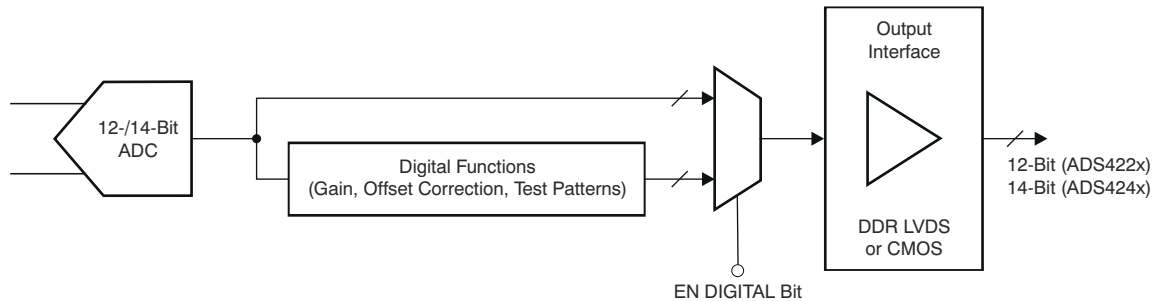


Figure 8-15. Digital Processing Block

8.3.4 Gain for SFDR/SNR Trade-off

The ADS424x/422x include gain settings that can be used to get improved SFDR performance (compared to no gain). The gain is programmable from 0 dB to 6 dB (in 0.5-dB steps). For each gain setting, the analog input full-scale range scales proportionally, as shown in [Table 8-2](#).

The SFDR improvement is achieved at the expense of SNR; for each gain setting, the SNR degrades approximately between 0.5 dB and 1 dB. The SNR degradation is reduced at high input frequencies. As a result, the gain is very useful at high input frequencies because the SFDR improvement is significant with marginal degradation in SNR. Therefore, the gain can be used as a trade-off between SFDR and SNR. Note that the default gain after reset is 0 dB.

Table 8-2. Full-Scale Range Across Gains

| GAIN (dB) | TYPE | FULL-SCALE (V _{PP}) |
|-----------|---------------------|-------------------------------|
| 0 | Default after reset | 2 |
| 1 | Fine, programmable | 1.78 |
| 2 | Fine, programmable | 1.59 |
| 3 | Fine, programmable | 1.42 |
| 4 | Fine, programmable | 1.26 |
| 5 | Fine, programmable | 1.12 |
| 6 | Fine, programmable | 1 |

8.3.5 Offset Correction

The ADS424x/422x have an internal offset correction algorithm that estimates and corrects dc offset up to ± 10 mV. The correction can be enabled using the ENABLE OFFSET CORR serial register bit. Once enabled, the algorithm estimates the channel offset and applies the correction every clock cycle. The time constant of the correction loop is a function of the sampling clock frequency. The time constant can be controlled using the OFFSET CORR TIME CONSTANT register bits, as described in [Table 8-3](#).

After the offset is estimated, the correction can be frozen by setting FREEZE OFFSET CORR = 0. Once frozen, the last estimated value is used for the offset correction of every clock cycle. Note that offset correction is disabled by default after reset.

Table 8-3. Time Constant of Offset Correction Algorithm

| OFFSET CORR TIME CONSTANT | TIME CONSTANT, TC_{CLK} (Number of Clock Cycles) | TIME CONSTANT, $TC_{CLK} \times 1/f_S$ (ms) ⁽¹⁾ |
|---------------------------|---|--|
| 0000 | 1M | 7 |
| 0001 | 2M | 13 |
| 0010 | 4M | 26 |
| 0011 | 8M | 52 |
| 0100 | 16M | 105 |
| 0101 | 32M | 210 |
| 0110 | 64M | 419 |
| 0111 | 128M | 839 |
| 1000 | 256M | 1678 |
| 1001 | 512M | 3355 |
| 1010 | 1G | 6711 |
| 1011 | 2G | 13422 |
| 1100 | Reserved | — |
| 1101 | Reserved | — |
| 1110 | Reserved | — |
| 1111 | Reserved | — |

(1) Sampling frequency, $f_S = 160$ MSPS.

8.4 Device Functional Modes

8.4.1 Power-Down

The ADS424x/422x have two power-down modes: global power-down and channel standby. These modes can be set using either the serial register bits or using the control pins CTRL1 to CTRL3 (as shown in [Table 8-4](#)).

Table 8-4. Power-Down Settings

| CTRL1 | CTRL2 | CTRL3 | DESCRIPTION |
|-------|-------|-------|--|
| Low | Low | Low | Default |
| Low | Low | High | Not available |
| Low | High | Low | Not available |
| Low | High | High | Not available |
| High | Low | Low | Global power-down |
| High | Low | High | Channel A powered down, channel B is active |
| High | High | Low | Not available |
| High | High | High | MUX mode of operation, channel A and B data is multiplexed and output on DB[10:0] pins |

8.4.1.1 Global Power-Down

In this mode, the entire chip (including ADCs, internal reference, and output buffers) are powered down, resulting in reduced total power dissipation of approximately 20 mW when the CTRL pins are used, and 3 mW when the PDN GLOBAL serial register bit is used. The output buffers are in high-impedance state. The wake-up time from global power-down to data becoming valid in normal mode is typically 100µs.

8.4.1.2 Channel Standby

In this mode, each ADC channel can be powered down. The internal references are active, resulting in a quick wake-up time of 50 µs. The total power dissipation in standby is approximately 200 mW at 160 MSPS.

8.4.1.3 Input Clock Stop

In addition to the previous modes, the converter enters a low-power mode when the input clock frequency falls below 1 MSPS. The power dissipation is approximately 160 mW.

8.5 Programming

8.5.1

The ADS424x/422x can be configured independently using either parallel interface control or serial interface programming.

8.5.2 Parallel Configuration Only

To put the device into parallel configuration mode, keep RESET tied high (AVDD). Then, use the SEN, SCLK, CTRL1, CTRL2, and CTRL3 pins to directly control certain modes of the ADC. The device can be easily configured by connecting the parallel pins to the correct voltage levels (as described in [Table 8-5](#) to [Table 8-8](#)). There is no need to apply a reset and SDATA can be connected to ground.

In this mode, SEN and SCLK function as parallel interface control pins. Some frequently-used functions can be controlled using these pins. [Table 8-5](#) describes the modes controlled by the parallel pins.

Table 8-5. Parallel Pin Definition

| PIN | CONTROL MODE |
|-------|---|
| SCLK | Low-speed mode selection |
| SEN | Output data format and output interface selection |
| CTRL1 | Together, these pins control the power-down modes |
| CTRL2 | |
| CTRL3 | |

8.5.3 Serial Interface Configuration Only

To enable this mode, the serial registers must first be reset to the default values and the RESET pin must be kept low. SEN, SDATA, and SCLK function as serial interface pins in this mode and can be used to access the internal registers of the ADC. The registers can be reset either by applying a pulse on the RESET pin or by setting the RESET bit high. The [Section 8.6](#) section describes the register programming and the register reset process in more detail.

8.5.4 Using Both Serial Interface and Parallel Controls

For increased flexibility, a combination of serial interface registers and parallel pin controls (CTRL1 to CTRL3) can also be used to configure the device. To enable this option, keep RESET low. The parallel interface control pins CTRL1 to CTRL3 are available. After power-up, the device is automatically configured according to the voltage settings on these pins (see [Table 8-8](#)). SEN, SDATA, and SCLK function as serial interface digital pins and are used to access the internal registers of the ADC. The registers must first be reset to the default values either by applying a pulse on the RESET pin or by setting the RESET bit to '1'. After reset, the RESET pin must be kept low. The [Section 8.6](#) section describes register programming and the register reset process in more detail.

8.5.5 Parallel Configuration Details

The functions controlled by each parallel pin are described in [Table 8-6](#), [Table 8-7](#), and [Table 8-8](#). A simple way of configuring the parallel pins is shown in [Figure 8-16](#).

Table 8-6. SCLK Control Pin

| VOLTAGE APPLIED ON SCLK | DESCRIPTION |
|-------------------------|--|
| Low | Low-speed mode is disabled |
| High | Low-speed mode is enabled ⁽¹⁾ |

(1) Low-speed mode is enabled in the ADS4222/42 by default.

Table 8-7. SEN Control Pin

| VOLTAGE APPLIED ON SEN | DESCRIPTION |
|-------------------------|--|
| 0 (+50 mV/0 mV) | Twos complement and parallel CMOS output |
| (3/8) AVDD (±50 mV) | Offset binary and parallel CMOS output |
| (5/8) 2AVDD (±50 mV) | Offset binary and DDR LVDS output |
| AVDD (0 mV/–50 mV) | Twos complement and DDR LVDS output |

Table 8-8. CTRL1, CTRL2, and CTRL3 Pins

| CTRL1 | CTRL2 | CTRL3 | DESCRIPTION |
|-------|-------|-------|--|
| Low | Low | Low | Normal operation |
| Low | Low | High | Not available |
| Low | High | Low | Not available |
| Low | High | High | Not available |
| High | Low | Low | Global power-down |
| High | Low | High | Channel A standby, channel B is active |
| High | High | Low | Not available |
| High | High | High | MUX mode of operation, channel A and B data are multiplexed and output on the DB[13:0] pins. |

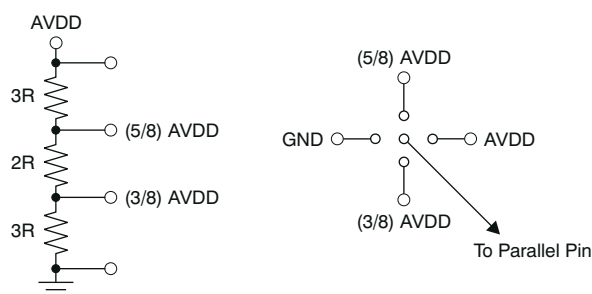


Figure 8-16. Simple Scheme to Configure the Parallel Pins

8.5.6 Serial Interface Details

The ADC has a set of internal registers that can be accessed by the serial interface formed by the SEN (serial interface enable), SCLK (serial interface clock), and SDATA (serial interface data) pins. Serial shift of bits into the device is enabled when SEN is low. Serial data SDATA are latched at every SCLK falling edge when SEN is active (low). The serial data are loaded into the register at every 16th SCLK falling edge when SEN is low. When the word length exceeds a multiple of 16 bits, the excess bits are ignored. Data can be loaded in multiples of 16-bit words within a single active SEN pulse. The first eight bits form the register address and the remaining

eight bits are the register data. The interface can work with SCLK frequencies from 20 MHz down to very low speeds (of a few hertz) and also with non-50% SCLK duty cycle.

8.5.6.1 Register Initialization

After power-up, the internal registers must be initialized to the default values. Initialization can be accomplished in one of two ways:

1. Either through hardware reset by applying a high pulse on the RESET pin (of width greater than 10ns), as shown in Figure 8-17; or
2. By applying a software reset. When using the serial interface, set the RESET bit high. This setting initializes the internal registers to the default values and then self-resets the RESET bit low. In this case, the RESET pin is kept low.

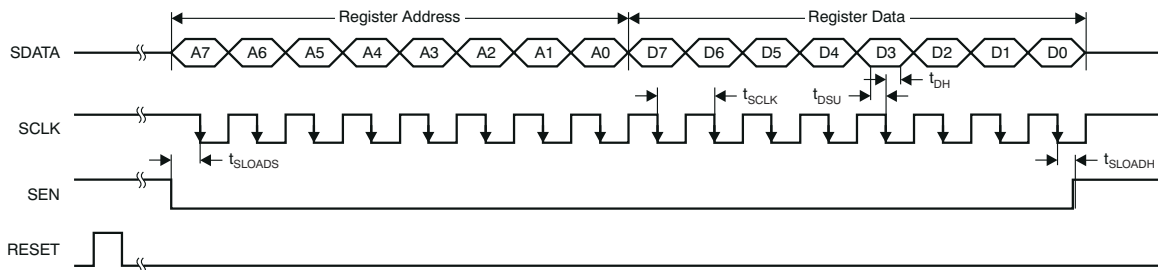


Figure 8-17. Serial Interface Timing

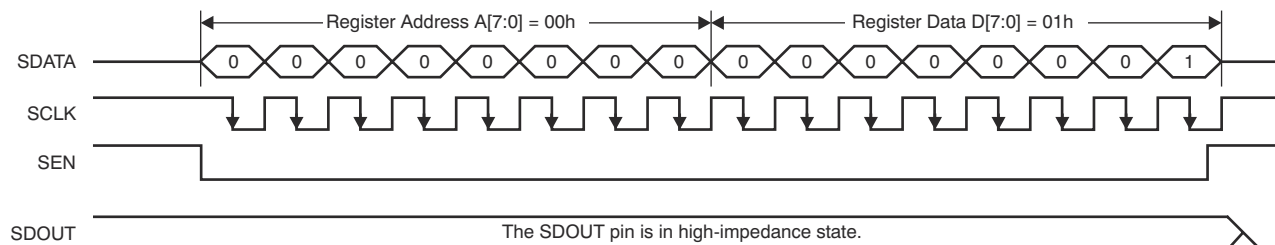
8.5.6.2 Serial Register Readout

The device includes a mode where the contents of the internal registers can be read back. This readback mode may be useful as a diagnostic check to verify the serial interface communication between the external controller and the ADC. To use readback mode, follow this procedure:

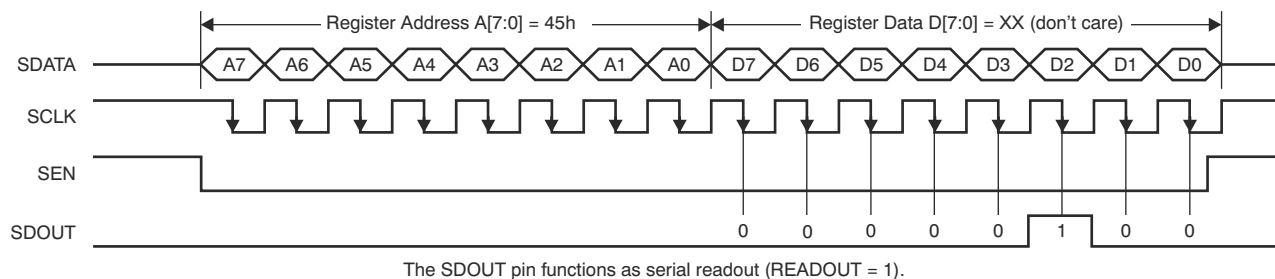
1. Set the READOUT register bit to 1. This setting disables any further writes to the registers.
2. Initiate a serial interface cycle specifying the address of the register (A7 to A0) whose content has to be read.
3. The device outputs the contents (D7 to D0) of the selected register on the SDOUT pin (pin 64).
4. The external controller can latch the contents at the SCLK falling edge.
5. To enable register writes, reset the READOUT register bit to 0.

The serial register readout works with both CMOS and LVDS interfaces on pin 64.

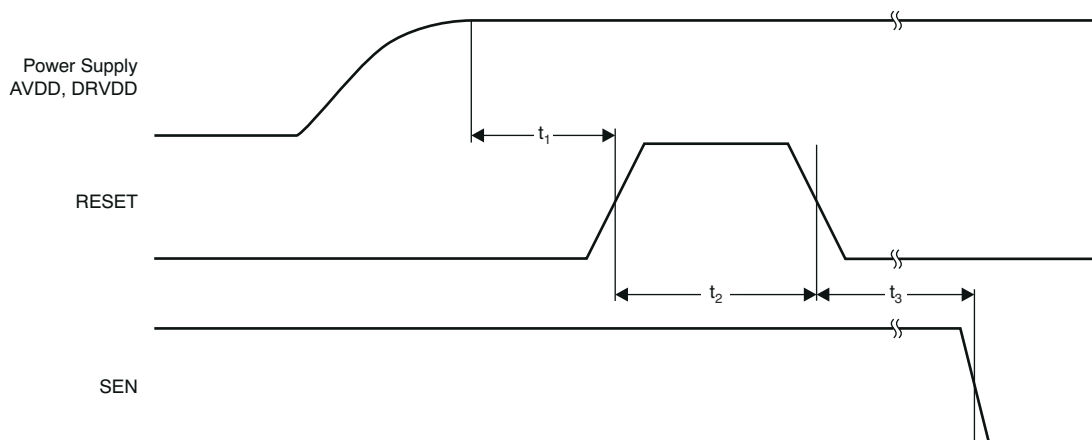
When READOUT is disabled, the SDOUT pin is in high-impedance state. If serial readout is not used, the SDOUT pin must float.



a) Enable serial readout (READOUT = 1)



b) Read contents of Register 45h. This register has been initialized with 04h (device is put into global power-down mode.)

Figure 8-18. Serial Readout Timing Diagram

A high pulse on the RESET pin is required in the serial interface mode when initialized through a hardware reset. For parallel interface operation, RESET must be permanently tied high.

Figure 8-19. Reset Timing Diagram

8.5.7 Digital Output Information

The ADS424x/422x provide 14-bit/12-bit digital data for each channel and an output clock synchronized with the data.

8.5.7.1 Output Interface

Two output interface options are available: double data rate (DDR) LVDS and parallel CMOS. They can be selected using the serial interface register bit or by setting the proper voltage on the SEN pin in parallel configuration mode.

8.5.7.2 DDR LVDS Outputs

In this mode, the data bits and clock are output using low-voltage differential signal (LVDS) levels. Two data bits are multiplexed and output on each LVDS differential pair, as shown in [Figure 8-20](#).

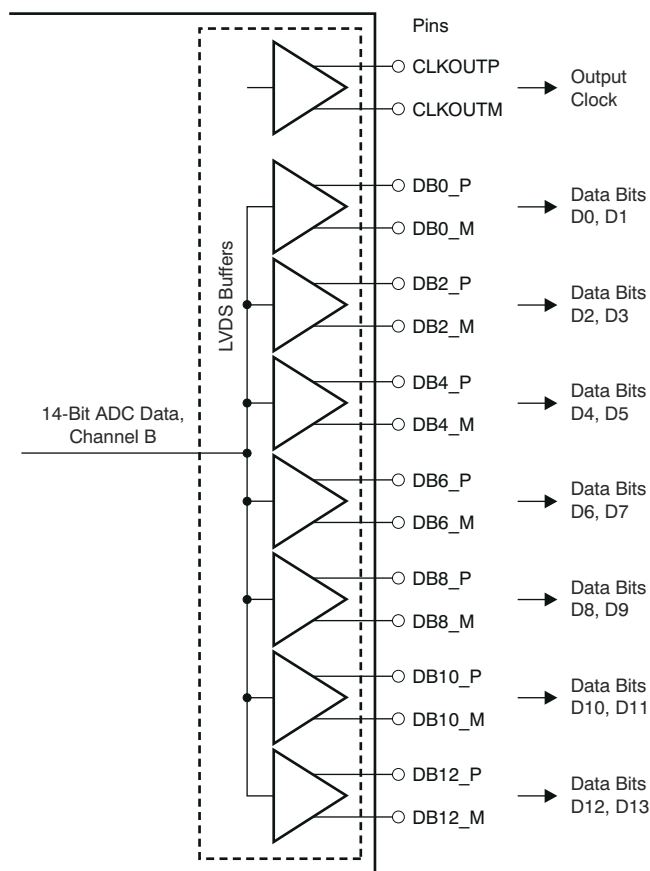


Figure 8-20. LVDS Interface

Even data bits (D0, D2, D4, etc.) are output at the CLKOUTP rising edge and the odd data bits (D1, D3, D5, etc.) are output at the CLKOUTP falling edge. Both the CLKOUTP rising and falling edges must be used to capture all the data bits, as shown in [Figure 8-21](#).

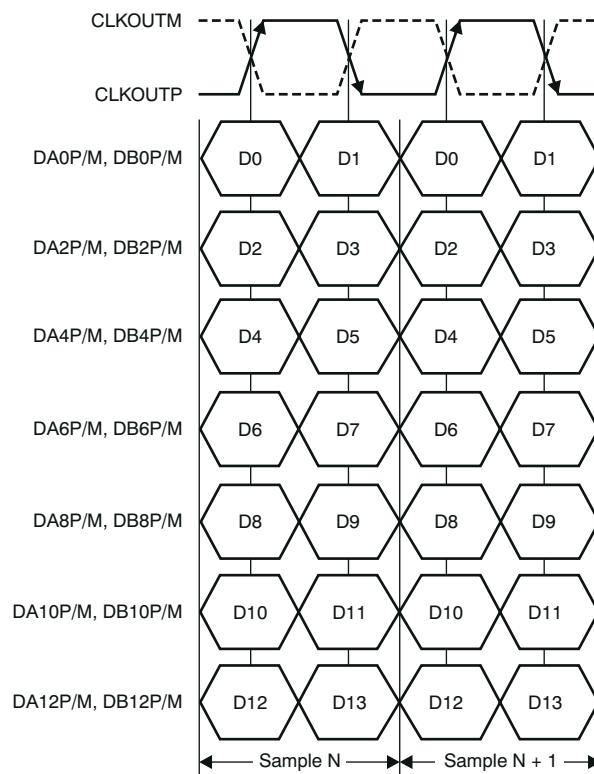
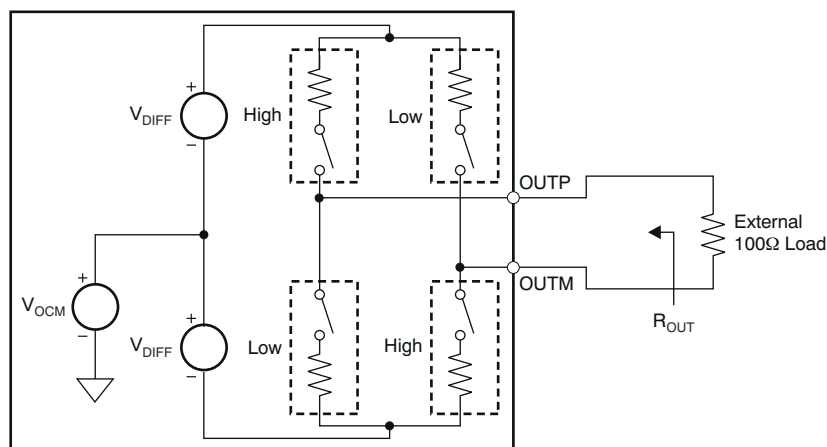


Figure 8-21. DDR LVDS Interface Timing

8.5.7.3 LVDS Buffer

The equivalent circuit of each LVDS output buffer is shown in Figure 8-22. After reset, the buffer presents an output impedance of 100 Ω to match with the external 100- Ω termination.



Default swing across 100- Ω load is ± 350 mV. Use the LVDS SWING bits to change the swing.

Figure 8-22. LVDS Buffer Equivalent Circuit

The V_{DIFF} voltage is nominally 350 mV, resulting in an output swing of ± 350 mV with 100- Ω external termination. The V_{DIFF} voltage is programmable using the LVDS SWING register bits from ± 125 mV to ± 570 mV.

Additionally, a mode exists to double the strength of the LVDS buffer to support 50- Ω differential termination, as shown in Figure 8-23. This mode can be used when the output LVDS signal is routed to two separate receiver chips, each using a 100- Ω termination. The mode can be enabled using the LVDS DATA STRENGTH and LVDS CLKOUT STRENGTH register bits for data and output clock buffers, respectively.

The buffer output impedance behaves in the same way as a source-side series termination. By absorbing reflections from the receiver end, it helps to improve signal integrity.

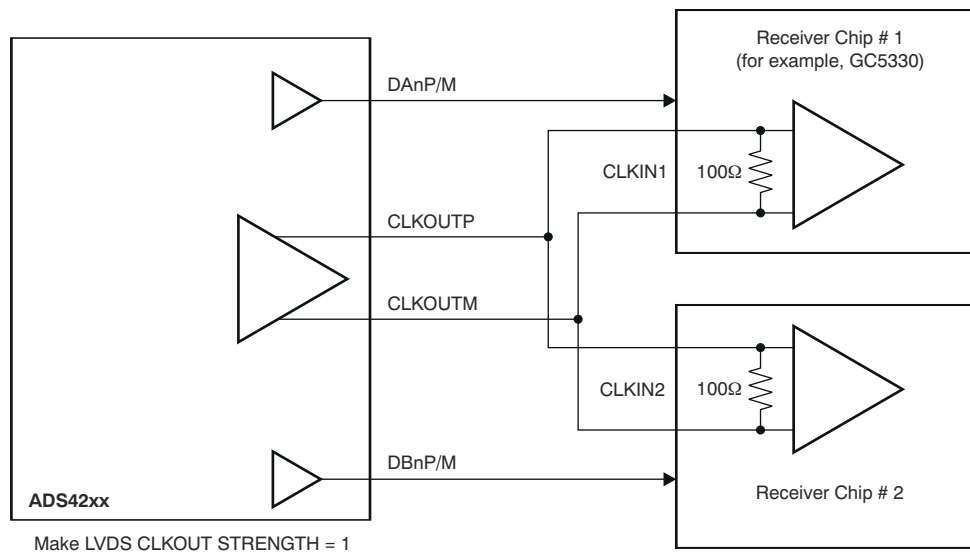


Figure 8-23. LVDS Buffer Differential Termination

8.5.7.4 Parallel CMOS Interface

In the CMOS mode, each data bit is output on separate pins as CMOS voltage level, every clock cycle, as [Figure 8-24](#) shows. The rising edge of the output clock CLKOUT can be used to latch data in the receiver. It is recommended to minimize the load capacitance of the data and clock output pins by using short traces to the receiver. Furthermore, match the output data and clock traces to minimize the skew between them.

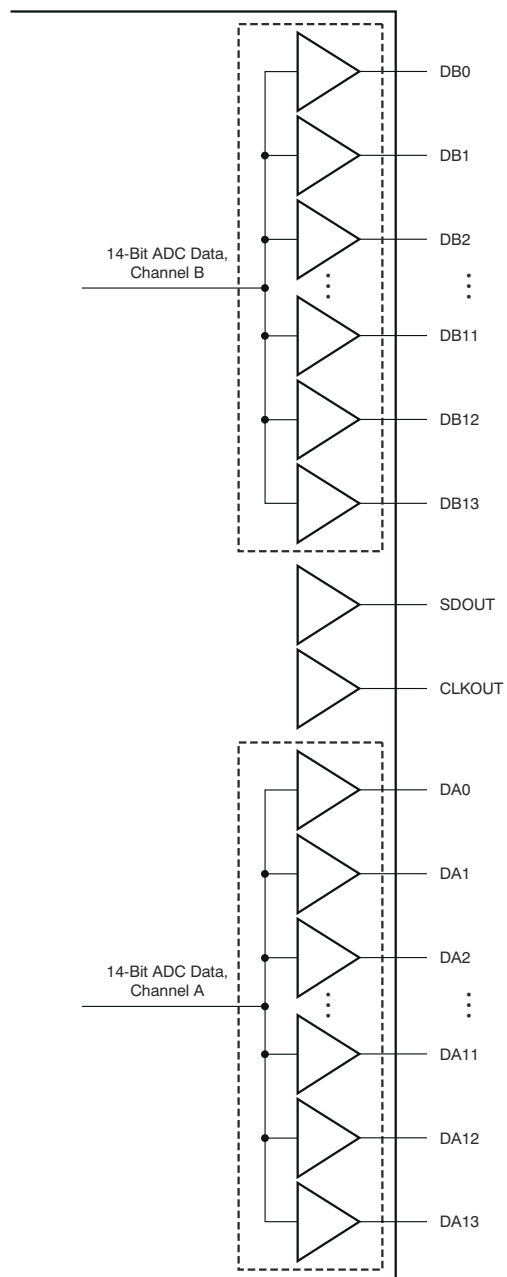


Figure 8-24. CMOS Outputs

8.5.7.5 CMOS Interface Power Dissipation

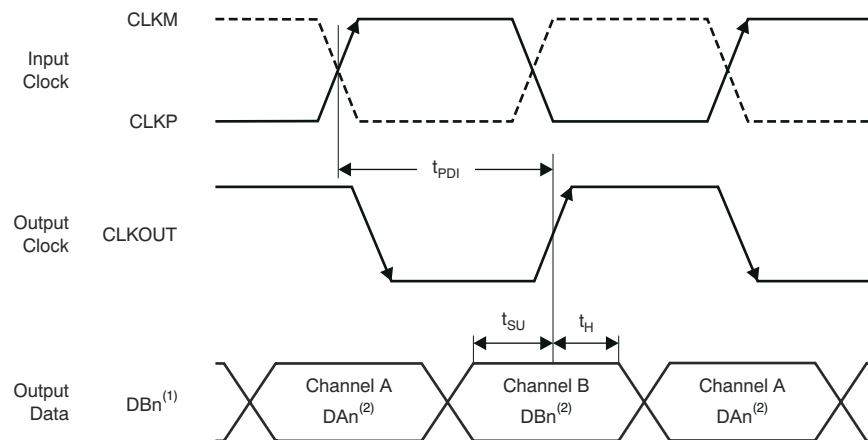
With CMOS outputs, the DRVDD current scales with the sampling frequency and the load capacitance on every output pin. The maximum DRVDD current occurs when each output bit toggles between 0 and 1 every clock cycle. In actual applications, this condition is unlikely to occur. The actual DRVDD current would be determined by the average number of output bits switching, which is a function of the sampling frequency and the nature of the analog input signal. This relationship is shown by the formula:

Digital current as a result of CMOS output switching = $C_L \times \text{DRVDD} \times (N \times F_{\text{AVG}})$,

where C_L = load capacitance, $N \times F_{\text{AVG}}$ = average number of output bits switching.

8.5.7.6 Multiplexed Mode of Operation

In this mode, the digital outputs of both channels are multiplexed and output on a single bus (DB[13:0] pins), as shown in Figure 8-25. The channel A output pins (DA[13:0]) are in 3-state. Because the output data rate on the DB bus is effectively doubled, this mode is recommended only for low sampling frequencies (less than 80MSPS). This mode can be enabled using the POWER-DOWN MODE register bits or using the CTRL[3:1] parallel pins.



- A. In multiplexed mode, both channels outputs come on the channel B output pins.
- B. Dn = bits D0, D1, D2, etc.

Figure 8-25. Multiplexed Mode Timing Diagram

8.5.7.7 Output Data Format

Two output data formats are supported: twos complement and offset binary. The format can be selected using the DATA FORMAT serial interface register bit or by controlling the DFS pin in parallel configuration mode.

In the event of an input voltage overdrive, the digital outputs go to the appropriate full-scale level. For a positive overdrive, the output code is FFFh for the ADS422x and 3FFFh for the ADS424x in offset binary output format; the output code is 7FFh for the ADS422x and 1FFFh for the ADS424x in twos complement output format. For a negative input overdrive, the output code is 0000h in offset binary output format and 800h for the ADS422x and 2000h for the ADS424x in twos complement output format.

8.6 Register Maps

8.6.1

Table 8-9 summarizes the functions supported by the serial interface.

Table 8-9. Serial Interface Register Map⁽¹⁾

| REGISTER ADDRESS | REGISTER DATA | | | | | | | |
|------------------|--------------------------|-------------------------|---------------------------|--|---------------------------------------|--------------------|----------------|---------------------------------------|
| A[7:0] (Hex) | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 00 | 0 | 0 | 0 | 0 | 0 | 0 | RESET | READOUT |
| 01 | LVDS SWING | | | | | | 0 | 0 |
| 03 | 0 | 0 | 0 | 0 | 0 | 0 | HIGH PERF MODE | |
| 25 | CH A GAIN | | | | 0 | CH A TEST PATTERNS | | |
| 29 | 0 | 0 | 0 | DATA FORMAT | | 0 | 0 | 0 |
| 2B | CH B GAIN | | | | 0 | CH B TEST PATTERNS | | |
| 3D | 0 | 0 | ENABLE OFFSET CORR | 0 | 0 | 0 | 0 | 0 |
| 3F | 0 | 0 | CUSTOM PATTERN D[13:8] | | | | | |
| 40 | CUSTOM PATTERN D[7:0] | | | | | | | |
| 41 | LVDS CMOS | | CMOS CLKOUT STRENGTH | | 0 | 0 | DIS OBUF | |
| 42 | CLKOUT FALL POSN | | CLKOUT RISE POSN | | EN DIGITAL | 0 | 0 | 0 |
| 45 | STBY | LVDS CLKOUT STRENGTH | LVDS DATA STRENGTH | 0 | 0 | PDN GLOBAL | 0 | 0 |
| 4A | 0 | 0 | 0 | 0 | 0 | 0 | 0 | HIGH FREQ MODE CH B ⁽³⁾ |
| 58 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | HIGH FREQ MODE CH A ⁽³⁾ |
| BF | CH A OFFSET PEDESTAL | | | | | | 0 | 0 |
| C1 | CH B OFFSET PEDESTAL | | | | | | 0 | 0 |
| CF | FREEZE OFFSET CORR | 0 | OFFSET CORR TIME CONSTANT | | | | 0 | 0 |
| DB | 0 | 0 | 0 | 0 | 0 | 0 | 0 | LOW SPEED MODE CH B ⁽²⁾ |
| EF | 0 | 0 | 0 | EN LOW SPEED MODE ⁽²⁾ | 0 | 0 | 0 | 0 |
| F1 | 0 | 0 | 0 | 0 | 0 | 0 | EN LVDS SWING | |
| F2 | 0 | 0 | 0 | 0 | LOW SPEED MODE CH A ⁽²⁾ | 0 | 0 | 0 |

(1) Multiple functions in a register can be programmed in a single write operation. All registers default to 0 after reset.

(2) Low-speed mode is not applicable for the ADS4242 and ADS4222.

(3) These bits improve SFDR on high frequencies. The frequency limit is 200 MHz.

8.6.2 Description Of Serial Registers

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|-------|---------|
| 0 | 0 | 0 | 0 | 0 | 0 | RESET | READOUT |

Bits[7:2] Always write 0

Bit 1 RESET: Software reset applied

This bit resets all internal registers to the default values and self-clears to 0 (default = 1).

Bit 0 READOUT: Serial readout

This bit sets the serial readout of the registers.

0 = Serial readout of registers disabled; the SDOOUT pin is placed in high-impedance state.

1 = Serial readout enabled; the SDOOUT pin functions as a serial data readout with CMOS logic levels running from the DRVDD supply. See the [Serial Register Readout](#) section.

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------------|---|---|---|---|---|---|---|
| LVDS SWING | | | | | | 0 | 0 |

Bits[7:2] LVDS SWING: LVDS swing programmability

These bits program the LVDS swing. Set the EN LVDS SWING bit to 1 before programming swing.

000000 = Default LVDS swing; ± 350 mV with external 100- Ω termination

011011 = LVDS swing increases to ± 410 mV

110010 = LVDS swing increases to ± 465 mV

010100 = LVDS swing increases to ± 570 mV

111110 = LVDS swing decreases to ± 200 mV

001111 = LVDS swing decreases to ± 125 mV

Bits[1:0] Always write 0

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|----------------|---|
| 0 | 0 | 0 | 0 | 0 | 0 | HIGH PERF MODE | |

Bits[7:2] Always write 0

Bits[1:0] HIGH PERF MODE: High-performance mode

00 = Default performance

01 = Do not use

10 = Do not use

11 = Obtain best performance across sample clock and input signal frequencies

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------|---|---|---|---|--------------------|---|---|
| CH A GAIN | | | | 0 | CH A TEST PATTERNS | | |

Bits[7:4] CH A GAIN: Channel A gain programmability

These bits set the gain programmability in 0.5-dB steps for channel A.

0000 = 0-dB gain (default after reset)
 0001 = 0.5-dB gain
 0010 = 1-dB gain
 0011 = 1.5-dB gain
 0100 = 2-dB gain
 0101 = 2.5-dB gain
 0110 = 3-dB gain
 0111 = 3.5-dB gain
 1000 = 4-dB gain
 1001 = 4.5-dB gain
 1010 = 5-dB gain
 1011 = 5.5-dB gain
 1100 = 6-dB gain

Bit 3 Always write 0**Bits[2:0] CH A TEST PATTERNS: Channel A data capture**

These bits verify data capture for channel A.

000 = Normal operation
 001 = Outputs all 0s
 010 = Outputs all 1s
 011 = Outputs toggle pattern.
 For the ADS424x, output data D[13:0] are an alternating sequence of 10101010101010 and 01010101010101.
 For the ADS422x, the output data D[11:0] are an alternating sequence of 101010101010 and 010101010101.
 100 = Outputs digital ramp.
 For the ADS424x, output data increment by one LSB (14-bit) every clock cycle from code 0 to code 16383.
 For the ADS422x, output data increment by one LSB (12-bit) every fourth clock cycle from code 0 to code 4095.
 101 = Outputs custom pattern; use registers 3Fh and 40h to set the custom pattern
 110 = Unused
 111 = Unused

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|-------------|---|---|---|---|
| 0 | 0 | 0 | DATA FORMAT | | 0 | 0 | 0 |

Bits[7:5] Always write 0**Bits[4:3] DATA FORMAT: Data format selection**

00 = Twos complement
 01 = Twos complement
 10 = Twos complement
 11 = Offset binary

Bits[2:0] Always write 0

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------|---|---|---|---|--------------------|---|---|
| CH B GAIN | | | | 0 | CH B TEST PATTERNS | | |

Bits[7:4] CH B GAIN: Channel B gain programmability

These bits set the gain programmability in 0.5-dB steps for channel B.

0000 = 0-dB gain (default after reset)
 0001 = 0.5-dB gain
 0010 = 1-dB gain
 0011 = 1.5-dB gain
 0100 = 2-dB gain
 0101 = 2.5-dB gain
 0110 = 3-dB gain
 0111 = 3.5-dB gain
 1000 = 4-dB gain
 1001 = 4.5-dB gain
 1010 = 5-dB gain
 1011 = 5.5-dB gain
 1100 = 6-dB gain

Bit 3 Always write 0
Bits[2:0] CH B TEST PATTERNS: Channel B data capture

These bits verify data capture for channel B.

000 = Normal operation
 001 = Outputs all 0s
 010 = Outputs all 1s
 011 = Outputs toggle pattern.
 For the ADS424x, output data D[13:0] are an alternating sequence of *10101010101010* and *01010101010101*.
 For the ADS422x, the output data D[11:0] are an alternating sequence of *101010101010* and *010101010101*.
 100 = Outputs digital ramp.
 For the ADS424x, output data increment by one LSB (14-bit) every clock cycle from code 0 to code 16383.
 For the ADS422x, output data increment by one LSB (12-bit) every fourth clock cycle from code 0 to code 4095.
 101 = Outputs custom pattern; use registers 3Fh and 40h to set the custom pattern
 110 = Unused
 111 = Unused

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|-----------------------|---|---|---|---|---|
| 0 | 0 | ENABLE OFFSET CORR | 0 | 0 | 0 | 0 | 0 |

Bits[7:6] Always write 0

Bit 5 ENABLE OFFSET CORR: Offset correction setting

This bit enables the offset correction.
0 = Offset correction disabled
1 = Offset correction enabled

Bits[4:0] Always write 0

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|-----------------------|-----------------------|-----------------------|-----------------------|----------------------|----------------------|
| 0 | 0 | CUSTOM PATTERN D13 | CUSTOM PATTERN D12 | CUSTOM PATTERN D11 | CUSTOM PATTERN D10 | CUSTOM PATTERN D9 | CUSTOM PATTERN D8 |

Bits[7:6] Always write 0

Bits[5:0] CUSTOM PATTERN D[13:8]

These are the six upper bits of the custom pattern available at the output instead of ADC data.
Note that for the ADS424x, the custom pattern is 14-bit. The ADS422x custom pattern is 12-bit.

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----------------------|----------------------|----------------------|----------------------|----------------------|----------------------|----------------------|----------------------|
| CUSTOM PATTERN D7 | CUSTOM PATTERN D6 | CUSTOM PATTERN D5 | CUSTOM PATTERN D4 | CUSTOM PATTERN D3 | CUSTOM PATTERN D2 | CUSTOM PATTERN D1 | CUSTOM PATTERN D0 |

Bits[7:0] CUSTOM PATTERN D[7:0]

These are the eight upper bits of the custom pattern available at the output instead of ADC data.
Note that for the ADS424x, the custom pattern is 14-bit. The ADS422x custom pattern is 12-bit; use the CUSTOM PATTERN D[13:2] register bits.

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------|---|----------------------|---|---|---|----------|---|
| LVDS CMOS | | CMOS CLKOUT STRENGTH | | 0 | 0 | DIS OBUF | |

Bits[7:6] LVDS CMOS: Interface selection

These bits select the interface.

00 = DDR LVDS interface

01 = DDR LVDS interface

10 = DDR LVDS interface

11 = Parallel CMOS interface

Bits[5:4] CMOS CLKOUT STRENGTH

These bits control the strength of the CMOS output clock.

00 = Maximum strength (recommended)

01 = Medium strength

10 = Low strength

11 = Very low strength

Bits[3:2] Always write 0

Bits[1:0] DIS OBUF

These bits power down data and clock output buffers for both the CMOS and LVDS output interface. When powered down, the output buffers are in 3-state.

00 = Default

01 = Power-down data output buffers for channel B

10 = Power-down data output buffers for channel A

11 = Power-down data output buffers for both channels as well as the clock output buffer

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------------------|------------------|---|------------|---|---|---|---|
| CLKOUT FALL POSN | CLKOUT RISE POSN | | EN DIGITAL | 0 | 0 | 0 | 0 |

Bits[7:6] CLKOUT FALL POSN

In LVDS mode:
 00 = Default
 01 = The falling edge of the output clock advances by 450 ps
 10 = The falling edge of the output clock advances by 150 ps
 11 = The falling edge of the output clock is delayed by 550 ps
 In CMOS mode:
 00 = Default
 01 = The falling edge of the output clock is delayed by 150 ps
 10 = Do not use
 11 = The falling edge of the output clock advances by 100 ps

Bits[5:6] CLKOUT RISE POSN

In LVDS mode:
 00 = Default
 01 = The rising edge of the output clock advances by 450 ps
 10 = The rising edge of the output clock advances by 150 ps
 11 = The rising edge of the output clock is delayed by 250 ps
 In CMOS mode:
 00 = Default
 01 = The rising edge of the output clock is delayed by 150 ps
 10 = Do not use
 11 = The rising edge of the output clock advances by 100 ps

Bit 3 EN DIGITAL: Digital function enable

0 = All digital functions disabled
 1 = All digital functions (such as test patterns, gain, and offset correction) enabled

Bits[2:0] Always write 0

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|----------------------|--------------------|---|---|------------|---|---|
| STBY | LVDS CLKOUT STRENGTH | LVDS DATA STRENGTH | 0 | 0 | PDN GLOBAL | 0 | 0 |

Bit 7 STBY: Standby setting

0 = Normal operation

1 = Both channels are put in standby; wakeup time from this mode is fast (typically 50 μ s).

Bit 6 LVDS CLKOUT STRENGTH: LVDS output clock buffer strength setting

0 = LVDS output clock buffer at default strength to be used with 100- Ω external termination

1 = LVDS output clock buffer has double strength to be used with 50- Ω external termination

Bit 5 LVDS DATA STRENGTH

0 = All LVDS data buffers at default strength to be used with 100- Ω external termination

1 = All LVDS data buffers have double strength to be used with 50- Ω external termination

Bits[4:3] Always write 0

Bit 2 PDN GLOBAL

0 = Normal operation

1 = Total power down; all ADC channels, internal references, and output buffers are powered down. Wakeup time from this mode is slow (typically 100 μ s).

Bits[1:0] Always write 0

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---------------------|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | HIGH FREQ MODE CH B |

Bits[7:1] Always write 0

Bit 0 HIGH FREQ MODE CH B: High-frequency mode for channel B

0 = Default

1 = Use this mode for high input frequencies

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---------------------|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | HIGH FREQ MODE CH A |

Bits[7:1] Always write 0

Bit 0 HIGH FREQ MODE CH A: High-frequency mode for channel A

0 = Default

1 = Use this mode for high input frequencies

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----------------------|---|---|---|---|---|---|---|
| CH A OFFSET PEDESTAL | | | | | | 0 | 0 |

Bits[7:2] CH A OFFSET PEDESTAL: Channel A offset pedestal selection

When the offset correction is enabled, the final converged value after the offset is corrected is the ADC midcode value. A pedestal can be added to the final converged value by programming these bits. See the [Offset Correction](#) section. Channels can be independently programmed for different offset pedestals by choosing the relevant register address.

For the ADS424x, the pedestal ranges from –32 to +31, so the output code can vary from midcode-32 to midcode+32 by adding pedestal D7-D2.

For the ADS422x, the pedestal ranges from –8 to +7, so the output code can vary from midcode-8 to midcode+7 by adding pedestal D7-D4.

| ADS422x (Program Bits D[7:4]) | ADS424x (Program Bits D[7:2]) |
|-------------------------------|-------------------------------|
| 0111 = Midcode+7 | 011111 = Midcode+31 |
| 0110 = Midcode+6 | 011110 = Midcode+30 |
| 0101 = Midcode+5 | 011101 = Midcode+29 |
| ... | ... |
| 0000 = Midcode | 000000 = Midcode |
| 1111 = Midcode-1 | 111111 = Midcode-1 |
| 1110 = Midcode-2 | 111110 = Midcode-2 |
| 1101 = Midcode-3 | 111101 = Midcode-3 |
| ... | ... |
| 1000 = Midcode-8 | 100000 = Midcode-32 |

Bits[1:0] Always write 0

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----------------------|---|---|---|---|---|---|---|
| CH B OFFSET PEDESTAL | | | | | | 0 | 0 |

Bits[7:2] CH B OFFSET PEDESTAL: Channel B offset pedestal selection

When offset correction is enabled, the final converged value after the offset is corrected is the ADC midcode value. A pedestal can be added to the final converged value by programming these bits; see the [Offset Correction](#) section. Channels can be independently programmed for different offset pedestals by choosing the relevant register address.

For the ADS424x, the pedestal ranges from –32 to +31, so the output code can vary from midcode-32 to midcode+32 by adding pedestal D[7:2]. For the ADS422x, the pedestal ranges from –8 to +7, so the output code can vary from midcode-8 to midcode+7 by adding pedestal D[7:4].

| ADS422x (Program Bits D[7:4]) | ADS424x (Program Bits D[7:2]) |
|-------------------------------|-------------------------------|
| 0111 = Midcode+7 | 011111 = Midcode+31 |
| 0110 = Midcode+6 | 011110 = Midcode+30 |
| 0101 = Midcode+5 | 011101 = Midcode+29 |
| ... | ... |
| 0000 = Midcode | 000000 = Midcode |
| 1111 = Midcode-1 | 111111 = Midcode-1 |
| 1110 = Midcode-2 | 111110 = Midcode-2 |
| 1101 = Midcode-3 | 111101 = Midcode-3 |
| ... | ... |
| 1000 = Midcode-8 | 100000 = Midcode-32 |

Bits[1:0] Always write 0

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------------|---|---------------------------|---|---|---|---|---|
| FREEZE OFFSET CORR | 0 | OFFSET CORR TIME CONSTANT | | | | 0 | 0 |

Bit 7 **FREEZE OFFSET CORR: Freeze offset correction setting**

This bit sets the freeze offset correction estimation.

0 = Estimation of offset correction is not frozen (the EN OFFSET CORR bit must be set)

1 = Estimation of offset correction is frozen (the EN OFFSET CORR bit must be set); when frozen, the last estimated value is used for offset correction of every clock cycle. See the [Offset Correction](#) section.

Bit 6 **Always write 0****Bits[5:2]** **OFFSET CORR TIME CONSTANT**

The offset correction loop time constant in number of clock cycles. Refer to the [Offset Correction](#) section.

Bits[1:0] **Always write 0**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|------------------------|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | LOW SPEED MODE CH B |

Bits[7:1] **Always write 0****Bit 0** **LOW SPEED MODE CH B: Channel B low-speed mode enable**

This bit enables the low-speed mode for channel B. Set the EN LOW SPEED MODE bit to 1 before using this bit.

0 = Low-speed mode is disabled for channel B

1 = Low-speed mode is enabled for channel B

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|----------------------|---|---|---|---|
| 0 | 0 | 0 | EN LOW SPEED MODE | 0 | 0 | 0 | 0 |

Bits[7:5] **Always write 0****Bit 4** **EN LOW SPEED MODE: Enable control of low-speed mode through serial register bits (ADS42x5 and ADS42x6 only)**

This bit enables the control of the low-speed mode using the LOW SPEED MODE CH B and LOW SPEED MODE CH A register bits.

0 = Low-speed mode is disabled

1 = Low-speed mode is controlled by serial register bits

Bits[3:0] **Always write 0**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---------------|---|
| 0 | 0 | 0 | 0 | 0 | 0 | EN LVDS SWING | |

Bits[7:2] Always write 0

Bits[1:0] EN LVDS SWING: LVDS swing enable

These bits enable LVDS swing control using the LVDS SWING register bits.
 00 = LVDS swing control using the LVDS SWING register bits is disabled
 01 = Do not use
 10 = Do not use
 11 = LVDS swing control using the LVDS SWING register bits is enabled

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|------------------------|---|---|---|
| 0 | 0 | 0 | 0 | LOW SPEED MODE CH A | 0 | 0 | 0 |

Bits[7:4] Always write 0

Bit 3 LOW SPEED MODE CH A: Channel A low-speed mode enable

This bit enables the low-speed mode for channel A. Set the EN LOW SPEED MODE bit to 1 before using this bit.
 0 = Low-speed mode is disabled for channel A
 1 = Low-speed mode is enabled for channel A

Bits[2:0] Always write 0

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The ADS424x/422x belong to TI's ultralow-power family of dual-channel 12-bit and 14-bit analog-to-digital converters (ADCs). At every rising edge of the input clock, the analog input signal of each channel is simultaneously sampled. The sampled signal in each channel is converted by a pipeline of low-resolution stages. In each stage, the sampled/held signal is converted by a high-speed, low-resolution, flash sub-ADC. The difference between the stage input and the quantized equivalent is gained and propagates to the next stage. At every clock, each succeeding stage resolves the sampled input with greater accuracy. The digital outputs from all stages are combined in a digital correction logic block and digitally processed to create the final code after a data latency of 16 clock cycles. The digital output is available as either DDR LVDS or parallel CMOS and coded in either straight offset binary or binary twos complement format. The dynamic offset of the first stage sub-ADC limits the maximum analog input frequency to approximately 400 MHz (with 2- V_{PP} amplitude) or approximately 600 MHz (with 1 V_{PP} amplitude).

9.2 Typical Application

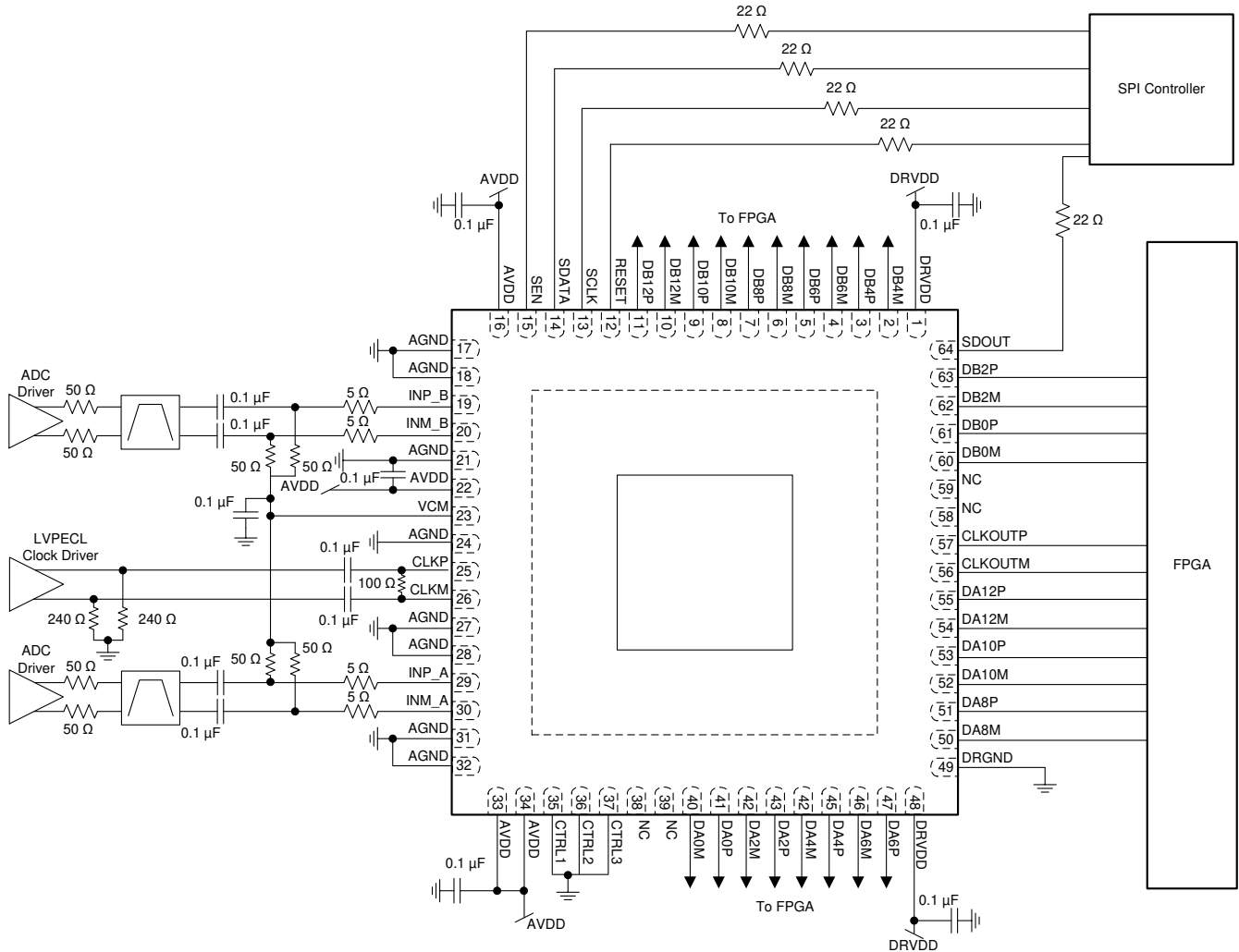


Figure 9-1. Example Schematic for ADS4246

9.2.1 Design Requirements

Example design requirements are listed in [Table 9-1](#) for the ADC portion of the signal chain. These do not necessarily reflect the requirements of an actual system, but rather demonstrate why the ADS4246 may be chosen for a system based on a set of requirements.

Table 9-1. Example Design Requirements for ADS4246

| Design Parameter | Example Design Requirement | ADS4246 CAPABILITY |
|--------------------------|---|---|
| Sampling rate | ≥ 122.88 Msps to allow 80 MHz of unaliased bandwidth | Max sampling rate: 160 Msps |
| Input frequency | > 125 MHz to accommodate full 2nd nyquist zone | Large signal -3 dB bandwidth: 400-MHz operation |
| SNR | > 68 dBFS at -1 dBFS, 170 MHz | 70.4 dBFS at -1 dBFS, 170 MHz |
| SDFR | > 77 dBc at -1 dBFS, 170 MHz | 82 dBc at -1 dBFS, 170 MHz |
| Input full scale voltage | 2 Vpp | 2 Vpp |
| Overload recovery time | < 3 clock cycles | 1 clock cycle |
| Digital interface | DDR LVDS | DDR LVDS |
| Power consumption | < 200 mW per channel | 166 mW per channel |

9.2.2 Detailed Design Procedure

9.2.2.1 Analog Input

The analog input of the ADS42xx is typically driven by a fully differential amplifier. The amplifier must have sufficient bandwidth for the frequencies of interest. The noise and distortion performance of the amplifier will affect the combined performance of the ADC and amplifier. The amplifier is often AC coupled to the ADC to allow both the amplifier and ADC to operate at the optimal common mode voltages. It is possible to DC couple the amplifier to the ADC if required. An alternate approach is to drive the ADC using transformers. DC coupling cannot be used with the transformer approach.

9.2.2.2 Clock Driver

The ADS42xx should be driven by a high performance clock driver such as a clock jitter cleaner. The clock needs to have low noise to maintain optimal performance. LVPECL is the most common clocking interface, but LVDS and LVCMOS can be used as well. It is not advised to drive the clock input from an FPGA unless the noise degradation can be tolerated, such as for input signals near DC where the clock noise impact is minimal.

9.2.2.3 Digital Interface

The ADS42xx supports both LVDS and CMOS interfaces. The LVDS interface should be used for best performance when operating at maximum sampling rate. The LVDS outputs can be connected directly to the FPGA without any additional components. When using CMOS outputs resistors should be placed in series with the outputs to reduce the output current spikes to limit the performance degradation. The resistors should be large enough to limit current spikes but not so large as to significantly distort the digital output waveform. An external CMOS buffer should be used when driving distances greater than a few inches to reduce ground bounce within the ADC.

9.2.2.4 SNR and Clock Jitter

The signal-to-noise ratio (SNR) of the ADC is limited by three different factors, as shown in [Equation 1](#). Quantization noise is typically not noticeable in pipeline converters and is 96 dBFS for a 16-bit ADC. Thermal noise limits SNR at low input frequencies and clock jitter sets SNR for higher input frequencies.

$$\text{SNR}_{\text{ADC}}[\text{dBc}] = -20 \times \log \sqrt{\left(10 - \frac{\text{SNR}_{\text{Quantization_Noise}}}{20}\right)^2 + \left(10 - \frac{\text{SNR}_{\text{ThermalNoise}}}{20}\right)^2 + \left(10 - \frac{\text{SNR}_{\text{Jitter}}}{20}\right)^2} \quad (1)$$

SNR limitation is a result of sample clock jitter and can be calculated by [Equation 2](#)

$$\text{SNR}_{\text{Jitter}}[\text{dBc}] = -20 \times \log(2\pi \times f_{\text{IN}} \times t_{\text{Jitter}}) \quad (2)$$

The total clock jitter (T_{Jitter}) has three components: the internal aperture jitter ($85 f_s$ for the device) is set by the noise of the clock input buffer, the external clock jitter, and the jitter from the analog input signal. T_{Jitter} can be calculated by [Equation 3](#):

$$T_{\text{Jitter}} = \sqrt{(T_{\text{Jitter,Ext.Clock_Input}})^2 + (T_{\text{Aperture_ADC}})^2} \quad (3)$$

External clock jitter can be minimized by using high-quality clock sources and jitter cleaners as well as band-pass filters at the clock input while a faster clock slew rate improved ADC aperture jitter. The device has a 74.1-dBFS thermal noise and an $85 f_s$ internal aperture jitter. The SNR value depends on the amount of external jitter for different input frequencies, as shown in Figure.

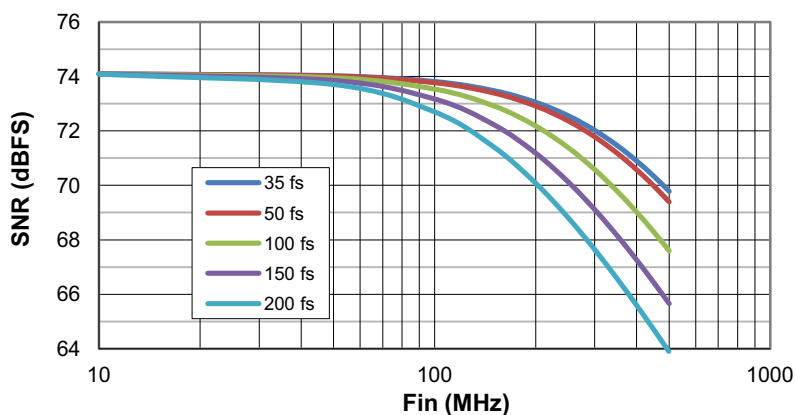


Figure 9-2. SNR versus Input Frequency and External Clock Jitter

9.2.3 Application Curves

Figure 9-3 and Figure 9-4 show performance obtained at 100-MHz and 270-MHz input frequencies, respectively, using the appropriate driving circuit.

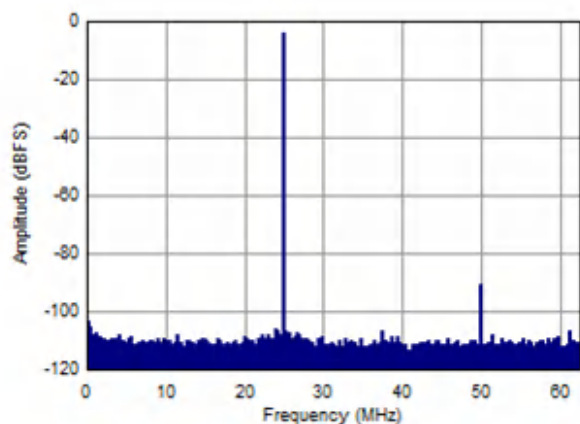


Figure 9-3. FFT for 100-MHz Input Signal

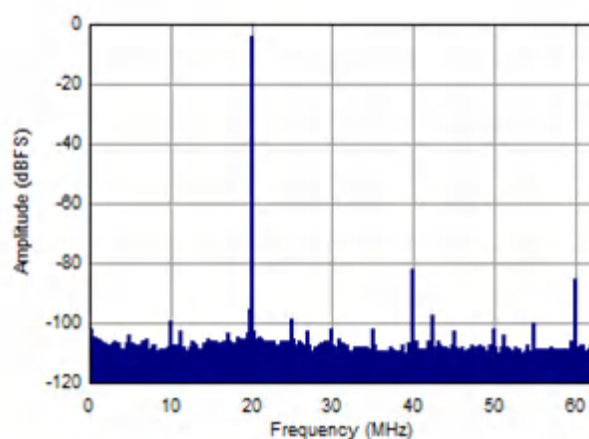


Figure 9-4. FFT for 270-MHz Input Signal

9.3 Power Supply Recommendations

The ADS42xx has two power supplies, one analog (AVDD) and one digital (DRVDD) supply. Both supplies have a nominal voltage of 1.8 V. The AVDD supply is noise sensitive and the digital supply is not.

9.3.1 Sharing DRVDD and AVDD Supplies

For best performance, the AVDD supply should be driven by a low noise linear regulator (LDO) and separated from the DRVDD supply. It is possible to have AVDD and DRVDD share a single supply, but they should be isolated by a ferrite bead and bypass capacitors in a PI-filter configuration, at a minimum. The digital noise will be concentrated at the sampling frequency and harmonics of the sampling frequency and could contain noise related to the sampled signal. While developing schematics, it is a good idea to leave extra placeholders for additional supply filtering.

9.3.2 Using DC/DC Power Supplies

DC/DC switching power supplies can be used to power DRVDD without issue. It is also possible to power AVDD from a switching regulator. Noise and spurs on the AVDD power supply will affect the SNR and SFDR of the ADC and will show up near DS and as a modulated component around the input frequency. If a switching regulator is used, then it should be designed to have minimal voltage ripple. Supply filtering should be used to limit the amount of spurious noise at the AVDD supply pins. Extra placeholders should be placed on the schematic for additional filtering. Optimization of filtering in the final system will likely be needed to achieve the desired performance. The choice of power supply ultimately depends on the system requirements. For instance, if very low phase noise is required then use of a switching regulator is not recommended.

9.3.3 Power Supply Bypassing

Because the ADS42xx already includes internal decoupling, minimal external decoupling can be used without loss in performance. Note that decoupling capacitors can help filter external power-supply noise. Thus, the optimum number of capacitors depends on the actual application. A 0.1- μ F capacitor is recommended near each supply pin. The decoupling capacitors should be placed very close to the converter supply pins.

9.4 Layout

9.4.1 Layout Guidelines

9.4.1.1 Grounding

A single ground plane is sufficient to give good performance, provided the analog, digital, and clock sections of the board are cleanly partitioned. See the [ADS4226 Evaluation Module \(SLAU333\)](#) for details on layout and grounding.

9.4.1.2 Supply Decoupling

Because the ADS424x/422x already includes internal decoupling, minimal external decoupling can be used without loss in performance. Note that decoupling capacitors can help filter external power-supply noise; thus, the optimum number of capacitors depends on the actual application. The decoupling capacitors should be placed very close to the converter supply pins.

9.4.1.3 Exposed Pad

In addition to providing a path for heat dissipation, the PowerPAD is also electrically connected internally to the digital ground. Therefore, it is necessary to solder the exposed pad to the ground plane for best thermal and electrical performance. For detailed information, see application notes [QFN Layout Guidelines \(SLOA122\)](#) and [QFN/SON PCB Attachment \(SLUA271\)](#), both available for download at www.ti.com.

9.4.1.4 Routing Analog Inputs

It is advisable to route differential analog input pairs (INP_x and INM_x) close to each other. To minimize the possibility of coupling from a channel analog input to the sampling clock, the analog input pairs of both channels should be routed perpendicular to the sampling clock. See the [ADS4226 Evaluation Module \(SLAU333\)](#) for reference routing. [Figure 9-5](#) shows a snapshot of the PCB layout from the ADS424x EVM.

9.4.2 Layout Example

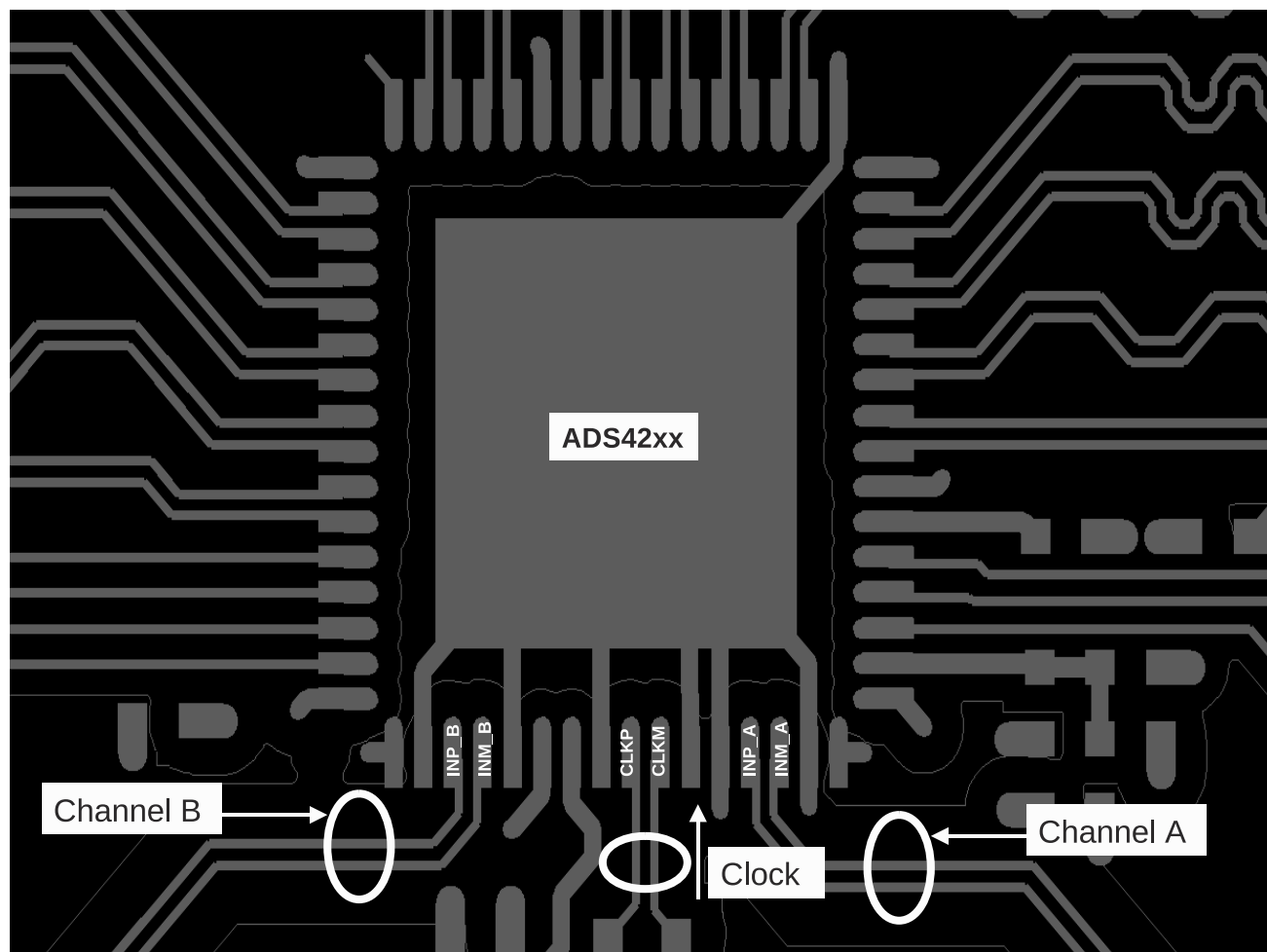


Figure 9-5. ADS42xx EVM PCB Layout

10 Device and Documentation Support

10.1 Device Support

10.1.1 Device Nomenclature

Analog Bandwidth – The analog input frequency at which the power of the fundamental is reduced by 3 dB with respect to the low-frequency value.

Aperture Delay – The delay in time between the rising edge of the input sampling clock and the actual time at which the sampling occurs. This delay is different across channels. The maximum variation is specified as aperture delay variation (channel-to-channel).

Aperture Uncertainty (Jitter) – The sample-to-sample variation in aperture delay.

Clock Pulse Width/Duty Cycle – The duty cycle of a clock signal is the ratio of the time the clock signal remains at a logic high (clock pulse width) to the period of the clock signal. Duty cycle is typically expressed as a percentage. A perfect differential sine-wave clock results in a 50% duty cycle.

Maximum Conversion Rate – The maximum sampling rate at which specified operation is given. All parametric testing is performed at this sampling rate unless otherwise noted.

Minimum Conversion Rate – The minimum sampling rate at which the ADC functions.

Differential Nonlinearity (DNL) – An ideal ADC exhibits code transitions at analog input values spaced exactly 1LSB apart. The DNL is the deviation of any single step from this ideal value, measured in units of LSBs.

Integral Nonlinearity (INL) – The INL is the deviation of the ADC transfer function from a best fit line determined by a least squares curve fit of that transfer function, measured in units of LSBs.

Gain Error – Gain error is the deviation of the ADC actual input full-scale range from its ideal value. The gain error is given as a percentage of the ideal input full-scale range. Gain error has two components: error as a result of reference inaccuracy (E_{GREF}) and error as a result of the channel (E_{GCHAN}). Both errors are specified independently as E_{GREF} and E_{GCHAN} .

To a first-order approximation, the total gain error is $E_{TOTAL} \sim E_{GREF} + E_{GCHAN}$.

For example, if $E_{TOTAL} = \pm 0.5\%$, the full-scale input varies from $(1 - 0.5/100) \times FS_{ideal}$ to $(1 + 0.5/100) \times FS_{ideal}$.

Offset Error – The offset error is the difference, given in number of LSBs, between the ADC actual average idle channel output code and the ideal average idle channel output code. This quantity is often mapped into millivolts.

Temperature Drift – The temperature drift coefficient (with respect to gain error and offset error) specifies the change per degree Celsius of the parameter from T_{MIN} to T_{MAX} . It is calculated by dividing the maximum deviation of the parameter across the T_{MIN} to T_{MAX} range by the difference $T_{MAX} - T_{MIN}$.

Signal-to-Noise Ratio – SNR is the ratio of the power of the fundamental (P_S) to the noise floor power (P_N), excluding the power at dc and the first nine harmonics.

$$SNR = 10 \log_{10} \frac{P_S}{P_N} \quad (4)$$

SNR is either given in units of dBc (dB to carrier) when the absolute power of the fundamental is used as the reference, or dBFS (dB to full-scale) when the power of the fundamental is extrapolated to the converter full-scale range.

Signal-to-Noise and Distortion (SINAD) – SINAD is the ratio of the power of the fundamental (P_S) to the power of all the other spectral components including noise (P_N) and distortion (P_D), but excluding dc.

$$SINAD = 10 \log_{10} \frac{P_S}{P_N + P_D} \quad (5)$$

SINAD is either given in units of dBc (dB to carrier) when the absolute power of the fundamental is used as the reference, or dBFS (dB to full-scale) when the power of the fundamental is extrapolated to the converter full-scale range.

Effective Number of Bits (ENOB) – ENOB is a measure of the converter performance as compared to the theoretical limit based on quantization noise.

$$\text{ENOB} = \frac{\text{SINAD} - 1.76}{6.02} \quad (6)$$

Total Harmonic Distortion (THD) – THD is the ratio of the power of the fundamental (P_S) to the power of the first nine harmonics (P_D).

$$\text{THD} = 10 \log_{10} \frac{P_S}{P_N} \quad (7)$$

THD is typically given in units of dBc (dB to carrier).

Spurious-Free Dynamic Range (SFDR) – The ratio of the power of the fundamental to the highest other spectral component (either spur or harmonic). SFDR is typically given in units of dBc (dB to carrier).

Two-Tone Intermodulation Distortion – IMD3 is the ratio of the power of the fundamental (at frequencies f_1 and f_2) to the power of the worst spectral component at either frequency $2f_1 - f_2$ or $2f_2 - f_1$. IMD3 is either given in units of dBc (dB to carrier) when the absolute power of the fundamental is used as the reference, or dBFS (dB to full-scale) when the power of the fundamental is extrapolated to the converter full-scale range.

DC Power-Supply Rejection Ratio (DC PSRR) – DC PSRR is the ratio of the change in offset error to a change in analog supply voltage. The dc PSRR is typically given in units of mV/V.

AC Power-Supply Rejection Ratio (AC PSRR) – AC PSRR is the measure of rejection of variations in the supply voltage by the ADC. If ΔV_{SUP} is the change in supply voltage and ΔV_{OUT} is the resultant change of the ADC output code (referred to the input), then:

$$\text{PSRR} = 20 \log_{10} \frac{\Delta V_{\text{OUT}}}{\Delta V_{\text{SUP}}} \quad (\text{Expressed in dBc}) \quad (8)$$

Voltage Overload Recovery – The number of clock cycles taken to recover to less than 1% error after an overload on the analog inputs. This is tested by separately applying a sine wave signal with 6 dB positive and negative overload. The deviation of the first few samples after the overload (from the expected values) is noted.

Common-Mode Rejection Ratio (CMRR) – CMRR is the measure of rejection of variation in the analog input common-mode by the ADC. If $\Delta V_{\text{CM_IN}}$ is the change in the common-mode voltage of the input pins and ΔV_{OUT} is the resulting change of the ADC output code (referred to the input), then:

$$\text{CMRR} = 20 \log_{10} \frac{\Delta V_{\text{OUT}}}{\Delta V_{\text{CM}}} \quad (\text{Expressed in dBc}) \quad (9)$$

Crosstalk (only for multi-channel ADCs) – This is a measure of the internal coupling of a signal from an adjacent channel into the channel of interest. It is specified separately for coupling from the immediate neighboring channel (near-channel) and for coupling from channel across the package (far-channel). It is usually measured by applying a full-scale signal in the adjacent channel. Crosstalk is the ratio of the power of the coupling signal (as measured at the output of the channel of interest) to the power of the signal applied at the adjacent channel input. It is typically expressed in dBc.

10.2 Documentation Support

10.2.1 Related Documentation

For related documentation, see the following:

- QFN Layout Guidelines ([SLOA122](#))
- QFN/SON PCB Attachment ([SLUA271](#))
- ADS42xx Evaluation Module ([SLAU333A](#))

10.3 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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10.4 Trademarks

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10.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.6 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package Pins | Package qty Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|------------------------------|---------------|----------------------|-----------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------|
| ADS4222IRGCR | Active | Production | VQFN (RGC) 64 | 2000 LARGE T&R | Yes | NIPDAUAG | Level-3-260C-168 HR | -40 to 85 | AZ4222 |
| ADS4222IRGCR.A | Active | Production | VQFN (RGC) 64 | 2000 LARGE T&R | Yes | NIPDAUAG | Level-3-260C-168 HR | -40 to 85 | AZ4222 |
| ADS4222IRGCT | Active | Production | VQFN (RGC) 64 | 250 SMALL T&R | Yes | NIPDAUAG | Level-3-260C-168 HR | -40 to 85 | AZ4222 |
| ADS4222IRGCT.A | Active | Production | VQFN (RGC) 64 | 250 SMALL T&R | Yes | NIPDAUAG | Level-3-260C-168 HR | -40 to 85 | AZ4222 |
| ADS4225IRGCR | Active | Production | VQFN (RGC) 64 | 2000 LARGE T&R | Yes | NIPDAUAG | Level-3-260C-168 HR | -40 to 85 | AZ4225 |
| ADS4225IRGCR.A | Active | Production | VQFN (RGC) 64 | 2000 LARGE T&R | Yes | NIPDAUAG | Level-3-260C-168 HR | -40 to 85 | AZ4225 |
| ADS4225IRGCT | Active | Production | VQFN (RGC) 64 | 250 SMALL T&R | Yes | NIPDAUAG | Level-3-260C-168 HR | -40 to 85 | AZ4225 |
| ADS4225IRGCT.A | Active | Production | VQFN (RGC) 64 | 250 SMALL T&R | Yes | NIPDAUAG | Level-3-260C-168 HR | -40 to 85 | AZ4225 |
| ADS4226IRGCR | Active | Production | VQFN (RGC) 64 | 2000 LARGE T&R | Yes | NIPDAUAG | Level-3-260C-168 HR | -40 to 85 | AZ4226 |
| ADS4226IRGCR.A | Active | Production | VQFN (RGC) 64 | 2000 LARGE T&R | Yes | NIPDAUAG | Level-3-260C-168 HR | -40 to 85 | AZ4226 |
| ADS4226IRGCT | Active | Production | VQFN (RGC) 64 | 250 SMALL T&R | Yes | NIPDAUAG | Level-3-260C-168 HR | -40 to 85 | AZ4226 |
| ADS4226IRGCT.A | Active | Production | VQFN (RGC) 64 | 250 SMALL T&R | Yes | NIPDAUAG | Level-3-260C-168 HR | -40 to 85 | AZ4226 |
| ADS4242IRGCR | Active | Production | VQFN (RGC) 64 | 2000 LARGE T&R | Yes | NIPDAUAG | Level-3-260C-168 HR | -40 to 85 | AZ4242 |
| ADS4242IRGCR.A | Active | Production | VQFN (RGC) 64 | 2000 LARGE T&R | Yes | NIPDAUAG | Level-3-260C-168 HR | -40 to 85 | AZ4242 |
| ADS4242IRGCT | Active | Production | VQFN (RGC) 64 | 250 SMALL T&R | Yes | NIPDAUAG | Level-3-260C-168 HR | -40 to 85 | AZ4242 |
| ADS4242IRGCT.A | Active | Production | VQFN (RGC) 64 | 250 SMALL T&R | Yes | NIPDAUAG | Level-3-260C-168 HR | -40 to 85 | AZ4242 |
| ADS4245IRGCR | Active | Production | VQFN (RGC) 64 | 2000 LARGE T&R | Yes | NIPDAUAG | Level-3-260C-168 HR | -40 to 85 | AZ4245 |
| ADS4245IRGCR.A | Active | Production | VQFN (RGC) 64 | 2000 LARGE T&R | Yes | NIPDAUAG | Level-3-260C-168 HR | -40 to 85 | AZ4245 |
| ADS4245IRGCT | Active | Production | VQFN (RGC) 64 | 250 SMALL T&R | Yes | NIPDAUAG | Level-3-260C-168 HR | -40 to 85 | AZ4245 |
| ADS4245IRGCT.A | Active | Production | VQFN (RGC) 64 | 250 SMALL T&R | Yes | NIPDAUAG | Level-3-260C-168 HR | -40 to 85 | AZ4245 |
| ADS4246IRGCR | Active | Production | VQFN (RGC) 64 | 2000 LARGE T&R | Yes | NIPDAUAG | Level-3-260C-168 HR | -40 to 85 | AZ4246 |
| ADS4246IRGCR.A | Active | Production | VQFN (RGC) 64 | 2000 LARGE T&R | Yes | NIPDAUAG | Level-3-260C-168 HR | -40 to 85 | AZ4246 |
| ADS4246IRGCT | Active | Production | VQFN (RGC) 64 | 250 SMALL T&R | Yes | NIPDAUAG | Level-3-260C-168 HR | -40 to 85 | AZ4246 |
| ADS4246IRGCT.A | Active | Production | VQFN (RGC) 64 | 250 SMALL T&R | Yes | NIPDAUAG | Level-3-260C-168 HR | -40 to 85 | AZ4246 |

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF ADS4245 :

- Enhanced Product : [ADS4245-EP](#)

NOTE: Qualified Version Definitions:

- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|--------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| ADS4222IRGCR | VQFN | RGC | 64 | 2000 | 330.0 | 16.4 | 9.3 | 9.3 | 1.5 | 12.0 | 16.0 | Q2 |
| ADS4225IRGCR | VQFN | RGC | 64 | 2000 | 330.0 | 16.4 | 9.3 | 9.3 | 1.5 | 12.0 | 16.0 | Q2 |
| ADS4226IRGCR | VQFN | RGC | 64 | 2000 | 330.0 | 16.4 | 9.3 | 9.3 | 1.5 | 12.0 | 16.0 | Q2 |
| ADS4242IRGCR | VQFN | RGC | 64 | 2000 | 330.0 | 16.4 | 9.3 | 9.3 | 1.5 | 12.0 | 16.0 | Q2 |
| ADS4245IRGCR | VQFN | RGC | 64 | 2000 | 330.0 | 16.4 | 9.3 | 9.3 | 1.5 | 12.0 | 16.0 | Q2 |
| ADS4246IRGCR | VQFN | RGC | 64 | 2000 | 330.0 | 16.4 | 9.3 | 9.3 | 1.5 | 12.0 | 16.0 | Q2 |

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|--------------|--------------|-----------------|------|------|-------------|------------|-------------|
| ADS4222IRGCR | VQFN | RGC | 64 | 2000 | 350.0 | 350.0 | 43.0 |
| ADS4225IRGCR | VQFN | RGC | 64 | 2000 | 350.0 | 350.0 | 43.0 |
| ADS4226IRGCR | VQFN | RGC | 64 | 2000 | 350.0 | 350.0 | 43.0 |
| ADS4242IRGCR | VQFN | RGC | 64 | 2000 | 350.0 | 350.0 | 43.0 |
| ADS4245IRGCR | VQFN | RGC | 64 | 2000 | 350.0 | 350.0 | 43.0 |
| ADS4246IRGCR | VQFN | RGC | 64 | 2000 | 350.0 | 350.0 | 43.0 |

GENERIC PACKAGE VIEW

RGC 64

VQFN - 1 mm max height

9 x 9, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4224597/A

VQFN - 1 mm max height

[illegible]

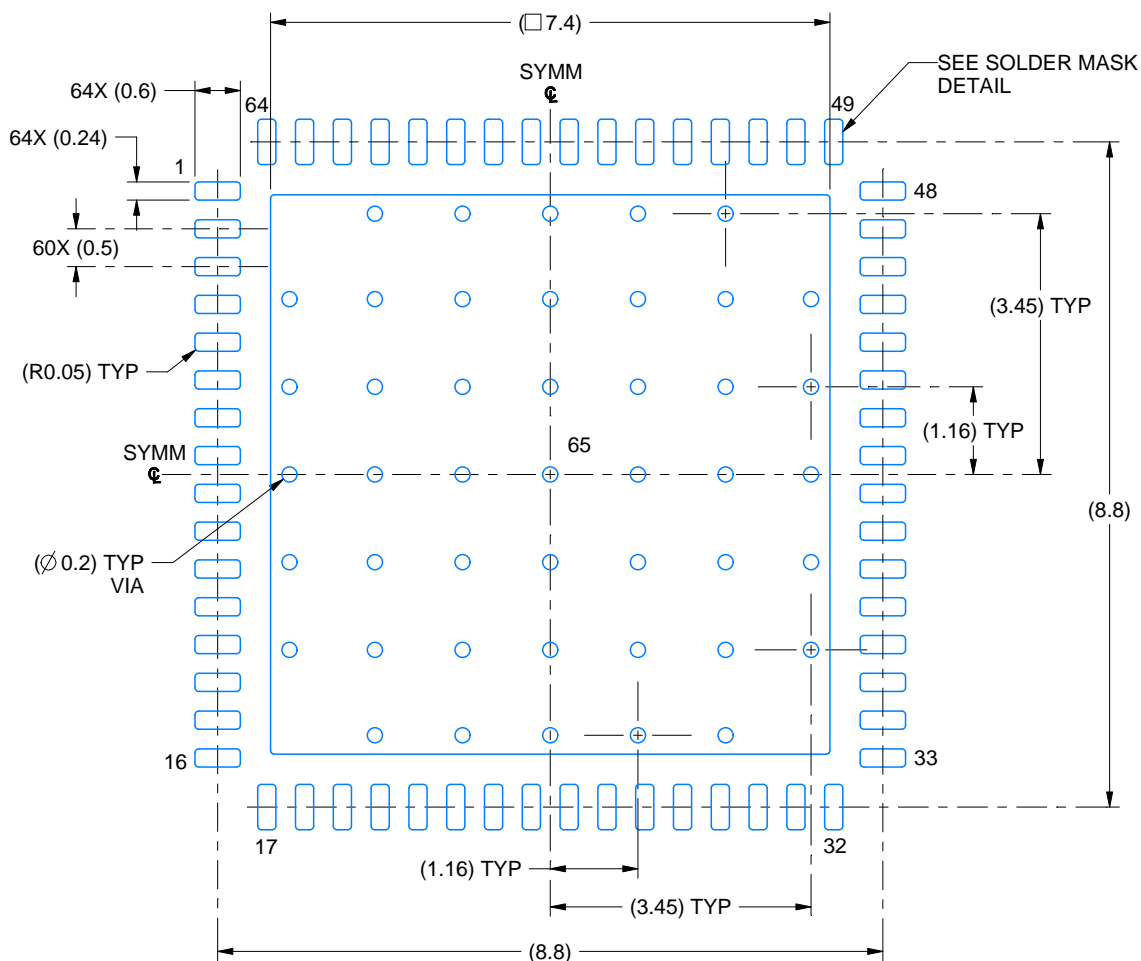
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

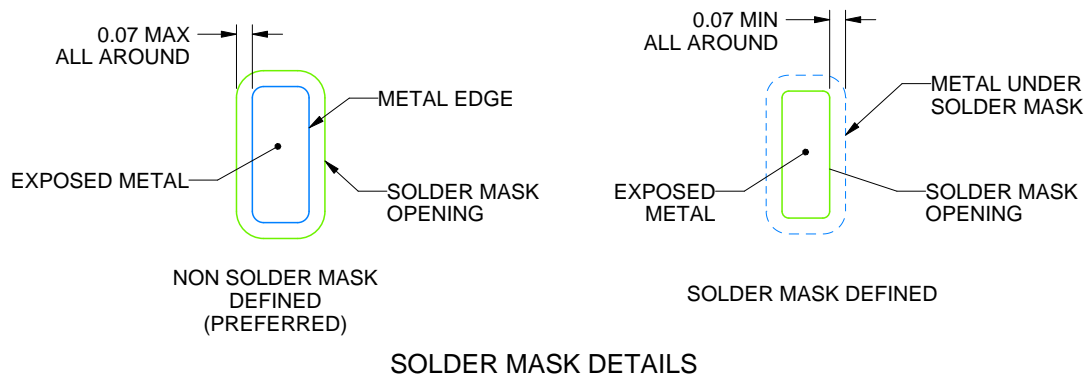
RGC0064H

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

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NOTES: (continued)

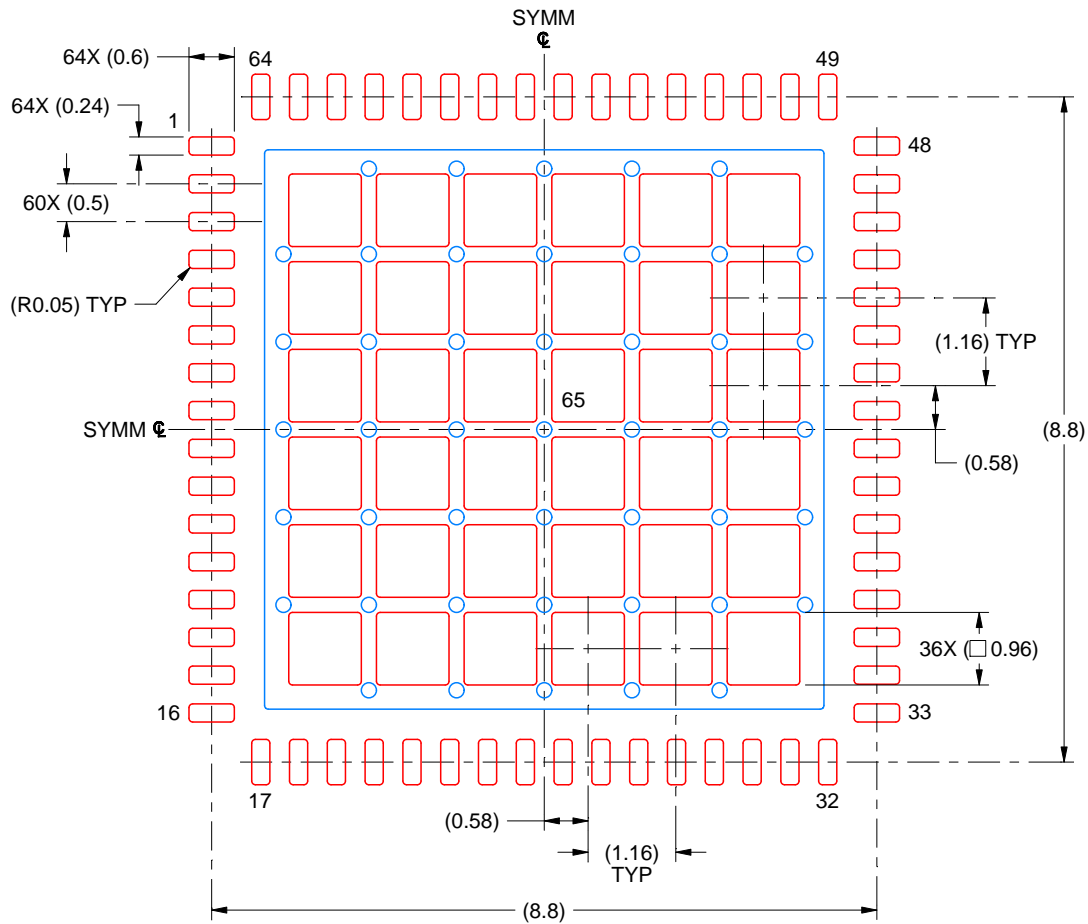
- This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/sluea271).
- Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

RGC0064H

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 10X

EXPOSED PAD 65
61% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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