

10BASE-T/100BASE-TX INTEGRATED PHYCEIVER WITH RMII INTERFACE
ICS1894-40

Description

The ICS1894-40 is a low-power, physical-layer device (PHY) that supports the ISO/IEC 10Base-T and 100Base-TX Carrier-Sense Multiple Access/Collision Detection (CSMA/CD) Ethernet standards, ISO/IEC 8802-3.

The ICS1894-40 is intended for MII, Node applications that require the Auto-MDIX feature that automatically corrects crossover errors in plant wiring.

The ICS1894-40 incorporates Digital-Signal Processing (DSP) control in its Physical-Medium Dependent (PMD) sub layer. As a result, it can transmit and receive data on unshielded twisted-pair (UTP) category 5 cables with attenuation in excess of 24 dB at 100MHz. With this IDT-patented technology, the ICS1894-40 can virtually eliminate errors from killer packets.

The ICS1894-40 provides a Serial-Management Interface for exchanging command and status information with a Station-Management (STA) entity. The ICS1894-40 Media-Dependent Interface (MDI) can be configured to provide either half- or full-duplex operation at data rates of 10 Mb/s or 100Mb/s.

In addition, the ICS1894-40 includes a programmable interrupt output function. This function consists of a digital output pin, an interrupt control register, a set of interrupt status register bits and a corresponding set of interrupt enable bits, and a pre-defined set of events which can be assigned as one of the interrupt sources. The purpose of this function is to notify the host of this PHY device when certain event happens via interrupt (the logic level on interrupt output pin going low or going high) instead of polling by the host. The events that could be used to generate interrupts are: receiver error, Jabber, page received, parallel detect fault, link partner acknowledge, link status change, auto-negotiation complete, remote fault, collision, etc

Applications: NIC cards, PC motherboards, switches, routers, DSL and cable modems, game machines, printers, network connected appliances, and industrial equipment.

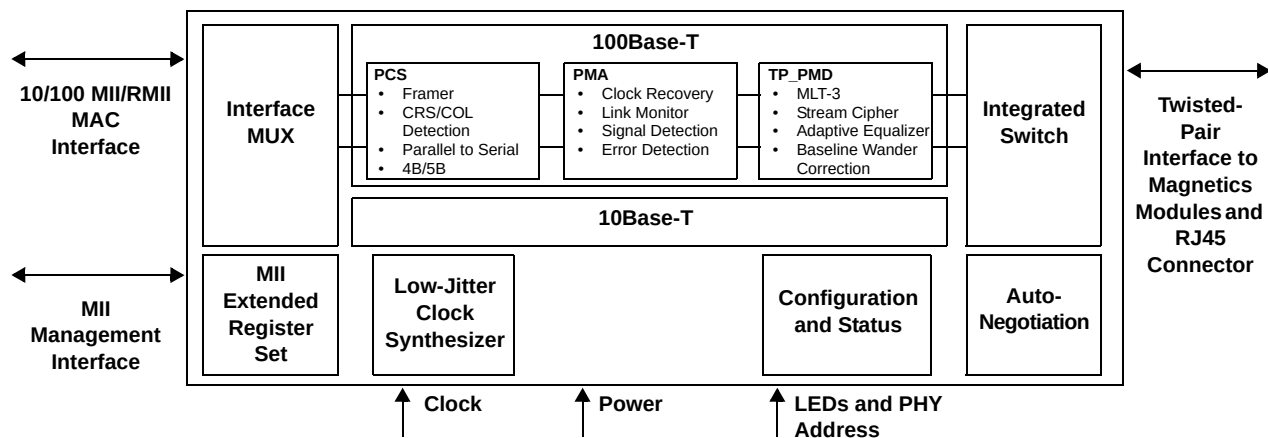
Features

- Supports category 5 cables with attenuation in excess of 24dB at 100 MHz.
- Single-chip, fully integrated PHY provides PCS, PMA, PMD, and AUTONEG sub layers functions of IEEE standard.
- 10Base-T and 100Base-TX IEEE 8802.3 compliant
- MIIM (MDC/MDIO) management bus for PHY register configuration
- RMII interface support with external 50 MHz system clock
- Single 3.3V power supply
- Highly configurable, supports:
 - Media Independent Interface (MII)
 - Auto-Negotiation with Parallel detection
 - Node applications, managed or unmanaged
 - 10M or 100M full and half-duplex modes
 - Loopback mode for Diagnostic Functions

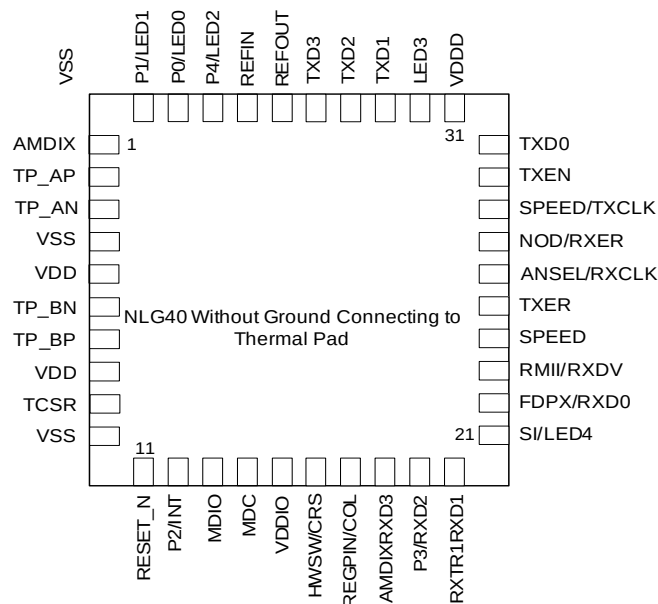
Auto-MDI/MDIX crossover correction

- Low-power CMOS (typically 300 mW)
- Power-Down mode typically 21mW
- Clock and crystal supported
- Interrupt pin option
- Fully integrated, DSP-based PMD includes:
 - Adaptive equalization and baseline-wander correction
 - Transmit wave shaping and stream cipher scrambler
 - MLT-3 encoder and NRZ/NRZI encoder
- Single power supply (3.3 V)
- Built-in 1.8 V regulator for core
- Available in 40-pin (5mm x 5mm) QFN package, Pb-free
- Available in Industrial Temp and Lead Free

Block Diagram



Pin Assignment



40-pin MLF

40-pin 6mm x 6mm QFN

Pin Descriptions

Pin Number	Pin Name	Pin Type	Pin Description
1	AMDIX	IN/Ipu	AMDIX Enable
2	TP_AP	AIO	Twisted pair port A (for either transmit or receive) positive signal
3	TP_AN	AIO	Twisted pair port A (for either transmit or receive) negative signal
4	VSS	Ground	Connect to ground.
5	VDD	Power	3.3V Power Supply
6	TP_BN	AIO	Twisted pair port B (for either transmit or receive) negative signal
7	TP_BP	AIO	Twisted pair port B (for either transmit or receive) positive signal
8	VDD	Power	3.3V Power Supply
9	TCSR	AIO	Transmit Current bias pin, connected to Vdd and ground via two resistors.
10	VSS	Ground	Connect to ground.
11	RESET_N	Input	Hardware reset for the whole chip (active low)
12	P2/INT	IO/lpd	PHY address Bit 2 as input (during power on reset and hardware reset) Interrupt output as output (default active low, can be programmed to active high)
13	MDIO	IO	Management Data Input/Output
14	MDC	Input	Management Data Clock
15	VDDIO	Power	3.3 V IO Power Supply.
16	HWSW/ CRS	IO/Ipu	Hard pin select enable as input (during power on reset and hardware reset) and MII CRS as output
17	Regpin/ COL	IO/lpd	Full register access enable as input (during power on reset and hardware reset) and MII COL output
18	AMDIX/RXD3	IO/Ipu	AMDIX enable as input (during power on reset and hardware reset) Receive data Bit 3 for MII
19	P3/RXD2	IO/lpd	PHY address Bit 3 as input (during power on reset and hardware reset) Receive data Bit 2 for MII as output.
20	RXTRI/ RXD1	IO/Ipu	RX isolate enable (during power on reset and hardware reset) Received data Bit 1 for both RMII and MII
21	SI/LED4	IO/lpd	MII/SI mode select as input (during power on reset and hardware reset) and LED # 4 as output
22	FDPX/ RXD0	IO/Ipu	Full duplex enable (during power on reset and hardware reset) Received data Bit 0 for both RMII and MII
23	RMII/RXDV	IO/lpd	RMII/MII select as input (during power on reset and hardware reset) Receive data valid for MII and CRS_DV for RMII as output
24	SPEED	lpd	10/100M input select. 1 = 100M mode, 0 = 10M mode.
25	TXER	IN	TXER Input
26	ANSEL/ RXCLK9	IO/Ipu	Auto-negotiation enable(during power on reset and hardware reset) Receive clock MII
27	NOD/ RXER	IO/lpd	Node/repeater select (during power on reset and hardware reset) Receive error

Pin Number	Pin Name	Pin Type	Pin Description
28	SPEED/ TXCLK	IO/Ipu	10M/100M select as input (during power on reset and hardware reset) Transmit clock for MII as output
29	TXEN	Input	Transmit enable for both RMII and MII
30	TXD0	Input	Transmit data Bit 0 for both RMII and MII
31	VDDD	Power	Core Power Supply
32	LED3	IO/Ipd	LED3 output
33	TXD1	Input	Transmit data Bit 1 for both RMII and MII
34	TXT2	Input	Transmit data Bit 2 for MII
35	TXD3	Input	Transmit data Bit 3 for MII
36	REF_OUT	Output	25 MHz crystal output
37	REF_IN	Input	25 MHz crystal (or clock) input for MII. 50MHz clock input for RMII
38	P4/LED2	IO/Ipu	PHY address Bit 4 as input (during power on reset and hardware reset) And LED # 2 as output
39	P0/LED0	IO	PHY address Bit 0 as input (during power on reset and hardware reset) and LED # 0(function configurable, default is "activity/no activity") as output
40	P1/LED1	IO	PHY address Bit 1 as input (during power on reset and hardware reset) and LED # 1 (function configurable, default is "10/100 mode") as output

Notes:

1. Ipd = Input with internal pull-down.
Ipu = Input with internal pull-up.
Opu = Output with internal pull-up.
Ipu/O = Input with internal pull-up during power-up/reset; output pin otherwise.
Ipd/O = Input with internal pull-down during power-up/reset; output pin otherwise.
2. MII Rx Mode: The RXD[3..0] bits are synchronous with RXCLK. When RXDV is asserted, RXD[3..0] presents valid data to MAC through the MII. RXD[3..0] is invalid when RXDV is de-asserted.
3. RMII Rx Mode: The RXD[1:0] bits are synchronous with REF_CLK. For each clock period in which CRS_DV is asserted, two bits of recovered data are sent from the PHY.
4. MII Tx Mode: The TXD[3..0] bits are synchronous with TXCLK. When TXEN is asserted, TXD[3..0] presents valid data from the MAC through the MII. TXD[3..0] has no effect when TXEN is de-asserted.
5. RMII Tx Mode: The TXD[1:0] bits are synchronous with REF_CLK. For each clock period in which TX_EN is asserted, two bits of data are received by the PHY from the MAC.

Strapping Options

Pin Number	Pin Name	Pin Type ¹	Pin Function
1	AMDIX	IN/lpu	1 = AMDIX enable 0 = AMDIX disable
16	HWSW/CRS	IO/lpd	Hardware pin select enable. Active during power-on and hardware reset.
17	REGPIN/COL	IO/lpd	Full register access enable. Active during power-on and hardware reset.
18	AMDIX/RXD2	IO/lpu	1 = AMDIX enable 0 = AMDIX disable
38	P4/LED2	IO/lpu	The PHY address is set by P[4:0] at power-on reset. P0 and P1 must have external pull-up or pull-down to set address at start up.
19	P3/RXD2	IO/lpd	
12	P2/INT	IO/lpd	
40	P1/LED1	IO/	
39	P0/LED0	IO/	
21	SI/LED4	IO/lpd	MII/SI mode select. Active during power-on and hardware reset.
20	RXTRI/RXD1	IO/lpd	1=RX tri-state for MII/RMII interface 0=RX output enable
22	FDPX/RXD0	IO/lpu	1=Full duplex 0=Half duplex Ignored if Auto negotiation is enabled
23	RMII/RXDV	IO/lpd	[1x]=RMII mode [01]=SI mode (Serial interface mode) [00]=MII mode
24	SPEED	IO/lpu	1=100M mode 0=10M mode
26	ANSEL/RXCLK	IO/lpu	1=Enable auto negotiation 0=Disable auto negotiation
27	NOD/RXER	IO/lpd	0=Node mode 1=repeater mode
28	SPEED/TXCLK	IO/lpu	1=100M mode 0=10M mode Ignored if Auto negotiation is enabled
32	LED3	IO/lpu	LED3 output

1. lpu/O = Input with internal pull-up during power-up/reset; output pin otherwise.

lpd/O = Input with internal pull-down during power-up/reset; output pin otherwise.

Functional Description

The ICS1894-32 is a stream processor. During data transmission, it accepts sequential nibbles from its MAC (Media Access Control) converts them into a serial bit stream, encodes them, and transmits them over the medium through an external isolation transformer. When receiving data, the ICS1894-32 converts and decodes a serial bit stream (acquired from an isolation transformer that

interfaces with the medium) into sequential nibbles. It subsequently presents these nibbles to its MAC Interface.

The ICS1894-32 implements the OSI model's physical layer, consisting of the following, as defined by the ISO/IEC 8802-3 standard:

- Physical Coding sublayer (PCS)

- Physical Medium Attachment sublayer (PMA)
- Physical Medium Dependent sublayer (PMD)
- Auto-Negotiation sublayer

The ICS1894-32 is transparent to the next layer of the OSI model, the link layer. The link layer has two sublayers: the Logical Link Control sublayer and the MAC sublayer. The ICS1894-32 can interface directly to the MAC.

The ICS1894-32 transmits framed packets acquired from its MAC Interface and receives encapsulated packets from another PHY, which it translates and presents to its MAC Interface.

Note: As per the ISO/IEC standard, the ICS1894-32 does not affect, nor is it affected by, the underlying structure of the MAC frame it is conveying.

100Base-TX Operation

During 100Base-TX data transmission, the ICS1894-32 accepts packets from a MAC and inserts Start-of-Stream Delimiters (SSDs) and End-of-Stream Delimiters (ESDs) into the data stream. The ICS1894-32 encapsulates each MAC frame, including the preamble, with an SSD and an ESD. As per the ISO/IEC Standard, the ICS1894-32 replaces the first octet of each MAC preamble with an SSD and appends an ESD to the end of each MAC frame.

When receiving data from the medium, the ICS1894-32 removes each SSD and replaces it with the pre-defined preamble pattern before presenting the nibbles to its MAC Interface. When the ICS1894-32 encounters an ESD in the received data stream, signifying the end of the frame, it ends the presentation of nibbles to its MAC Interface. Therefore, the local MAC receives an unaltered copy of the transmitted frame sent by the remote MAC.

During periods when MAC frames are being neither transmitted nor received, the ICS1894-32 signals and detects the IDLE condition on the Link Segment. In the 100Base-TX mode, the ICS1894-32 transmit channel sends a continuous stream of scrambled ones to signify the IDLE condition. Similarly, the ICS1894-32 receive channel continually monitors its data stream and looks for a pattern of scrambled ones. The results of this signaling and monitoring provide the ICS1894-32 with the means to establish the integrity of the Link Segment between itself and its remote link partner and inform its Station

Management Entity (STA) of the link status.

For 100M data transmission, the ICS1894-32 MAC Interface is configured to provide a 100M Media Independent Interface (MII).

10Base-T Operation

During 10Base-T data transmission, the ICS1894-32 inserts only the IDL delimiter into the data stream. The ICS1894-32 appends the IDL delimiter to the end of each MAC frame. However, since the 10Base-T preamble already has a Start-of-Frame delimiter (SFD), it is not required that the ICS1894-32 insert an SSD-like delimiter.

When receiving data from the medium (such as a twisted-pair cable), the ICS1894-32 uses the preamble to synchronize its receive clock. When the ICS1894-32 receive clock establishes lock, it presents the preamble nibbles to its MAC Interface. The 10M MAC Interface uses the standard MII Interface.

In 10M operations, during periods when MAC frames are being neither transmitted nor received, the ICS1894-32 signals and detects Normal Link Pulses. This action allows the integrity of the Link Segment with the remote link partner to be established and then reported to the ICS1894-32's STA.

SQE and Jabber Function (10Base-T only)

In 10Base-T operation, a short pulse is put out on the COL pin after each frame is transmitted. This SQE Test is required as a test of the 10Base-T transmit/receive path. If transmit enable (TXEN) is high for more than 20 ms (jabbering), the 10Base-T transmitter is disabled and COL is asserted high. If TXEN is then driven low for more than 250 ms, the 10Base-T transmitter is re-enabled and COL is de-asserted (returns to low).

Auto-Negotiation

The ICS1894-40 conforms to the auto-negotiation protocol, defined in Clause 28 of the IEEE 802.3u specification. Autonegotiation is enabled by either hardware pin strapping (pin 20) or software (register 0h bit 12).

Auto-negotiation allows unshielded twisted pair (UTP) link partners to select the highest common mode of operation. Link partners advertise their capabilities to each other, and then compare their own capabilities with those they received from their link partners. The highest speed and duplex

setting that is common to the two link partners is selected as the mode of operation.

The following list shows the speed and duplex operation mode from highest to lowest.

- Priority 1: 100Base-TX, full-duplex
- Priority 2: 100Base-TX, half-duplex
- Priority 3: 10Base-T, full-duplex
- Priority 4: 10Base-T, half-duplex

If auto-negotiation is not supported or the ICS1894-40 link partner is forced to bypass auto-negotiation, the ICS1894-40 sets its operating mode by observing the signal at its receiver. This is known as parallel detection, and allows the ICS1894-40 to establish link by listening for a fixed signal protocol in the absence of auto-negotiation advertisement protocol.

MII Management (MIIM) Interface

The ICS1894-40 supports the IEEE 802.3 MII Management Interface, also known as the Management Data Input / Output (MDIO) Interface. This interface allows upper-layer devices to monitor and control the state of the ICS1894-40. An external device with MIIM capability is used to read the

PHY status and/or configure the PHY settings. Additional details on the MIIM interface can be found in Clause 22.2.4.5 of the IEEE 802.3u Specification.

The MIIM interface consists of the following:

- A physical connection that incorporates the clock line (MDC) and the data line (MDIO).
- A specific protocol that operates across the aforementioned physical connection that allows an external controller to communicate with one or more ICS1894-40 devices. Each ICS1894-40 device is assigned a PHY address between 1 and 7 by the P[4:0] strapping pins.
- An internal addressable set of thirteen 16-bit MDIO registers. Register [0:6] are required, and their functions are defined by the IEEE 802.3u Specification. The additional registers are provided for expanded functionality.

The ICS1894-40 supports MIIM in both MII mode and RMII mode.

The following table shows the MII Management frame format for the ICS1894-40.

MII Management Frame Format

	Preamble	Start of Frame	Read/Write OP Code	PHY Address Bits [4:0]	REG Address Bits [4:0]	TA	Data Bits [15:0]	Idle
Read	32 1's	01	10	00AAA	RRRRR	Z0	DDDDDDDD_DDDDDDDD	Z
Write	32 1's	01	01	00AAA	RRRRR	10	DDDDDDDD_DDDDDDDD	Z

Interrupt (INT)

INT (pin 12) is an optional interrupt signal that is used to inform the external controller that there has been a status update in the ICS1894-40 PHY register. Bits[15:8] of register 1Bh are the interrupt control bits, and are used to enable and disable the conditions for asserting the INT signal. Bits[7:0] of register 1Bh are the interrupt status bits, and are used to indicate which interrupt conditions have occurred. The interrupt status bits are cleared after reading register 1Bh. Bit 9 of register 1Fh sets the interrupt level to active high or active low.

MII Data Interface

The Media Independent Interface (MII) is specified in Clause 22 of the IEEE 802.3u Specification. It provides a

common interface between physical layer and MAC layer devices, and has the following key characteristics:

- Supports 10Mbps and 100Mbps data rates.
- Uses a 25MHz reference clock, sourced by the PHY.
- Provides independent 4-bit wide (nibble) transmit and receive data paths.
- Contains two distinct groups of signals: one for transmission and the other for reception.

By default, the ICS1894-40 is configured in MII mode after it is power-up or reset with the following:

- A 25MHz crystal connected to REF_IN, REF_OUT (pins 37, 36), or an external 25MHz clock source (oscillator) connected to REF_IN.

MII Signal Definition

The following table describes the MII signals. Refer to Clause 22 of the IEEE 802.3u Specification for detailed information.

MII Signal Name	Direction (with respect to PHY, ICS1894-40 signal)	Direction (with respect to MAC)	Description
TXCLK	Output	Input	Transmit Clock (2.5MHz for 10Mbps; 25MHz for 100Mbps)
TXEN	Input	Output	Transmit Enable
TXD[3:0]	Input	Output	Transmit Data [3:0]
RXCLK	Output	Input	Receive Clock (2.5MHz for 10Mbps; 25MHz for 100Mbps)
RXDV	Output	Input	Receive Data Valid
RXD[3:0]	Output	Input	Receive Data [3:0]
RXER	Output	Input, or (not required)	Receive Error
CRS	Output	Input	Carrier Sense
COL	Output	Input	Collision Detection

Transmit Clock (TXCLK)

TXCLK is sourced by the PHY. It is a continuous clock that provides the timing reference for TXEN and TXD[3:0]. TXCLK is 2.5MHz for 10Mbps operation and 25MHz for 100Mbps operation.

Transmit Enable (TXEN)

TXEN indicates the MAC is presenting nibbles on TXD[3:0] for transmission. It is asserted synchronously with the first nibble of the preamble and remains asserted while all nibbles to be transmitted are presented on the MII, and is negated prior to the first TXCLK following the final nibble of a frame. TXEN transitions synchronously with respect to TXCLK.

Transmit Data [3:0] (TXD[3:0])

TXD[3:0] transitions synchronously with respect to TXCLK. When TXEN is asserted, TXD[3:0] are accepted for transmission by the PHY. TXD[3:0] is "00" to indicate idle when TXEN is de-asserted. Values other than "00" on TXD[3:0] while TXEN is de-asserted are ignored by the PHY.

Receive Clock (RXCLK)

RXCLK provides the timing reference for RXDV, RXD[3:0], and RXER.

- In 10Mbps mode, RXCLK is recovered from the line while carrier is active. RXCLK is derived from the PHY's reference clock when the line is idle, or link is down.
- In 100Mbps mode, RXCLK is continuously recovered from the line. If link is down, RXCLK is derived from the PHY's reference clock.

RXCLK is 2.5MHz for 10Mbps operation and 25MHz for 100Mbps operation.

Receive Data Valid (RXDV)

RXDV is driven by the PHY to indicate that the PHY is presenting recovered and decoded nibbles on RXD[3:0].

- In 10Mbps mode, RXDV is asserted with the first nibble of the SFD (Start of Frame Delimiter), "5D", and remains asserted until the end of the frame.
- In 100Mbps mode, RXDV is asserted from the first nibble of the preamble to the last nibble of the frame.

RXDV transitions synchronously with respect to RXCLK.

Receive Data [3:0] (RXD[3:0])

RXD[3:0] transitions synchronously with respect to RXC. For each clock period in which RXDV is asserted, RXD[3:0] transfers a nibble of recovered data from the PHY.

Receive Error (RXER)

RXER is asserted for one or more RXCLK periods to indicate that an error (e.g. a coding error or any error that a PHY is capable of detecting, and that may otherwise be undetectable by the MAC sub-layer) was detected somewhere in the frame presently being transferred from the PHY. RXER transitions synchronously with respect to RXC. While RXDV is de-asserted, RXER has no effect on the MAC.

Carrier Sense (CRS)

CRS is asserted and de-asserted as follows:

- In 10Mbps mode, CRS assertion is based on the reception of valid preambles. CRS de-assertion is based on the reception of an end-of-frame (EOF) marker.
- In 100Mbps mode, CRS is asserted when a start-of-stream delimiter, or /J/K symbol pair is detected. CRS is deasserted when an end-of-stream delimiter, or /T/R symbol pair is detected. Additionally, the PMA layer de-asserts CRS if IDLE symbols are received without /T/R.

Collision (COL)

COL is asserted in half-duplex mode whenever the transmitter and receiver are simultaneously active on the line. This is used to inform the MAC that a collision has occurred during its transmission to the PHY.

COL transitions asynchronously with respect to TXCLK and RXCLK.

Reduced MII (RMII) Data Interface

The Reduced Media Independent Interface (RMII) specifies a low pin count Media Independent Interface (MII). It provides a common interface between physical layer and MAC layer devices, and has the following key characteristics:

- Supports 10Mbps and 100Mbps data rates.
- Uses a single 50MHz reference clock provided by the MAC or the system board.
- Provides independent 2-bit wide (di-bit) transmit and receive data paths.
- Contains two distinct groups of signals: one for transmission and the other for reception.

The ICS1894-40 is configured in RMII mode after it is

power-up or reset with the following:

- A 50MHz reference clock connected to REF_IN (pin 37). In RMII mode, unused MII signals, TXD[3:2] (pins 35, 34), are tied to ground.

RMII Signal Definition

The following table describes the RMII signals. Refer to RMII Specification for detailed information.

RMII Signal Name	Direction (with respect to PHY, ICS1894-40 signal)	Direction (with respect to MAC)	Description
REF_CLK	Input	Input or Output	Synchronous 50 MHz clock reference for receive, transmit and control interface
TX_EN	Input	Output	Transmit Enable
TXD[1:0]	Input	Output	Transmit Data [1:0]
CRS_DV	Output	Input	Carrier Sense/Receive Data Valid
RXD[1:0]	Output	Input	Receive Data [1:0]
RX_ER	Output	Input, or (not required)	Receive Error

Reference Clock (REF_CLK)

REF_CLK is sourced by the MAC or system board. It is a continuous 50MHz clock that provides the timing reference for TX_EN, TXD[1:0], CRS_DV, RXD[1:0], and RX_ER.

Transmit Enable (TX_EN)

TX_EN indicates that the MAC is presenting di-bits on TXD[1:0] for transmission. It is asserted synchronously with the first nibble of the preamble and remains asserted while all di-bits to be transmitted are presented on the RMII, and is negated prior to the first REF_CLK following the final di-bit of a frame. TX_EN transitions synchronously with respect to REF_CLK.

Transmit Data [1:0] (TXD[1:0])

TXD[1:0] transitions synchronously with respect to REF_CLK. When TX_EN is asserted, TXD[1:0] are accepted for transmission by the PHY. TXD[1:0] is "00" to indicate idle when TX_EN is de-asserted. Values other than "00" on TXD[1:0] while TX_EN is de-asserted are ignored by the PHY.

Carrier Sense/Receive Data Valid (CRS_DV)

CRS_DV is asserted by the PHY when the receive medium is non-idle. It is asserted asynchronously on detection of carrier. This is when squelch is passed in 10Mbps mode, and when 2 non-contiguous zeroes in 10 bits are detected in 100Mbps mode. Loss of carrier results in the de-assertion of CRS_DV. So long as carrier detection criteria are met, CRS_DV remains asserted continuously from the first recovered di-bit of the frame through the final recovered di-bit, and it is negated prior to the first REF_CLK that

follows the final di-bit. The data on RXD[1:0] is considered valid once CRS_DV is asserted. However, since the assertion of CRS_DV is asynchronous relative to REF_CLK, the data on RXD[1:0] is "00" until proper receive signal decoding takes place.

Receive Data [1:0] (RXD[1:0])

RXD[1:0] transitions synchronously to REF_CLK. For each clock period in which CRS_DV is asserted, RXD[1:0] transfers two bits of recovered data from the PHY. RXD[1:0] is "00" to indicate idle when CRS_DV is de-asserted. Values other than "00" on RXD[1:0] while CRS_DV is de-asserted are ignored by the MAC.

Receive Error (RX_ER)

RX_ER is asserted for one or more REF_CLK periods to indicate that an error (e.g. a coding error or any error that a PHY is capable of detecting, and that may otherwise be undetectable by the MAC sub-layer) was detected somewhere in the frame presently being transferred from the PHY. RX_ER transitions synchronously with respect to REF_CLK. While CRS_DV is de-asserted, RX_ER has no effect on the MAC.

Auto-MDI/MDIX Crossover

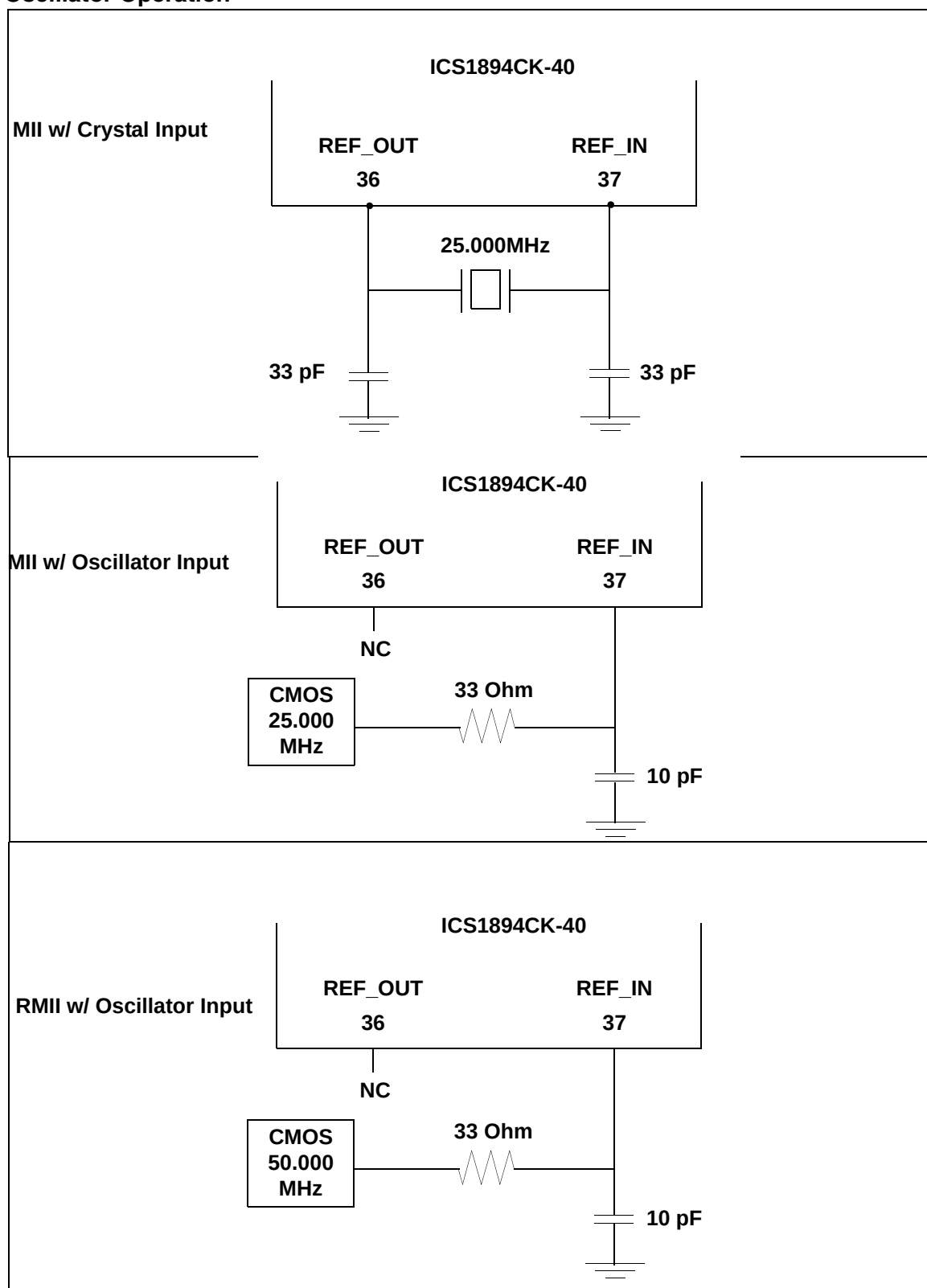
The ICS1894-40 includes the auto-MDI/MDIX crossover feature. In a typical CAT 5 Ethernet installation the transmit twisted pair signal pins of the RJ45 connector are crossed over in the CAT 5 wiring to the partners receive twisted pair signal pins and receive twisted pair to the partners transmit twisted pair. This is usually accomplished in the wiring plant. Hubs generally wire the RJ45 connector crossed to accomplish the crossover. Two types of CAT 5 cables (straight and crossed) are available to achieve the correct connection. The Auto-MDI/MDIX feature automatically corrects for miss-wired installations by automatically swapping transmit and receive signal pairs at the PHY when no link results. Auto-MDI/MDIX is automatic, but may be disabled for test purposes by writing MDIO register 19 Bits 9:8 in the MDIO register. The Auto-MDI/MDIX function is independent of Auto-Negotiation and preceeds Auto-Negotiation when enabled.

Power Management

Clock Reference Interface

The REF_IN pin provides the ICS1894-40 Clock Reference Interface. The ICS1894-40 requires a single clock reference with a frequency of 25 MHz $\pm$ 50 parts per million. This accuracy is necessary to meet the interface requirements of the ISO/IEEE 8802-3 standard, specifically clauses 22.2.2.1 and 24.2.3.4. The ICS1894-40 supports two clock source configurations: a CMOS oscillator or a CMOS driver. The input to REF_IN is CMOS (10% to 90% VDD), not TTL. Alternately, a 25MHz crystal may be used.

Crystal or Oscillator Operation



If a crystal is used as the clocking source, connect it to both the REF_IN (pin 37) and REF_OUT (pin 36) pins of the ICS1894-40. A pair of bypass capacitors on either side of the crystal are connected to ground. The crystal is used in the parallel resonance or anti-resonance mode. The value of the load caps serve to adjust the final frequency of the crystal oscillation. Typical applications would use 33pF load caps. The exact value will be affected by the board routing capacitance on REF_IN and REF_OUT pins. Smaller load capacitors raise the frequency of oscillation.

Once the exact value of load capacitance is established it will be the same for all boards using the same specification crystal. The best way to measure the crystal frequency is to measure the frequency of TXCLK (pin 28) using a frequency counter with a 1 second gate time. Using the buffered output TXCLK prevents the crystal frequency from being affected by the measurement. The crystal specification is shown in the *25MHz Crystal Specification* table.

25 MHz Crystal Specification Table

Specifications	Symbol	Minimum	Typical	Maximum	Unit
Fundamental Frequency (tolerance is sum of freq., temp., stability and aging.)	F0	24.99875	25.00000	25.00125	MHz
Freq. Tolerance	$\Delta F/f$			± 50	ppm
Input Capacitance	Cin		3		pF

25 MHz Oscillator Specification table

Specifications	Symbol	Minimum	Typical	Maximum	Unit
Output Frequency	F0	24.99875	25.00000	25.00125	MHz
Freq. Stability (including aging)	$\Delta F/f$			± 50	ppm
Duty cycle CMOS level one-half VDD	Tw/T	35		65	%
VIH		2.79			Volts
VIL				0.33	Volts
Period Jitter	Tjitter			500	pS
Input Capacitance	CIN		3		pF

50 MHz Oscillator Specification table

Specifications	Symbol	Minimum	Typical	Maximum	Unit
Output Frequency	F0	49.9975	50.00000	50.0025	MHz
Freq. Stability (including aging)	$\Delta F/f$			± 50	ppm
Duty cycle CMOS level one-half VDD	Tw/T	35		65	%
VIH		2.79			Volts
VIL				0.33	Volts
Period Jitter	Tjitter			500	pS
Input Capacitance	CIN		3		pF

Status Interface

The ICS1894-40 provides five multi-function configuration pins that report the results of continual link monitoring by providing signals that are intended for driving LEDs.

Pins for Monitoring the Data Link table

Pin	LED Driven by the Pin's Output Signal
P0AC	AC (Link Activity) LED
P1CL	CL (Collisions) LED
P2LI	LI (Link Integrity) LED
P3TD	TD (Transmit Data) LED
P4RD	RD (Receive Data) LED

Note:

1. During either a power-on reset or a hardware reset, each multi-function configuration pin is an input that is sampled when the ICS1894-40 exits the reset state. After sampling is complete, these pins are output pins that can drive status LEDs.
2. A software reset does not affect the state of a multi-function configuration pin. During a software reset, all multi-function configuration pins are outputs.
3. Each multi-function configuration pin must be pulled either up or down with a resistor to establish the address of

the ICS1894-40. LEDs may be placed in series with these resistors to provide a designated status indicator as described in the *Pins for Monitoring the Data Link* table. Use 1K Ω resistors.

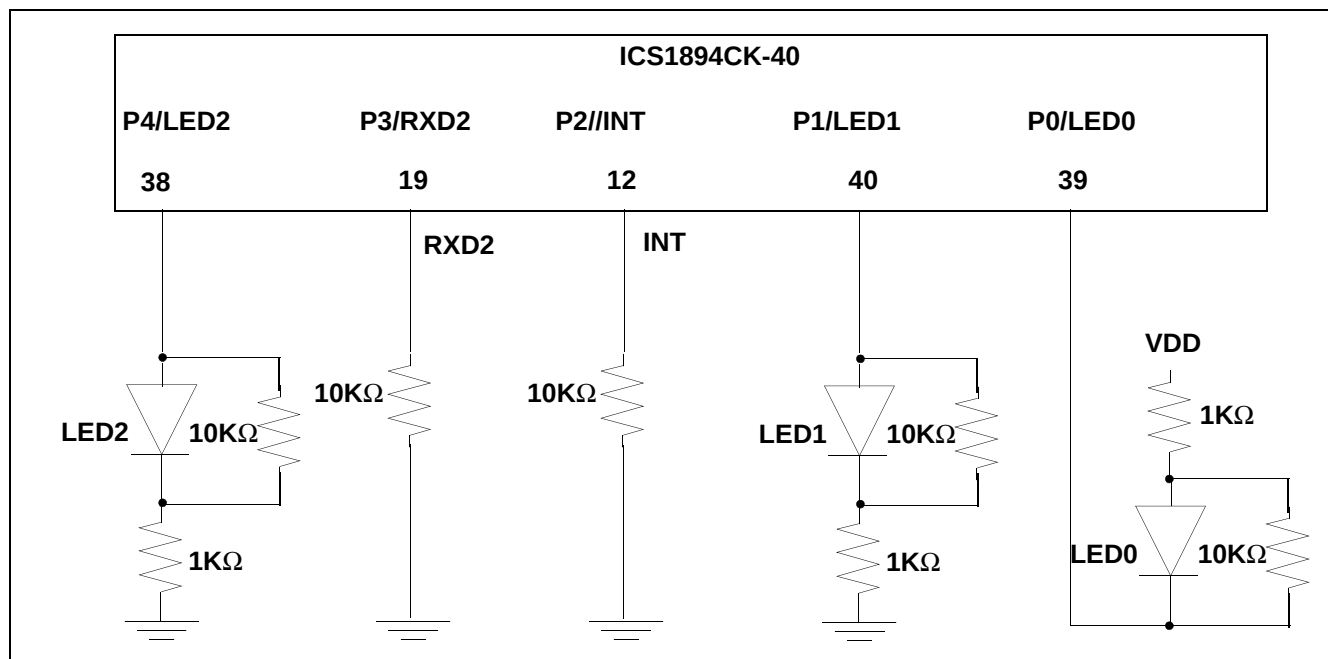
Caution: All pins listed in the *Pins for Monitoring the Data Link* table must not float.

4. As outputs, the asserted state of a multi-function configuration pin is the inverse of the sense sampled during reset. This inversion provides a signal that can illuminate an LED during an asserted state. For example, if a multi-function configuration pin is pulled down to ground through an LED and a current-limiting resistor, then the sampled sense of the input is low. To illuminate this LED for the asserted state, the output is driven high.

5. Adding 10K Ω resistors across the LEDs ensures the PHY address is fully defined during slow VDD power-ramp conditions.

6. PHY address 00 tri-states the MII interface. (Do not select PHY address 00 unless you want the MII tri-stated.)

The following figure shows typical biasing and LED connections for the ICS1894-40.



This circuit decodes to PHY address = 1

Register Map

Register Address	Register Name	Basic / Extended
0	Control	Basic
1	Status	Basic
2,3	PHY Identifier	Extended
4	Auto-Negotiation Advertisement	Extended
5	Auto-Negotiation Link Partner Ability	Extended
6	Auto-Negotiation Expansion	Extended
7	Auto-Negotiation Next Page Transmit	Extended
8	Auto-Negotiation Next Page Link Partner Ability	Extended
9 through 15	Reserved by IEEE	Extended
16 through 31	Vendor-Specific (ICS) Registers	Extended

Register Description

Bit	Definition	When Bit = 0	When Bit = 1	Access	SF	Default	Hex
Register 0h - Control							
0.15	Reset	No effect	ICS1893CF enters Reset mode	R/W	SC	0	3
0.14	Loopback enable	Disable Loopback mode	Enable Loopback mode	R/W	–	0	
0.13	Speed select ¹	10 Mbps operation	100 Mbps operation	R/W	–	1	
0.12	Auto-Negotiation enable	Disable Auto-Negotiation	Enable Auto-Negotiation	R/W	–	1	
0.11	Low-power mode	Normal power mode	Low-power mode	R/W	–	0	0/4†
0.10	Isolate	No effect	Isolate ICS1893CF from MII	R/W	–	0/1†	
0.9	Auto-Negotiation restart	No effect	Restart Auto-Negotiation	R/W	SC	0	
0.8	Duplex mode ¹	Half-duplex operation	Full-duplex operation	R/W	–	0	
0.7	Collision test	No effect	Enable collision test	R/W	–	0	0
0.6	IEEE reserved	Always 0	N/A	RO	–	0‡	
0.5	IEEE reserved	Always 0	N/A	RO	–	0‡	
0.4	IEEE reserved	Always 0	N/A	RO	–	0‡	

Bit	Definition	When Bit = 0	When Bit = 1	Access	SF	Default	Hex
0.3	IEEE reserved	Always 0	N/A	RO	–	0†	0
0.2	IEEE reserved	Always 0	N/A	RO	–	0†	
0.1	IEEE reserved	Always 0	N/A	RO	–	0†	
0.0	IEEE reserved	Always 0	N/A	RO	–	0†	
Register 1h - Control							
1.15	100Base-T4	Always 0. (Not supported.)	N/A	RO	–	0	7
1.14	100Base-TX full duplex	Mode not supported	Mode supported	CW	–	1	
1.13	100Base-TX half duplex	Mode not supported	Mode supported	CW	–	1	
1.12	10Base-T full duplex	Mode not supported	Mode supported	CW	–	1	
1.11	10Base-T half duplex	Mode not supported	Mode supported	CW	–	1	8
1.10	IEEE reserved	Always 0	N/A	CW	–	0†	
1.9	IEEE reserved	Always 0	N/A	CW	–	0†	
1.8	IEEE reserved	Always 0	N/A	CW	–	0†	
1.7	IEEE reserved	Always 0	N/A	CW	–	0†	0
1.6	MF Preamble suppression	PHY requires MF Preambles	PHY does not require MF Preambles	RO	–	0	
1.5	Auto-Negotiation complete	Auto-Negotiation is in process, if enabled	Auto-Negotiation is completed	RO	LH	0	
1.4	Remote fault	No remote fault detected	Remote fault detected	RO	LH	0	
1.3	Auto-Negotiation ability	N/A	Always 1: PHY has Auto-Negotiation ability	RO	–	1	9
1.2	Link status	Link is invalid/down	Link is valid/established	RO	LL	0	
1.1	Jabber detect	No jabber condition	Jabber condition detected	RO	LH	0	
1.0	Extended capability	N/A	Always 1: PHY has extended capabilities	RO	–	1	
Register 2h, 3h - PHY Identifier							
2.15	OUI bit 3 c	N/A	N/A	CW	–	0	0
2.14	OUI bit 4 d	N/A	N/A	CW	–	0	
2.13	OUI bit 5 e	N/A	N/A	CW	–	0	
2.12	OUI bit 6 f	N/A	N/A	CW	–	0	
2.11	OUI bit 7 g	N/A	N/A	CW	–	0	0
2.10	OUI bit 8 h	N/A	N/A	CW	–	0	
2.9	OUI bit 9 i	N/A	N/A	CW	–	0	
2.8	OUI bit 10 j	N/A	N/A	CW	–	0	

Bit	Definition	When Bit = 0	When Bit = 1	Ac- cess	SF	De- fault	Hex
2.7	OUI bit 11 k	N/A	N/A	CW	–	0	1
2.6	OUI bit 12 l	N/A	N/A	CW	–	0	
2.5	OUI bit 13 m	N/A	N/A	CW	–	0	
2.4	OUI bit 14 n	N/A	N/A	CW	–	1	
2.3	OUI bit 15 o	N/A	N/A	CW	–	0	5
2.2	OUI bit 16 p	N/A	N/A	CW	–	1	
2.1	OUI bit 17 q	N/A	N/A	CW	–	0	
2.0	OUI bit 18 r	N/A	N/A	CW	–	1	
3.15	OUI bit 19 s	N/A	N/A	CW	–	1	F
3.14	OUI bit 20 t	N/A	N/A	CW	–	1	
3.13	OUI bit 21 u	N/A	N/A	CW	–	1	
3.12	OUI bit 22 v	N/A	N/A	CW	–	1	
3.11	OUI bit 23 w	N/A	N/A	CW	–	0	4
3.10	OUI bit 24 x	N/A	N/A	CW	–	1	
3.9	Manufacturer's Model Number bit 5	N/A	N/A	CW	–	0	
3.8	Manufacturer's Model Number bit 4	N/A	N/A	CW	–	0	
3.7	Manufacturer's Model Number bit 3	N/A	N/A	CW	–	0	5
3.6	Manufacturer's Model Number bit 2	N/A	N/A	CW	–	1	
3.5	Manufacturer's Model Number bit 1	N/A	N/A	CW	–	0	
3.4	Manufacturer's Model Number bit 0	N/A	N/A	CW	–	1	
3.3	Revision Number bit 3	N/A	N/A	CW	–	0	0
3.2	Revision Number bit 2	N/A	N/A	CW	–	0	
3.1	Revision Number bit 1	N/A	N/A	CW	–	0	
3.0	Revision Number bit 0	N/A	N/A	CW	–	0	
Register 4h - Auto-Negotiation Advertisement							
4.15	Next Page	Next page not supported	Next page supported	R/W	–	0	0
4.14	IEEE reserved	Always 0	N/A	CW	–	0†	
4.13	Remote fault	Locally, no faults detected	Local fault detected	R/W	–	0	
4.12	IEEE reserved	Always 0	N/A	CW	–	0†	

Bit	Definition	When Bit = 0	When Bit = 1	Access	SF	Default	Hex
4.11	IEEE reserved	Always 0	N/A	CW	–	0†	1
4.10	IEEE reserved	Always 0	N/A	CW	–	0†	
4.9	100Base-T4	Always 0. (Not supported.)	N/A	CW	–	0	
4.8	100Base-TX, full duplex	Do not advertise ability	Advertise ability	R/W	–	1	
4.7	100Base-TX, half duplex	Do not advertise ability	Advertise ability	R/W	–	1	E
4.6	10Base-T, full duplex	Do not advertise ability	Advertise ability	R/W	–	1	
4.5	10Base-T half duplex	Do not advertise ability	Advertise ability	R/W	–	1	
4.4	Selector Field bit S4	IEEE 802.3-specified default	N/A	CW	–	0	
4.3	Selector Field bit S3	IEEE 802.3-specified default	N/A	CW	–	0	1
4.2	Selector Field bit S2	IEEE 802.3-specified default	N/A	CW	–	0	
4.1	Selector Field bit S1	IEEE 802.3-specified default	N/A	CW	–	0	
4.0	Selector Field bit S0	N/A	IEEE 802.3-specified default	CW	–	1	
Register 5h - Auto-Negotiation Link Partner Ability							
5.15	Next Page	Next Page disabled	Next Page enabled	RO	–	0	0
5.14	Acknowledge	Always 0	N/A	RO	–	0	
5.13	Remote fault	No faults detected	Remote fault detected	RO	–	0	
5.12	IEEE reserved	Always 0	N/A	RO	–	0†	
5.11	IEEE reserved	Always 0	N/A	RO	–	0†	0
5.10	IEEE reserved	Always 0	N/A	RO	–	0†	
5.9	100Base-T4	Always 0. (Not supported.)	N/A	RO	–	0	
5.8	100Base-TX, full duplex	Link partner is not capable	Link partner is capable	RO	–	0	
5.7	100Base-TX, half duplex	Link partner is not capable	Link partner is capable	RO	–	0	0
5.6	10Base-T, full duplex	Link partner is not capable	Link partner is capable	RO	–	0	
5.5	10Base-T, half duplex	Link partner is not capable	Link partner is capable	RO	–	0	
5.4	Selector Field bit S4	IEEE 802.3 defined. Always 0.	N/A	RO	–	0	

Bit	Definition	When Bit = 0	When Bit = 1	Access	SF	Default	Hex
5.3	Selector Field bit S3	IEEE 802.3 defined. Always 0.	N/A	CW	–	0	0
5.2	Selector Field bit S2	IEEE 802.3 defined. Always 0.	N/A	CW	–	0	
5.1	Selector Field bit S1	IEEE 802.3 defined. Always 0.	N/A	CW	–	0	
5.0	Selector Field bit S0	N/A	IEEE 802.3 defined. Always 1.	CW	–	0	
Register 6h - Auto-Negotiation Expansion							
6.15	IEEE reserved	Always 0	N/A	CW	–	0†	0
6.14	IEEE reserved	Always 0	N/A	CW	–	0†	
6.13	IEEE reserved	Always 0	N/A	CW	–	0†	
6.12	IEEE reserved	Always 0	N/A	CW	–	0†	
6.11	IEEE reserved	Always 0	N/A	CW	–	0†	0
6.10	IEEE reserved	Always 0	N/A	CW	–	0†	
6.9	IEEE reserved	Always 0	N/A	CW	–	0†	
6.8	IEEE reserved	Always 0	N/A	CW	–	0†	
6.7	IEEE reserved	Always 0	N/A	CW	–	0†	0
6.6	IEEE reserved	Always 0	N/A	CW	–	0†	
6.5	IEEE reserved	Always 0	N/A	CW	–	0†	
6.4	Parallel detection fault	No Fault	Multiple technologies detected	RO	LH	0	
6.3	Link partner Next Page able	Link partner is not Next Page able	Link partner is Next Page able	RO	–	0	4
6.2	Next Page able	Local device is not Next Page able	Local device is Next Page able	RO	–	1	
6.1	Page received	Next Page not received	Next Page received	RO	LH	0	
6.0	Link partner Auto-Negotiation able	Link partner is not Auto-Negotiation able	Link partner is Auto-Negotiation able	RO	–	0	
Register 7h - Auto-Negotiation Next Page Transmit							
7.15	Next Page	Last Page	Additional Pages follow	RW	–	0	2
7.14	IEEE reserved	Always 0	N/A	RO	–	0†	
7.13	Message Page	Unformatted Page	Message Page	RW	–	1	
7.12	Acknowledge 2	Cannot comply with Message	Can comply with Message	RW	–	0	

Bit	Definition	When Bit = 0	When Bit = 1	Access	SF	Default	Hex
7.11	Toggle	Previous Link Code Word was zero	Previous Link Code Word was one	RO	–	0	0
7.10	Message code field /Unformatted code field	Bit value depends on the particular message	Bit value depends on the particular message	RW	–	0	
7.9	Message code field /Unformatted code field	Bit value depends on the particular message	Bit value depends on the particular message	RW	–	0	
7.8	Message code field /Unformatted code field	Bit value depends on the particular message	Bit value depends on the particular message	RW	–	0	0
7.7	Message code field /Unformatted code field	Bit value depends on the particular message	Bit value depends on the particular message	RW	–	0	
7.6	Message code field /Unformatted code field	Bit value depends on the particular message	Bit value depends on the particular message	RW	–	0	
7.5	Message code field /Unformatted code field	Bit value depends on the particular message	Bit value depends on the particular message	RW	–	0	
7.4	Message code field /Unformatted code field	Bit value depends on the particular message	Bit value depends on the particular message	RW	–	0	1
7.3	Message code field /Unformatted code field	Bit value depends on the particular message	Bit value depends on the particular message	RW	–	0	
7.2	Message code field /Unformatted code field	Bit value depends on the particular message	Bit value depends on the particular message	RW	–	0	
7.1	Message code field /Unformatted code field	Bit value depends on the particular message	Bit value depends on the particular message	RW	–	0	
7.0	Message code field /Unformatted code field	Bit value depends on the particular message	Bit value depends on the particular message	RW	–	1	
Register 8h - Auto-Negotiation Next Page Link Partner Ability							
8.15	Next Page	Last Page	Additional Pages follow	RO	–	0	0
8.14	IEEE reserved	Always 0	N/A	RO	–	0†	
8.13	Message Page	Unformatted Page	Message Page	RO	–	0	
8.12	Acknowledge 2	Cannot comply with Message	Can comply with Message	RO	–	0	0
8.11	Toggle	Previous Link Code Word was zero	Previous Link Code Word was one	RO	–	0	
8.10	Message code field /Unformatted code field	Bit value depends on the particular message	Bit value depends on the particular message	RO	–	0	
8.9	Message code field /Unformatted code field	Bit value depends on the particular message	Bit value depends on the particular message	RO	–	0	
8.8	Message code field /Unformatted code field	Bit value depends on the particular message	Bit value depends on the particular message	RO	–	0	

Bit	Definition	When Bit = 0	When Bit = 1	Access	SF	Default	Hex
8.7	Message code field /Unformatted code field	Bit value depends on the particular message	Bit value depends on the particular message	RO	–	0	0
8.6	Message code field /Unformatted code field	Bit value depends on the particular message	Bit value depends on the particular message	RO	–	0	
8.5	Message code field /Unformatted code field	Bit value depends on the particular message	Bit value depends on the particular message	RO	–	0	
8.4	Message code field /Unformatted code field	Bit value depends on the particular message	Bit value depends on the particular message	RO	–	0	
8.3	Message code field /Unformatted code field	Bit value depends on the particular message	Bit value depends on the particular message	RO	–	0	0
8.2	Message code field /Unformatted code field	Bit value depends on the particular message	Bit value depends on the particular message	RO	–	0	
8.1	Message code field /Unformatted code field	Bit value depends on the particular message	Bit value depends on the particular message	RO	–	0	
8.0	Message code field /Unformatted code field	Bit value depends on the particular message	Bit value depends on the particular message	RO	–	0	
Register 9 through 15h - Reserved by IEEE							
Register 16h - Extended Control Register							
16.15	Command Override Write enable	Disabled	Enabled	RW	SC	0	–
16.14	ICS reserved	Read unspecified	Read unspecified	RW/0	–	0	
16.13	ICS reserved	Read unspecified	Read unspecified	RW/0	–	0	
16.12	ICS reserved	Read unspecified	Read unspecified	RW/0	–	0	
16.11	ICS reserved	Read unspecified	Read unspecified	RW/0	–	0	–
16.10	PHY Address Bit 4			RO	–	P4RD†	
16.9	PHY Address Bit 3			RO	–	P3TD†	
16.8	PHY Address Bit 2			RO	–	P2LI†	
16.7	PHY Address Bit 1			RO	–	P1CL†	–
16.6	PHY Address Bit 0			RO	–	P0AC†	
16.5	Stream Cipher Test Mode	Normal operation	Test mode	RW	–	0	
16.4	ICS reserved	Read unspecified	Read unspecified	RW/0	–	–	

Bit	Definition	When Bit = 0	When Bit = 1	Access	SF	Default	Hex
16.3	NRZ/NRZI encoding	NRZ encoding	NRZI encoding	RW	–	1	8
16.2	Transmit invalid codes	Disabled	Enabled	RW	–	0	
16.1	ICS reserved	Read unspecified	Read unspecified	RW/0	–	0	
16.0	Stream Cipher disable	Stream Cipher enabled	Stream Cipher disabled	RW	–	0	
Register 17h - Quick Poll Detailed Status Register							
17.15	Data rate	10 Mbps	100 Mbps	RO	–	–	–
17.14	Duplex	Half duplex	Full duplex	RO	–	–	0
17.13	Auto-Negotiation Progress Monitor Bit 2	Reference Decode Table	Reference Decode Table	RO	LM X	0	
17.12	Auto-Negotiation Progress Monitor Bit 1	Reference Decode Table	Reference Decode Table	RO	LM X	0	
17.11	Auto-Negotiation Progress Monitor Bit 0	Reference Decode Table	Reference Decode Table	RO	LM X	0	
17.10	100Base-TX signal lost	Valid signal	Signal lost	RO	LH	0	0
17.9	100BasePLL Lock Error	PLL locked	PLL failed to lock	RO	LH	0	
17.8	False Carrier detect	Normal Carrier or Idle	False Carrier	RO	LH	0	
17.7	Invalid symbol detected	Valid symbols observed	Invalid symbol received	RO	LH	0	
17.6	Halt Symbol detected	No Halt Symbol received	Halt Symbol received	RO	LH	0	0
17.5	Premature End detected	Normal data stream	Stream contained two IDLE symbols	RO	LH	0	
17.4	Auto-Negotiation complete	Auto-Negotiation in process	Auto-Negotiation complete	RO	–	0	
17.3	100Base-TX signal detect	Signal present	No signal present	RO	–	0	
17.2	Jabber detect	No jabber detected	Jabber detected	RO	LH	0	0
17.1	Remote fault	No remote fault detected	Remote fault detected	RO	LH	0	
17.0	Link Status	Link is not valid	Link is valid	RO	LL	0	
Register 18h - 10Base-T Operations Register							
18.15	Remote Jabber Detect	No Remote Jabber Condition detected	Remote Jabber Condition Detected	RO	LH	0	–
18.14	Polarity reversed	Normal polarity	Polarity reversed	RO	LH	0	
18.13	Data Bus Mode	Bit18.13 is latched pin RXTRI Bit18.12 is latched SI [1x]=RMII mode [01]=SI mode (Serial interface mode) [00]=MII mode		R0	–	–	
18.12				R0	–	–	

Bit	Definition	When Bit = 0	When Bit = 1	Access	SF	Default	Hex
18.11	AMDIXEN	AMDIX disable	AMDIX enable	RW	—	—	—
18.10	RXTRI	RX output enable	RX tri-state for MII/RMII interface	RW	—	—	
18.9	REGEN	Vender reserved register access enable	Vender reserved register (byte25~byte31) access disable	RW	—	—	
18.8	TM_SWITCH	Switch TMUX2 to TMUX1, test control		RW	—	—	—
18.7	ICS reserved	Read unspecified	Read unspecified	RW/0	—	—	
18.6	ICS reserved	Read unspecified	Read unspecified	RW/0	—	—	
18.5	Jabber inhibit	Normal Jabber behavior	Jabber Check disabled	RW	—	0	0
18.4	ICS reserved	Read unspecified	Read unspecified	RW/1	—	1	
18.3	Auto polarity inhibit	Polarity automatically corrected	Polarity not automatically corrected	RW	—	0	
18.2	SQE test inhibit	Normal SQE test behavior	SQE test disabled	RW	—	0	
18.1	Link Loss inhibit	Normal Link Loss behavior	Link Always = Link Pass	RW	—	0	
18.0	Squelch inhibit	Normal squelch behavior	No squelch	RW	—	0	
Register 19h - Extended Control Register							
19.15	Node Mode	Node mode	Repeater mode	RW	—	0	4
19.14	Hardware/Software Mode	Use bit00.13 select speed	Use real time input pin 24(40NLG) select speed	RO	—	1	
19.13	Remote Fault	No faults detected	Remote fault detected	RO	—	0	
19.12	Register Bank select	[01]=Bank1, access register0x00~0x13 and ICS1893CF register 0x14~0x1F [00]=Bank0, access register0x00~0x13, new defined register 0x14~0x19 and ICS1893CF register 0x1A~0x1F [1x]=Bank0, same as [00]		RW	—	0	2
19.11				RW	—	0	
19.10	ICS reserved	Read unspecified	Read unspecified	RO	—	0	
19.9	AMDIX_EN	See Table 7-22	See Table 7-22	RW	—	1	
19.8	MDI_MODE	See Table 7-22	See Table 7-22	RW	—	0	
19.7	Twisted Pair Tri-State Enable, TPTRI	Twisted Pair Signals are not Tri-States or No effect	Twisted Pair Signals are Tri-States	RW	—	0	0
19.6	ICS reserved	Read unspecified	Read unspecified	RW	—	0	
19.5	ICS reserved	Read unspecified	Read unspecified	RW	—	0	
19.4	ICS reserved	Read unspecified	Read unspecified	RW	—	0	

Bit	Definition	When Bit = 0	When Bit = 1	Access	SF	Default	Hex
19.3	ICS reserved	Read unspecified	Read unspecified	RW	–	0	1
19.2	ICS reserved	Read unspecified	Read unspecified	RW	–	0	
19.1	ICS reserved	Read unspecified	Read unspecified	RW	–	0	
19.0	Automatic 100Base-TX Power Down	Do not automatically power down	Power down automatically	RW	–	1	
Register 20h - Extended Control Register							
20.15	Str_enhance	Normal digital output strength	Enhance digital output strength in 1.8V condition	RW			0
20.14	Fast_off	disable the function	Enable fast_off circuit	RW			0
20.13:12	LED4 Mode	00 = Receive Data 01 = Collision 10 = Full Duplex 11 = OFF (Default LED4)		RW			3
20.11:9	LED3 Mode	000 = Link Integrity 001 = activity/no activity 010 = Transmit Data 011 = Receive Data 100 = Collision 101 = 10/100 mode 110 = Full Duplex 111 = OFF (Default LED3)		RW			7
20.8:6	LED2 Mode	000 = Link Integrity 001 = activity/no activity 010 = Transmit Data 011 = Receive Data 100 = Collision 101 = 10/100 mode 110 = Full Duplex 111 = OFF (Default LED2)		RW			7
20.5:3	LED1 Mode	000 = Link Integrity 001 = activity/no activity 010 = Transmit Data 011 = Receive Data 100 = Collision 101 = 10/100 mode (Default LED1) 110 = Full Duplex 111 = OFF		RW			5
20.2:0	LED0 Mode	000 = Link Integrity 001 = activity/no activity (Default LED0) 010 = Transmit Data 011 = Receive Data 100 = Collision 101 = 10/100 mode 110 = Full Duplex 111 = LINK_STA		RW			1
Register 21h - Extended Control Register							

Bit	Definition	When Bit = 0	When Bit = 1	Access	SF	Default	Hex
21.15:0	RXER_CNT	Receive error count for RMII mode		RW			0
Register 22h - Extended Control Register							
22.15	Interrupt output enable	Disable interrupt output	Enable interrupt output				
22.14	Interrupt flag read clear enable	Interrupt flag clear by read disable	Interrupt flag clear by read enable				
22.13	Interrupt polarity	Output low when interrupt occur	Output high when interrupt occur				
22.12	Interrupt flag auto clear enable	Interrupt flag unchanged when interrupt condition removed	Interrupt flag cleared when interrupt condition removed				
22.11	Interrupt flag re-setup enable	Interrupt flag always cleared when write 1 to flag bit	Interrupt flag keep unchanged when interrupt condition exist when write 1 to flag bit.				
22.10	Interrupt Enable	Disable Deep power down wake up Interrupt	Enable Deep power down wake up Interrupt				
22.9	Interrupt Enable	Disable Deep power down Interrupt	Enable Deep power down Interrupt				
22.8	Interrupt Enable	Disable Auto-Negotiation Complete Interrupt	Enable Auto-Negotiation Complete Interrupt				
22.7	Interrupt Enable	Disable Jabber Interrupt	Enable Jabber Interrupt				
22.6	Interrupt Enable	Disable Receive Error Interrup	Enable Receive Error Interrupt				
22.5	Interrupt Enable	Disable Page Received Interrupt	Enable Page Received Interrupt				
22.4	Interrupt Enable	Disable Parallel Detect Fault Interrupt	Enable Parallel Detect Fault Interrupt				
22.3	Interrupt Enable	Disable Link Partner Acknowledge	Enable Link Partner Acknowledge Interrupt				
22.2	Interrupt Enable	Disable Link Down Interrupt	Enable Link Down Interrupt				
22.1	Interrupt	Disable Remote Fault Interrupt	Enable Remote Fault Interrupt				
22.0	Enable	Disable Link Up Interrupt	Enable Link Up Interrupt				
Register 23h - Extended Control Register							
23.15:11	Reserved	Reserved		RO			0
23.10	Deep power down wake up Interrupt	Deep power down wake up did not occurred	Deep power down wake up occurred	RO/SC			0
23.9	Deep power down Interrupt	Deep power down did not occurred	Deep power down occurred	RO/SC			0

Bit	Definition	When Bit = 0	When Bit = 1	Access	SF	Default	Hex
23.8	Auto-Negotiation Interrupt	Auto-Negotiation Complete did not occurred	Auto-Negotiation Complete occurred	RO/SC			0
23.7	Jabber Interrupt	Jabber did not occurred	Jabber occurred	RO/SC			0
23.6	Receive Error Interrupt	Receive Error did not occurred	Receive Error occurred	RO/SC			0
23.5	Page Receive Interrupt	Page Receive did not occurred	Page Receive occurred	RO/SC			0
23.4	Parallel Detect Fault Interrupt	Parallel Detect Fault did not occurred	Parallel Detect Fault occurred	RO/SC			0
23.3	Link Partner Acknowledge Interrupt	Link Partner Acknowledge did not occurred	Link Partner Acknowledge occurred	RO/SC			0
23.2	Link Down Interrupt	Link Down did not occurred	Link Down occurred	RO/SC			0
23.1	Remote Fault Interrupt	Remote Fault did not occurred	Remote Fault occurred	RO/SC			0
23.0	Link Up Interrupt	Link Up did not occurred	Link Up occurred	RO/SC			0
Register 24h - Extended Control Register							
24.15:12	FIFO Half	RMII FIFO half full bits ((n+3)*2 bit), RMII		RW			2
24.11:9	Reserved	Reserved		RW			0
24.8	Deep Power down enable	Deep power down(DPD) disable	Deep power down(DPD) enable	RW			0
24.7	Tp1l10_100 DPD Enable	Don't power down 10/100 PLL in DPD mode	Controlled auto power down10/100 PLL in DPD mode	RW			0
24.6	RX 100 DPD Enable	Don't power down RX block in DPD mode	Controlled auto power down of RX block in DPD mode	RW			0
24.5	Admix_TX DPD Enable	Don't power down admix_dac block in DPD mode	Control auto power down of admix_dac block in DPD mode	RW			0
24.4	Cdr100_cdr DPD Enable	don't power down in DPD mod	Control auto power down of CDR block in DPD mode	RW			0
24.3:0	Reserved	Reserved					0
Register 25h - Extended Control Register							
25.15:11	Reserved	Analog control bits		RW			0
25.10	ADD_BIAS	Disable	Enable	RW			1

Bit	Definition	When Bit = 0	When Bit = 1	Access	SF	Default	Hex
25.9:7	TX10BIAS_SET	The normal output current of Bias block for 10BaseT is 540uA. Change the register can modify the current with a step about 5% 000: output 80% current 001: output 85% current 010: output 90% current 011: output 95% current 100: output 100% current 101: output 105% current 110: output 110% current 111: output 115% current		RW			4
25.6:4	TX100BIAS_SET	The normal output current of Bias block for 100BaseTX is 180uA. Change the register can modify the current with a step about 5% 000: output 80% current 001: output 85% current 010: output 90% current 011: output 95% current 100: output 100% current 101: output 105% current 110: output 110% current 111: output 115% current		RW			4
25.3:2	OUTDLY_CTL	This register setting the delay time of digital control signal for xmit_dac. Increase the setting value can short the delay time. 00: the longest delay time (same as original design) 01: the long delay time 10: the short delay time 11: the shortest delay time		RW			0
25.1:0	RX_SET	The output current of Bias block for RX block is 108uA. The register can change the current with a step about 16.5% 00: output 83.5% current 01: output 100% current 10: output 116.5% current 11: output 133% current Change this value may modify the RX block performance.		RW			1
Register 26-31h - Reserved							

Note: 1 Ignored if Auto negotiation is enable

DC and AC Operating Conditions

Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the ICS1894-40. These ratings, which are standard values for ICS commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

Parameter	Rating
VDD (measured to VSS)	-0.3 V to 3.6V
Digital Inputs / Outputs	-0.3 V to VDD +0.3 V
Storage Temperature	-55° C to +150° C
Junction Temperature	125° C
Soldering Temperature	260° C
Power Dissipation	See section "DC Operating Conditions for Supply Current"

Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Units
Ambient Operating Temperature - Commercial	T _A	0	+70	°C
Ambient Operating Temperature - Industrial	T _A	-40	+85	°C
Power Supply Voltage (measured to VSS)	VDD	+3.14	+3.47	V

Recommended Component Values

Parameter	Minimum	Typical	Maximum	Tolerance	Units
Oscillator Frequency	–	25	–	±50 ppm †	MHz
TCSR Resistor Value	–	1.8k See figure <i>ICS1893CK-40</i> <i>TCSR</i>	–	1%	Ω
LED Resistor Value	510	1k	10k	–	Ω

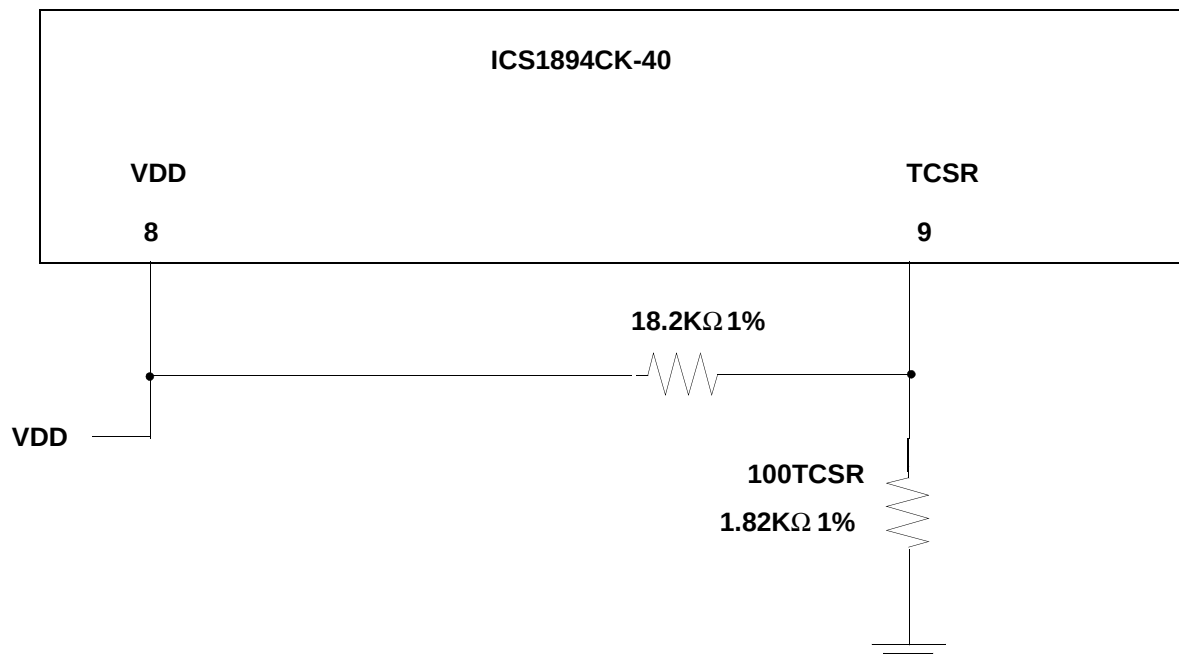
† There are two IEEE Std. 802.3 requirements that define the tolerance for the frequency of the oscillator.

- Clause 22.2.2.1 requires the MII TX_CLK to have an accuracy of ± 100 ppm.
- Clause 24.2.3.4 is more stringent. It requires the code-bit timer to have an accuracy of 0.005% (that is, ±50 ppm).

ICS1893CK-40 TCSR

Typical Board Layouts

TCSR Bias Resistors

**Note:**

1. The bias resistor networks set the 10baseT and 100baseTX output amplitude levels.
2. Amplitude is directly related to current sourced out of the TCSR pin.
3. Resistor values shown above are typical. User should check amplitudes and adjust for transformer effects.
4. The VDD connection to the 18.2K resistor can connect to any VDD. The 18.2K resistor provides negative feedback to compensate for VDD changes. Lowering the 18.2K value will lower the 100baseT amplitude.

DC Operating Characteristics for Supply Current

The table below lists the DC operating characteristics for the supply current to the ICS1894-40 under various conditions.

Note: All VDD_IO measurements are taken with respect to VSS (which equals 0 V).

Parameter	Operating Mode	Symbol	Min.	Typ.	Max.	Units
Supply Current†	100Base-TX‡	IDD_IO	–	–	11	mA
		IDD	–	–	125	mA
Supply Current†	10Base-T‡	IDD_IO	–	–	8	mA
		IDD	–	–	160	mA
Supply Current†	Auto-Negotiation	IDD_IO	–	–	8	mA
		IDD	–	–	90	mA
Supply Current†	Power-Down	IDD_IO	–	–	5	mA
		IDD	–	–	5	mA
Supply Current†	Reset	IDD	–	–	11	mA

† These supply current parameters are measured through VDD pins to the ICS1894-40. The supply current parameters include external transformer currents.

‡ Measurements taken with 100% data transmission and the minimum inter-packet gap.

DC Operating Characteristics for TTL Inputs and Outputs

The table below lists the 3.3V DC operating characteristics of the ICS1894-40 TTL inputs and outputs.

Note: All VDD_IO measurements are taken with respect to VSS (which equals 0 V).

Parameter	Symbol	Conditions		Min.	Max.	Units
TTL Input High Voltage	V _{IH}	VDD_IO = 3.47 V	–	2.0	–	V
TTL Input Low Voltage	V _{IL}	VDD_IO = 3.47 V	–	–	0.8	V
TTL Output High Voltage	V _{OH}	VDD_IO = 3.14 V	I _{OH} = –4 mA	2.4	–	V
TTL Output Low Voltage	V _{OL}	VDD_IO = 3.14 V	I _{OL} = +4 mA	–	0.4	V
TTL Driving CMOS, Output High Voltage	V _{OH}	VDD_IO = 3.14 V	I _{OH} = –4 mA	2.4	–	V
TTL Driving CMOS, Output Low Voltage	V _{OL}	VDD_IO = 3.14 V	I _{OL} = +4 mA	–	0.4	V

Parameter	Symbol	Conditions		Min.	Max.	Units
TTL Input High Voltage	V _{IH}	VDD_IO = 1.8V	–		–	V
TTL Input Low Voltage	V _{IL}	VDD_IO = 1.8V	–	–		V
TTL Output High Voltage	V _{OH}	VDD_IO = 1.8V	I _{OH} = –4 mA		–	V
TTL Output Low Voltage	V _{OL}	VDD_IO = 1.8V	I _{OL} = +4 mA	–		V
TTL Driving CMOS, Output High Voltage	V _{OH}	VDD_IO = 1.8V	I _{OH} = –4 mA		–	V
TTL Driving CMOS, Output Low Voltage	V _{OL}	VDD_IO = 1.8V	I _{OL} = +4 mA	–		V

DC Operating Characteristics for REF_IN

The table below lists the 3.3V DC characteristics for the REF_IN pin.

Note: The REF_IN input switch point is 50% of VDD.

Parameter	Symbol	Test Conditions	Min.	Max.	Units
Input High Voltage	V_{IH}	$V_{DD_IO} = 3.47\text{ V}$	2.97	–	V
Input Low Voltage	V_{IL}	$V_{DD_IO} = 3.14\text{ V}$	–	0.33	V

DC Operating Characteristics for Media Independent Interface

The table below lists DC operating characteristics for the Media Independent Interface (MII) for the ICS1894-40.

Parameter	Conditions	Min.	Typ.	Max.	Units
MII Input Pin Capacitance	–	–	–	8	pF
MII Output Pin Capacitance	–	–	–	14	pF
MII Output Drive Impedance	$V_{DD_IO} = 3.3\text{V}$	–	60	–	Ω

Timing Diagrams

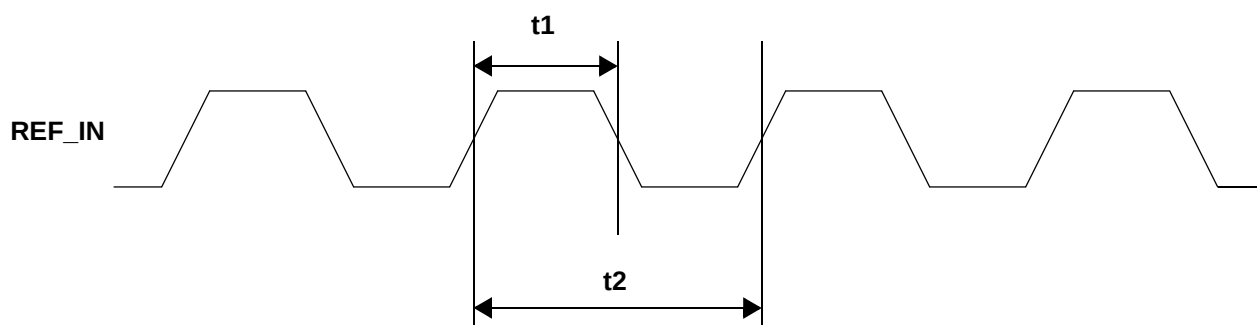
Timing for Clock Reference In (REF_IN) Pin

The table below lists the significant time periods for signals on the clock reference in (REF_IN) pin. The *REF_IN Timing Diagram* figure shows the timing diagram for the time periods.

Note: The REF_IN switching point is 50% of VDD.

Time Period	Parameter	Conditions	Min.	Typ.	Max.	Units
t1	REF_IN Duty Cycle	–	45	50	55	%
t2	REF_IN Period	–	–	40	–	ns

REF_IN Timing Diagram

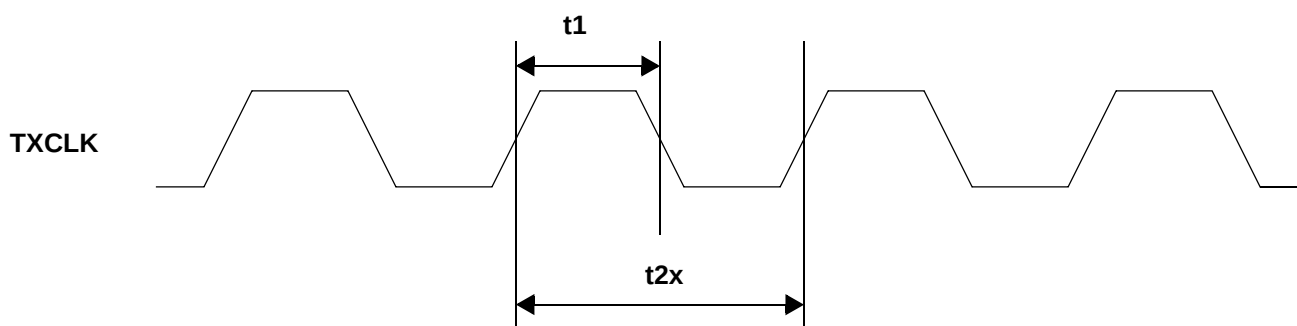


Timing for Transmit Clock (TXCLK) Pins

The table below lists the significant time periods for signals on the Transmit Clock (TXCLK) pins for the various interfaces. The *Transmit Clock Timing Diagram* figure shows the timing diagram for the time periods.

Time Period	Parameter	Conditions	Min.	Typ.	Max.	Units
t1	TXCLK Duty Cycle	–	35	50	65	%
t2a	TXCLK Period	100M MII (100Base-TX)	–	40	–	ns
t2b	TXCLK Period	10M MII (10Base-T)	–	400	–	ns

Transmit Clock Timing Diagram

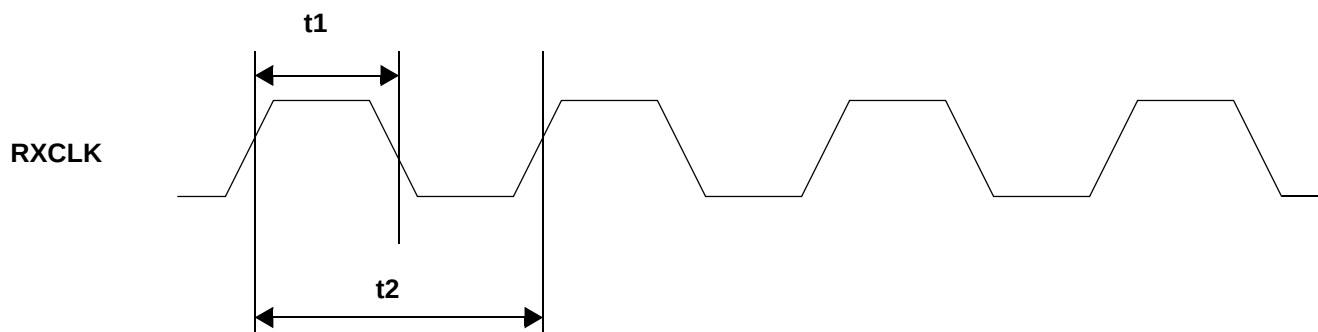


Timing for Receive Clock (RXCLK) Pins

The table below lists the significant time periods for signals on the Receive Clock (RXCLK) pins for the various interfaces. The *Receive Clock Timing Diagram* figure shows the timing diagram for the time periods.

Time Period	Parameter	Conditions	Min.	Typ.	Max.	Units
t1	RXCLK Duty Cycle	–	35	50	65	%
t2a	RXCLK Period	100M MII (100Base-TX)	–	40	–	ns
t2b	RXCLK Period	10M MII (10Base-T)	–	400	–	ns

Receive Clock Timing Diagram



100M MII: Synchronous Transmit Timing

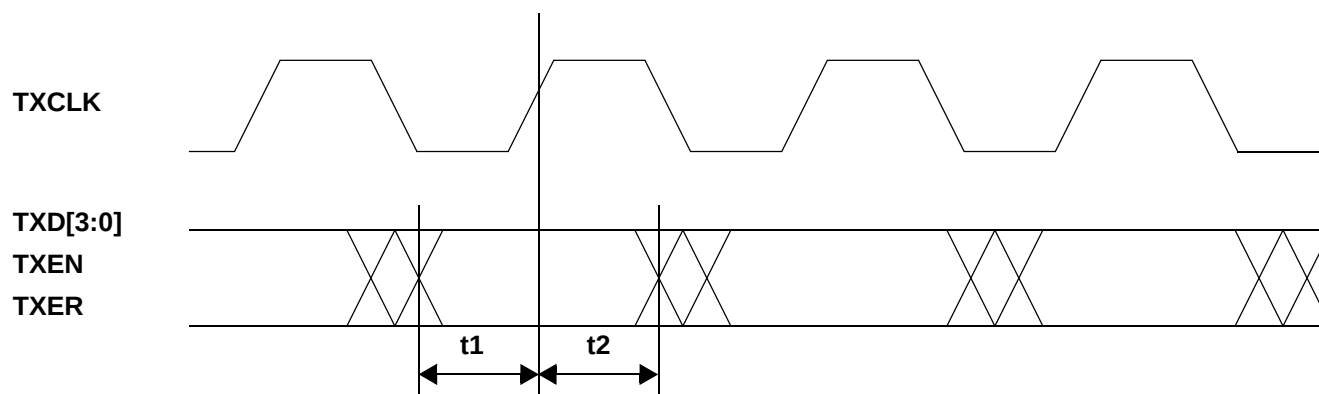
The table below lists the significant time periods for the 100M MII Interface synchronous transmit timing. The time periods consist of timings of signals on the following pins:

- TXCLK
- TXD[3:0]
- TXEN
- TXER

The *100M MII/100M Stream Interface Synchronous Transmit Timing Diagram* figure shows the timing diagram for the time periods.

Time Period	Parameter	Conditions	Min.	Typ.	Max.	Units
t1	TXD[3:0], TXEN, TXER Setup to TXCLK Rise	—	15	—	—	ns
t2	TXD[3:0], TXEN, TXER Hold after TXCLK Rise	—	0	—	—	ns

100M MII/100M Stream Interface Synchronous Transmit Timing Diagram



10M MII: Synchronous Transmit Timing

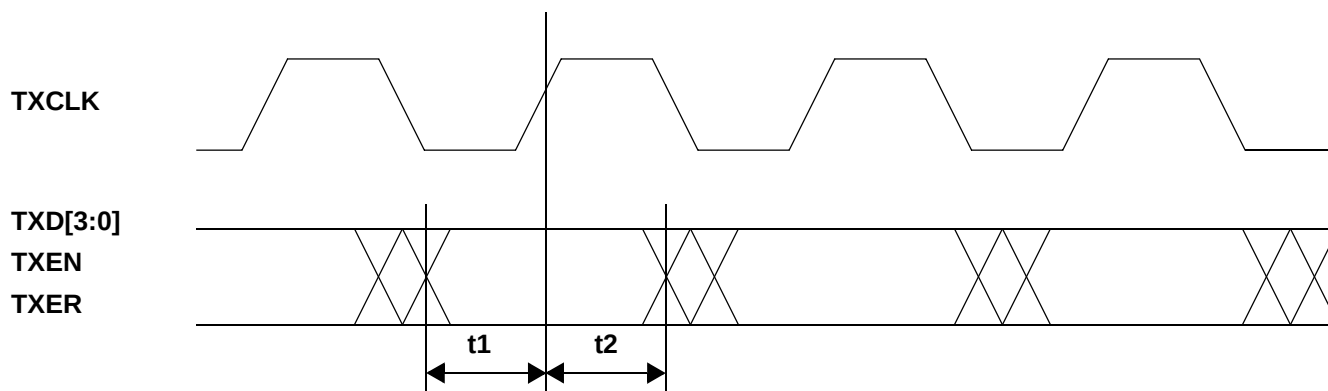
The table below lists the significant time periods for the 10M MII synchronous transmit timing. The time periods consist of timings of signals on the following pins:

- TXCLK
- TXD[3:0]
- TXEN
- TXER

The *10M MII Synchronous Transmit Timing Diagram* figure shows the timing diagram for the time periods.

Time Period	Parameter	Conditions	Min.	Typ.	Max.	Units
t1	TXD[3:0], TXEN, TXER Setup to TXCLK Rise	—	375	—	—	ns
t2	TXD[3:0], TXEN, TXER Hold after TXCLK Rise	—	0	—	—	ns

10M MII Synchronous Transmit Timing Diagram



100M/II Media Independent Interface: Synchronous Receive Timing

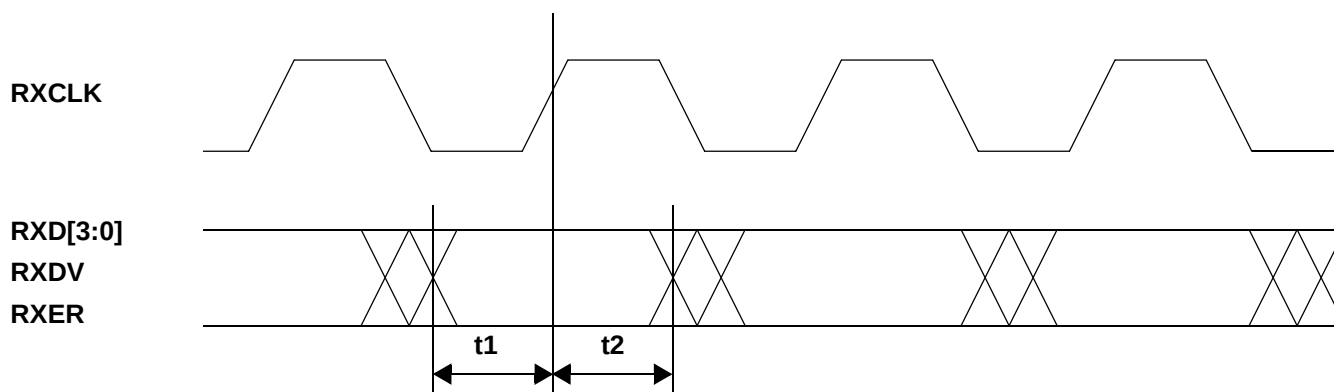
The table below lists the significant time periods for the MII/100M Stream Interface synchronous receive timing. The time periods consist of timings of signals on the following pins:

- RXCLK
- RXD[3:0]
- RXDV
- RXER

The *MII Interface: Synchronous Receive Timing* figure shows the timing diagram for the time periods.

Time Period	Parameter	Min.	Typ.	Max.	Units
t1	RXD[3:0], RXDV, and RXER Setup to RXCLK Rise	10.0	–	–	ns
t2	RXD[3:0], RXDV, and RXER Hold after RXCLK Rise	10.0	–	–	ns

MII Interface: Synchronous Receive Timing



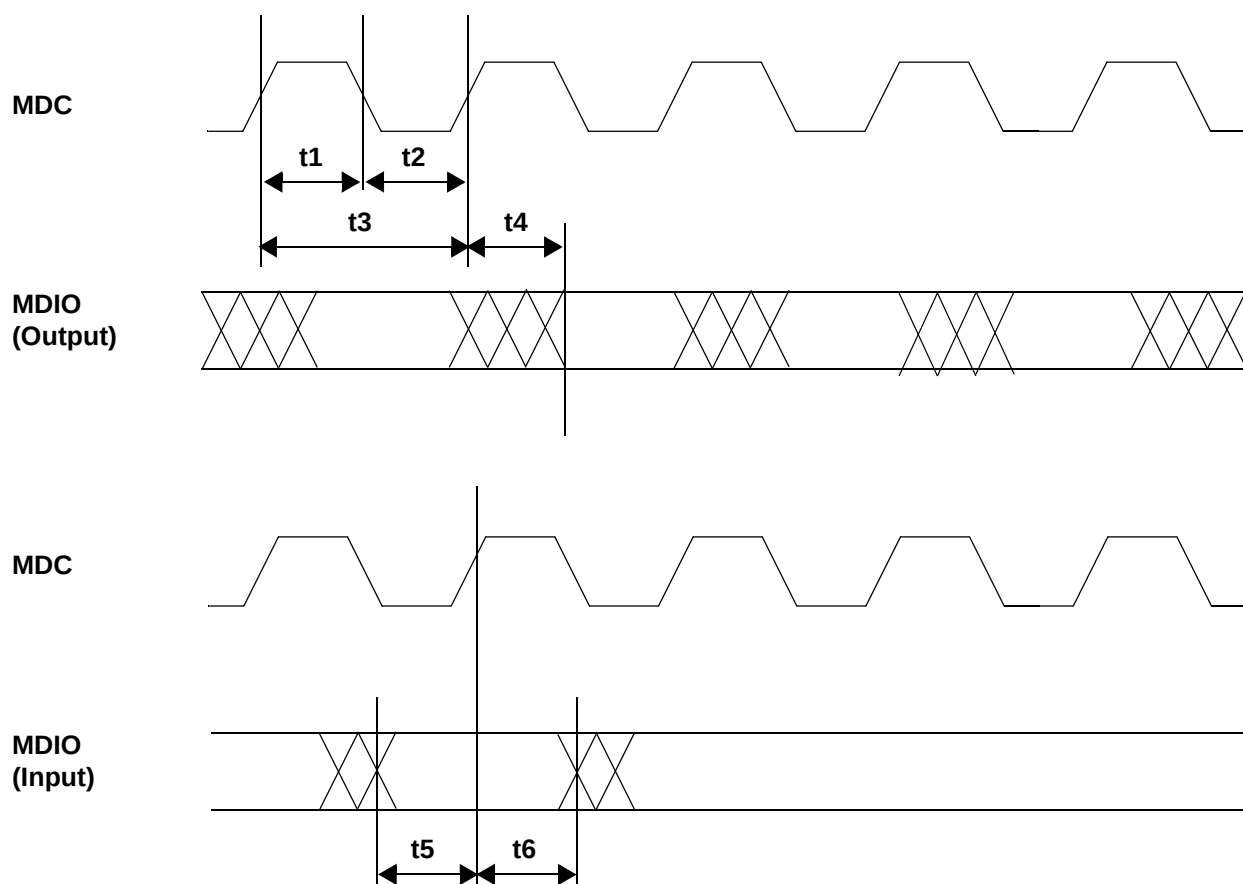
MII Management Interface Timing

The table below lists the significant time periods for the MII Management Interface timing (which consists of timings of signals on the MDC and MDIO pins). The *MII Management Interface Timing Diagram* figure shows the timing diagram for the time periods.

Time Period	Parameter	Conditions	Min.	Typ.	Max.	Units
t1	MDC Minimum High Time	–	160	–	–	ns
t2	MDC Minimum Low Time	–	160	–	–	ns
t3	MDC Period	–	400†	†	–	ns
t4	MDC Rise Time to MDIO Valid	–	0	–	300	ns
t5	MDIO Setup Time to MDC	–	10	–	–	ns
t6	MDIO Hold Time after MDC	–	10	–	–	ns

†The ICS1894-40 is tested at 25 MHz (a 40ns period) with a 50pF load. Designs must account for all board loading of MDC.

MII Management Interface Timing Diagram



10M Media Independent Interface: Receive Latency

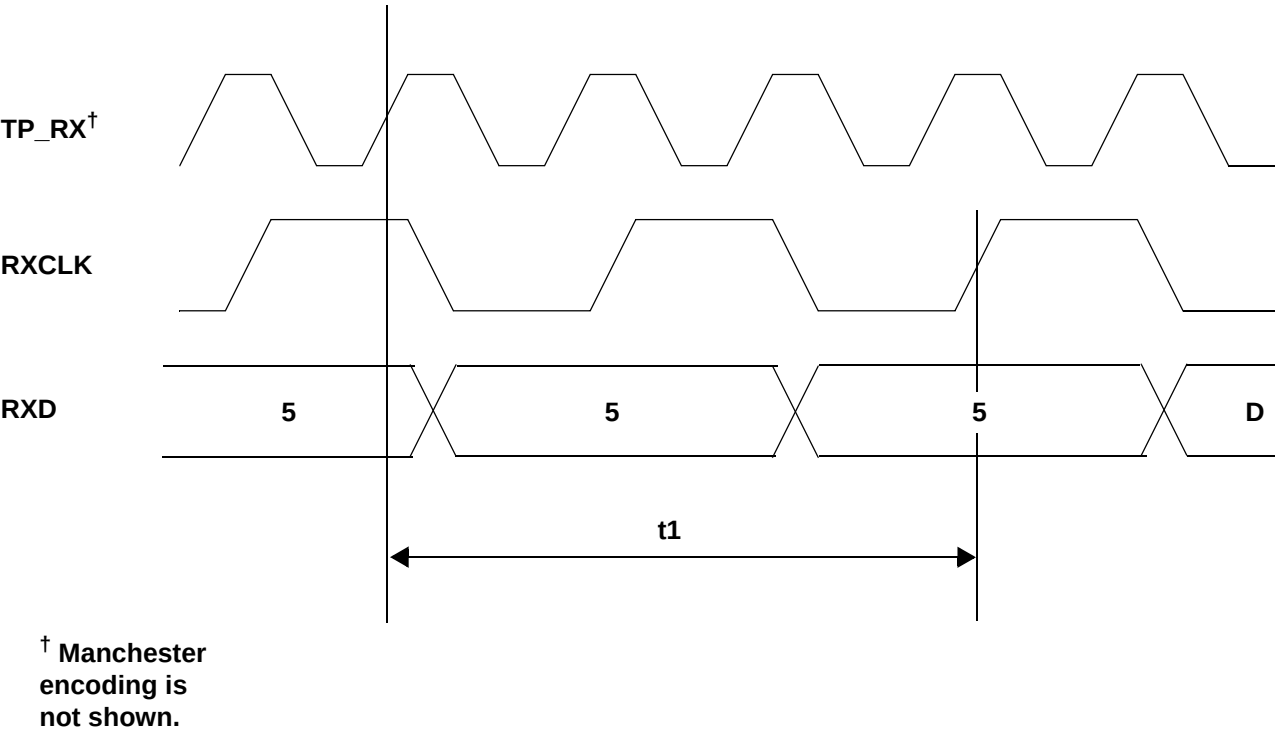
The table below lists the significant time periods for the 10M MII timing. The time periods consist of timings of signals on the following pins:

- TP_RX (that is, the MII TP_RXP and TP_RXN pins)
- RXCLK
- RXD

The *10M MII Receive Latency Timing Diagram* shows the timing diagram for the time periods.

Time Period	Parameter	Conditions	Min.	Typ.	Max.	Units
t1	First Bit of /5/ on TP_RX to /5/D/ on RXD	10M MII	–	6.5	7	Bit times

10M MII Receive Latency Timing Diagram



10M Media Independent Interface: Transmit Latency

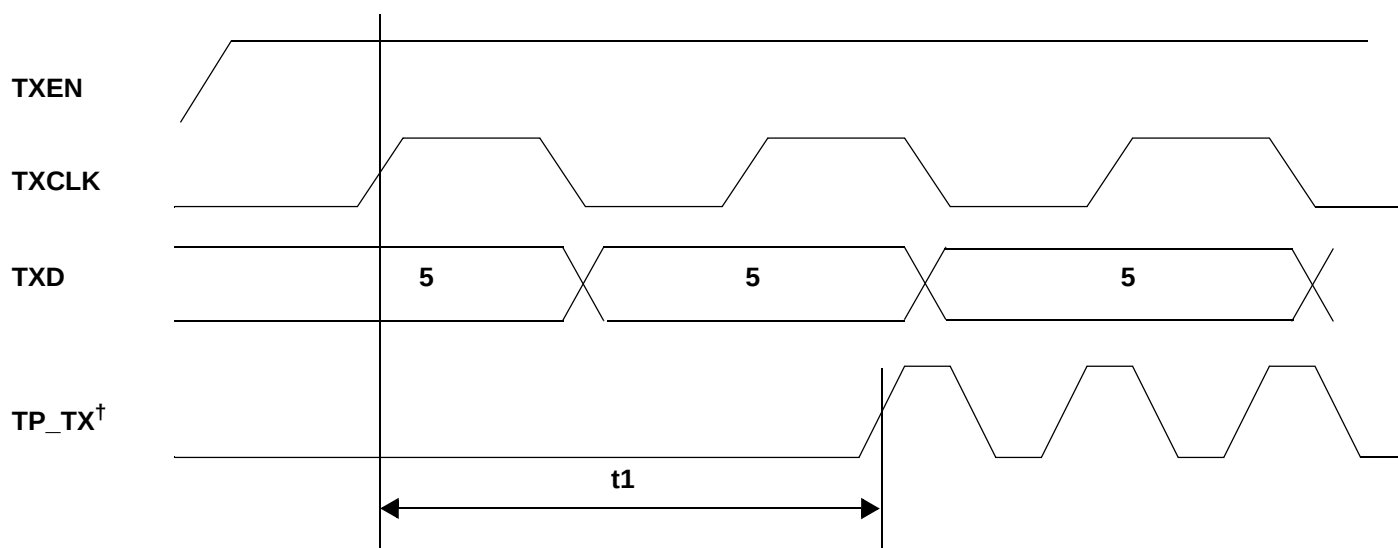
The table below lists the significant time periods for the 10M MII transmit latency. The time periods consist of timings of signals on the following pins:

- TXEN
- TXCLK
- TXD (that is, TXD[3:0])
- TP_TX (that is, TP_TXP and TP_TXN)

The *10M MII Transmit Latency Timing Diagram* shows the timing diagram for the time periods.

Time Period	Parameter	Conditions	Min.	Typ.	Max.	Units
t1	TXD Sampled to MDI Output of First Bit	10M MII	–	1.2	2	Bit times

10M MII Transmit Latency Timing Diagram



† Manchester encoding is not shown.

100M / MII Media Independent Interface: Transmit Latency

The table below lists the significant time periods for the MII/100 Stream Interface transmit latency. The time periods consist of timings of signals on the following pins:

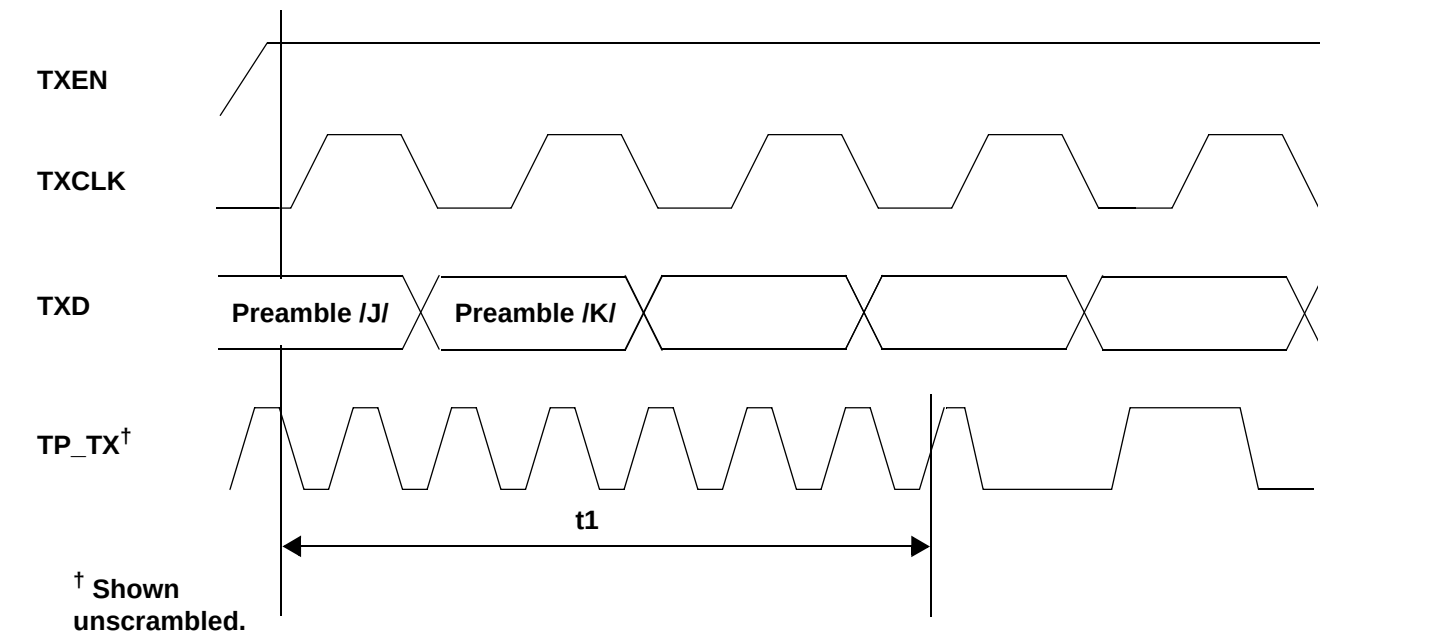
- TXEN
- TXCLK
- TXD (that is, TXD[3:0])
- TP_TX (that is, TP_TXP and TP_TXN)

The *MII/100M Stream Interface Transmit Latency Timing Diagram* shows the timing diagram for the time periods.

Time Period	Parameter	Conditions	Min.	Typ.	Max.	Units
t1	TXEN Sampled to MDI Output of First Bit of /J/ †	MII mode	–	2.8	3	Bit times

† The IEEE maximum is 18 bit times.

MII/100M Stream Interface Transmit Latency Timing Diagram



100M MII: Carrier Assertion/De-Assertion (Half-Duplex Transmission)

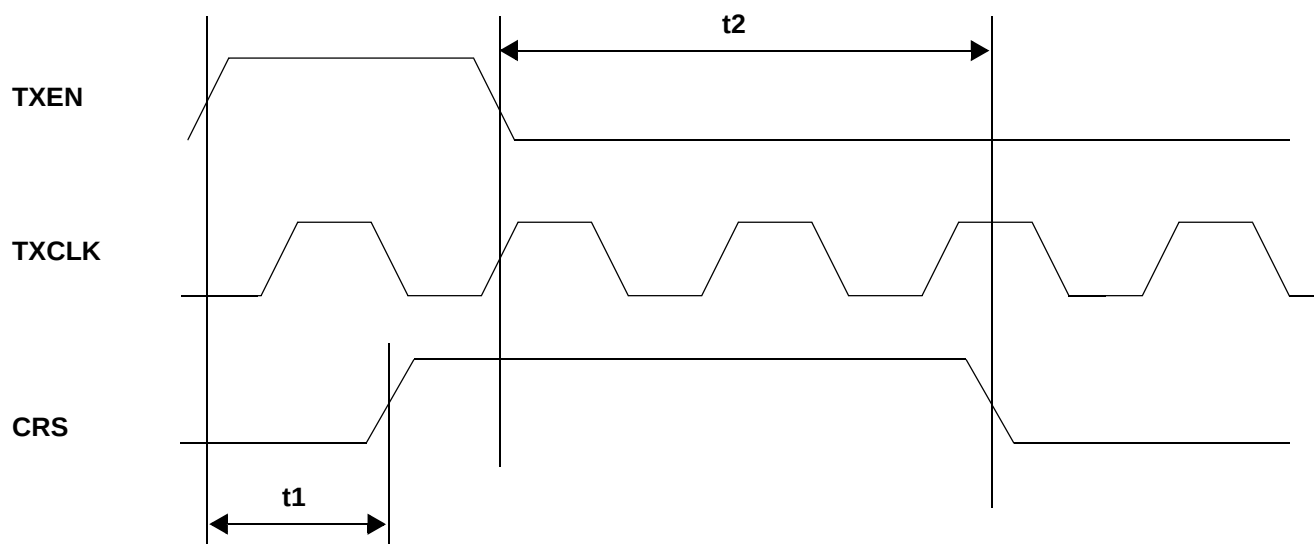
The table below lists the significant time periods for the 100M MII carrier assertion/de-assertion during half-duplex transmission. The time periods consist of timings of signals on the following pins:

- TXEN
- TXCLK
- CRS

The *100M MII Carrier Assertion/De-Assertion Timing Diagram (Half-Duplex Transmission Only)* shows the timing diagram for the time periods.

Time Period	Parameter	Conditions	Min.	Typ.	Max.	Units
t1	TXEN Sampled Asserted to CRS Assert		0	3	4	Bit times
t2	TXEN De-Asserted to CRS De-Asserted		0	3	4	Bit times

100M MII Carrier Assertion/De-Assertion Timing Diagram (Half-Duplex Transmission Only)



10M MII: Carrier Assertion/De-Assertion (Half-Duplex Transmission)

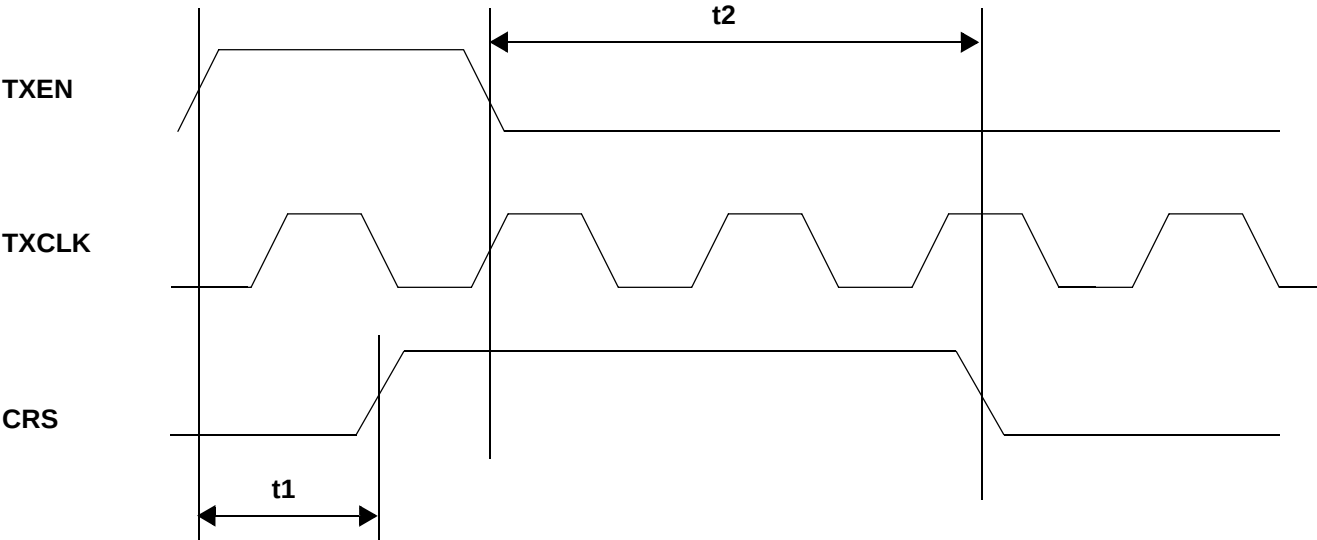
The table below lists the significant time periods for the 10M MII carrier assertion/de-assertion during half-duplex transmission. The time periods consist of timings of signals on the following pins:

- TXEN
- TXCLK
- CRS

The *10M MII Carrier Assertion/De-Assertion Timing Diagram (Half-Duplex Transmission Only)* shows the timing diagram for the time periods.

Time Period	Parameter	Conditions	Min.	Typ.	Max.	Units
t1	TXEN Asserted to CRS Assert		0	–	2	Bit times
t2	TXEN De-Asserted to CRS De-Asserted		0	2	4	Bit times

10M MII Carrier Assertion/De-Assertion Timing Diagram (Half-Duplex Transmission Only)



100M MII Media Independent Interface: Receive Latency

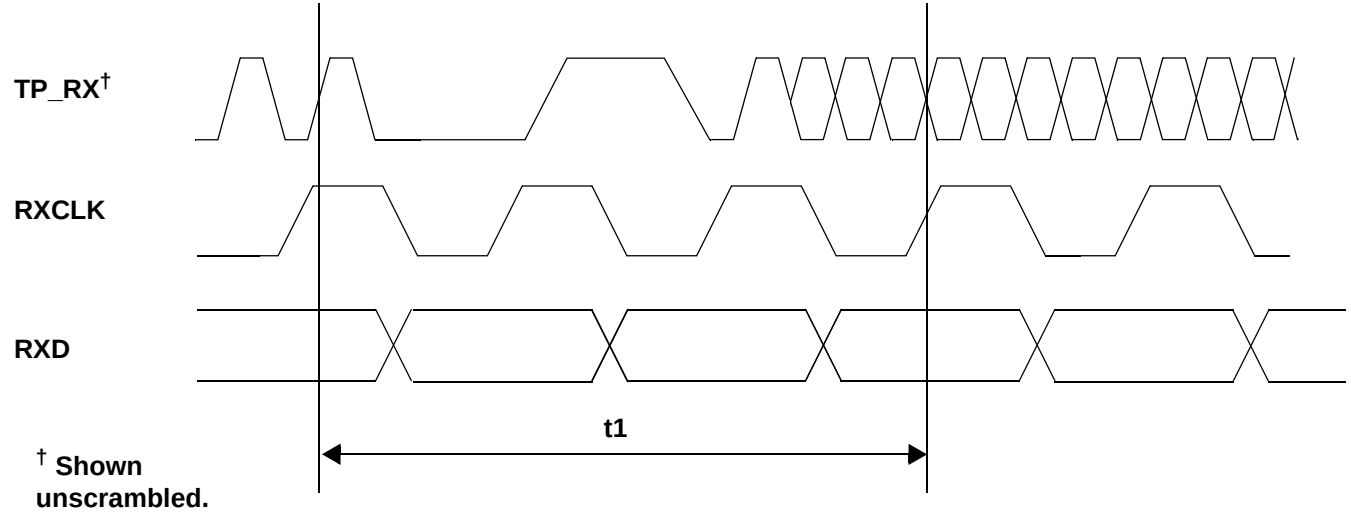
The table below lists the significant time periods for the 100M MII/100M Stream Interface receive latency. The time periods consist of timings of signals on the following pins:

- TP_RX (that is, TP_RXP and TP_RXN)
- RXCLK
- RXD (that is, RXD[3:0])

The *100M MII/100M Stream Interface: Receive Latency Timing Diagram* shows the timing diagram for the time periods.

Time Period	Parameter	Conditions	Min.	Typ.	Max.	Units
t1	First Bit of /J/ into TP_RX to /J/ on RXD	100M MII	–	16	17	Bit times

100M MII/100M Stream Interface: Receive Latency Timing Diagram



100M Media Independent Interface: Input-to-Carrier Assertion/De-Assertion

The table below lists the significant time periods for the 100M MDI input-to-carrier assertion/de-assertion. The time periods consist of timings of signals on the following pins:

- TP_RX (that is, TP_RXP and TP_RXN)
- CRS
- COL

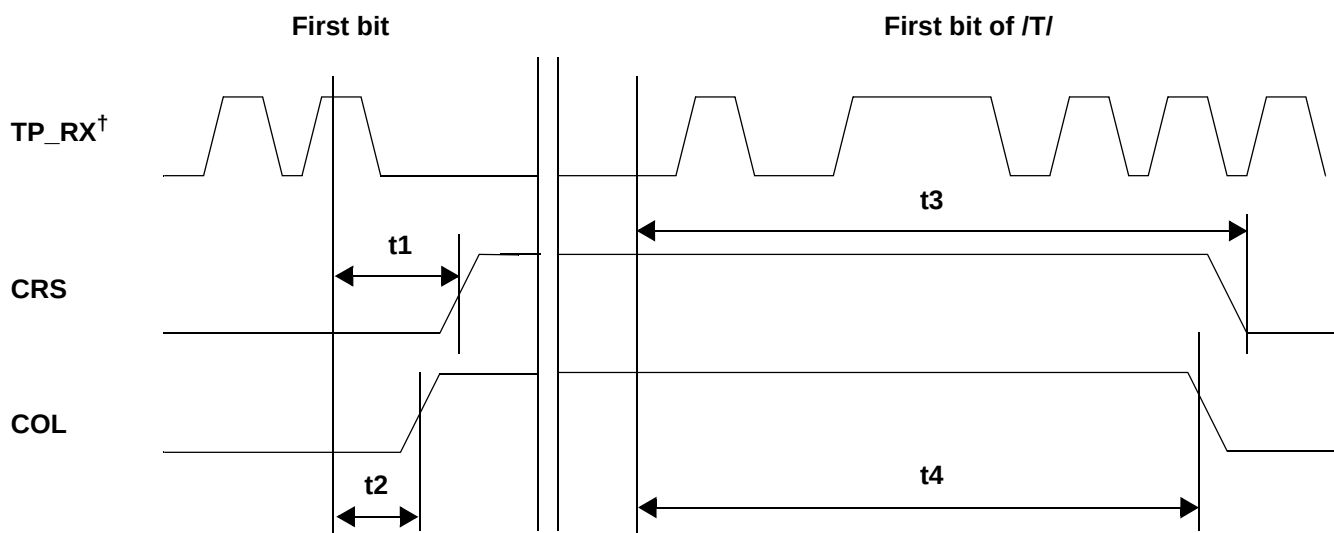
The *100M MDI Input to Carrier Assertion/De-Assertion Timing Diagram* shows the timing diagram for the time periods.

Time Period	Parameter	Conditions	Min.	Typ.	Max.	Units
t1	First Bit of /J/ into TP_RX to CRS Assert †	–	10	–	14	Bit times
t2	First Bit of /J/ into TP_RX while Transmitting Data to COL Assert †	Half-Duplex Mode	9	–	13	Bit times
t3	First Bit of /T/ into TP_RX to CRS De-Assert ‡	–	13	–	18	Bit times
t4	First Bit of /T/ Received into TP_RX to COL De-Assert ‡	Half-Duplex Mode	13	–	18	Bit times

† The IEEE maximum is 20 bit times.

‡ The IEEE minimum is 13 bit times, and the maximum is 24 bit times.

100M MDI Input to Carrier Assertion/De-Assertion Timing Diagram



† Shown unscrambled.

Reset: Power-On Reset

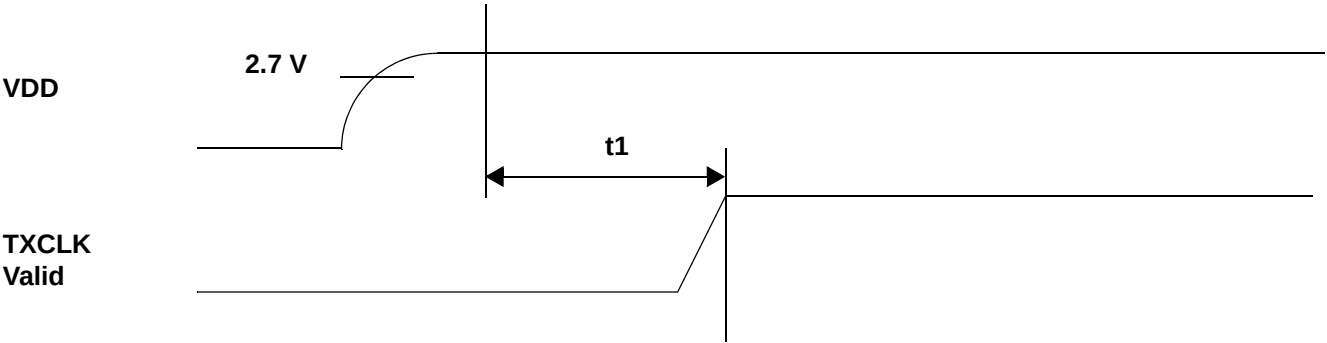
The table below lists the significant time periods for the power-on reset. The time periods consist of timings of signals on the following pins:

- VDD
- TXCLK

The *Power-On Reset Timing Diagram* shows the timing diagram for the time periods.

Time Period	Parameter	Conditions	Min.	Typ.	Max.	Units
t1	VDD ≥ 2.7 V to Reset Complete	–	40	45	500	ms

Power-On Reset Timing Diagram



Reset: Hardware Reset and Power-Down

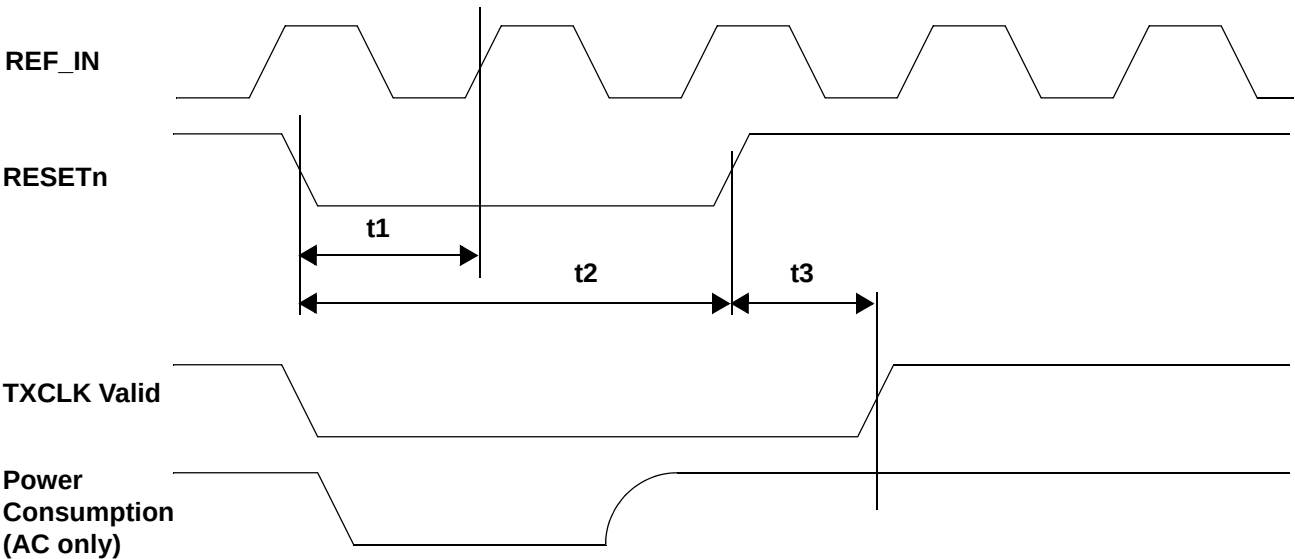
The table below lists the significant time periods for the hardware reset and power-down reset. The time periods consist of timings of signals on the following pins:

- REF_IN
- RESETn
- TXCLK

The *Hardware Reset and Power-Down Timing Diagram* shows the timing diagram for the time periods.

Time Period	Parameter	Conditions	Min.	Typ.	Max	Units
t1	RESETn Active to Device Isolation and Initialization	–	–	60	–	ns
t2	Minimum RESETn Pulse Width	–	200		–	ns
t3	RESETn Released to TXCLK Valid	–	–	35	500	ms

Hardware Reset and Power-Down Timing Diagram



10Base-T: Heartbeat Timing (SQE)

The table below lists the significant time periods for the 10Base-T heartbeat (that is, the Signal Quality Error). The time periods consist of timings of signals on the following pins:

- TXEN
- TXCLK
- COL

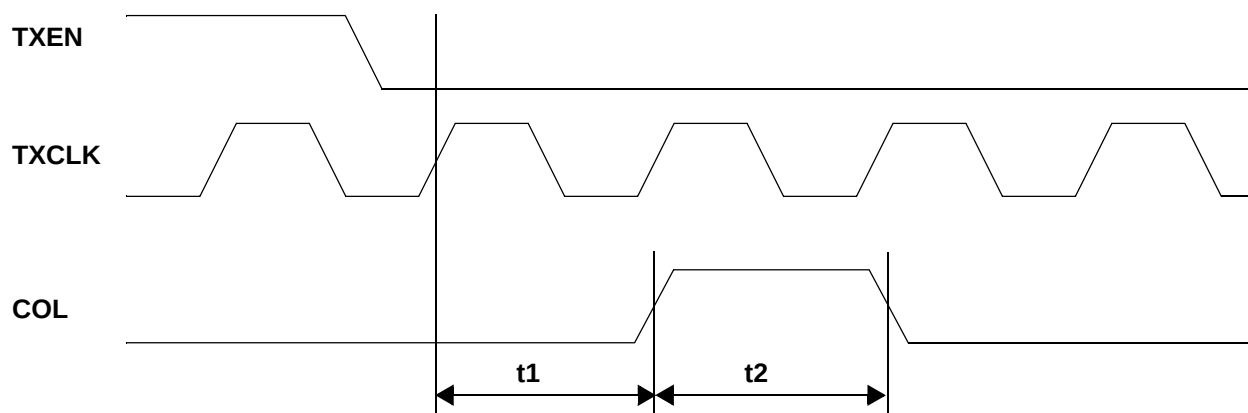
The *10Base-T Heartbeat (SQE) Timing Diagram* shows the timing diagram for the time periods.

Note:

1. For more information on 10Base-T SQE operations, see the section “10Base-T Operation: SQE Test”.
2. In 10Base-T mode, one bit time = 100 ns.

Time Period	Parameter	Conditions	Min.	Typ.	Max.	Units
t1	COL Heartbeat Assertion Delay from TXEN De-Assertion	10Base-T Half Duplex	–	850	1500	ns
t2	COL Heartbeat Assertion Duration	10Base-T Half Duplex	–	1000	1500	ns

10Base-T Heartbeat (SQE) Timing Diagram



10Base-T: Jabber Timing

The table below lists the significant time periods for the 10Base-T jabber. The time periods consist of timings of signals on the following pins:

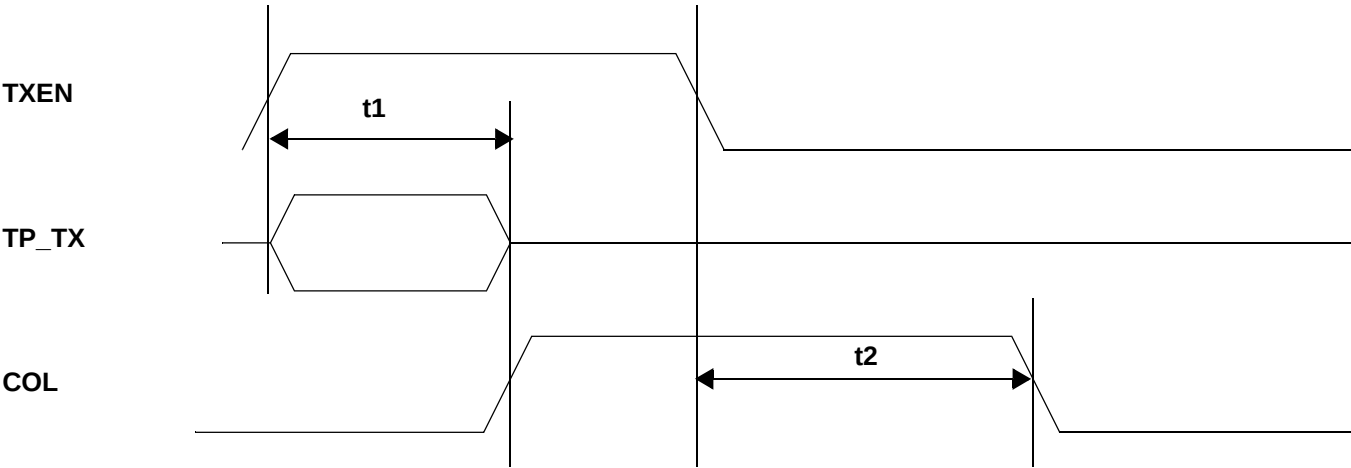
- TXEN
- TP_TX (that is, TP_TXP and TP_TXN)
- COL

The *10Base-T Jabber Timing Diagram* shows the timing diagram for the time periods.

Note: For more information on 10Base-T jabber operations, see the section, “10Base-T Operation: Jabber”.

Time Period	Parameter	Conditions	Min.	Typ.	Max.	Units
t1	Jabber Activation Time	10Base-T Half Duplex	20	–	35	ms
t2	Jabber De-Activation Time	10Base-T Half Duplex	300	–	325	ms

10Base-T Jabber Timing Diagram

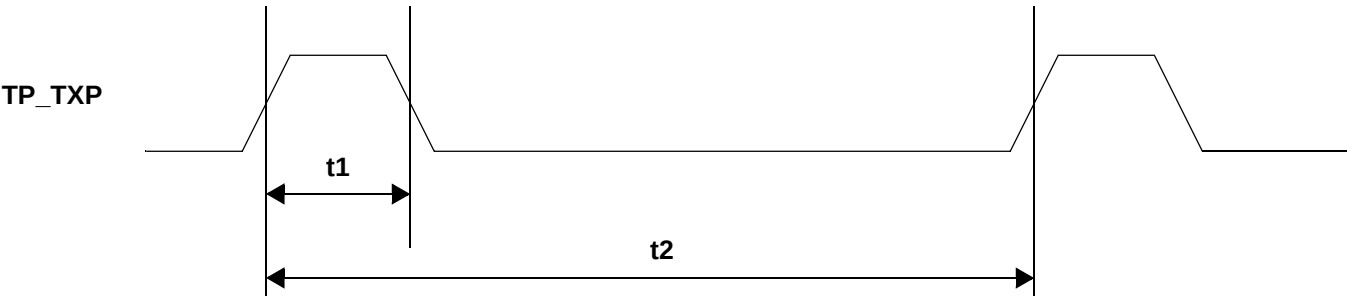


10Base-T: Normal Link Pulse Timing

The table below lists the significant time periods for the 10Base-T Normal Link Pulse (which consists of timings of signals on the TP_TXP pins). The *10Base-T Normal Link Pulse Timing Diagram* shows the timing diagram for the time periods.

Time Period	Parameter	Conditions	Min.	Typ.	Max.	Units
t1	Normal Link Pulse Width	10Base-T	–	100	–	ns
t2	Normal Link Pulse to Normal Link Pulse Period	10Base-T	8	20	25	ms

10Base-T Normal Link Pulse Timing Diagram



Auto-Negotiation Fast Link Pulse Timing

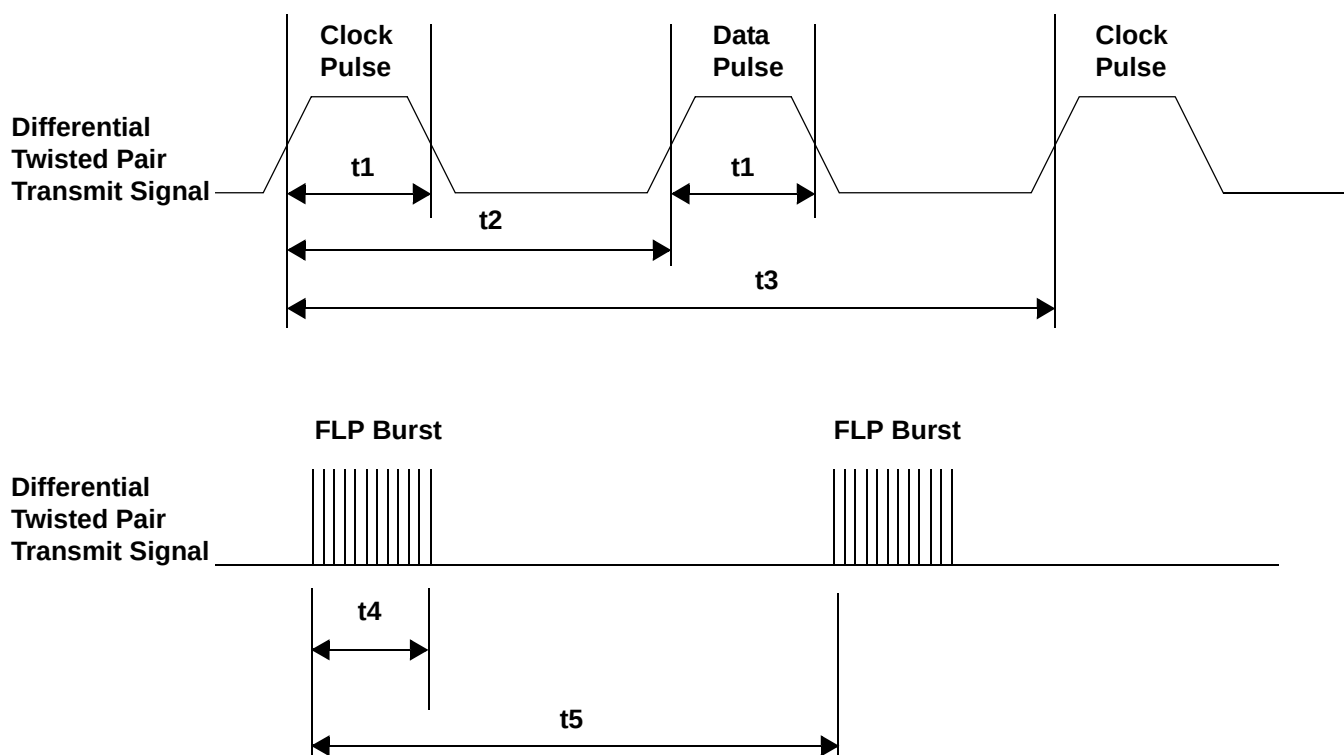
The table below lists the significant time periods for the ICS1894-40 Auto-Negotiation Fast Link Pulse. The time periods consist of timings of signals on the following pins:

- TP_TXP
- TP_TXN

The *Auto-Negotiation Fast Link Pulse Timing Diagram* shows the timing diagram for one pair of these differential signals, for example TP_TXP minus TP_TXN.

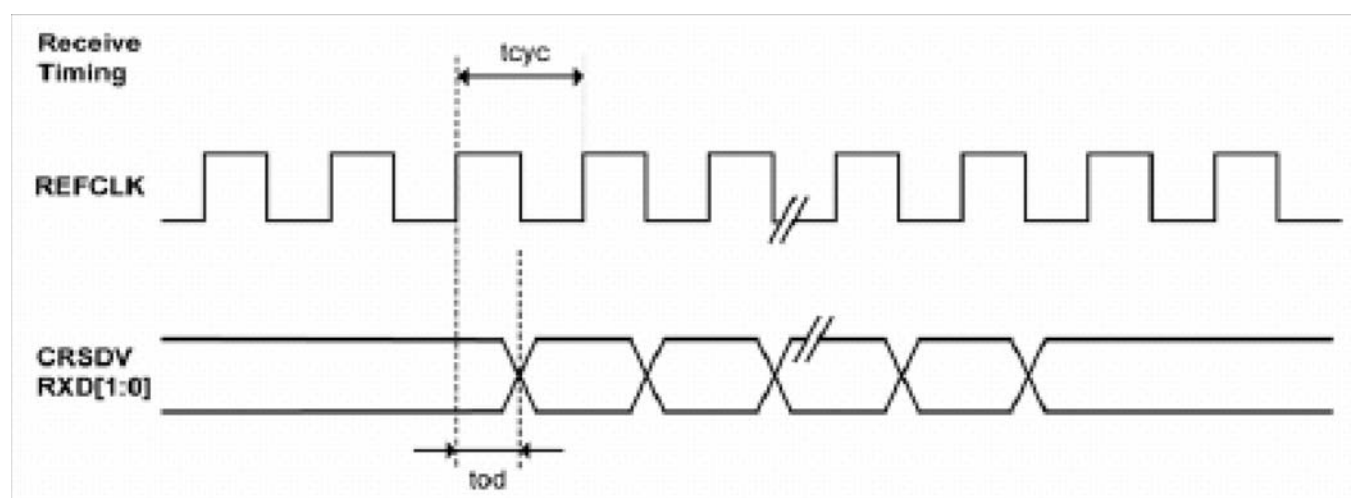
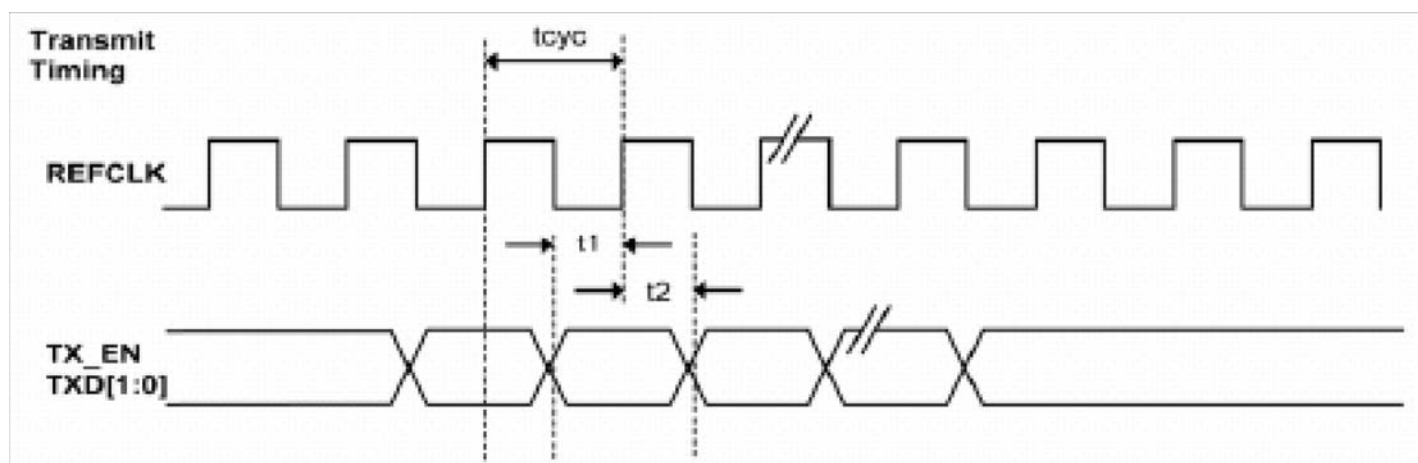
Time Period	Parameter	Conditions	Min.	Typ.	Max.	Units
t1	Clock/Data Pulse Width	—	—	90	—	ns
t2	Clock Pulse-to-Data Pulse Timing	—	55	60	70	μs
t3	Clock Pulse-to-Clock Pulse Timing	—	110	125	140	μs
t4	Fast Link Pulse Burst Width	—	—	5	—	ms
t5	Fast Link Pulse Burst to Fast Link Pulse Burst	—	10	15	25	ms
t6	Number of Clock/Data Pulses in a Burst	—	15	20	30	pulses

Auto-Negotiation Fast Link Pulse Timing Diagram



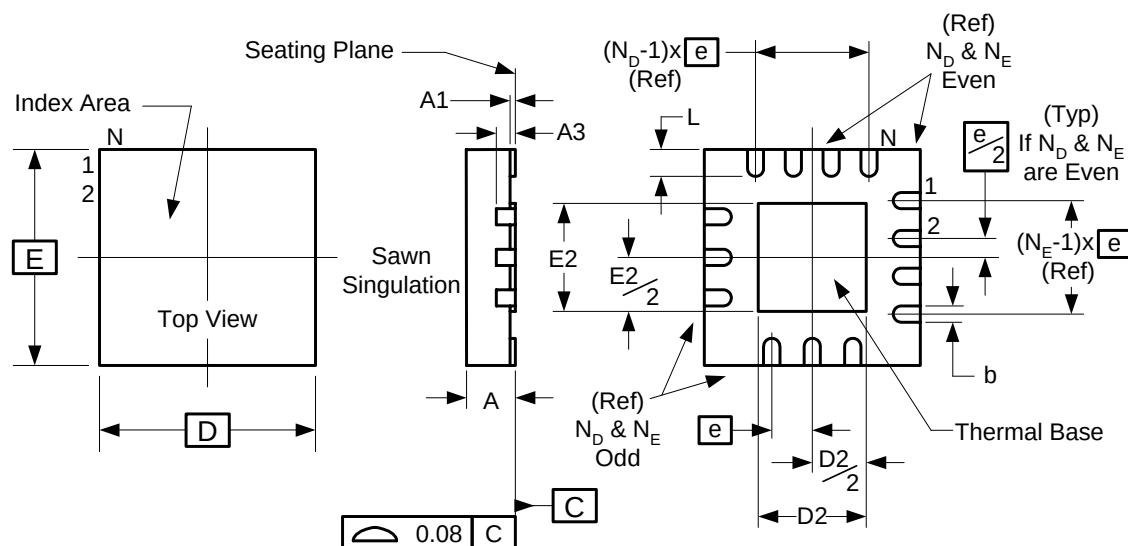
RMII Timing

Time Param	Description	Min.	Typ.	Max.	Units
t_{cyc}	Clock Cycle	–	20		ns
t_1	Setup time	4			ns
t_2	Hold time	2			ns
t_{OD}	Output delay	2.8		10	ns



Package Outline and Package Dimensions (40-pin 6mm x 6mm QFN)

Package dimensions are kept current with JEDEC Publication No. 95



Symbol	Millimeters	
	Min	Max
A	0.80	1.00
A1	0	0.05
A3	0.25 Reference	
b	0.18	0.30
e	0.50 BASIC	
N	40	
N _D	10	
N _E	10	
D x E BASIC	6.00 x 6.00	
D2	1.75	4.80
E2	1.75	4.80
L	0.30	0.50

Ordering Information

Part / Order Number	Marking	Shipping Packaging	Package	Temperature
1894-40KLF	TBD	Tubes	40-pin QFN	0 to +70° C
1894-40KLFT		Tape and Reel	40-pin QFN	0 to +70° C

"LF" after the two-letter package code are the Pb-Free configuration and are RoHS compliant.

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