P-Channel Enhancement-Mode Transistor

Characteristics

- P-channel Vertical DMOS
- Macro-Model (Subcircuit)
- Level 3 MOS
- Applicable for Both Linear and Switchmode
- Applicable Over a -55 to 125°C Temperature Range
- Models Gate Charge, Transient, and Diode Reverse Recovery Characteristics

Description

The attached SPICE Model describes typical electrical characteristics of the n-channel vertical DMOS. The subcircuit model was extracted and optimized over a 25°C to 125°C temperature range under pulse conditions for 0 to -10 volt gate drives. Saturated output impedance model accuracy has been maximized for gate biases near threshold. A novel gate-to-drain feedback capacitor network is used to model gate charge characteristics while avoiding convergence problems of switched C_{gd} model. Model parameter values are optimized to provide a best fit to measured electrical data and are not intended as an exact physical description of a device.

Model Subcircuit

Model Evaluation

P-Channel Device (T_J=25°C Unless Otherwise Noted)

Parameter	Symbol	Test Conditions	Typ	Unit
Static				
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = -250µA	**1.62**	V
On-State Drain Current[a]	$I_{D(on)}$	V_{DS} = **-5**V, V_{GS} = **-10**V	**474**	A
		V_{DS} = **-5**V, V_{GS} = **-4.5**V	**76**	
Drain-Source On-State Resistance[a]	$r_{DS(on)}$	V_{GS} = **-10**V, I_D = **-15**A	**0.009**	Ω
		V_{GS} = **-4.5**V, I_D = **-15**A	**0.015**	
		V_{GS} = **-10**V, I_D = **-15**A, Tj = 125C	**0.013**	
Forward Transconductance[a]	g_{fs}	V_{DS} = **-15**V, I_D = **-15**A	**29**	S
Diode Forward Voltage[a]	V_{SD}	I_F = I_S = **-1.6**A, V_{GS} = 0V	**0.8**	V
Dynamic				
Total Gate Charge[b]	Q_g	V_{DS} = **-15**V, V_{GS} = **-10**V, I_D = **-45**A	**92**	nC
Gate-Source Charge[b]	Q_{gs}		**22**	
Gate-Drain Charge[b]	Q_{gd}		**18**	
Turn-On Delay Time[b,c]	$t_{d(on)}$	V_{DD} = **-15**V, R_L = **0.33Ω** I_D ≅ **-45**A, V_{GEN} = **-10**V, R_G = 2.4**Ω**	**69**	ns
Rise Time[b,c]	t_r		**129**	
Turn-Off Delay Time[b,c]	$t_{d(off)}$		**88**	
Fall Time[b,c]	t_f		**46**	
Reverse Recovery Time	t_{rr}	I_F = **-45**A, di/dt = 100A/µs	**54**	

Notes:

a) Pulse test: Pulse Width ≤ 300 µsec, Duty Cycle ≤ 2%.
b) Independent of operating temperature.
c) Include only parasitic components presented in the model circuit

Comparison of Model with Measured Data
(T_J=25°C Unless Otherwise Noted)