### SPICE Device Model SUD45P03-10



### P-Channel Enhancement-Mode Transistor

### Characteristics

- P-channel Vertical DMOS
- Macro-Model (Subcircuit)
- Level 3 MOS
- Applicable for Both Linear and Switchmode
- Applicable Over a -55 to 125°C Temperature Range
- Models Gate Charge, Transient, and Diode Reverse Recovery Characteristics

## Description

The attached SPICE Model describes typical electrical characteristics of the n-channel vertical DMOS. The subcircuit model was extracted and optimized over a 25°C to 125°C temperature range under pulse conditions for 0 to -10 volt gate drives. Saturated output impedance model accuracy has been maximized for gate biases near threshold. A novel gate-to-drain feedback

capacitor network is used to model gate charge characteristics while avoiding convergence problems of switched  $C_{\rm gd}$  model. Model parameter values are optimized to provide a best fit to measured electrical data and are not intended as an exact physical description of a device.

### Model Subcircuit

This document is intended as a SPICE modeling guideline and does not constitute a commercial product data sheet. Designers should refer to the appropriate data sheet of the same number for guaranteed specification limits.

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# **SPICE Device Model SUD45P03-10**



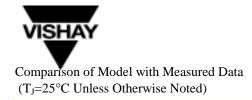
# P-Channel Device (T<sub>J</sub>=25°C Unless Otherwise Noted)

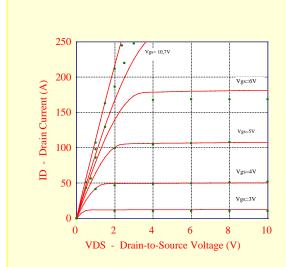
Parameter	Symbol	Test Conditions	Тур	Unit
Static				
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_{D} = -250 \mu A$	1.62	V
On-State Drain Current <sup>a</sup>	$I_{D(on)}$	$V_{DS} = -5V, V_{GS} = -10V$	474	A
		$V_{DS} = -5V, V_{GS} = -4.5V$	76	
Drain-Source On-State Resistance <sup>a</sup>	$r_{\mathrm{DS(on)}}$	$V_{GS} = -10V, I_D = -15A$	0.009	Ω
		$V_{GS} = -4.5V, I_D = -15A$	0.015	
		$V_{GS} = -10V, I_D = -15A,$	0.013	
		Tj = 125C		
Forward Transconductance <sup>a</sup>	$g_{ m fs}$	$V_{DS} = -15V$ , $I_D = -15A$	29	S
Diode Forward Voltage <sup>a</sup>	$V_{\mathrm{SD}}$	$I_F = I_S = -1.6A, V_{GS} = 0V$	0.8	V
Dynamic				
Total Gate Charge <sup>b</sup>	$Q_{\mathrm{g}}$		92	
Gate-Source Charge <sup>b</sup>	$Q_{gs}$	$V_{DS} = -15V, V_{GS} = -10V,$	22	nC
		$I_D = -45A$		
Gate-Drain Charge <sup>b</sup>	$Q_{\mathrm{gd}}$		18	
Turn-On Delay Time <sup>b,c</sup>	$t_{d(on)}$		69	
Rise Time <sup>b,c</sup>	$t_{\rm r}$	$V_{\rm DD} = -15 V, R_{\rm L} = 0.33 \Omega$	129	
Turn-Off Delay Time <sup>b,c</sup>	$t_{d(off)}$	$I_{\rm D} \cong -45 {\rm A}, V_{\rm GEN} = -10 {\rm V},$	88	ns
		$R_G = 2.4\Omega$		
Fall Time <sup>b,c</sup>	$t_{ m f}$	7	46	
Reverse Recovery Time	t <sub>rr</sub>	$I_{\rm F} = -45 {\rm A},$	54	
		$di/dt = 100A/\mu s$		

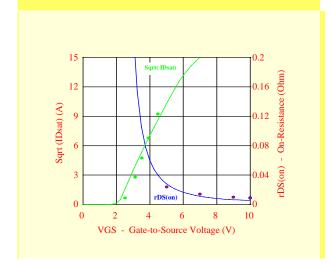
#### Notes

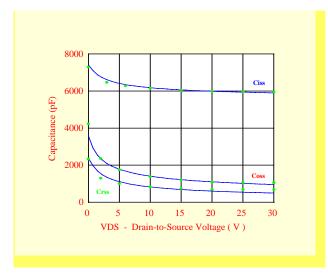
- a) Pulse test: Pulse Width  $\leq$  300 µsec, Duty Cycle  $\leq$  2%.
- b) Independent of operating temperature.
- c) Include only parasitic components presented in the model circuit

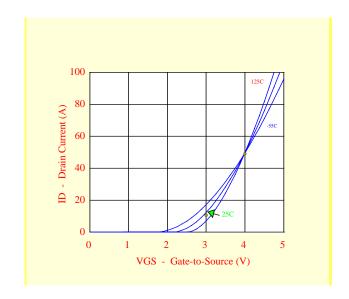


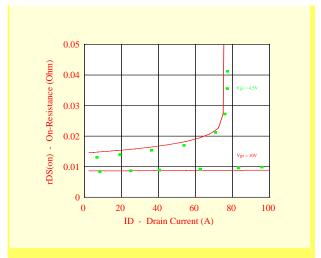


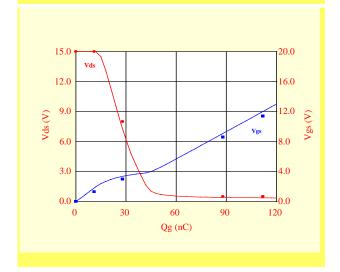












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