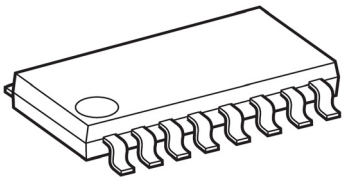
Toshiba BiCD Integrated Circuit Silicon Monolithic

TB6818FG

Power Factor Correction Control for CCM

Features

- Operating voltage range : 8.4 V (MIN) to 26V (MAX)
- Starting voltage / current : 10.0 V (typ.) / 30 μA (MAX)
- Pulse output mute function (Starting)
- Avoiding PFC transformer noise
- Maximum drive current : 1.0 A (typ.)
- Consumption current : 250 μA (typ.) (Standby mode)
- AC instantaneously-stop detection
- Built-in protection circuits
  - DC input OVP (OVP-1)
  - PFC output OVP (OVP-2)
  - UVLO
  - Feedback loop open detection (FOD)
  - TSD



SSOP16-P-225-1.00A

Weight : 0.16 g (typ.)

Note : Carefully handle this IC by using an earth band, a conductive sheet, or an ionizer to reduce ESD. Pay attention to temperature and humidity to protect the IC from ESD.

Note : Do not insert devices in the wrong orientation to prevent from destroying the IC.

The TB6818FG is RoHS compatible

With regard to solderability, the following conditions have been confirmed

- Solderability

  (1) Use of Sn-37Pb solder bath
  - solder bath temperature: 230°C
  - dipping time: 5 seconds
  - the number of times: once
  - use of R-type flux

  (2) Use of Sn-3.0Ag-0.5Cu solder bath
  - solder bath temperature: 245°C
  - dipping time: 5 seconds
  - the number of times: once
  - use of R-type flux

Block Diagram

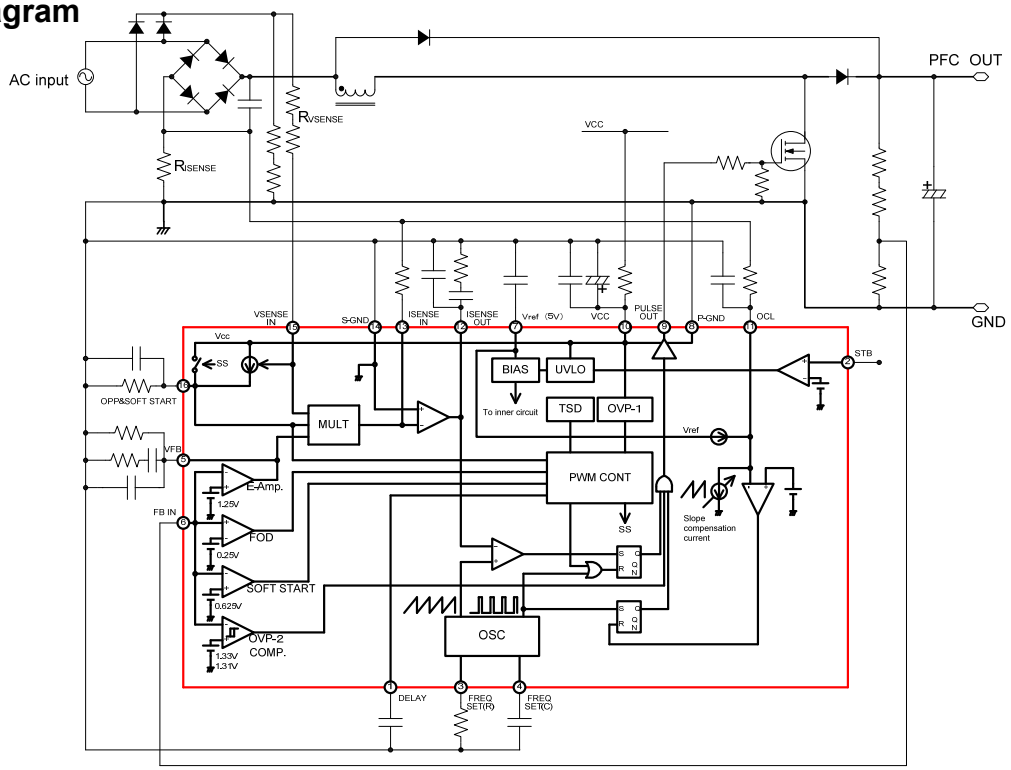


Fig. 1 Block Diagram

Pin Assignment and Descriptions

No.	Pin name	Descriptions	Remarks
1	DELAY	Pin for setting time of instantaneous-stop detection. Connect the capacitor to the GND.	—
2	STB	Pin for controlling ON and OFF for the IC. 1.5 V（MAX）or less: Operation mode; 3.5 V（MIN）or more: Standby mode	—
3	FREQ. SET（R）	Pin for setting oscillation frequency. Connect the resistance to the GND.	—
4	FREQ. SET（C）	Pin for setting oscillation frequency. Connect the capacitor to the GND.	—
5	VFB	Outputting error amplifier.	—
6	FB IN	Feed back pin of output voltage (inputting error amplifier).	—
7	Vref	Pin for outputting reference voltage of internal IC. Connect the capacitor to the GND. Voltage of 5.0 V (typ.) is outputted for this pin. Take care not to supply the current to the exterior from this pin.	—
8	P-GND	GND pin of PULSE OUT drive circuit.	—
9	PULSE OUT	Output pin for switching pulse to the FET gate.	—
10	VCC	Supply voltage input pin for IC operation. Operation voltage range: 8.4 V（MIN）to 26 V（MAX）.	—
11	OCL	Pin for detecting over-current which flows to FET gate.	—
12	ISENSE OUT	Output pin of amplifier for detecting current waveform.	—
13	ISENSE IN	Input pin of amplifier for detecting current waveform.	—
14	S-GND	GND pin of signal control circuit.	—
15	VSENSE IN	Pin for detecting full-wave rectification voltage waveform of AC.	—
16	OPP & SOFT START	Pin for setting soft start time in IC startup. Assign the resistance and the capacitor in parallel and connect them to the GND.	—

Application Circuit

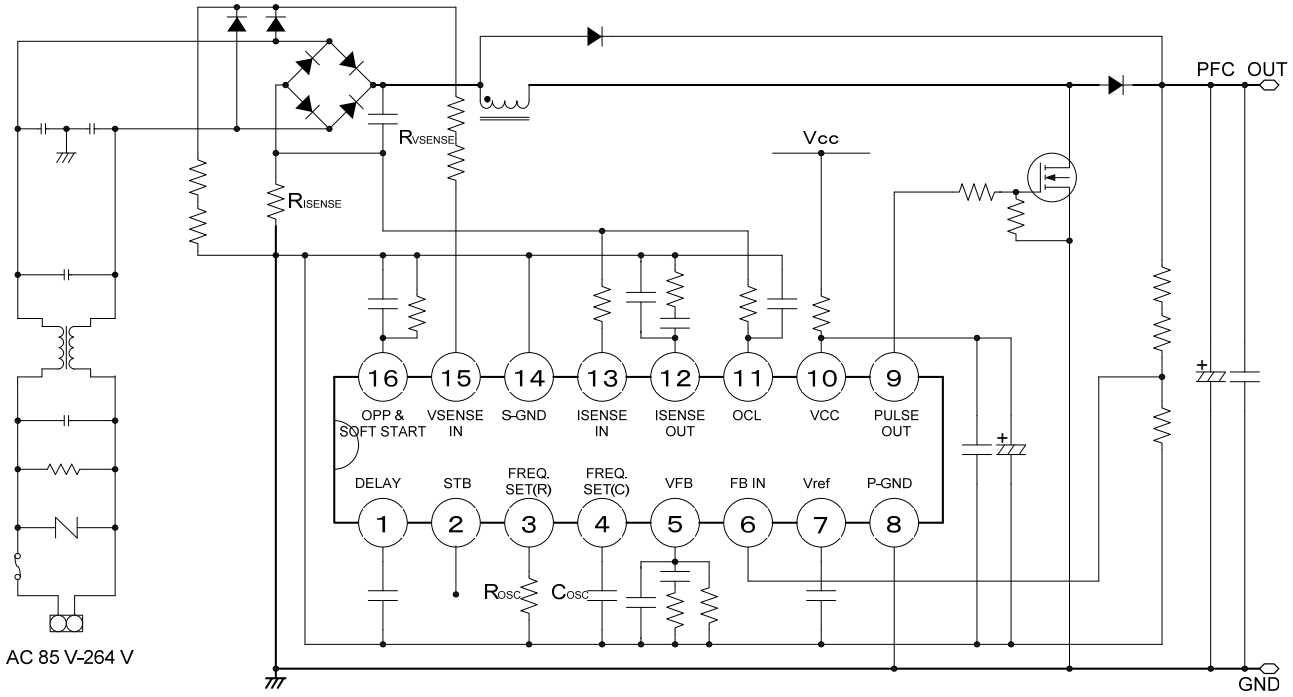


Fig. 2 Application Circuit (External Vcc supply)

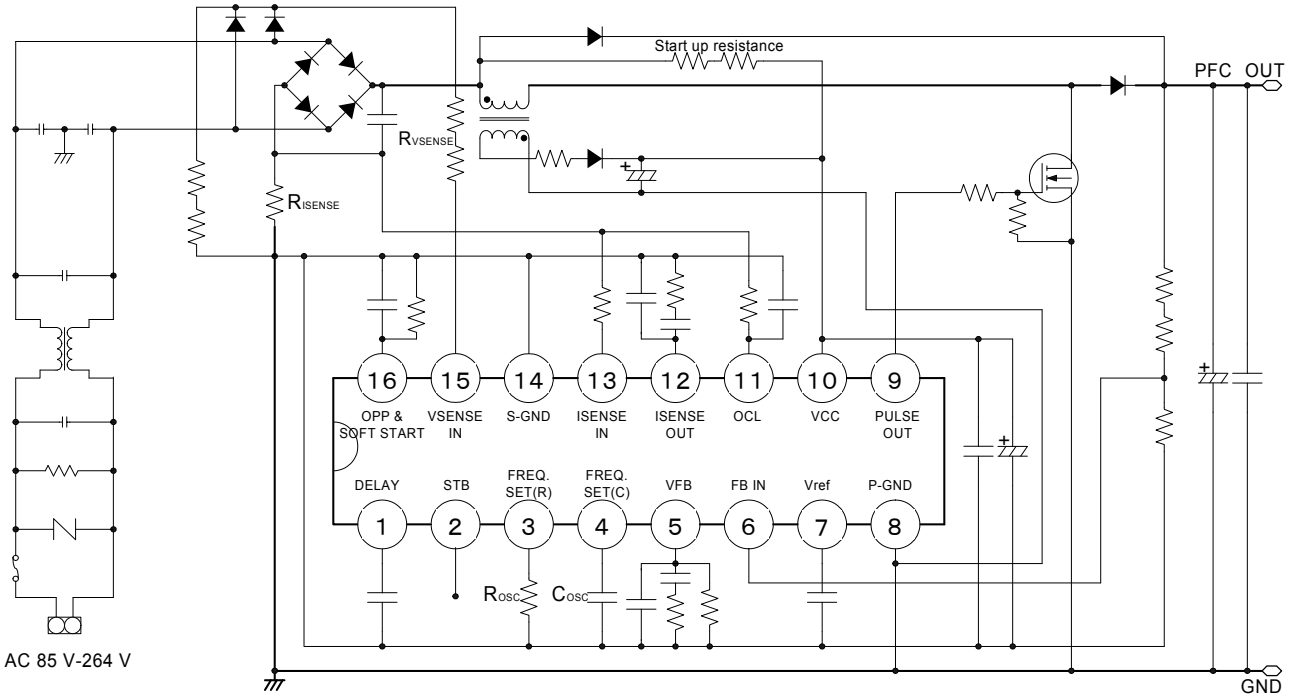


Fig. 3 Application Circuit (Self Vcc supply)

Absolute maximum rating (Ta = 25°C)

Item	Symbol	Rating	Unit
Power supply voltage	Vccmax	28.0	V
Maximum excitation voltage of each pin	Vinmax	(*3)	V
Minimum excitation voltage of each pin	Vinmin	GND－0.3	V
Power drop 1 (*1)	PDmax	1190	mW
Operating temperature (*2)	Topr	－25 to 85	°C
Junction temperature	Tj	150	°C
Storage temperature	Tstg	－55 to 150	°C

(*1) When Ta is 25°C or more, it decreases at the rate of 9.52 mW per 1°C rise in temperature.

(*2) Within this range, the IC operates without any problems.

(*3) Maximum excitation voltage of each pin

No.	Pin name	Rating	Unit
1	DELAY	5.0	V
2	STB	Vcc-0.3	
3	FREQ. SET (R)	(*4)	
4	FREQ. SET (C)	(*4)	
5	VFB	5.0	
6	FB IN	5.0	
7	Vref	(*4)	
8	GND	—	

No.	Pin name	Rating	Unit
9	PULSE OUT	(*4)	V
10	VCC	28.0	
11	OCL	5.0	
12	ISENSE OUT	5.0	
13	ISENSE IN	5.0	
14	SENSE GND	0.3	
15	VSENSE IN	5.0	
16	OPP & SOFT START	5.0	

(*4) Do not apply voltage externally.

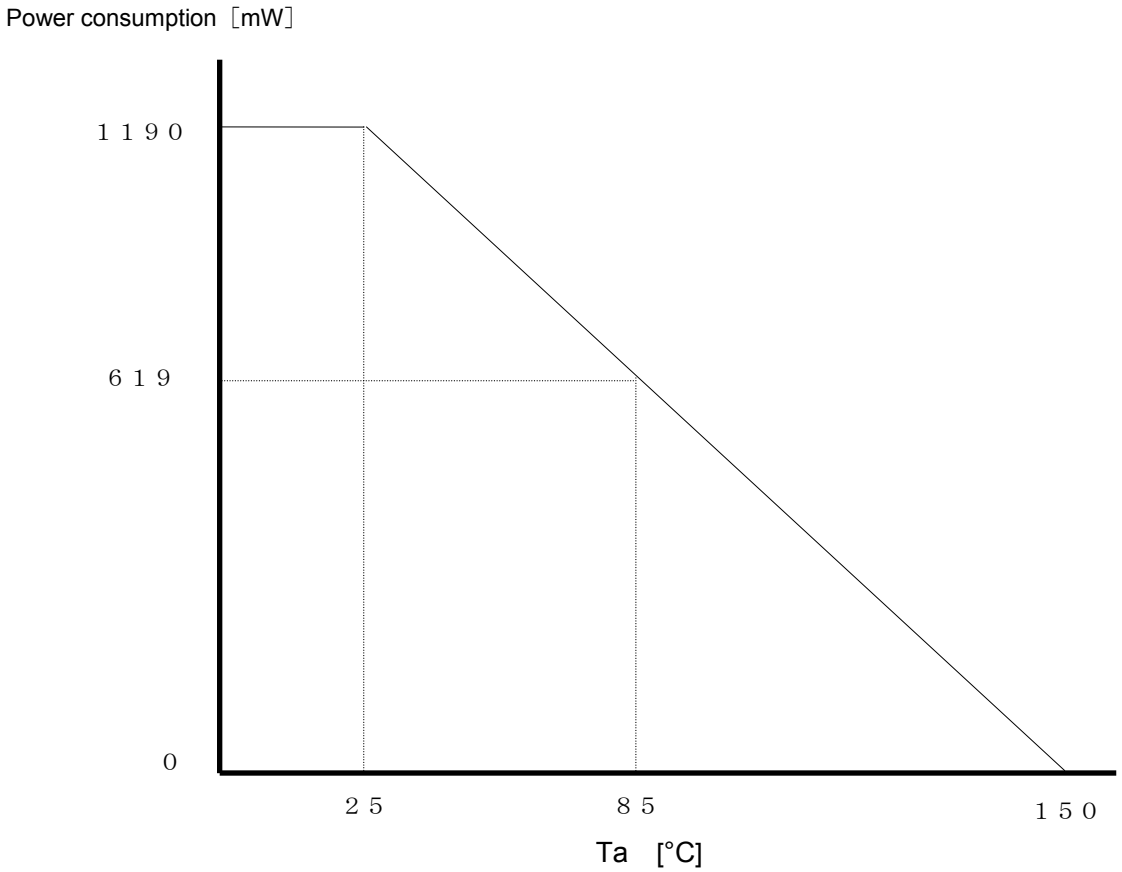


Fig. 4 Relationship between temperature drop and power consumption

Operating Conditions (Ta = 25°C)

Item	Pin No.	Min.	Typ.	Max.	Unit
Power supply voltage (Note 3)	No. 10 pin	8.4	—	26.0	V

(Note 3) The power supply voltage range to operate the IC stably.
10.0V (typ.) or more should be applied to start the IC.

Electrical Characteristics

1) DC Characteristics (Unless otherwise specified, Vcc = 15 V and Ta = 25°C)

Item	Pin No.	Symbol	Min.	Typ.	Max.	Unit
Consumption current 1	No. 10 pin	I Load Off	3.3	5.0	7.2	mA
Condition: Pin 10 (PULSE OUT) is open. Vstb = 1.0 V Rosc = 12 kΩ Cosc = 470 pF fosc = 75 kHz						
Consumption current 2	No. 10 pin	I On	80	100	120	mA
Condition: Resistance load (150 Ω) is connected between pin 10 (PULSE OUT). Vstb=4.0 V → 1.0 V Rosc=12 kΩ Cosc=470 pF fosc=75 kHz						
Consumption current 3	No. 10 pin	I STB	20	50	100	μA
Condition: Resistance load (150 Ω) is connected between pin 10 (PULSE OUT). Vstb = 1.0 V → 4.0 V (Standby mode) Rosc = 12 kΩ Cosc = 470 pF fosc : Oscillation stop mode						

Electrical characteristics （Unless otherwise specified, VCC= 15V, Ta = 25°C）

Item	Symbol		Remarks	Min.	Typ.	Max.	Unit
Startup current	Istart		During startup	—	—	30	μA
Soft start time	Tsoft		Csoft = 1 μF Rsoft = 20 kΩ	20	—	—	ms
Minimum oscillation frequency	f oscmin			—	—	20	kHz
Maximum oscillation frequency	f oscmax			150	—	—	kHz
Output pulse maximum voltage	Vomax		Output load current 100 mA	Vcc-2.0	—	—	V
Output pulse minimum voltage	Vomin		Output load current 100 mA	—	—	0.4	V
Output pulse（SOURCE） maximum current	Id source			—	-1.0	—	A
Output pulse（SINK） maximum current	Id sink			—	1.0	—	A
Output pulse leading edge time	TRPF		Capacitor load 3300 pF	—	50	—	ns
Output pulse training edge time	TSPF		Capacitor load 3300 pF	—	50	—	ns
Output pulse maximum duty	Dmax		Oscillation frequency: 75 kHz	98.0	99.0	—	%
Mode voltage of STB pin	Vstbon		Drive ON	—	—	1.5	V
	Vstboff		Drive OFF（Standby）	3.5	—	—	
Input current of STB pin	Ictr			-0.5	—	0.5	μA
DC input OVP operating voltage	V_{OVP-1}		Drive O N	26.2	27.5	—	V
			Drive OFF	—	22.7	—	
PFC output OVP operating voltage	V_{OVP-2}		Drive O N	1.30	1.33	1.36	V
			Drive OFF	1.28	1.31	1.34	
OCL operating voltage	V_{OCL}			-0.1	0	0.1	V
FOD operating voltage	V_{FOD}		Feedback loop open detection	0.23	0.25	0.27	V
UVLO operating voltage	V_{UVLO}		Shut down voltage	7.6	8.0	8.4	V
			Starting voltage	9.5	10.0	10.5	
Heat protect circuit operating temperature	TSD			150	175	—	°C

Pin description

(1) DELAY terminal (1 Pin)

It sets the time of instantaneous stop detection. The capacitor should be connected against the ground terminal.
When supply of AC voltage stops during operation, the voltage of the OPP & SOFT STATY terminal (16 Pin) starts decreasing. When this voltage decreases below 0.6 V (typ.), the capacitor connected to the DELAY terminal starts charging and the voltage of the DELAY terminal increases from 0 V. At this time, when the supply of AC voltage starts again before the voltage of the DELAY terminal reaches 1.25 V (typ.), the voltage of the OPP & SOFT START terminal (16 Pin) increases. Then when this voltage reaches 0.65 V (typ.), the charged capacitor is discharged and becomes 0 V.
In this case, the IC determines that instantaneous stop has recovered and PFC operation remains the same as the state before stopping the supply of AC voltage.

However, if the supply of AC voltage does not start before the voltage of the DELAY terminal reaches 1.25 V (typ.), the IC determines that it is not an instantaneous stop and forcedly outputs low level for PULSE OUT terminal (9 Pin). Then PFC operation stops. After that, when the supply of AC voltage starts again, the IC starts normal operation.

Time of instantaneous stop detection is determined by the formula below.

$$t\ (ms) = 50 \times C\ (\mu F)$$

(2) STB terminal (2 Pin)

It controls ON and OFF of the IC operation.
Operation mode: 1.5 V (MAX) or less
Stand by mode: 3.5 V (MIN) or more

When the operation switches to standby mode when operating at 10.0 V (typ.) or less, UVLO is released and the IC operation stops. The IC does not restart by switching operation mode (releasing standby mode).
The IC can restart when Vcc is 10.0 V (typ.) or more before it switches to standby mode.

(3) FREQ.SET(R) terminal (3 Pin), FREQ.SET(C) terminal (4 Pin)

It sets the oscillation frequency. Resistance (Rosc) is connected to 3 Pin against the ground terminal. Capacitor (Cosc) is connected to 4 Pin against the ground pin.
Resistance of 12 kΩ is recommended. (Refer to the supplemental notes.)

Oscillation frequency (fosc) can be found by the following theoretical formula.

$$fosc = \frac{4.24 \times 10^5}{Cosc \cdot Rosc}\ (kHz)$$

Cosc : (pF)
Rosc : (kΩ)

(4) VFB terminal (5 Pin)

It outputs the current of error amplifier (trans-conductor amplifier).
The filter is constructed to set the gain 0 dB or less with double frequency of AC input frequency which is superimposed to PFC output, and to have sufficient phase.

(5) FB IN terminal (6 Pin)

It is a feedback terminal for PFC output voltage (Input terminal of error amplifier).
PFC output is input divided by the resistance. Reference voltage of error amplifier is set 1.25 V (typ.).

This terminal has other functions as follows.

1) Over voltage detection of PFC output (OVP-2)

When PFC output voltage exceeds 106% of the setting voltage, output signal of PULSE OUT terminal (9 Pin) is forcedly set low and PFC operation stops. The operation restarts when the voltage becomes 105% or less of the setting voltage.

2) Open detection (FOD) of feedback (input of error amplifier) loop

When the feedback loop is open, output of PULSE OUT terminal (9 Pin) is set low level and PFC operation stops.

3) Decision whether to perform soft start or not during restart.

When the voltage of this terminal is 0.625 V (typ.) or less, the operation restarts with soft start.

(6) Vref terminal (7 Pin)

It outputs the reference voltage of the internal IC. The capacitor of 0.1 μF is connected against the ground terminal. A voltage of 5.0 V (typ.) is output to this terminal. Do not supply current to the exterior from this terminal.

(7) P-GND terminal (8 Pin)

GND terminal of driving circuit which outputs PULSE to the PULSE OUT terminal (9 Pin).

(8) PULSE OUT terminal (9 Pin)

It outputs switching pulse for FET switching gate.

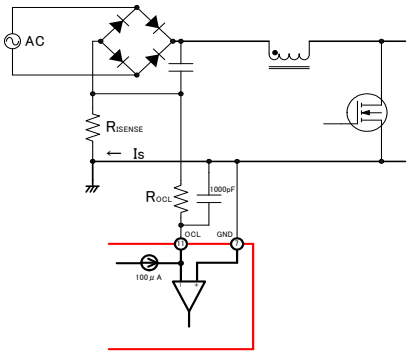
(9) Vcc terminal (10 Pin)

Input terminal of power supply for IC operation.
Operation voltage range is from 8.4 V (MIN) to 26 V (MAX). Be aware that when first powered on, a voltage of 10.0 V (typ.) or more must be applied. (Hysteresis function of UVLO)

Note: If it short-circuits nearby the PULSE OUT terminal (9 Pin), the IC may be damaged (or possibly ignite or produce smoke). To avoid IC damage, be sure to insert protective resistance of 1 Ω between the supply line and Vcc.

(10) OCL terminal (11 Pin)

It detects over-current which flows through the FET switch.
In order to detect the source current while the FET switch turns ON, current is converted to voltage by external "RIsense" and input.
When OCL operates, PFC operation stops by forcedly lowering the output of the PULSE OUT terminal (9 Pin).



Constant current of 100 μA is output from this terminal, so the voltage of this terminal is ROCL (kΩ) × 100 (μA).

When the source current (Is) of the FET switch increases, the voltage drop by "RIsense" resistance (RIsense (Ω) × Is (A)) increases. OCL starts operating under the below condition.

ROCL (kΩ) × 100 (μA) = RIsense (Ω) × Is (A)

Therefore, the value of the source current (Is (OCL)) which starts the OCL operation can be found as follows.

$$Is_{(OCL)} = \frac{R_{OCL}\ (k\Omega) \times 100\ (\mu A)}{R_{Isense}\ (\Omega)}\ (A)$$

OCL detection is invalid for 170 ns (typ.) after the FET switch turns on (output of PULSE OUT terminal (9 Pin) is high level) to avoid OCL operation introducing errors from needle-like pulse noise generated at the moment the FET switches ON

Connect the capacitor of 1000 pF against GND terminal in order to reduce needle-like pulse noise.

(11) ISENSE OUT terminal (12 Pin)

It outputs current (100 μA (MAX) of current detecting amplifier (Trans conductor amplifier).
Filter is constructed to set the gain to 0 dB or less around the switching frequency, and to have sufficient phase.

When voltage of this terminal increases, the pulse duty output to the PULSE OUT terminal (9 Pin) becomes narrow.
And when the voltage decreases, this duty becomes wide.

(12) ISENSE IN terminal (13 Pin)

It inputs current detecting amplifier (Trans conductor amplifier).
This terminal is connected to current output of multiple part internally. A maximum current of 200 μA can be output. This current is converted to voltage by external resistance and inputs to the current detecting amplifier.

(13) S-GND terminal (14 Pin)

GND terminal for current detecting amplifier (Trans conductor amplifier) and other signal lines.
This terminal should be separated from the line of P-GND terminal (8 Pin).
If it is connected near the P-GND terminal, PFC may not operate correctly because of the noise.

(14) VSENSE IN terminal (15 Pin)

It detects waveform of full-wave commutating voltage of AC voltage.
This terminal should be connected to the voltage line, where AC voltage is commutated with full-wave. And high resistance should be inserted. The voltage is converted to current in the IC and becomes the reference signal for PFC operation.
This terminal also detects zero-cross of AC input voltage. In order to detect zero-cross certainly, input waveform of full-wave commutating voltage should be commutated fully in special circuit, not in the line which is bridge commutated in the main circuit. (Refer to the application circuit)

(15) OPP&SOFT START terminal (16 Pin)

It sets the soft-start time at IC power on. Resistance and capacitor should be assigned in parallel and are connected against GND terminal. At IC power on, voltage of this terminal rises to 4.75 V.
After that, it falls slowly and settles the constant voltage corresponding to the output load of PFC. During this time, the pulse duty output to the PULSE OUT terminal (9 Pin) spreads slowly from zero.(soft-start function) This function avoids generating rush current in the FET switch and PFC coil at IC power on.

Supplemental note

To set the oscillation frequency (fosc), resistance (Rosc), which is connected to 3 Pin and against GND, determines the current value of the reference supply in this IC.
The current of the reference supply is also supplied to the error amplifier (trans-conductor amplifier) and the current waveform detecting amplifier (trans-conductor amplifier). So gm of each amplifier can be found as follows.

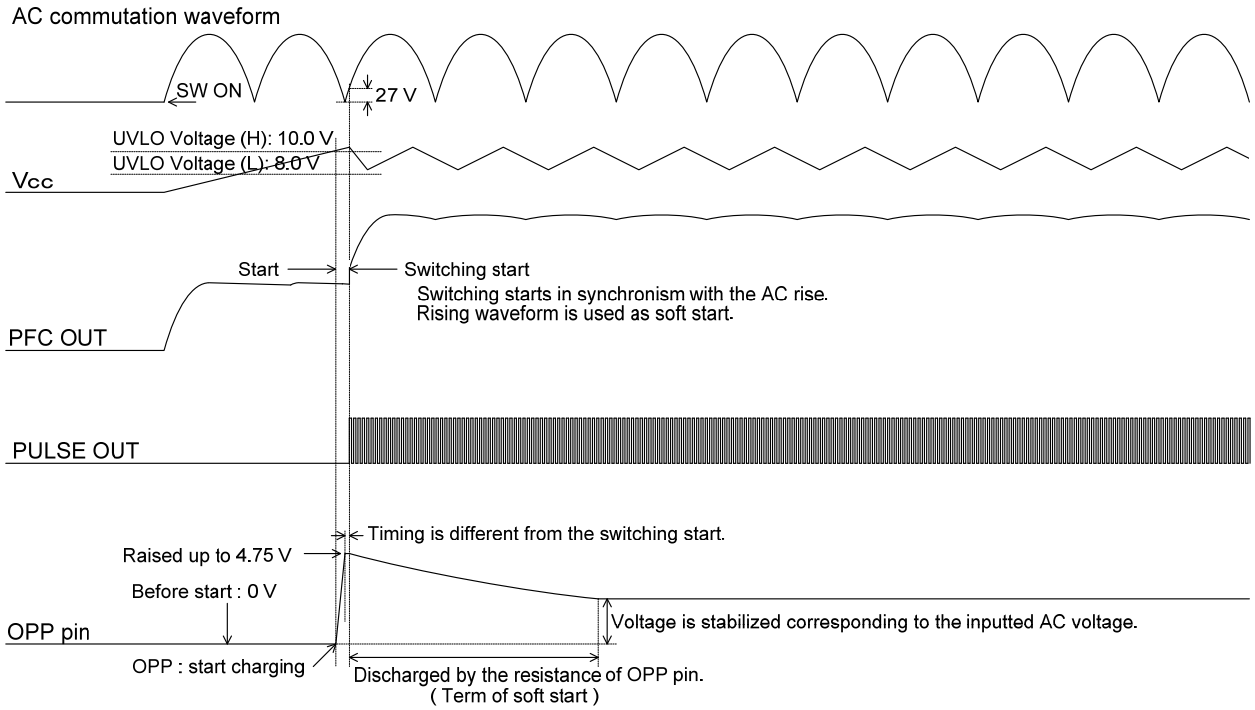
gm is calculated from the following theoretical formula.

$$gm = \frac{23.16 \times 10^3}{Rosc\ (k\Omega)} \quad (\mu S)$$

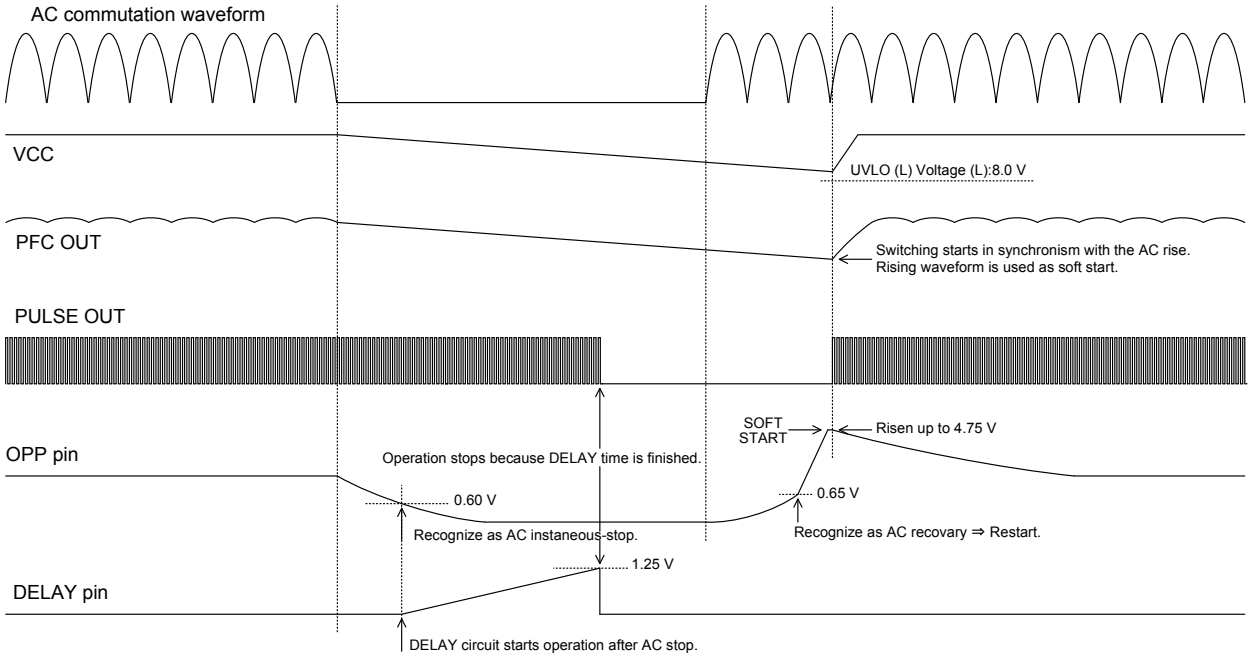
In applying recommended resistance (12 kΩ), gm of each amplifier is 1.93 (mS). However, if gm is changed please change the resistance.

Operation Sequence

（1）Start up

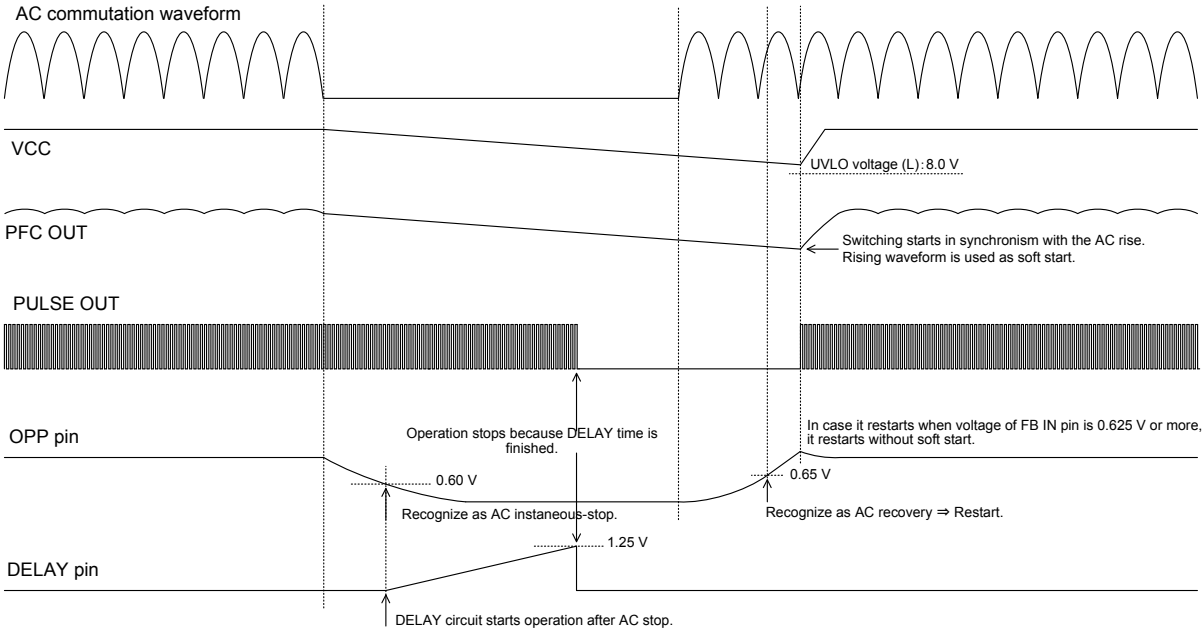


（2）Recovery from AC instantaneous-stop -1-1

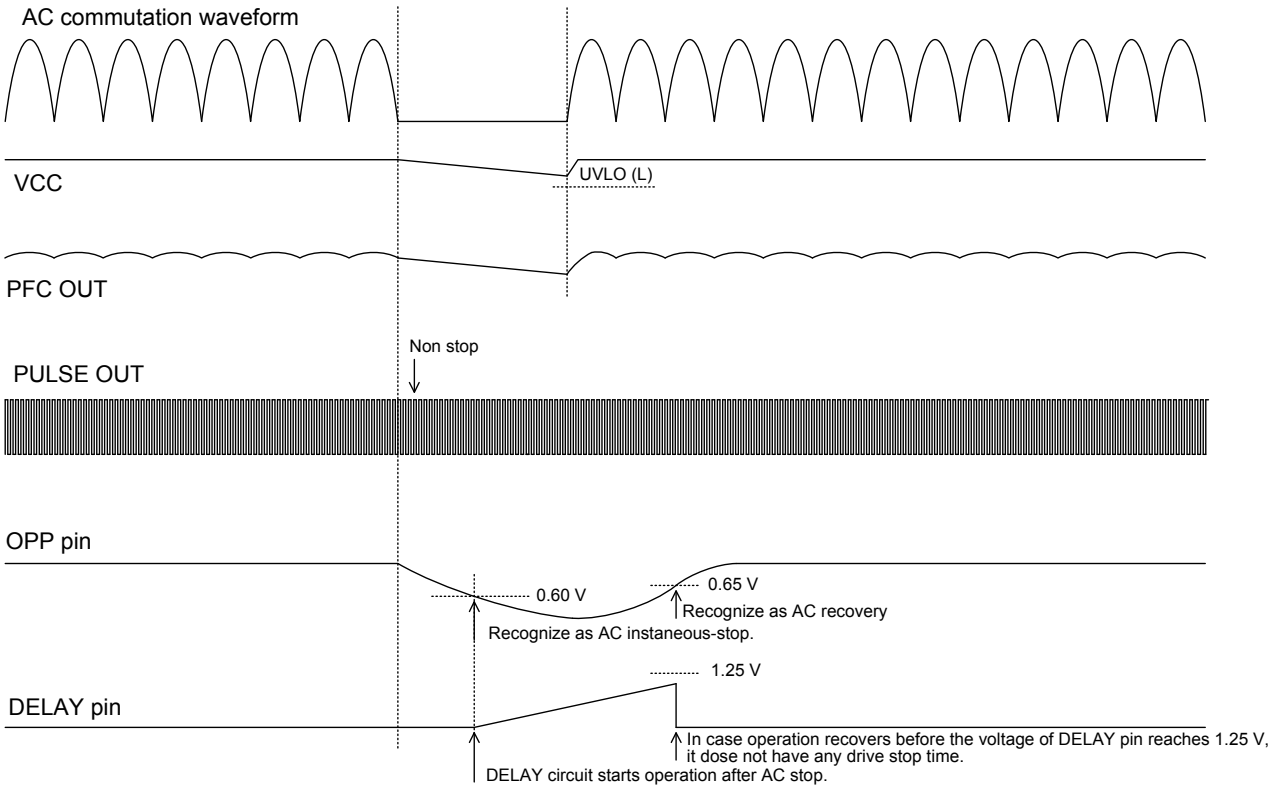


Operation sequence

（3） Recovery from AC instantaneous-stop -1-2

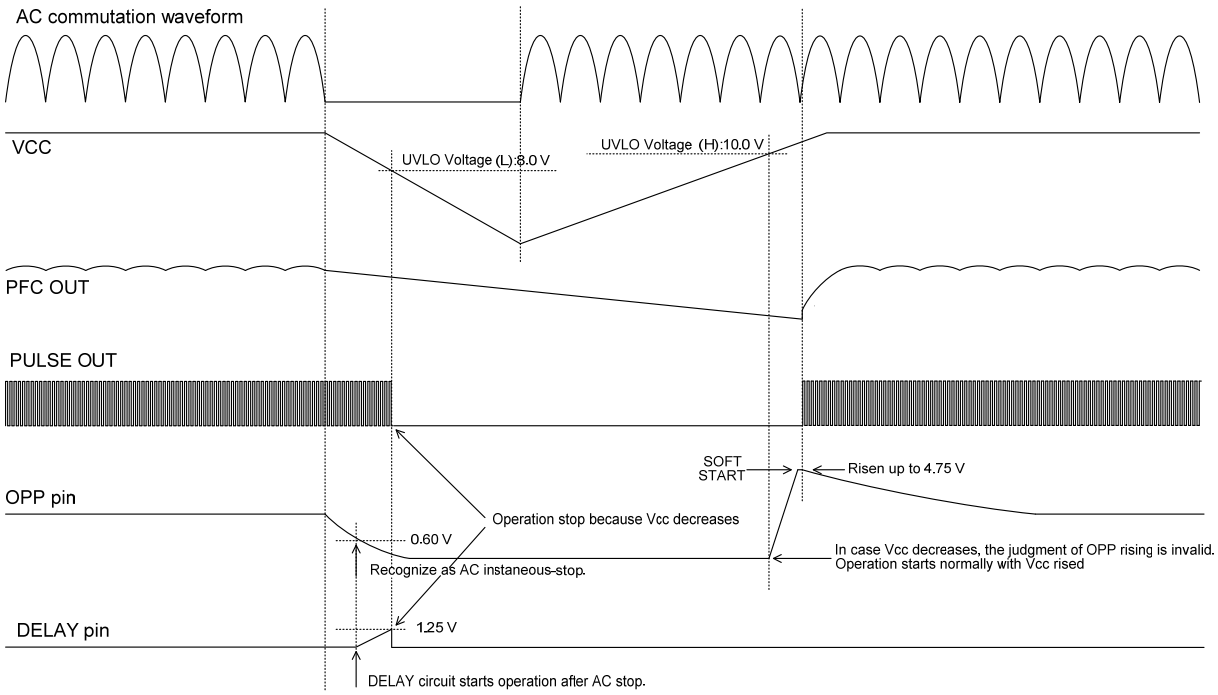


（4） Recovery from AC instantaneous-stop -2

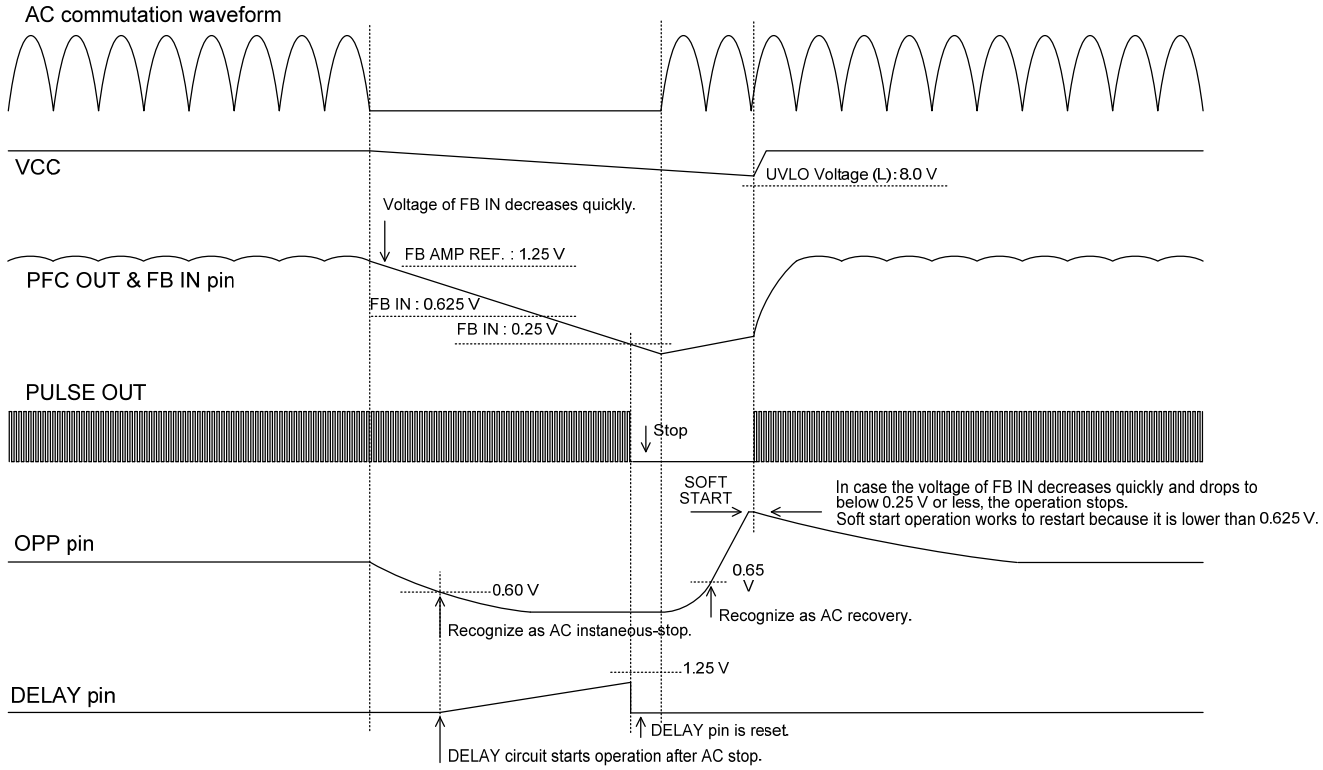


Operation sequence

（5）Recovery from AC instantaneous-stop -3 (When Vcc is supplied from secondary side of PFC transformer)

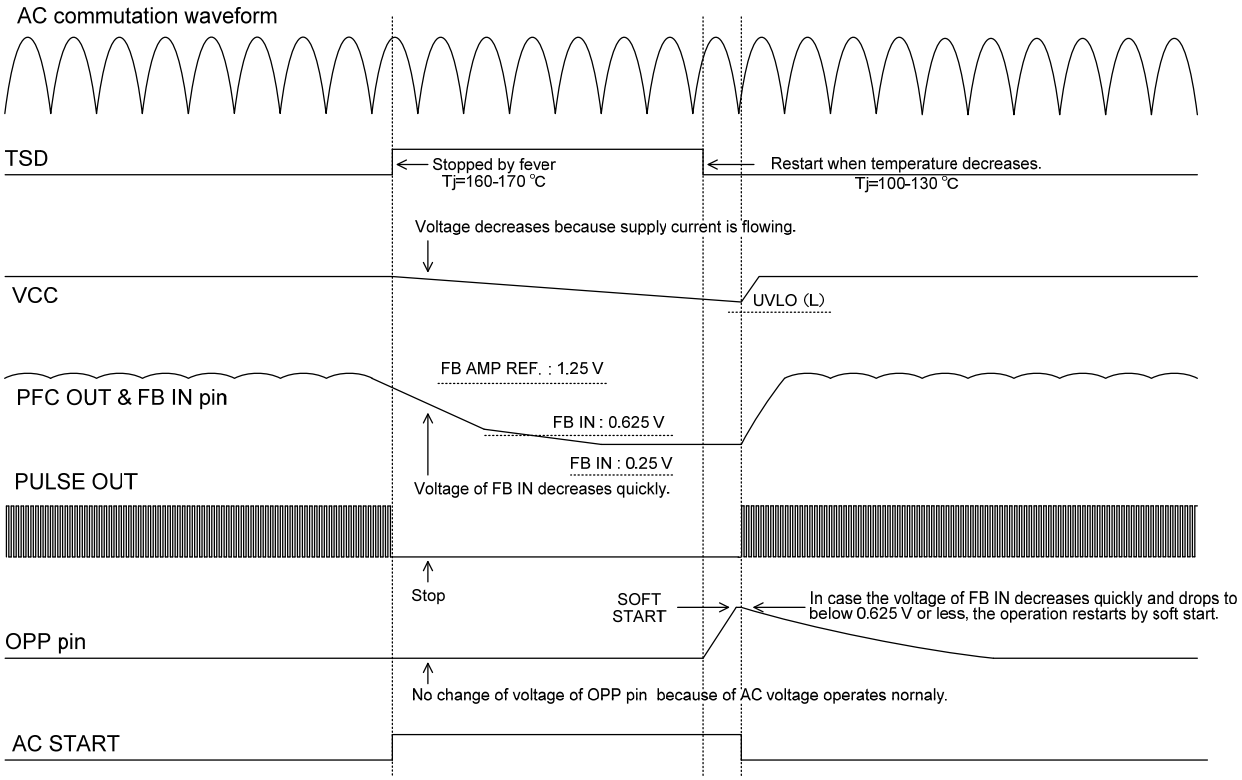


（6）Recovery from AC instantaneous-stop -4

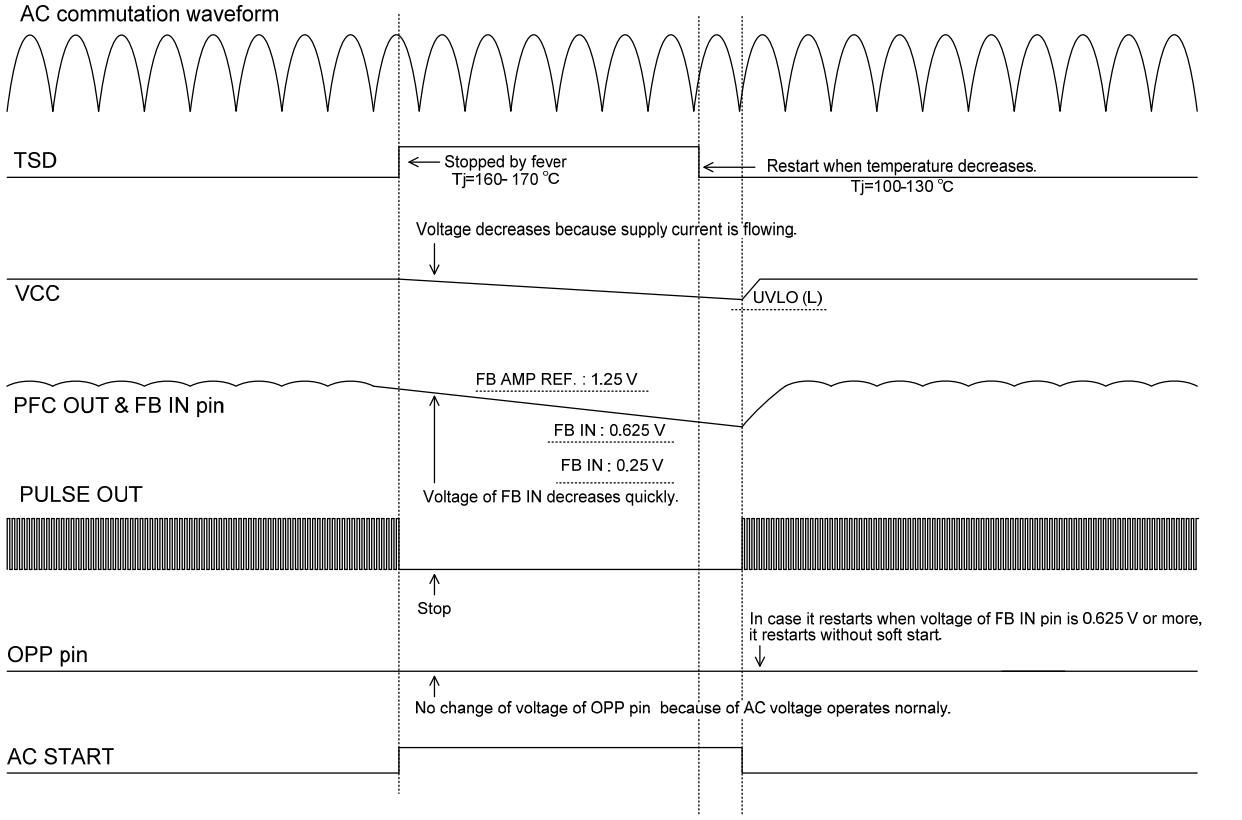


Operation sequence

（7） Recovery from thermal shutdown -1

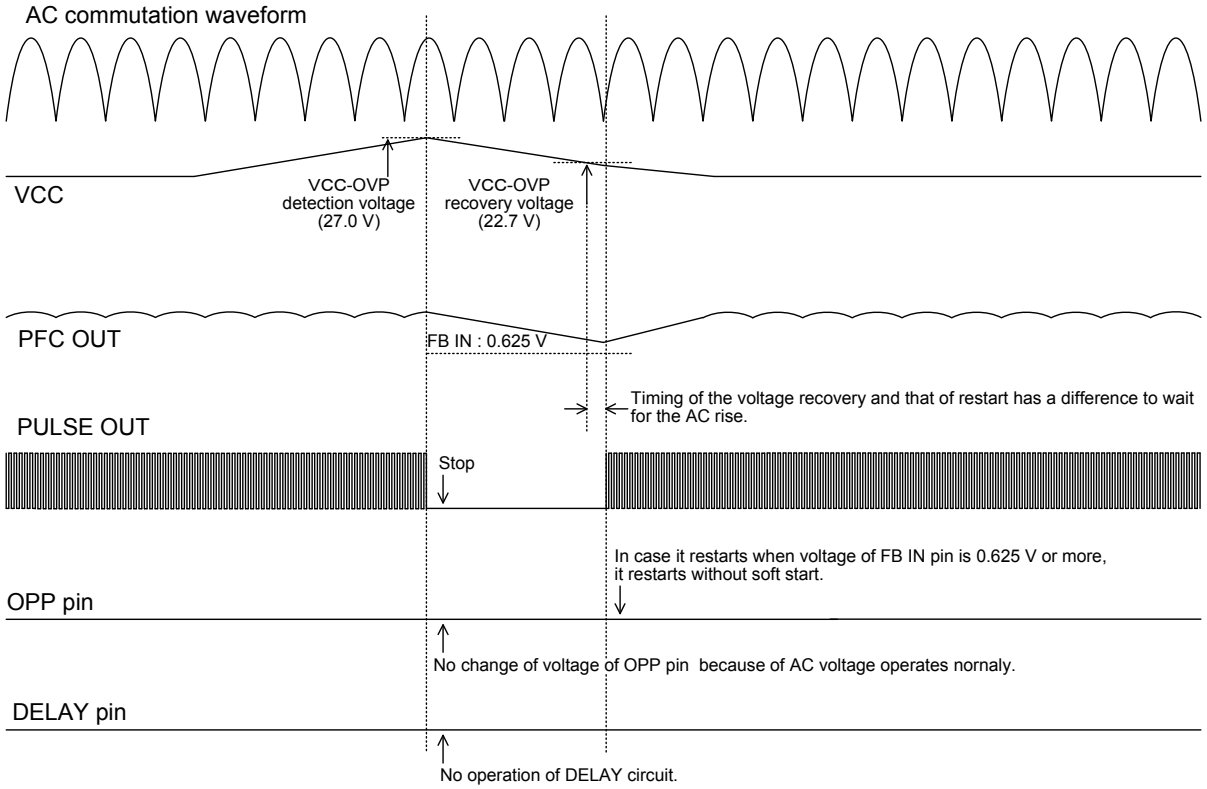


（8） Recovery from thermal shutdown -2

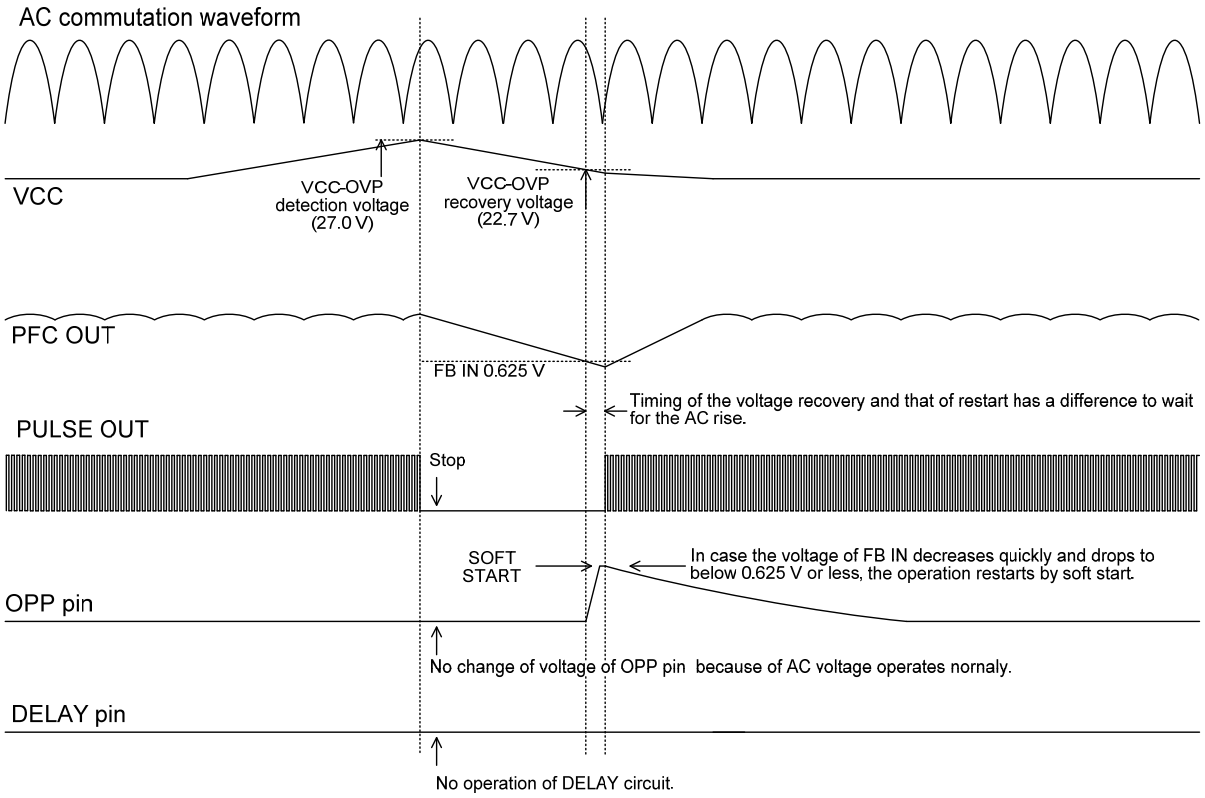


Operation sequence

（９）Recover from OVP-1 operation -1

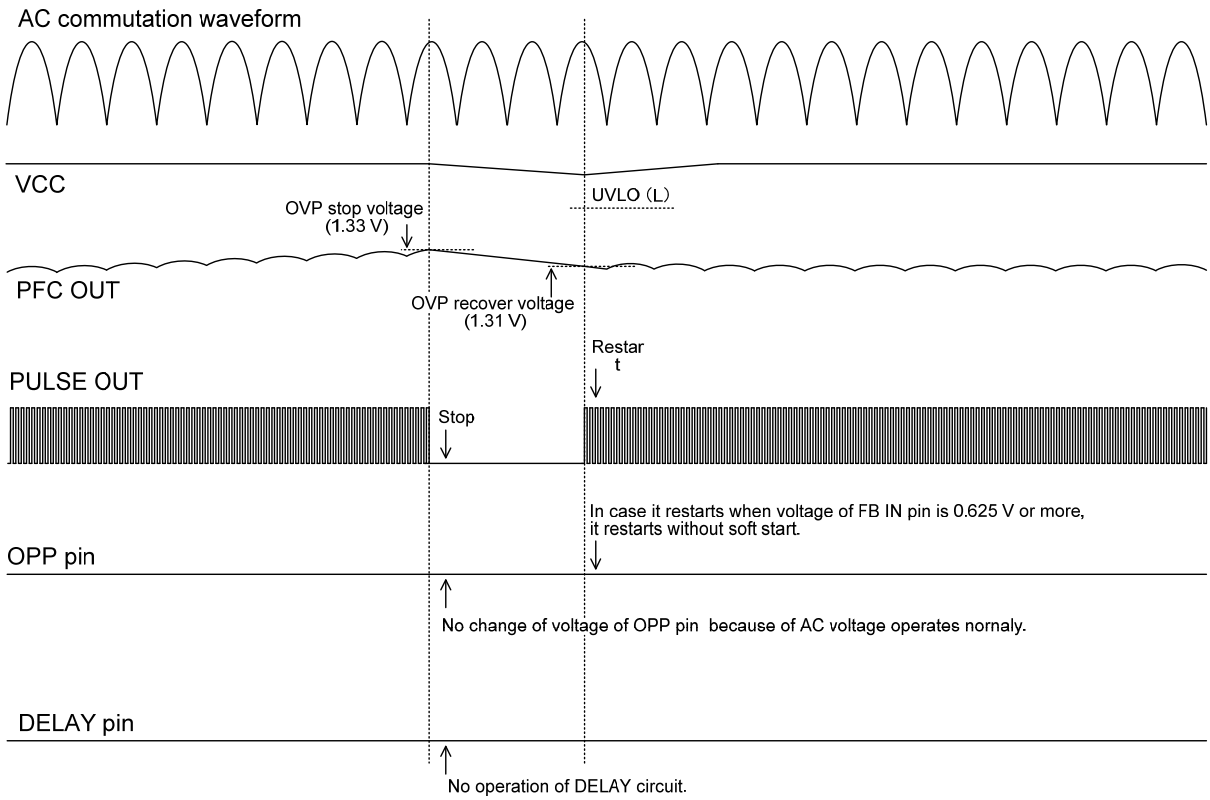


（１０）Recover from OVP-1 operation -2

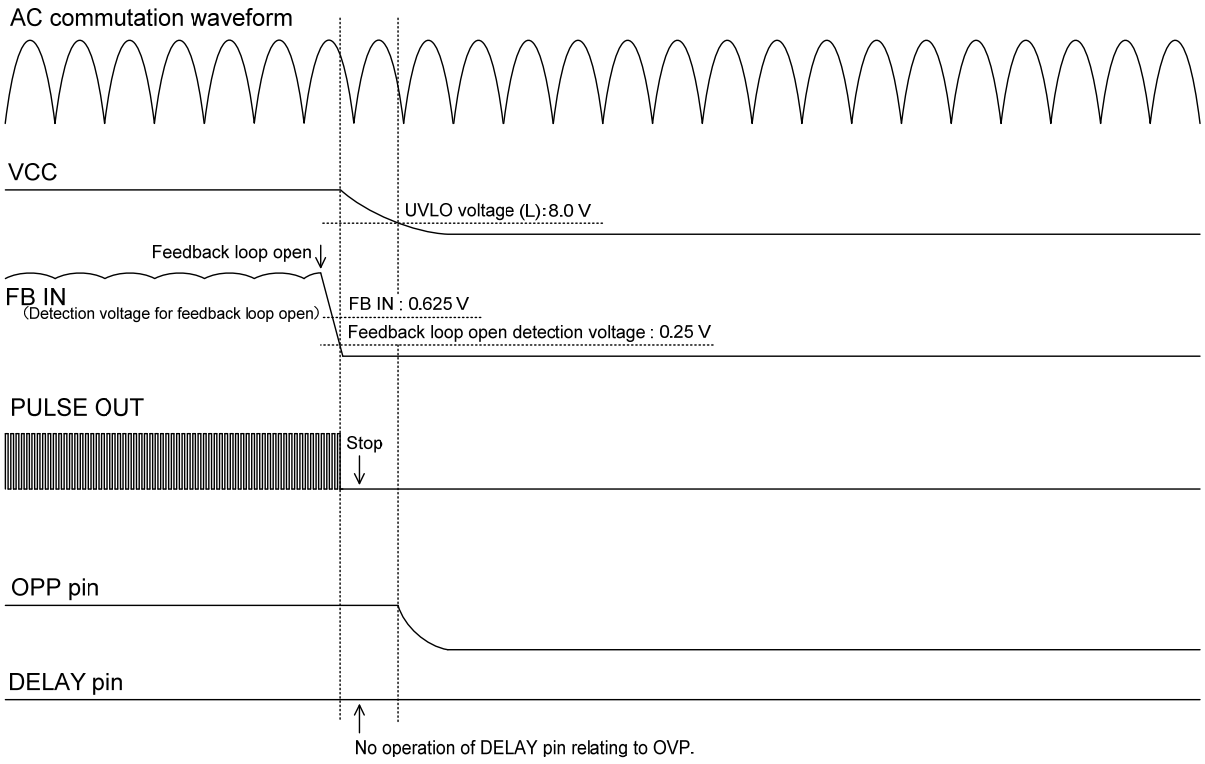


Operation sequence

（１１）Recover from OVP-2 operation

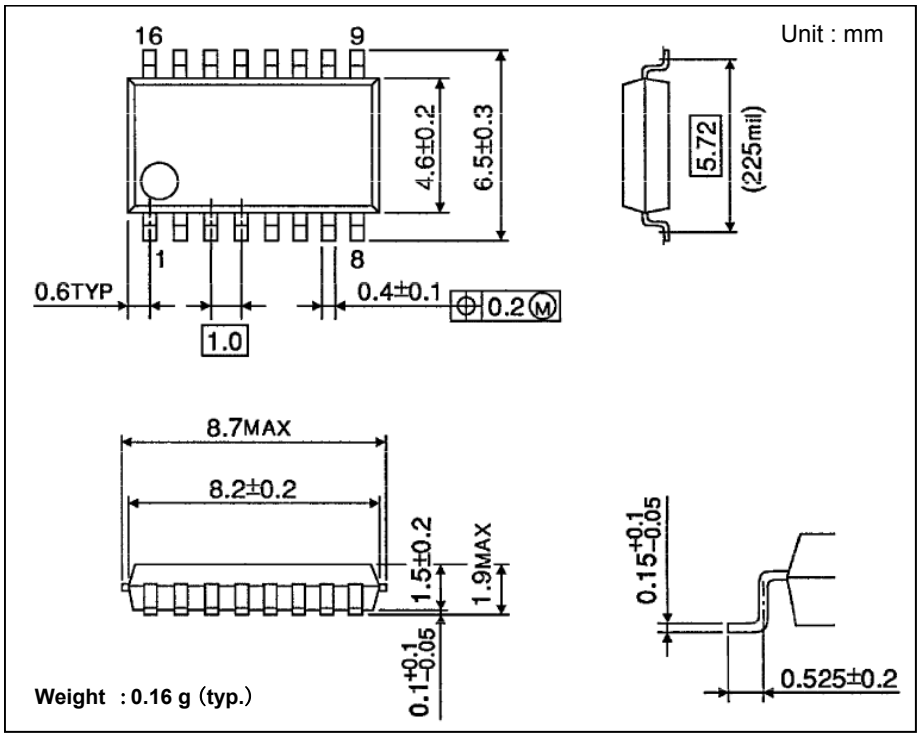


（１２）FOD operation

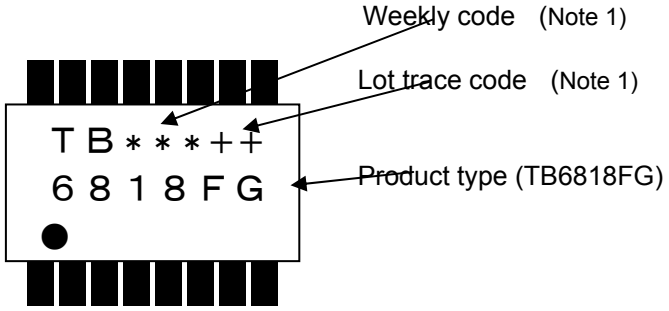


Package Dimensions

MFP16（SSOP16-P-225-1.00A）



Identification Indication



(Note 1) 5 characters

For example : 935A2

2009 35th Week Lot trace code

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