

# DATA SHEET



## **SAA7705H**

### **Car radio Digital Signal Processor (DSP)**

Preliminary specification  
File under Integrated Circuits, IC01

1999 Aug 16

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# Car radio Digital Signal Processor (DSP)

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## 1 FEATURES

### 1.1 Hardware

- Three 3rd-order Switched Capacitor Analog-to-Digital converters (SCADs)
- Digital-to-Analog Converters (DACs) with four times oversampling and noise shaping
- Digital stereo decoder for the FM multiplex signal
- Improved digital Interference Absorption Circuit (IAC) for FM
- Radio Data System (RDS) processing with an optional 16-bit buffer via a separate channel (two tuners possible)
- Auxiliary high Common-Mode Rejection Ratio (CMRR) analog CD input (CD-walkman, speech, economic CD-changer, etc.)
- I<sup>2</sup>C-bus controlled
- Four channel 5-band I<sup>2</sup>C-bus controlled parametric equalizer
- Two separate full I<sup>2</sup>S-bus and LSB-justified formats high performance input interfaces
- Audio output short-circuit protected
- Separate AM left and right inputs
- Phase-Locked Loop (PLL) to generate the high frequency DSP clock from a common fundamental oscillator crystal
- Analog single-ended tape inputs
- I<sup>2</sup>S-bus subwoofer output (mono or stereo)
- Expandable with additional DSPs for sophisticated features through an I<sup>2</sup>S-bus gateway
- Operating ambient temperature from –40 to +85 °C.

### 1.2 Software

- Improved FM weak signal processing
- Integrated 19 kHz MPX filter and de-emphasis
- Electronic adjustments: FM/AM level, FM channel separation and Dolby level
- Baseband audio processing (treble, bass, balance, fader and volume)
- Dynamic loudness or bass boost
- Audio level meter
- Tape equalisation (tape analog playback)



- Music Search System (MSS) detection for tape
- Dolby-B tape noise reduction
- Adjustable dynamics compressor
- CD de-emphasis processing
- Improved AM reception
- Soft audio mute
- AM IAC
- Pause detection for RDS updates
- Signal level, noise and multipath detection for AM/FM signal quality information.

## 2 APPLICATIONS

- Car radio systems.

## 3 GENERAL DESCRIPTION

The SAA7705H performs all the signal functions in front of the power amplifiers and behind the AM and FM multiplex demodulation of a car radio or the tape input.

These functions are:

- Interference absorption
- Stereo decoding
- RDS decoding
- FM and AM weak signal processing (soft mute, sliding stereo, etc.)
- Dolby-B tape noise reduction
- Audio controls (volume, balance, fader and tone).

Some functions have been implemented in the hardware (stereo decoder, RDS decoding and IAC for FM multiplex) and are not freely programmable. Digital audio signals from external sources with the Philips I<sup>2</sup>S-bus format or the LSB-justified 16, 18 or 20 bits format are accepted. There are four independent analog output channels. The channels have a hardware implemented 5-band parametric equalizer, controlled via the I<sup>2</sup>C-bus.

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- The DSP contains a basic program that enables a set with:
- AM/FM reception
  - Sophisticated FM weak signal functions
  - Music Search System (MSS) detection for tape
  - Dolby-B tape noise reduction system
  - CD play with compressor function
  - Separate bass and treble tone control and fader or balance control additional to the equalizers.

## 4 QUICK REFERENCE DATA

| SYMBOL  | PARAMETER                                       | CONDITIONS   | MIN. | TYP.  | MAX.       | UNIT |
|---|---|--|------|-------|------------|------|
| <b>Supply</b>   |   |  |      |       |            |      |
| $V_{DD3V}$  | digital supply voltage<br>3.3 V for DSP core    | $V_{DD3Vx}$ pins with respect to $V_{SS}$  | 3    | 3.3   | 3.6        | V    |
| $I_{DD3V}$  | supply current of the<br>3.3 V digital DSP core | high activity of the DSP at<br>27 MHz DSP frequency                                    | –    | 80    | 110        | mA   |
| $V_{DD5V}$  | supply voltage 5 V for<br>periphery             | $V_{DD5Vx}$ pins with respect to $V_{SS}$  | 4.5  | 5     | 5.5        | V    |
| $I_{DD5V}$  | supply current of the 5 V<br>digital periphery  |  | –    | 3     | 5          | mA   |
| $V_{DDA}$   | analog supply voltage<br>3.3 V                  | $V_{DDAx}$ pins with respect to $V_{SS}$   | 3    | 3.3   | 3.6        | V    |
| $I_{DDA}$   | analog supply current                           | zero input and output signal   | –    | 40    | 50         | mA   |
| <b>Analog level inputs (AML and FML); <math>T_{amb} = 25\text{ }^{\circ}\text{C}</math>; <math>V_{DDA1} = 3.3\text{ V}</math>; unless otherwise specified</b> |   |  |      |       |            |      |
| $S/N_{LAD}$   | level-ADC signal-to-noise<br>ratio              | 0 to 29 kHz bandwidth;<br>maximum input level;<br>unweighted                           | 48   | 54    | –          | dB   |
| $V_{i(LAD)}$  | input voltage level-ADC<br>for full-scale       |  | 0    | –     | $V_{DDA1}$ | V    |
| <b>Analog inputs; <math>T_{amb} = 25\text{ }^{\circ}\text{C}</math>; <math>V_{DDA1} = 3.3\text{ V}</math>; unless otherwise specified</b>                     |   |  |      |       |            |      |
| $THD_{FMMPX}$   | total harmonic distortion<br>FMMPX input        | input signal 0.35 V (RMS) at<br>1 kHz; bandwidth = 19 kHz;<br>note 1                   | –    | –70   | –65        | dB   |
|   |   |  | –    | 0.03  | 0.056      | %    |
| $S/N_{FMMPX(m)}$  | signal-to-noise ratio<br>FMMPX input mono       | input signal at 1 kHz;<br>0 dB reference = 0.35 V (RMS);<br>bandwidth = 19 kHz; note 1 | 80   | 83    | –          | dB   |
| $S/N_{FMMPX(s)}$  | signal-to-noise ratio<br>FMMPX input stereo     | input signal at 1 kHz;<br>0 dB reference = 0.35 V (RMS);<br>bandwidth = 40 kHz; note 1 | 74   | 77    | –          | dB   |
| $THD_{CD}$  | total harmonic distortion<br>CD inputs          | input signal 0.55 V (RMS) at<br>1 kHz; input gain = 1;<br>bandwidth = 20 kHz           | –    | –83   | –78        | dB   |
|   |   |  | –    | 0.007 | 0.013      | %    |
| $S/N_{CD}$  | signal-to-noise ratio CD<br>inputs              | input signal at 1 kHz;<br>0 dB reference = 0.55 V (RMS);<br>bandwidth = 20 kHz         | 81   | 84    | –          | dB   |
| $THD_{AM}$  | total harmonic distortion<br>AM inputs          | input signal 0.55 V (RMS) at<br>1 kHz; bandwidth = 5 kHz                               | –    | –80   | –76        | dB   |
|   |   |  | –    | 0.01  | 0.016      | %    |

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| SYMBOL   | PARAMETER   | CONDITIONS   | MIN. | TYP.    | MAX.  | UNIT |
|--|---|--|------|---------|-------|------|
| $S/N_{AM}$   | signal-to-noise ratio AM inputs                             | input signal at 1 kHz;<br>0 dB reference = 0.55 V (RMS);<br>bandwidth = 5 kHz                      | 83   | 88      | —     | dB   |
| $THD_{TAPE}$   | total harmonic distortion TAPE inputs                       | input signal 0.55 V (RMS) at<br>1 kHz; bandwidth = 20 kHz;   | —    | −80     | −76   | dB   |
|  |   |  | —    | 0.01    | 0.016 | %    |
| $S/N_{TAPE}$   | signal-to-noise ratio TAPE inputs                           | input signal at 1 kHz;<br>0 dB reference = 0.55 V (RMS);<br>bandwidth = 20 kHz                     | 81   | 83      | —     | dB   |
| $V_{i(con)(max)(rms)}$   | maximum conversion input level at analog inputs (RMS value) | $THD < 1\%$  | 0.6  | 0.66    | —     | V    |
| <b>Analog outputs; <math>T_{amb} = 25\text{ }^{\circ}\text{C}</math>; <math>V_{DDA2} = 3.3\text{ V}</math>; unless otherwise specified</b> |   |  |      |         |       |      |
| $(THD + N)/S$  | total harmonic distortion-plus-noise to signal ratio        | output signal 0.72 V (RMS) at<br>$f = 1\text{ kHz}$ ; $R_L > 5\text{ k}\Omega$ (AC);<br>A-weighted | —    | −75     | −65   | dBA  |
| DR   | dynamic range   | output signal −60 dB at 1 kHz;<br>0 dB reference = 0.77 V (RMS);<br>A-weighted                     | 92   | 102     | —     | dBA  |
| DS   | digital silence   | output signal at<br>20 Hz to 17 kHz;<br>0 dB reference = 0.77 V (RMS);<br>A-weighted               | —    | −108    | −102  | dBA  |
| <b>Oscillator (<math>f_{osc} = 11.2896\text{ MHz}</math>)</b>  |   |  |      |         |       |      |
| $f_{xtal}$   | crystal frequency   |  | —    | 11.2896 | —     | MHz  |
| $f_{clk(DSP)}$   | clock frequency DSP core                                    |  | —    | 27.1656 | —     | MHz  |

**Note**

1. FMRDS and FMMPX input sensitivity setting '000' (see Table 17).

**5 ORDERING INFORMATION**

| TYPE NUMBER | PACKAGE |  |          |
|-------------|---------|--|----------|
|             | NAME    | DESCRIPTION  | VERSION  |
| SAA7705H    | QFP80   | plastic quad flat package; 80 leads (lead length 1.95 mm);<br>body $14 \times 20 \times 2.8\text{ mm}$ | SOT318-2 |

# Car radio Digital Signal Processor (DSP)

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## 6 BLOCK DIAGRAM

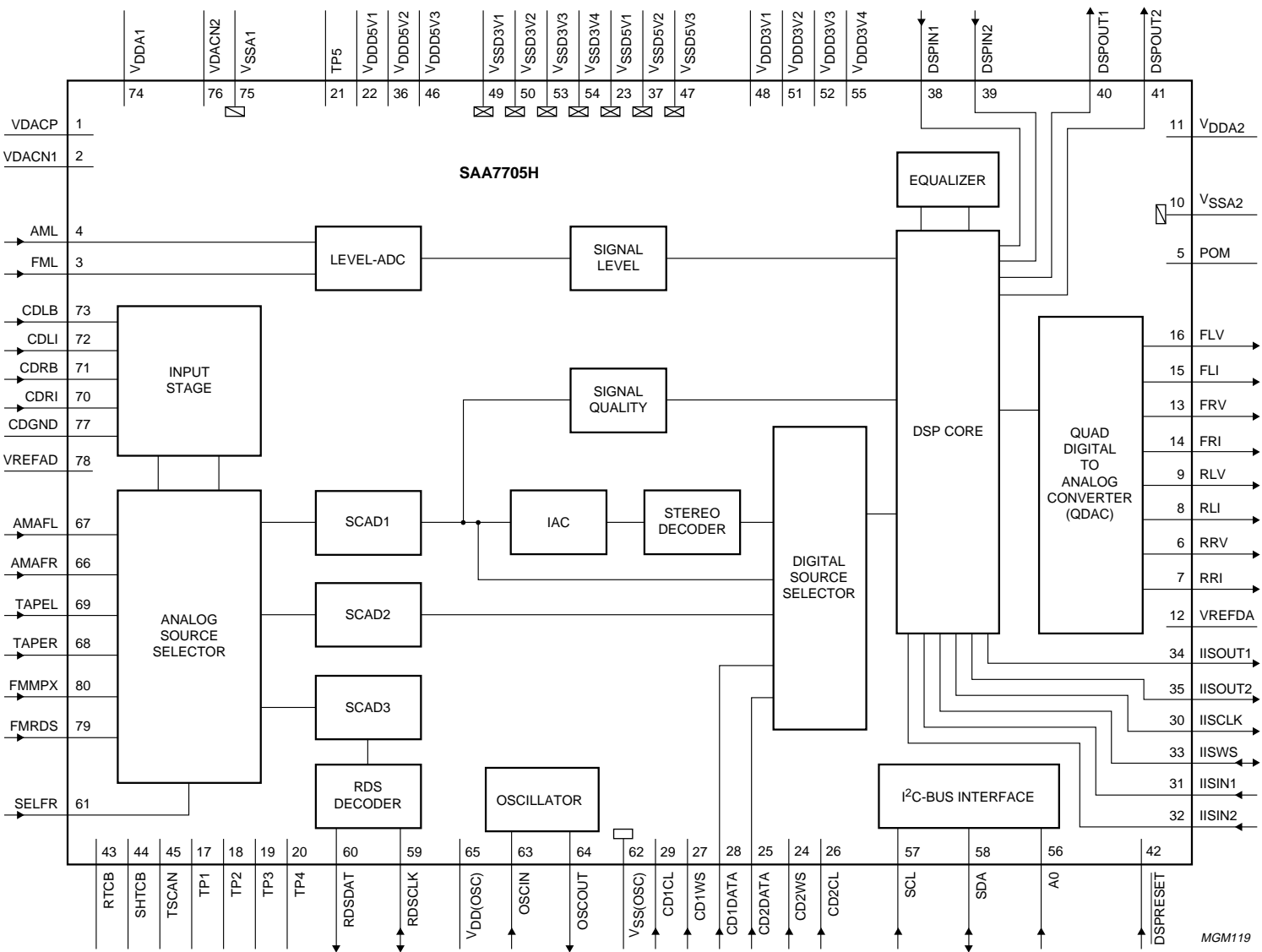


Fig.1 Block diagram.

## Car radio Digital Signal Processor (DSP)

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## 7 PINNING

| SYMBOL  | PIN | PIN TYPE | DESCRIPTION  |
|---------|-----|----------|--|
| VDACP   | 1   | AP2D     | positive reference voltage for SCAD1, SCAD2, SCAD3 and level-ADC   |
| VDACN1  | 2   | AP2D     | ground reference voltage 1 for SCAD1, SCAD2, SCAD3 and level-ADC   |
| FML     | 3   | AP2D     | FM level input; via this pin the level of the FM signal is fed to the SAA7705H; the level information is needed for a correct functioning of the weak signal behaviour |
| AML     | 4   | AP2D     | AM level input; via this pin the level of the AM signal is fed to the SAA7705H   |
| POM     | 5   | AP2D     | power-on mute of the QDAC; timing is determined by an external capacitor   |
| RRV     | 6   | AP2D     | rear right audio voltage output of the QDAC  |
| RRI     | 7   | AP2D     | rear right audio current output of the QDAC  |
| RLI     | 8   | AP2D     | rear left audio current output of the QDAC   |
| RLV     | 9   | AP2D     | rear left audio voltage output of the QDAC   |
| VSSA2   | 10  | APVSS    | ground supply for the analog part of the QDAC  |
| VDDA2   | 11  | APVDD    | positive supply for the analog part of the QDAC  |
| VREFDA  | 12  | AP2D     | decoupling for voltage reference of the analog part of the QDAC  |
| FRV     | 13  | AP2D     | front right audio voltage output of the QDAC   |
| FRI     | 14  | AP2D     | front right audio current output of the QDAC   |
| FLI     | 15  | AP2D     | front left audio current output of the QDAC  |
| FLV     | 16  | AP2D     | front left audio voltage output of the QDAC  |
| TP1     | 17  | BT4CR    | test pin, used in factory test mode, must not be connected   |
| TP2     | 18  | BT4CR    | test pin, used in factory test mode, must not be connected   |
| TP3     | 19  | BT4CR    | test pin, used in factory test mode, must not be connected   |
| TP4     | 20  | BT4CR    | test pin, used in factory test mode, must not be connected   |
| TP5     | 21  | IBUFD    | test pin, used in factory test mode, must be connected to V <sub>DD5V</sub>  |
| VDD5V1  | 22  | VDDE5    | positive supply 1 for peripheral cells   |
| VSS5V1  | 23  | VSSE5    | ground supply 1 for peripheral cells   |
| CD2WS   | 24  | IBUFD    | word select input 2 from a digital audio source (I <sup>2</sup> S-bus or LSB-justified format)   |
| CD2DATA | 25  | IBUFD    | left or right data input 2 from a digital audio source (I <sup>2</sup> S-bus or LSB-justified format)  |
| CD2CL   | 26  | IBUFD    | clock input 2 from a digital audio source (I <sup>2</sup> S-bus or LSB-justified format)   |
| CD1WS   | 27  | IBUFD    | word select input 1 from a digital audio source (I <sup>2</sup> S-bus or LSB-justified format)   |
| CD1DATA | 28  | IBUFD    | left or right data input 1 from a digital audio source (I <sup>2</sup> S-bus or LSB-justified format)  |
| CD1CL   | 29  | IBUFD    | clock input 1 from a digital audio source (I <sup>2</sup> S-bus or LSB-justified format)   |
| IISCLK  | 30  | BT4CR    | clock output to extra DSP chip (I <sup>2</sup> S-bus)  |
| IISIN1  | 31  | IBUFD    | data input channel 1 (front) from extra DSP chip (I <sup>2</sup> S-bus)  |
| IISIN2  | 32  | IBUFD    | data input channel 2 (rear) from extra DSP chip (I <sup>2</sup> S-bus)   |
| IISWS   | 33  | BD4CR    | word select input or output for extra DSP chip (I <sup>2</sup> S-bus)  |
| IISOUT1 | 34  | BD4CR    | data output to extra DSP chip (I <sup>2</sup> S-bus)   |
| IISOUT2 | 35  | BD4CR    | subwoofer output (I <sup>2</sup> S-bus)  |
| VDD5V2  | 36  | VDDE5    | positive supply 2 for peripheral cells   |
| VSS5V2  | 37  | VSSE5    | ground supply 2 for peripheral cells   |
| DSPIN1  | 38  | IBUFD    | digital input 1 of the DSP core (flag F0 of the status register)   |
| DSPIN2  | 39  | IBUFD    | digital input 2 of the DSP core (flag F1 of the status register)   |

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| SYMBOL               | PIN | PIN TYPE | DESCRIPTION   |
|----------------------|-----|----------|---|
| DSPOUT1              | 40  | B4CR     | digital output 1 of the DSP core (flag F2 of the status register)   |
| DSPOUT2              | 41  | B4CR     | digital output 2 of the DSP core (flag F3 of the status register)   |
| DSPRESET             | 42  | IBUFU    | reset input to the DSP core (active LOW)  |
| RTCB                 | 43  | IBUFD    | asynchronous reset test control block, connect to ground  |
| SHTCB                | 44  | IBUFD    | shift clock test control block, connect to ground   |
| TSCAN                | 45  | IBUFD    | scan control (active HIGH), connect to ground   |
| V <sub>DD5V3</sub>   | 46  | VDDE5    | positive supply 3 for peripheral cells  |
| V <sub>SS5V3</sub>   | 47  | VSSE5    | ground supply 3 for peripheral cells  |
| V <sub>DD3V1</sub>   | 48  | VDDI3    | positive supply 1 for DSP core  |
| V <sub>SS3V1</sub>   | 49  | VSSI3    | ground supply 1 for DSP core  |
| V <sub>SS3V2</sub>   | 50  | VSSI3    | ground supply 2 for DSP core  |
| V <sub>DD3V2</sub>   | 51  | VDDI3    | positive supply 2 for DSP core  |
| V <sub>DD3V3</sub>   | 52  | VDDI3    | positive supply 3 for DSP core  |
| V <sub>SS3V3</sub>   | 53  | VSSI3    | ground supply 3 for DSP core  |
| V <sub>SS3V4</sub>   | 54  | VSSI3    | ground supply 4 for DSP core  |
| V <sub>DD3V4</sub>   | 55  | VDDI3    | positive supply 4 for DSP core  |
| A0                   | 56  | IBUFD    | I <sup>2</sup> C-bus address selection  |
| SCL                  | 57  | SCHMITCD | serial clock input (I <sup>2</sup> C-bus)   |
| SDA                  | 58  | BD4SCI4  | serial data input/output (I <sup>2</sup> C-bus)   |
| RDSCCLK              | 59  | BD4CR    | RDS bit clock output or RDS external clock input  |
| RDSDAT               | 60  | BT4CR    | RDS data output   |
| SELFR                | 61  | IBUFD    | AD input selection switch; to enable high-ohmic FMMPX input at fast tuner search on pin FMRDS; if SELFR is HIGH, the input at pin FMRDS is put through to SCAD1 and FMRDS gets high-ohmic; this pin works together with the AD register bit SELTWOTUN (see Table 9) |
| V <sub>SS(OSC)</sub> | 62  | APVSS    | ground supply for crystal oscillator circuit  |
| OSCIN                | 63  | AP2D     | crystal oscillator input: crystal oscillator sense for gain control or forced input in slave mode   |
| OSCOUT               | 64  | AP2D     | crystal oscillator output: drive output to 11.2896 MHz crystal  |
| V <sub>DD(OSC)</sub> | 65  | APVDD    | positive supply for crystal oscillator circuit  |
| AMAFR                | 66  | AP2D     | AM audio frequency analog input (right channel)   |
| AMAFI                | 67  | AP2D     | AM audio frequency analog input (left channel)  |
| TAPER                | 68  | AP2D     | tape analog input (right channel)   |
| TAPEL                | 69  | AP2D     | tape analog input (left channel)  |
| CDRI                 | 70  | AP2D     | CD analog input (right channel)   |
| CDRB                 | 71  | AP2D     | feedback input of the CD analog input (right channel)   |
| CDLI                 | 72  | AP2D     | CD analog input (left channel)  |
| CDLB                 | 73  | AP2D     | feedback input of the CD analog input (left channel)  |
| V <sub>DDA1</sub>    | 74  | APVDD    | analog positive supply for SCAD1, SCAD2, SCAD3 and level-ADC  |
| V <sub>SSA1</sub>    | 75  | APVSS    | analog ground supply SCAD1, SCAD2, SCAD3 and level-ADC  |
| VDACN2               | 76  | AP2D     | ground reference voltage 2 for SCAD1, SCAD2, SCAD3 and level-ADC  |



## Car radio Digital Signal Processor (DSP)

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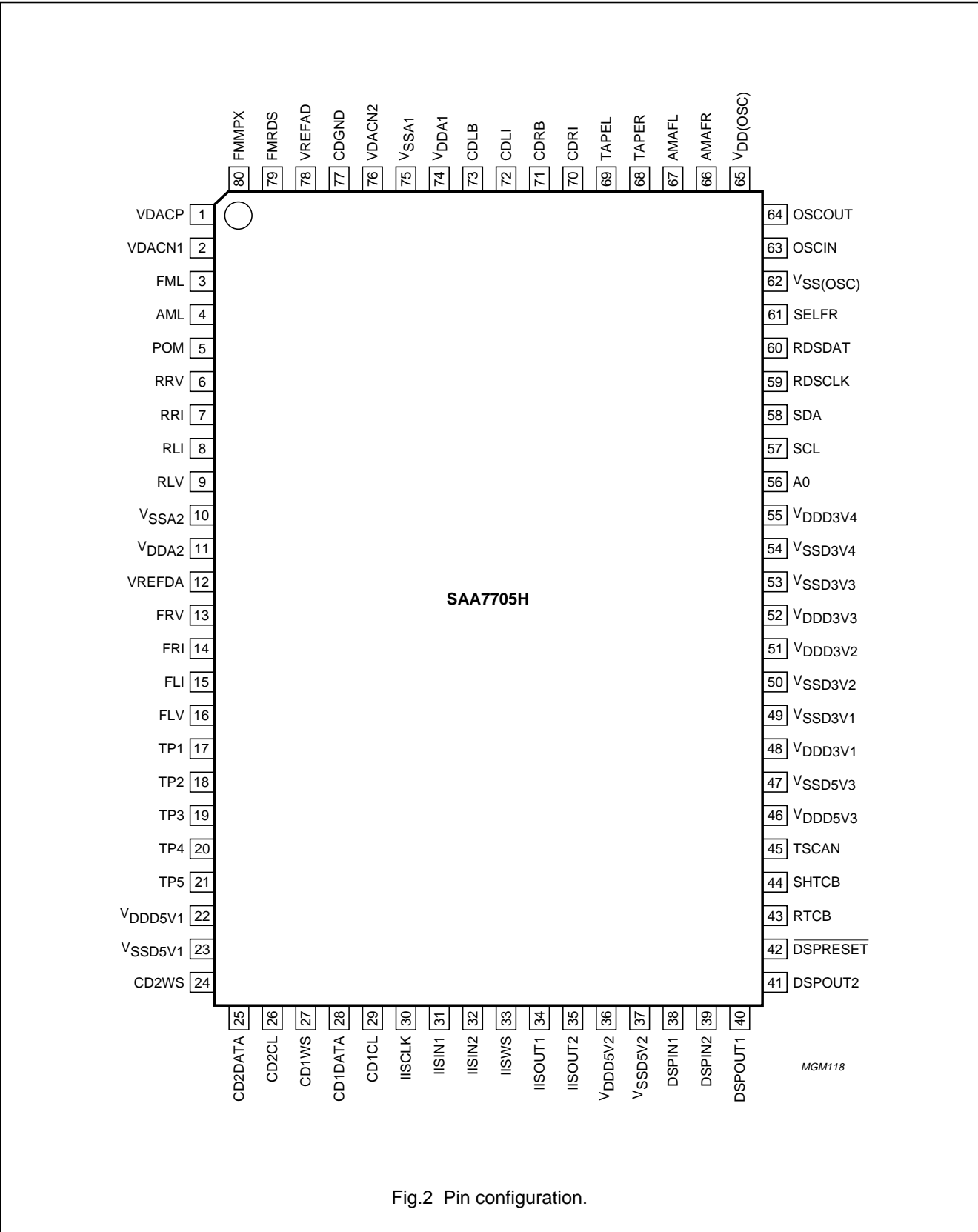
| SYMBOL | PIN | PIN TYPE | DESCRIPTION   |
|--------|-----|----------|---|
| CDGND  | 77  | AP2D     | positive reference for analog CD block                          |
| VREFAD | 78  | AP2D     | common-mode reference voltage SCAD1, SCAD2, SCAD3 and level-ADC |
| FMRDS  | 79  | AP2D     | FM RDS analog input   |
| FMMPX  | 80  | AP2D     | FM multiplex analog input                                       |

**Table 1** Explanation of pin types

| PIN TYPE | DESCRIPTION  |
|----------|--|
| AP2D     | analog input/output  |
| APVDD    | analog supply  |
| APVSS    | analog ground  |
| VDDE5    | 5 V peripheral supply  |
| VSSE5    | 5 V peripheral ground connection, no connection to the substrate                   |
| VDDI3    | 3.3 V supply to digital core and internal I/O pads                                 |
| VSSI3    | 3.3 V ground to digital core and internal I/O pads, no connection to the substrate |
| SCHMITCD | CMOS, Schmitt trigger input with active pull-down                                  |
| IBUFU    | CMOS, active pull-up to all VDDE5 pads   |
| IBUFD    | CMOS, active pull-down to all VSSE5 pads   |
| BD4CR    | bidirectional CMOS I/O buffer, 4 mA, slew rate control                             |
| BT4CR    | 4 mA CMOS 3-state output buffer, slew rate control                                 |
| B4CR     | 4 mA CMOS output buffer, slew rate control   |
| BD4SCI4  | CMOS I/O pad with open-drain output  |

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### 8 FUNCTIONAL DESCRIPTION

The SAA7705H consists of a DSP core and periphery. The DSP core is described in Sections 8.6, 8.7 and 8.11. The periphery handles the following tasks:

- FM and level information processing (see Section 8.1)
- Analog source selection and analog-to-digital conversion of the analog audio sources (see Section 8.2)
- Digital-to-analog conversion of the DSP output QDAC (see Section 8.3)
- Clock circuit and oscillator (see Section 8.4)
- Equalizer accelerator circuit (see Section 8.5)
- I<sup>2</sup>C-bus interface (see Section 8.8 and Chapter 12)
- RDS decoder (see Section 8.10).

#### 8.1 FM and level information processing

##### 8.1.1 SIGNAL PATH FOR LEVEL INFORMATION

For FM weak signal processing and for AM and FM purposes (absolute level and multipath), an FM level and an AM level input is implemented (pins FML and AML). In the case of radio reception clocking of the filters and the level-ADC is based on a 38 kHz sample frequency. The DC input signal is converted by a bitstream first-order Sigma-Delta ADC followed by a decimation filter.

The input signal has to be obtained from the radio part. Two different configurations for AM and FM reception are possible:

- A circuit with two separate level signals: one for FM level and one for AM level
- A combined circuit with AM and FM level information on the FM level input.

The level input is selected with bit LEVAM-FM of the SEL register (see Table 12 and Chapter 12).

##### 8.1.2 SIGNAL PATH FROM FMMPX INPUT TO IAC AND STEREO DECODER

The SAA7705H has four analog audio source channels. One of the analog inputs is the FM multiplex signal. Selection of this signal can be achieved by the SEL register bits AUX-FM and CD-TAPE (see Table 12). The multiplexed FM signal is converted to the digital domain in SCAD1, a bitstream third-order SCAD. The first decimation with a factor of 16 takes place in down sample filter ADF1. This decimation filter can be switched by means of the SEL register bit WIDE-NARROW (see Table 12) in the wide or narrow band position. In case

of FM reception, it must be in the narrow position.

The FMMPX path is followed by the sample-and-hold switch of the IAC (see Section 8.1.5) and the 19 kHz pilot signal regeneration circuit. A second decimation filter reduces the output of the IAC to a lower sample rate. One of the two filter outputs contains the multiplexed signal with a frequency range of 0 to 60 kHz.

The outputs of this signal path to the DSP (which are all running on a sample frequency of 38 kHz) are:

- Pilot presence indication: Pilot-I. This one bit signal is LOW for a pilot frequency deviation <4 kHz and HIGH for a pilot frequency deviation >4 kHz and locked on a pilot tone.
- FM reception stereo signal. This is the 18-bit output of the stereo decoder after the matrix decoding in Information System Network (ISN) I<sup>2</sup>S-bus format. This signal is fed via a multiplexer to a general I<sup>2</sup>S-bus interface block that communicates with the DSP core.
- A noise level indication. This signal is derived from the first MPX decimation filter via a wide band noise filter. Detection is done with an envelope detector. This noise level is filtered in the DSP core and is used to optimize the FM weak signal processing.

##### 8.1.3 INPUT SENSITIVITY FOR FM AND RDS SIGNALS

The FM and RDS input sensitivity is designed for tuner front ends which deliver an output voltage varying from 65 to 225 mV (RMS) at a sweep of 22.5 kHz for a 1 kHz tone. The intermediate standard input sensitivities can be reached in steps of 1.6 dB, to be programmed with the AD register bits VOLFM and VOLRDS (see Tables 9 and 17). The volume control of the FMMPX and the FMRDS input can be controlled separately. VOLFM and VOLRDS = 000 is the most sensitive position, VOLFM and VOLRDS = 111 the least sensitive position. Due to the analog circuit control of the volume gain, the input impedance of pin FMMPX or pin FMRDS changes with the volume setting.

##### 8.1.4 AD INPUT SELECTION SWITCH

Pin SELFR makes it possible to change to another transmitter frequency with the same radio program to assess the quality of that signal. In case of a stronger transmitter signal the decision can be made by the software to switch to the new transmitter. The FMMPX input is normally used to process the FM signal. This FMMPX input is connected via a relative large capacitor to the MPX tuner output. Switching the tuner to another transmitter frequency means another DC voltage level on the MPX output of the tuner and a charging of the

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series capacitor (because the FMMPX input of the SAA7705H is low-ohmic). Pulling SELFR HIGH during such an update, causes the FMMPX input to become high-ohmic, preventing charging of the capacitor. The signal probing of the new transmitter quality is done via the FMRDS input.

#### 8.1.5 INTERFERENCE ABSORPTION CIRCUIT

The Interference Absorption Circuit (IAC) detects and suppresses ignition interference. This hardware IAC is a modified, digitized and extended version of the analog circuit which is in use for many years already.

The IAC consists of an MPX mute function switched by mute pulses from two ignition interference pulse detectors. A third detector inhibits muting.

The three detectors are:

- **Interference detector:** The input signal of the first detector is the output signal of SCAD1. This interference detector analyses the high frequency contents of the MPX signal. The discrimination between interference pulses and other signals is performed by a special Philips patented fuzzy logic such as algorithm and is

based on probability calculations. This detector performs optimally with higher antenna voltages.

On detection of ignition interference, this logic will send appropriate pulses to the MPX mute switch.

- **Level detector:** The input signal of the second detector is the FM level signal (the output of the level-ADC). This detector performs optimally with lower antenna voltages. It is therefore complementary to the first detector. The characteristics of both ignition interference pulse detectors can be adapted to the properties of different FM front ends by means of the coefficients in the IAC register and the level-IAC register (see Section 12.4). Both IAC detectors can be switched on or off independently. Both IAC detectors can mute the MPX signal independently.
- **Dynamic detector:** The third detector is the dynamic IAC circuit. This detector switches off the IAC completely if the frequency deviation of the FM multiplex signal is too high. The use of narrow band IF filters can result in AM modulation. This AM modulation could be interpreted by the IAC circuitry as interference caused by the car's engine.

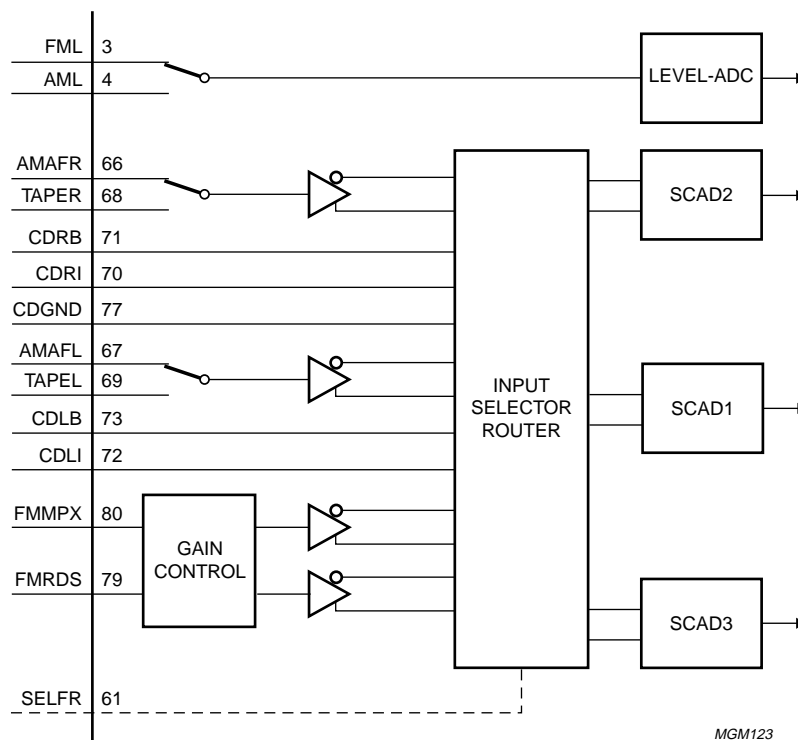


Fig.3 Analog input switching circuit.

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Parameter setting for the IAC detectors is done by means of 5 different coefficients. Upon reset, the nominal setting for a good performing IAC detector is selected.

### 8.1.5.1 AGC set point (1 bit)

In case the sensitivity and feed-forward factor are out of range in a certain application, the set point of the AGC can be shifted. The set point controls the sensitivity of the other IAC control parameters. See bit 11 of the IAC register (Table 11).

### 8.1.5.2 Threshold sensitivity offset (3 bits)

With this parameter the threshold sensitivity of the comparator in the interfering pulse detectors can be set. It also influences the amount of unwanted triggering. Settings are according to Table 25.

### 8.1.5.3 Deviation feed-forward factor (3 bits)

This parameter determines the reduction of the sensitivity of the detector by the absolute value of the MPX signal. This mechanism prevents the detector from unwanted triggering at noise with modulation peaks. In Table 24 the possible values are given.

### 8.1.5.4 Suppression stretch time (3 bits)

This parameter sets the duration of the pulse suppression after the detector has stopped sending a trigger pulse. It can be switched off by setting the value '000'. The duration can be selected in steps of one period of the 304 kHz (3.3  $\mu$ s) sample frequency. In Table 23 the possible values are given.

### 8.1.5.5 MPX delay (2 bits)

With this parameter the delay time between 2 and 5 samples of the 304 kHz sample frequency can be selected. The needed value depends on the used front end of the car radio. Settings are according to Table 22.

### 8.1.5.6 Level-IAC threshold (4 bits)

With this parameter the sensitivity of the comparator in the ignition interference pulse detector can be set. It also influences the amount of unwanted triggering. The possible values are given in Table 21. The prefix value '0000' switches off the level-IAC function.

### 8.1.5.7 Level-IAC feed-forward setting (2 bits)

This parameter allows for adjusting delay differences in the signal paths from the FM antenna to the MPX mute, namely, via the FM level-ADC and level-IAC detection and

via the FM demodulator and MPX conversion and filtering. These differences depend on the front end used in the car radio. With a simultaneous appearance of a peak disturbance at the FM level input and the MPX ADC input of the IC, a zero delay setting takes care for the level-IAC mute pulse to coincide with the passage of the disturbance in the MPX mute circuit. The setting for the level-IAC feed-forward allows to advance the mute pulse by 1 sample period or to delay it by 1 or 2 sample periods of the 304 kHz clock, with respect to the default value. The appropriate register bits for each setting are given in Table 20.

### 8.1.5.8 Level-IAC suppression stretch time (2 bits)

This parameter sets the time that the mute pulse is stretched when the FM level input has stopped exceeding the threshold. The duration can be selected in steps of one period of the 304 kHz (3.3  $\mu$ s) sample frequency. In Table 19 the possible values are given.

### 8.1.5.9 Dynamic IAC threshold levels

If enabled by bit 15 of the LEVELIAC register, this block will disable temporarily all IAC actions if the MPX mono signal exceeds a threshold deviation (threshold 1) for a given time with a given excess amount (threshold 2). This MPX mono signal is separated from the MPX signal with a low-pass filter with the -3 dB corner point at 15 kHz. The possible values of this threshold are given in Table 18.

### 8.1.5.10 IAC testing mode

The internal IAC trigger signal is visible on pin DSPOUT2 if bit IACTRIGGER of the IAC register is set. In this mode the effect of the parameter settings on the IAC performance can be verified.

## 8.2 Analog source selection and analog-to-digital conversion

### 8.2.1 INPUT SELECTION SWITCHES

In Fig.3 the block diagram of the input is shown. The input selection is controlled by bits in the input selector control register and the input selection pin SELFR. The relationship between these bits and the switches is indicated in Table 26.

### 8.2.2 SIGNAL FLOW OF THE AM, ANALOG CD AND TAPE INPUTS

The signal of the two single-ended stereo AM inputs can be selected by the correct values of the SEL register bits according to Table 26.

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The AM and the TAPE inputs are buffered with an operational amplifier to ensure a high-impedance input which enables the use of an external resistor divider for signal reduction. For correct biasing of the first operational amplifier a resistor must be connected between the input and pin VREFAD, which acts as a virtual ground (see Fig.21). The analog input switching circuit is shown in Fig.3. The input for an analog CD player is explained in more detail in Section 8.2.3.

### 8.2.3 THE ANALOG CD BLOCK

Special precautions are taken to realize a high Common-Mode Rejection Ratio (CMRR) in case of the use of a CD player output processed via analog inputs. The block diagram is shown in Fig.4. The operational amplifiers OAR and OAL are used as buffers. The gain of these operational amplifiers can be adjusted via the external resistors and is in this case 0.54 by using a 8.2 k $\Omega$  and a 15 k $\Omega$  resistor.

The reference inputs of these operational amplifiers are connected to a separate pin CDGND. This pin is on one side AC connected to the ground shielding of the cable coming from the CD player and via a resistor  $>1\text{ M}\Omega$  to pin VREFAD. In this configuration the common-mode signal propagates all the way to the SCAD block inputs of SCAD1 and SCAD2. The SCADs themselves have a good rejection ratio for in-phase common-mode signals.

Which part of the common-mode signal is processed as the real input signal depends on the ratio of the CDGND resistor and the series resistor in the cable and the difference in input offset of the operational amplifiers. The induced signals on the CDLI and CDRI lines are of the same amplitude and therefore rejected as common-mode signals in the SCADs.

#### 8.2.4 PIN VREFAD

The middle reference voltage of the SCAD1, SCAD2, SCAD3 and level-ADC can be filtered via this pin. This voltage is used as half the supply reference of the SCAD1, SCAD2, SCAD3 and as the positive reference for the level-ADC and buffers. External capacitors (connected to  $V_{SSA1}$ ) prevent crosstalk between the SCADs and buffers and improve the power supply rejection ratio of all blocks. This pin must also be used as a reference for the inputs AMAFL, AMAFR, TAPEL, TAPER and CDGND.

### 8.2.5 PINS VDACN1, VDACN2 AND VDACP

These pins are used as ground and positive supply reference for the SCAD1, SCAD2, SCAD3 and the level-ADC. For optimal performance, pins VDACC1 and VDACC2 must be directly connected to the  $V_{SSA1}$  and pin VDACP to the filtered  $V_{DDA1}$ .

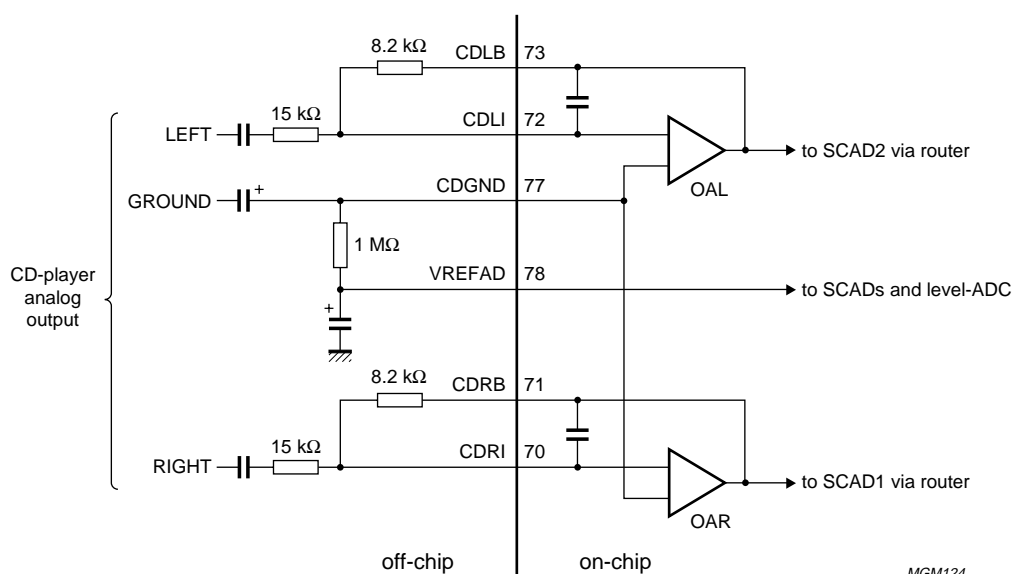


Fig.4 Analog CD block.

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8.2.6 SUPPLY OF THE ANALOG INPUTS

The analog input circuit has separate power supply connections to allow maximum filtering of the analog supply voltages:  $V_{SSA1}$  for the analog ground and  $V_{DDA1}$  for the analog supply.

8.3 Analog outputs

8.3.1 DACs

Each of the four low noise high dynamic range DACs consists of a 15-bit signed magnitude DAC with current output, followed by a buffer operational amplifier. For each of the four audio output channels a separate convertor is used. Each converter output is connected to the inverting input of one of the four internal CMOS operational amplifiers. The non-inverting input of this operational amplifier is connected to the internal reference voltage. Together with an internal resistor the conversion of current-to-voltage of the audio output is achieved.

8.3.2 UPSAMPLE FILTER

To reduce spectral components above the audio band, a fixed 4 times oversampling and interpolating 18-bit digital IIR filter is used. It is realized as a bit serial design and consists of two consecutive filters. The data path in these filters is 22 bits to prevent overflow and to maintain a

signal-to-noise ratio larger then 105 dB. The word clock for the upsample filter ( $4 \times f_s$ ) is derived from the audio source timing. If the internal audio source is selected, the sample frequency can be either 44.1 or 38 kHz. In case of external digital sources (CD1 and CD2), a sample frequency from 32 to 48 kHz is possible.

8.3.3 VOLUME CONTROL

The total volume control has a dynamic range of more than 100 dB (0 dB being maximal input on the I<sup>2</sup>S-bus input). With the signed magnitude noise shaped 15-bit DAC and the internal 18-bit registers (these registers provide the digital data communication between the DSP and the QDAC) of the DSP core a useful digital volume control range of 100 dB is possible by calculating the corresponding coefficients.

The step size is freely programmable and an additional analog volume control is not needed in this design. The SNR of the audio output at full-scale is determined by the total 15 bits of the converter. The noise at low outputs is fully determined by the noise performance of the DAC. Since it is a signed magnitude type, the noise at digital silence is also low. The disadvantage is that the total THD is higher than conventional DACs. The typical THD-plus-noise versus output level is shown in Fig.5.

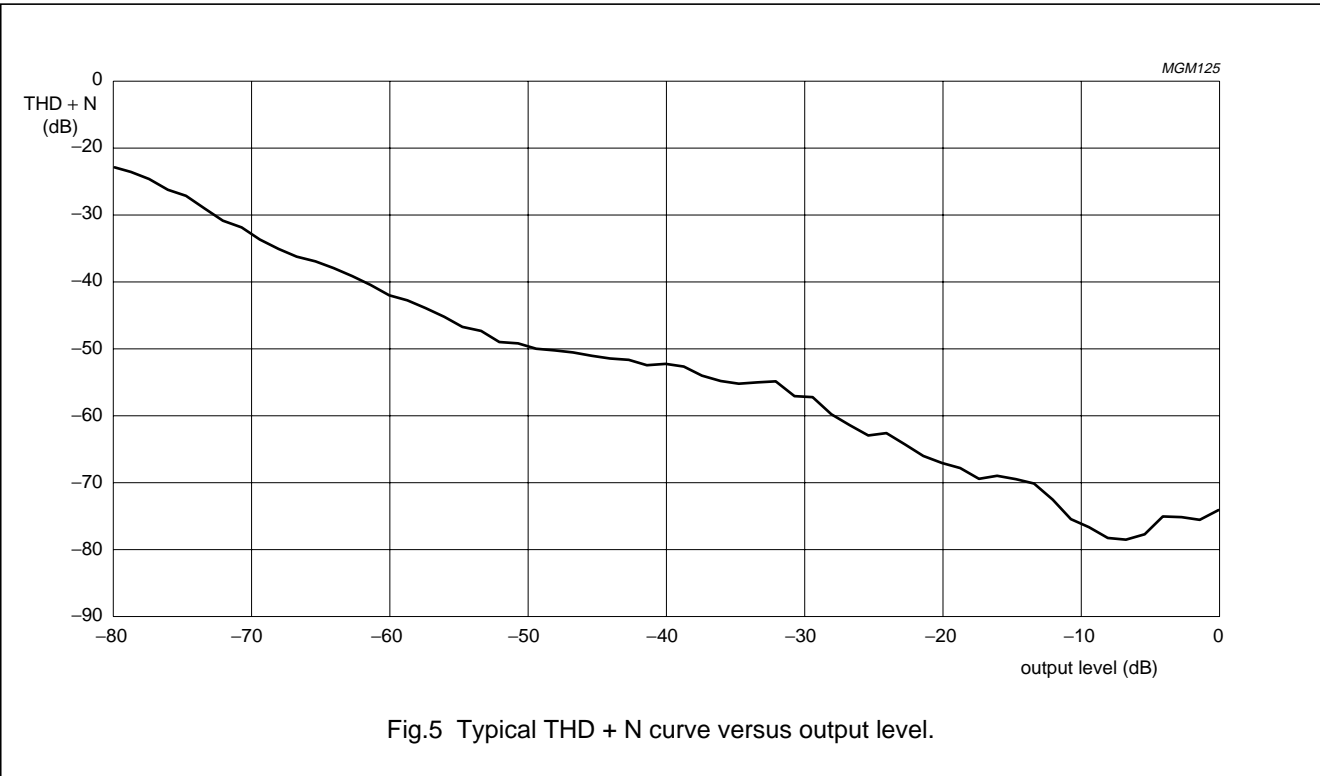


Fig.5 Typical THD + N curve versus output level.



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### 8.3.4 FUNCTION OF PIN POM

With pin POM it is possible to switch-off the reference current of the DAC. The capacitor on pin POM (see Fig.21) determines the time after which this current has a soft switch-on. At power-on, the current audio signal outputs are always muted. The external capacitor is loaded in two stages via two different current sources. The loading starts at a current level that is 9 times lower than the load current after the voltage on pin POM has risen above 1 V. This results in an almost dB-linear behaviour. However, the DAC has an asymmetrical supply and the DC output voltage will be half the supply voltage under functional conditions. During start-up the output voltage is not defined as long as the supply voltage is below the threshold voltages of the transistors. A small jump in DC is possible at start up. In this DC jump audio components can be present.

### 8.3.5 POWER-OFF PLOP SUPPRESSION

To avoid plops in a power amplifier, the supply voltage (3.3 V) for the analog part of the DAC can be supplied from the 5 V supply via a transistor. A capacitor is connected to  $V_{DDA2}$  to maintain power to the analog part if the 5 V supply is switched off fast. In this case the output voltage will decrease gradually allowing the power amplifier some extra time to switch-off without audible plops.

### 8.3.6 THE INTERNAL PIN VREFDA

Using two internal resistors, half of the supply voltage  $V_{DDA2}$  is obtained and coupled to an internal buffer. This reference voltage is used as a DC voltage for the output operational amplifiers and as a reference for the DAC. In order to obtain the lowest noise and to have the best ripple rejection, a capacitor has to be connected between this pin and ground.

### 8.3.7 INTERNAL DAC CURRENT REFERENCE

As a reference for the internal DAC current and also for the DAC current source output, a current is drawn from pin VREFDA to  $V_{SSA2}$  (ground) via an internal resistor. The value of this resistor determines also the DAC current (absolute value). Consequently, the absolute value of the current varies from device to device due to the spread of the reference resistor value. This, however, has no influence on the absolute output voltages because these voltages are derived from a conversion of the DAC current to the actual output voltage via internal resistors.

### 8.3.8 SUPPLY OF THE ANALOG OUTPUTS

All the analog circuitry of the DACs and the operational amplifiers are powered by 2 pins:  $V_{DDA2}$  and  $V_{SSA2}$ .  $V_{DDA2}$  must have sufficient decoupling to prevent high THD and to ensure a good Power Supply Rejection Ratio (PSRR). The digital part of the DAC is fully supplied from the DSP core supply.

## 8.4 Clock circuit and oscillator

The device has an on-chip oscillator. The block diagram of this Pierce oscillator is shown in Fig.6. The active element needed to compensate for the loss resistance of the crystal is the block  $G_m$ . This block is placed between the external pins OSCIN and OSCOUT. The gain of the oscillator is internally controlled by the AGC block. A sine wave with a peak-to-peak voltage close to the oscillator power supply voltage is generated. The AGC block prevents clipping of the sine wave and therefore the generation of harmonics as much as possible. At the same time the voltage of the sine wave is as high as possible which reduces the jitter going from the sine wave to the clock signal.

### 8.4.1 SUPPLY OF THE CRYSTAL OSCILLATOR

The supply of the oscillator is separated from the other supplies. This minimizes the feedback from the ground bounce of the chip to the oscillator circuit. Pin  $V_{SS(OSC)}$  is used as ground and pin  $V_{DD(OSC)}$  as positive supply.

### 8.4.2 THE PHASE-LOCKED LOOP CIRCUIT TO GENERATE THE DSP CLOCK AND OTHER DERIVED CLOCKS

A PLL circuit is used to generate the DSP clock and other derived clocks.

The minimum equalizer clock frequency is  $480f_s$ . If  $f_s$  equals 44.1 kHz, this results in a minimum oscillator frequency of 21.1687 MHz. Crystals for the crystal oscillator in the range of twice the required DSP clock frequency (approximately 40 MHz) are always third-overtone crystals and must be manufactured on customer demand. This makes these crystals expensive. The PLL enables the use of a commonly available crystal operating in fundamental mode. For this circuit a 11.2896 MHz ( $256 \times 44.1$  kHz) crystal is chosen. This type of crystal is widely used.



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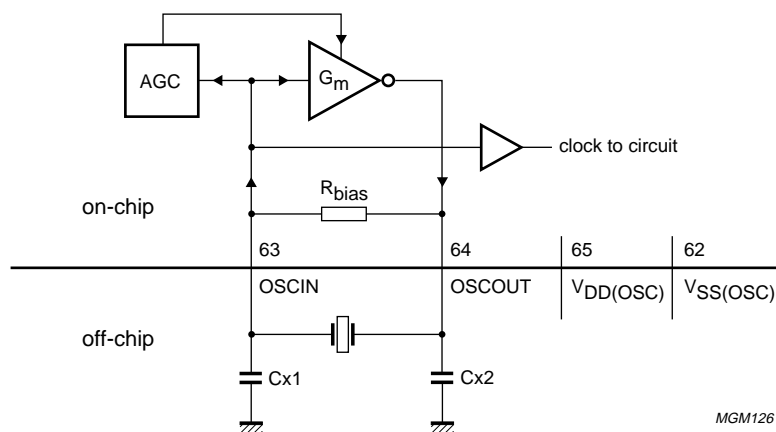


Fig.6 Block diagram of the oscillator circuit.

Although multiples of the crystal frequency of 11.2896 MHz fall within the FM reception band, this will not disturb the reception. The relatively low frequency crystal is driven in a controlled way and the resonating crystal produces harmonics of a very low amplitude in the FM reception band.

The block diagram of the programmable PLL is shown in Fig.7. The oscillator is used in a fundamental mode. The 11.2896 MHz oscillator frequency is divided by 256 and the resulting signal is fed to the phase detector as a reference signal. The base for the clock signal is a current controlled oscillator (free running frequency 70 to 130 MHz).

After having been divided by 4, the required clock frequency for the DSP core is available. To close the loop this signal is further divided by 4 and by the PLL clock division factor N. N can be programmed with the DCSCTR register bits PLL-DIV (see Tables 7 and 15) in the range from 93 to 181. This provides some flexibility in the choice of the crystal frequency.

With the recommended crystal,  $N = 154$  and the DSP clock frequency ( $f_{\text{DSP}}$ ) equals 27.1656 MHz.  $N = 154$  is the default position at start-up. By setting the AD register bit DSPTURBO (see Tables 9 and 15), the PLL output frequency, and consequently  $f_{\text{DSP}}$ , can be doubled. This feature is not used in the proposed application.

The clock frequency of the PLL oscillator divided by two ( $2f_{\text{DSP}}$ ) is also used as the clock for the DCS block.

#### 8.4.3 THE CLOCK BLOCK

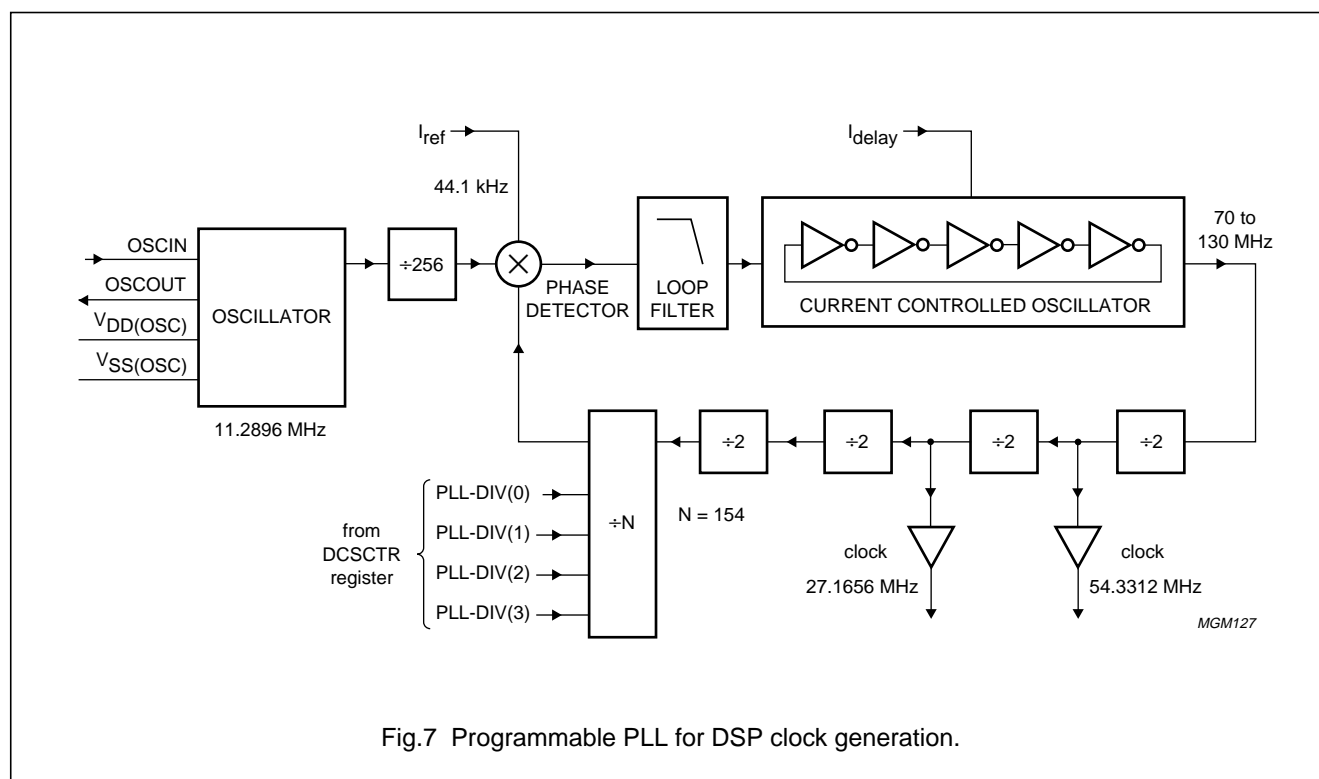
For the digital stereo decoder a clock signal is needed which is the 512-multiple of the pilot tone frequency of the FM multiplex signal. This is done by the Digitally Controlled Sampling (DCS) block, which generates this  $512 \times 19 \text{ kHz} = 9.728 \text{ MHz}$  clock, the DCS clock, by locking to the pilot frequency. This block is also able to generate other frequencies. It is controlled by the DCSCTR and DCSDIV registers (see Tables 7 and 8). Default settings of the DCS and the PLL guarantee correct functioning of the DCS block.

#### 8.4.4 SYNCHRONIZATION WITH THE CORE

In case of I<sup>2</sup>S-bus input the system can run on audio sample frequencies of  $f_s = 32 \text{ kHz}$ ,  $38 \text{ kHz}$ ,  $44.1 \text{ kHz}$  or  $48 \text{ kHz}$ . After processing of an input sample, the Input flag (I-flag) of the status register (see Section 8.7) of the DSP core is set to logic 1 during 4 clock cycles on the falling edge of the internal or external I<sup>2</sup>S-bus WS pulses. This flag can be tested with a conditional branch instruction in the DSP. This synchronisation starts in parallel with the input signal due to the short period that the I-flag is set. It is obvious that the higher  $f_s$  the lower the number of cycles available in the DSP program.

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## 8.5 Equalizer accelerator circuit

### 8.5.1 INTRODUCTION

The Equalizer accelerator (EQ) circuit is an equalizer circuit used as a hardware accelerator to the DSP core. Its inputs and outputs are stored in registers of the DSP core (these registers provide the digital data communication between the equalizer and the DSP core). The flag that starts the DSP program, refreshes the EQ input and output registers and starts the EQ controller.

The EQ circuit contains one second-order filter data path that is twenty-fold multiplexed. With this circuit, a two-channel equalizer of 10 second-order sections per channel or a four-channel equalizer of 5 second-order sections per channel can be realized.

The centre frequency, gain and Q-factor of all 20 second-order sections can be set independently from each other. Every section is followed by a variable attenuation of 0 or 6 dB. Per section, 4 bytes are needed to store the settings. During an audio sample period, all settings are read as 16-bit words in 80 read accesses to the coefficient memory.

### 8.5.2 EQ CIRCUIT OVERVIEW

This EQ circuit contains the following parts:

- A second-order filter data path, with programmable coefficients and with 40 state registers, supporting storage of the two filter states for 20 multiplexed filters; this part is clocked by a gated clock
- Signal routing around this filter data path, consisting of:
  - buses and selectors to configure the 20 filter sections for two or four channels;
  - input and output registers, with proper interfacing with the DSP core and with conversions between parallel and serial formats.
- A coefficient memory, to be loaded via the I<sup>2</sup>C-bus interface
- A controller, started by the write pulse for input and output registers, that controls the signal routing, controls the clock for the filter data path, addresses the coefficient memory and controls its programming.

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**Table 2** Equalizer port list

| NAME                         | DESCRIPTION  |
|------------------------------|--|
| <b>Data to/from DSP core</b> |  |
| IN FL                        | Front Left input bus, 18 bits  |
| IN FR                        | Front Right input bus, 18 bits   |
| IN RL                        | Rear Left input bus, 18 bits   |
| IN RR                        | Rear Right input bus, 18 bits  |
| OUT FL                       | Front Left output bus, 18 bits   |
| OUT FR                       | Front Right output bus, 18 bits  |
| OUT RL                       | Rear Left output bus, 18 bits  |
| OUT RR                       | Rear Right output bus, 18 bits   |
| <b>From EQ register</b>      |  |
| TWO-FOUR                     | two or four channel configuration switch, I <sup>2</sup> C-bus controlled; see Table 9 |
| <b>Control from DSP</b>      |  |
| clk <sub>CORE</sub>          | DSP core clock, at least 480f <sub>s</sub>   |
| start                        | new sample start pulse, input and output registers written                             |
| data-valid                   | new coefficient word available   |
| acknowledge                  | new coefficient word loaded in coefficient memory                                      |
| new-address                  | address for new coefficient word, 6 bits, range is from 0 to 39                        |
| new-coefword                 | new coefficient word, 16 bits  |

In Table 2 the port pinning is depicted. This equalizer accelerator circuit (EQ) can make a two-channel equalizer of 10 second-order sections per channel or a four-channel equalizer of 5 second-order sections per channel depending on the value of AD register bit TWO-FOUR (see Table 9). It takes an input sample set of 2 (stereo) samples or 4 (stereo front and rear) samples via 4 input registers. It delivers an output sample set of 2 or 4 samples via 4 output registers. All input and output registers are 18 bits wide.

A pulse of three clock cycles long of the signal start based on the word select of the used signal path refreshes the EQ input and output registers and starts up the EQ controller.

This sequence is shown in Fig.8.

### 8.5.3 CONTROLLER AND PROGRAMMING CIRCUIT

A controller is used to generate the bit control and word control signals for the filter section data path, the addresses for the coefficient memory and the control signals for the input and output selections and conversions. Depending on the AD register bit TWO-FOUR (see Table 9), control signals for a two- or four-channel equalizer are generated.

The 40 coefficient words should be addressed via 40 registers (addresses 0F80H to 0FA7H).

The new coefficient word rate must be slower than 0.5f<sub>s</sub>, e.g. 22 kHz. The equalizer is programmed by dedicated software.

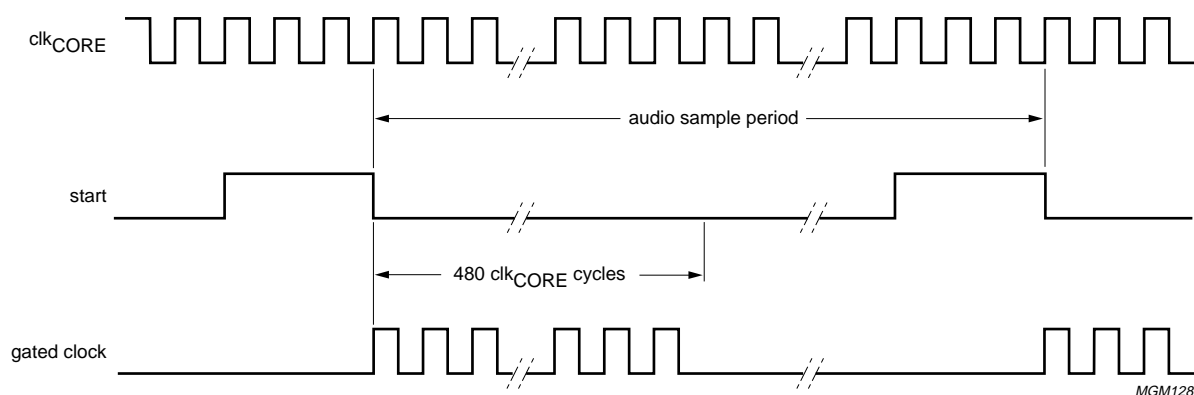


Fig.8 Derivation of the gated clock from clk<sub>CORE</sub>.

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### 8.6 The DSP core

This IC comprises a DSP core (the actual programmable embedded calculating machine) that is adapted to the required calculation power needed and as such is optimized on area.

This DSP core is also known under the name EPICS6, of which EPICS is the generic name of this type of DSP and 6 is the version number. This DSP is mainly a calculator designed for real time processing (at  $f_s = 38$  or  $44.1$  kHz) of the digitized audio data stream. A DSP is especially suited to calculate the sum of products of the data words representing the audio data. See Chapter 13 for document references on EPICS6.

### 8.7 External control pins and status register

The DSP core contains a 9-bit status register. These 9 flags contain information which is used by the conditional branch logic of the DSP core. For external use, the flags F0, F1, F2 and F3 are available. Pins DSPIN1 and DSPIN2 control the status of the flags F0 and F1. The two status flags F3 and F4 are controlled by the DSP core and can be read via the pins DSPOUT1 and DSPOUT2. The function of each pin depends on the DSP program. Another important flag is the I-flag. This flag is an input flag and is set the moment new I<sup>2</sup>S-bus data or another type of digital audio data is available to the DSP core.

### 8.8 I<sup>2</sup>C-bus interface (pins SCL and SDA)

The I<sup>2</sup>C-bus format is described in *"The I<sup>2</sup>C-bus and how to use it"*, order no. 9398 393 40011.

For the external control of the SAA7705H a fast I<sup>2</sup>C-bus is implemented. This is a 400 kHz bus which is downward compatible with the standard 100 kHz bus.

There are three different types of control instructions:

- Instructions to control the DSP program, programming the coefficient RAM and reading the values of parameters (level, multipath etc.)

- Instructions to control the equalizer and to program the equalizer coefficient RAM to be able to change the centre frequency, gain and Q-factor of the equalizer sections
- Instructions controlling the I<sup>2</sup>S-bus data flow, such as source selection, IAC control and clock speed.

The detailed description of the I<sup>2</sup>C-bus and the description of the different bits in the memory map is given in Chapter 12.

### 8.9 I<sup>2</sup>S-bus inputs and outputs

For communication with external digital sources, the I<sup>2</sup>S-bus digital interface bus is used. It is a serial 3-line bus, having one line for data, one line for clock and one line for the word select. For external digital sources the SAA7705H acts as a slave, so the external source is master and supplies the clock.

The I<sup>2</sup>S-bus input is capable of handling Philips I<sup>2</sup>S-bus and LSB-justified formats of 16, 18 and 20-bit word sizes. The selection of the digital audio format is described in Tables 13 and 28. See Fig.9 for the general waveform formats of the four possible formats.

The number of bit clock (BCK) pulses may vary in the application. When the applied word length is shorter than 18 bits (internal resolution), the LSBs will get internally a random value. When the applied word length exceeds 18 bits, the LSBs are skipped.

The input circuitry is limited in handling the number of BCK pulses per WS period. The maximum allowed number of bit clocks per WS channel (half of the symmetrical WS period) is 128.

The DSP program is synchronized with the external source via the word select signal. On every negative edge of the IISWS the I-flag of the status register is set.

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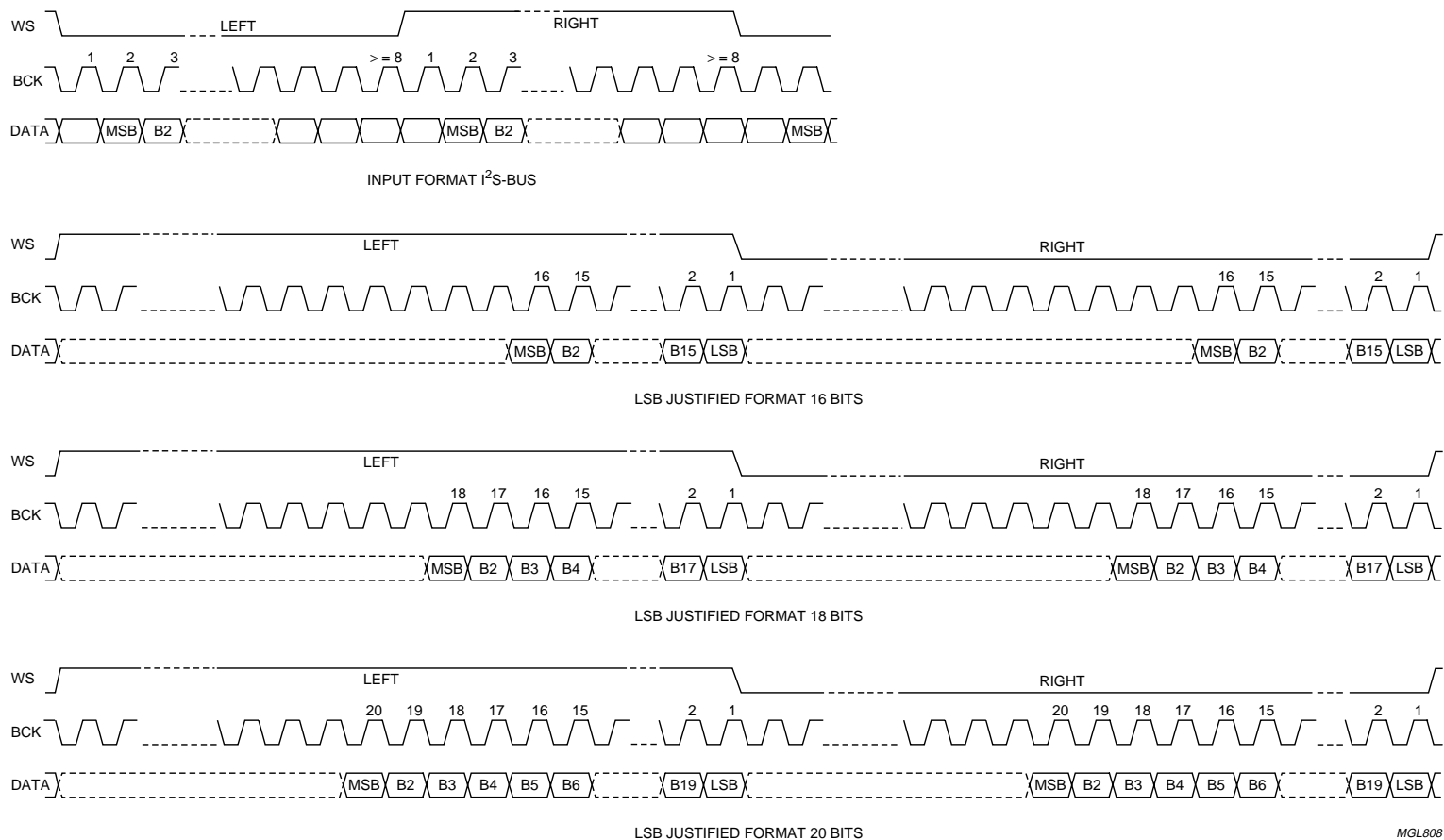


Fig.9 Available serial digital audio data in/output formats.

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**8.10 RDS decoder (pins RDSCCLK and RDSDAT)**

The RDS decoder recovers the additional inaudible RDS information which is transmitted by FM radio broadcasting. The (buffered) data is provided as output for further processing by a suitable decoder. The operational functions of the decoder are in accordance with the "European Broadcasting Union (EBU) specification EN 50067".

The RDS decoder has three different functions:

- Clock and data recovery from the FM multiplex signal
- Buffering of 16 bits, if selected
- Interfacing with the microcontroller.

**8.10.1 CLOCK AND DATA RECOVERY**

The RDS chain has a separate input. This enables RDS updates during tape play and also the use of a second receiver for monitoring the RDS information of signals from another transmitter (double tuner concept). It can as such be done without interruption of the audio program. The MPX signal from the main tuner of the car radio can be connected to this RDS input via the built-in source selector. The input selection is controlled by bit RDS-CLKIN of the RDSCTR register (see Table 14).

The RDS chain contains a third-order Sigma-Delta ADC, followed by two decimation filters. The first filter passes the multiplex band including the signals around 57 kHz and reduces the Sigma-Delta noise.

The second filter reduces the RDS bandwidth around 57 kHz.

The quadrature mixer converts the RDS band to the frequency spectrum around 0 Hz and contains the appropriate Q/I signal filters. The final decoder with CORDIC recovers the clock and data signals. These signals are output on pins RDSCCLK and RDSDAT.

**8.10.2 TIMING OF CLOCK AND DATA SIGNALS**

The timing of the clock and data output is derived from the incoming data signal. Under stable conditions the data will remain valid for 400  $\mu$ s after the clock transition.

The timing of the data change is 100  $\mu$ s before a positive clock change. This timing is suited for positive as well as negative triggered interrupts on a microcontroller.

The RDS timing is shown in Fig.10.

During poor reception it is possible that faults in phase occur, then the duty cycle of the clock and data signals will vary from minimum 0.5 times to a maximum of 1.5 times the standard clock periods. Normally, faults in phase do not occur on a cyclic basis.

**8.10.3 BUFFERING OF RDS DATA**

The repetition of the RDS data is around the 1187 Hz. This results in an interrupt on the microcontroller for every 842  $\mu$ s. In a second mode, the RDS interface has a double 16-bit buffer.

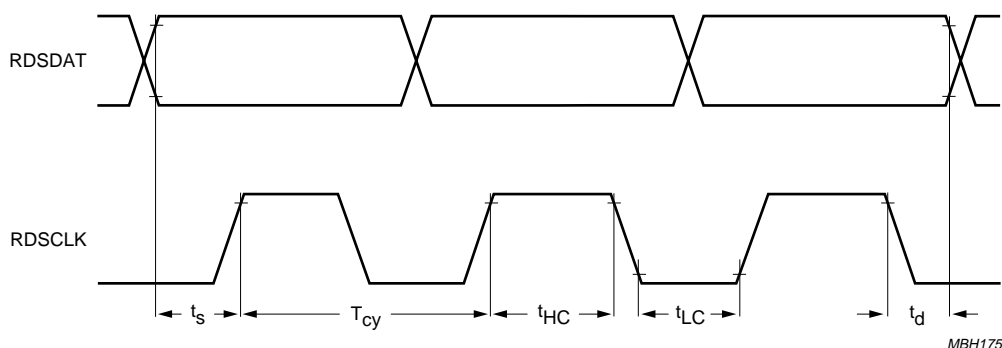


Fig.10 RDS timing (direct output mode).

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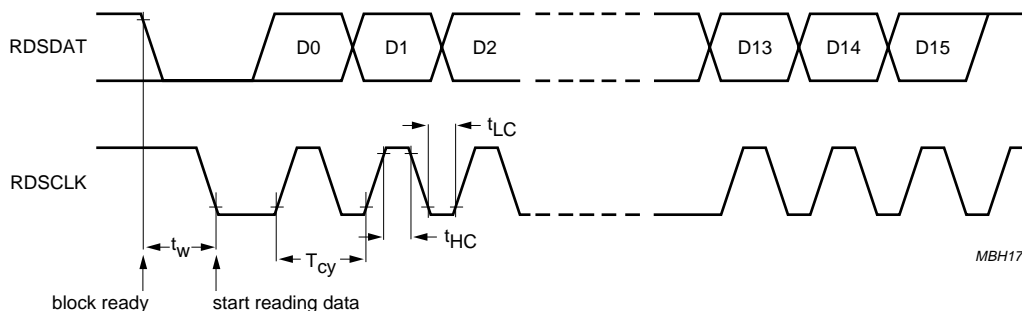


Fig.11 Interface signals RDS decoder and microcontroller (buffer mode).

## 8.10.4 BUFFER INTERFACE

The RDS interface buffers 16 data bits. Every time 16 bits are received, the data line is pulled LOW and the buffer is overwritten. The microcontroller has to monitor the data line in at most every 13.5 ms. This mode is selected by setting the RDS-CLKIN bit of the RDSCTR register (see Table 14) to logic 1. In Fig.11 the interface signals from the RDS decoder and the microcontroller in buffer mode are shown. When the buffer is filled with 16 bits the data line is pulled LOW. The data line will remain LOW until reading of the buffer is started by pulling the clock line LOW. The first bit is clocked out. After 16 clock pulses the reading of the buffer is ready and the data line is set HIGH until the buffer is filled again. The microcontroller stops communication by pulling the line HIGH. The data is written out just after the clock HIGH-to-LOW transition. The data is valid when the clock is HIGH.

When a new 16 bits buffer is filled before the other buffer is read, that buffer will be overwritten and the old data is lost.

## 8.11 DSP reset

Pin  $\overline{\text{DSPRESET}}$  is active LOW and has an internal pull-up resistor. Between this pin and pin  $V_{SSD3V}$  a capacitor should be connected to allow a proper switch-on of the supply voltage. The capacitor value is such that the chip is in reset state as long as the power supply is not stabilized.

A more or less fixed relationship between the  $\overline{\text{DSPRESET}}$  and the POM time constant is required. The voltage on the pin POM determines the current flowing in the DACs. When pin POM is at 0 V the DAC currents and output voltages are zero; at  $V_{DDA2}$  voltage the DAC currents are at their nominal (maximum) value. Some time before the QDAC outputs get to their nominal output voltages, the DSP must be in working mode to reset the output register. Therefore the DSP time constant must be less than the POM time constant. For recommended capacitors, see Figs 21 and 22.

The reset has the following functions:

- The bits of the IAC control register are set to logic 0
- The bits of the SEL register are set to their nominal values
- The DSP status registers are reset
- The program counter is set to address 0000H
- The two output flags in the status register are reset to logic 0 (pins DSPOUT1 and DSPOUT2 are LOW).

When the level on pin  $\overline{\text{DSPRESET}}$  is HIGH, the DSP program starts to run.

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**9 LIMITING VALUES**

In accordance with the Absolute Maximum Rating System (IEC 134).

| SYMBOL                      | PARAMETER   | CONDITIONS   | MIN. | MAX.      | UNIT |
|-----------------------------|---|--|------|-----------|------|
| $V_{DD3V}$                  | supply voltage                                      |  | -0.5 | +5        | V    |
| $V_{DD5V}$                  | supply voltage                                      | only valid for the voltages in connection with the 5 V I/Os                                      | -0.5 | +6.5      | V    |
| $\Delta V_{DD3Vx}$          | voltage difference between any two $V_{DD3Vx}$ pins |  | –    | 550       | mV   |
| $\Delta V_{DD5Vx}$          | voltage difference between any two $V_{DD5Vx}$ pins |  | –    | 550       | mV   |
| $I_{IK}$                    | DC input clamping diode current                     | $V_I < -0.5\text{ V}$ or $V_I > V_{DD} + 0.5\text{ V}$   | –    | $\pm 10$  | mA   |
| $I_{OK}$                    | DC output clamping diode current                    | output type 4 mA (BD4CR, BT4CR and B4CR); $V_O < -0.5\text{ V}$ or $V_O > V_{DD} + 0.5\text{ V}$ | –    | $\pm 20$  | mA   |
| $I_{O(\text{sink/source})}$ | DC output sink or source current                    | output type 4 mA (BD4CR, BT4CR and B4CR); $-0.5 < V_O < V_{DD} + 0.5\text{ V}$                   | –    | $\pm 20$  | mA   |
| $I_{DD}$                    | DC supply current per pin                           |  | –    | $\pm 750$ | mA   |
| $I_{SS}$                    | DC ground supply current per pin                    |  | –    | $\pm 750$ | mA   |
| $T_{\text{amb}}$            | ambient temperature                                 |  | -40  | +85       | °C   |
| $T_{\text{stg}}$            | storage temperature                                 |  | -65  | +150      | °C   |
| $V_{\text{ESD}}$            | ESD voltage   |  |      |           |      |
|                             | human body model                                    | 100 pF; 1500 $\Omega$  | 3000 | –         | V    |
|                             | machine model                                       | 100 pF; 2.5 $\mu\text{H}$ ; 0 $\Omega$   | 300  | –         | V    |
| $I_{\text{lu(prot)}}$       | latch-up protection current                         | CIC specification/test method  | 100  | –         | mA   |
| $P_{\text{out}}$            | power dissipation per output                        |  | –    | 100       | mW   |
| $P_{\text{tot}}$            | total power dissipation                             |  | –    | 1600      | mW   |

**10 THERMAL CHARACTERISTICS**

| SYMBOL               | PARAMETER                                   | CONDITION                        | VALUE | UNIT |
|----------------------|---|----------------------------------|-------|------|
| $R_{\text{th(j-a)}}$ | thermal resistance from junction to ambient | mounted on printed-circuit board | 45    | K/W  |



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## 11 CHARACTERISTICS

| SYMBOL  | PARAMETER  | CONDITIONS  | MIN.             | TYP.  | MAX.          | UNIT |
|---|--|---|------------------|-------|---------------|------|
| <b>Supplies; <math>T_{amb} = -40</math> to <math>+85</math> °C; <math>V_{DD5V} = 4.5</math> to <math>5.5</math> V; <math>V_{DD3V} = 3</math> to <math>3.6</math> V</b>    |  |   |                  |       |               |      |
| $V_{DD3V}$  | digital supply voltage<br>3.3 V for DSP core   | $V_{DD3Vx}$ pins with respect to $V_{SS}$           | 3                | 3.3   | 3.6           | V    |
| $V_{DDA}$   | analog supply voltage<br>3.3 V   | $V_{DDAx}$ pins with respect to $V_{SS}$            | 3                | 3.3   | 3.6           | V    |
| $V_{DDA1}$  | supply voltage analog<br>part ADC  |   | 3                | 3.3   | 3.6           | V    |
| $V_{DD5V}$  | supply voltage 5 V for<br>periphery  | $V_{DD5Vx}$ pins with respect to $V_{SS}$           | 4.5              | 5     | 5.5           | V    |
| $I_{DD3V}$  | supply current of the<br>3.3 V digital DSP core  | high activity of the DSP at<br>27 MHz DSP frequency | –                | 80    | 110           | mA   |
| $I_{DD5V}$  | supply current of the<br>5 V digital periphery   |   | –                | 3     | 5             | mA   |
| $I_{DDA1}$  | supply current of the<br>ADCs  | zero input and output<br>signal                     | –                | 35    | 43            | mA   |
| $I_{DDA2}$  | supply current of the<br>DACs  |   | –                | 4     | 5             | mA   |
| $I_{DD(OSC)}$   | supply current crystal<br>oscillator   | at start-up   | –                | 7     | 15            | mA   |
|   |  | at oscillation                                      | –                | 0.6   | 2             | mA   |
| $P_{tot}$   | total power dissipation  | high activity of the DSP at<br>27 MHz DSP frequency | –                | 0.352 | 0.535         | W    |
| <b>Digital I/O; <math>T_{amb} = -40</math> to <math>+85</math> °C; <math>V_{DD5V} = 4.5</math> to <math>5.5</math> V; <math>V_{DD3V} = 3</math> to <math>3.6</math> V</b> |  |   |                  |       |               |      |
| $V_{IH}$  | HIGH-level input<br>voltage all digital inputs<br>and I/Os; pin types:<br>IBUFD, IBUFU,<br>BD4CR, SCHMITCD |   | $0.7V_{DD5V}$    | –     | –             | V    |
| $V_{IL}$  | LOW-level input<br>voltage all digital inputs<br>and I/Os; pin types:<br>IBUFD, IBUFU,<br>BD4CR, SCHMITCD  |   | –                | –     | $0.3V_{DD5V}$ | V    |
| $V_{hys}$   | hysteresis voltage; pin<br>type: SCHMITCD  |   | 1                | 1.3   | –             | V    |
| $V_{OH}$  | HIGH-level output<br>voltage digital outputs;<br>pin types: B4CR,<br>BD4CR                                 | $I_O = -4$ mA                                       | $V_{DD5V} - 0.4$ | –     | –             | V    |
| $V_{OL}$  | LOW-level output<br>voltage digital outputs;<br>pin types: B4CR,<br>BD4CR                                  | $V_{DD5V} = 4.5$ V; $I_O = 4$ mA                    | –                | –     | 0.4           | V    |

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| SYMBOL              | PARAMETER   | CONDITIONS  | MIN.            | TYP.            | MAX.            | UNIT            |
|---------------------|---|---|-----------------|-----------------|-----------------|-----------------|
| $V_{OL(SDA)}$       | LOW-level output voltage I <sup>2</sup> C-bus data output (SDA); pin type: BD8SCI4  | $I_O = 8 \text{ mA}$  | –               | –               | 0.4             | V               |
| $I_{LO}$            | output leakage current 3-state outputs; pin types: BD4CR, BD8SCI4   | $V_O = 0 \text{ V}$ or $V_{DD5V}$   | –               | –               | $\pm 5$         | $\mu\text{A}$   |
| $R_{pu(VDDD)(int)}$ | internal pull-up resistor to $V_{DDD5V}$ ; pin type: IBUFU  |   | 23              | 50              | 80              | $k\Omega$       |
| $R_{pd(VSSD)(int)}$ | internal pull-down resistor to $V_{SSD5V}$ ; pin type: IBUFD  |   | 23              | 50              | 80              | $k\Omega$       |
| $t_{i(r)}$          | input rise time   | $V_{DDD5V} = 5.5 \text{ V}$   | –               | 6               | 200             | ns              |
| $t_{i(f)}$          | input fall time   | $V_{DDD5V} = 5.5 \text{ V}$   | –               | 6               | 200             | ns              |
| $t_{o(r)(min)}$     | minimum output rise time  | $V_{DDD5V} = 5.5 \text{ V};$<br>$V_{DDD3V} = 3.6 \text{ V};$<br>$T_j = -40 \text{ }^\circ\text{C}$<br>$C_L = 30 \text{ pF}$ | 7.6             | –               | 18.4            | ns              |
|                     | digital outputs except I <sup>2</sup> C-bus data output; pin types: B(D)(T)4CR<br>I <sup>2</sup> C-bus data output; pin type: BD4SCI4 | $C_L = 200 \text{ pF}$  | tb <sup>1</sup> | tb <sup>1</sup> | tb <sup>1</sup> | ns              |
| $t_{o(r)(max)}$     | maximum output rise time  | $V_{DDD5V} = 4.5 \text{ V};$<br>$V_{DDD3V} = 3 \text{ V}; T_j = 125 \text{ }^\circ\text{C}$<br>$C_L = 30 \text{ pF}$        | 13.7            | –               | 33.4            | ns              |
|                     | digital outputs except I <sup>2</sup> C-bus data output; pin types: B(D)(T)4CR<br>I <sup>2</sup> C-bus data output; pin type: BD4SCI4 | $C_L = 200 \text{ pF}$  | tb <sup>1</sup> | tb <sup>1</sup> | tb <sup>1</sup> | tb <sup>1</sup> |
| $t_{o(f)(min)}$     | minimum output fall time  | $V_{DDD5V} = 5.5 \text{ V};$<br>$V_{DDD3V} = 3.6 \text{ V};$<br>$T_j = -40 \text{ }^\circ\text{C}$<br>$C_L = 30 \text{ pF}$ | 7               | –               | 17              | ns              |
|                     | digital outputs except I <sup>2</sup> C-bus data output; pin types: B(D)(T)4CR<br>I <sup>2</sup> C-bus data output; pin type: BD4SCI4 | $C_L = 200 \text{ pF}$  | tb <sup>1</sup> | tb <sup>1</sup> | tb <sup>1</sup> | ns              |

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| SYMBOL  | PARAMETER   | CONDITIONS   | MIN.           | TYP.          | MAX.           | UNIT          |
|---|---|--|----------------|---------------|----------------|---------------|
| $t_{o(f)(max)}$   | maximum output fall time  | $V_{DD5V} = 4.5\text{ V};$<br>$V_{DD3V} = 3\text{ V}; T_j = 125\text{ }^{\circ}\text{C}$<br>$C_L = 30\text{ pF}$ | 12.7           | –             | 30.9           | ns            |
|   | digital outputs except I <sup>2</sup> C-bus data output; pin types: B(D)(T)4CR<br>I <sup>2</sup> C-bus data output; pin type: BD4SCI4 | $C_L = 200\text{ pF}$  | tbf            | tbf           | tbf            | ns            |
| <b>DC characteristics analog inputs; <math>T_{amb} = 25\text{ }^{\circ}\text{C}; V_{DDA1} = 3.3\text{ V}</math></b> |   |  |                |               |                |               |
| $V_{REFAD}$   | common-mode reference voltage for SCAD1, 2, 3 and level-ADC   | with reference to $V_{SSA1}$   | $0.47V_{DDA1}$ | $0.5V_{DDA1}$ | $0.53V_{DDA1}$ | V             |
| $Z_{o(VREFAD)}$   | output impedance at pin VREFAD  |  | –              | 600           | –              | $\Omega$      |
| $V_{VDACP}$   | positive reference voltage SCAD1, 2, 3 and level-ADC  |  | 3              | 3.3           | 3.6            | V             |
| $I_{VDACP}$   | positive reference current SCAD1, 2, 3 and level-ADC  |  | –              | –20           | –              | $\mu\text{A}$ |
| $V_{VDACN1},$<br>$V_{VDACN2}$   | negative reference voltage SCAD1, 2, 3 and level-ADC  |  | –0.3           | 0             | +0.3           | V             |
| $I_{VDACN1},$<br>$I_{VDACN2}$   | negative reference current SCAD1, 2 3 and level-ADC   |  | –              | 20            | –              | $\mu\text{A}$ |
| $V_{IO(SCAD)}$  | input offset voltage SCAD1, 2 and 3   |  | –              | 140           | –              | mV            |
| <b>AC characteristics analog inputs; <math>T_{amb} = 25\text{ }^{\circ}\text{C}; V_{DDA1} = 3.3\text{ V}</math></b> |   |  |                |               |                |               |
| $V_{i(con)(max)(rms)}$  | maximum conversion input level at analog input (RMS value)  | THD < 1%   | 0.6            | 0.66          | –              | V             |
| $R_i$   | input resistance (AM, CD and TAPE inputs)   |  | 1              | –             | –              | M $\Omega$    |
| $R_{i(FMMPX)}$  | input resistance at pin FMMPX   |  | 44             | –             | 164            | k $\Omega$    |
| THD <sub>FMMPX</sub>  | total harmonic distortion FMMPX input   | input signal 0.35 V (RMS) at 1 kHz; bandwidth = 19 kHz; note 1   | –              | –70           | –65            | dB            |
|   |   |  | –              | 0.03          | 0.056          | %             |
| $S/N_{FMMPX(m)}$  | signal-to-noise ratio FMMPX input mono  | input signal at 1 kHz; 0 dB reference = 0.35 V (RMS); bandwidth = 19 kHz; note 1                                 | 80             | 83            | –              | dB            |

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| SYMBOL             | PARAMETER  | CONDITIONS  | MIN. | TYP.  | MAX.  | UNIT |
|--------------------|--|---|------|-------|-------|------|
| $S/N_{FMMPX(s)}$   | signal-to-noise ratio<br>FMMPX input stereo                        | input signal at 1 kHz;<br>0 dB reference = 0.35 V<br>(RMS);<br>bandwidth = 40 kHz; note 1   | 74   | 77    | –     | dB   |
| $THD_{CD}$         | total harmonic<br>distortion CD inputs                             | input signal 0.55 V (RMS)<br>at 1 kHz; input gain = 1<br>(see Fig.4);<br>bandwidth = 20 kHz | –    | –83   | –78   | dB   |
|                    |  |   | –    | 0.007 | 0.013 | %    |
| $S/N_{CD}$         | signal-to-noise ratio<br>CD inputs                                 | input signal at 1 kHz;<br>0 dB reference = 0.55 V<br>(RMS);<br>bandwidth = 20 kHz           | 81   | 84    | –     | dB   |
| $THD_{AM}$         | total harmonic<br>distortion AM inputs                             | input signal 0.55 V (RMS)<br>at 1 kHz;<br>bandwidth = 5 kHz                                 | –    | –80   | –76   | dB   |
|                    |  |   | –    | 0.01  | 0.016 | %    |
| $S/N_{AM}$         | signal-to-noise ratio<br>AM inputs                                 | input signal at 1 kHz;<br>0 dB reference = 0.55 V<br>(RMS); bandwidth = 5 kHz               | 83   | 88    | –     | dB   |
| $THD_{TAPE}$       | total harmonic<br>distortion TAPE inputs                           | input signal 0.55 V (RMS)<br>at 1 kHz;<br>bandwidth = 20 kHz;                               | –    | –80   | –76   | dB   |
|                    |  |   | –    | 0.01  | 0.016 | %    |
| $S/N_{TAPE}$       | signal-to-noise ratio<br>TAPE inputs                               | input signal at 1 kHz;<br>0 dB reference = 0.55 V<br>(RMS);<br>bandwidth = 20 kHz           | 81   | 83    | –     | dB   |
| $\alpha_{19}$      | carrier and harmonic<br>suppression at the<br>output               | pilot signal<br>frequency = 19 kHz  | –    | 81    | –     | dB   |
|                    |  | unmodulated   | –    | 98    | –     | dB   |
| $\alpha_{38}$      | carrier and harmonic<br>suppression at the<br>output               | subcarrier<br>frequency = 38 kHz  | –    | 83    | –     | dB   |
|                    |  | unmodulated   | –    | 91    | –     | dB   |
| $\alpha_{57}$      | carrier and harmonic<br>suppression for<br>19 kHz, including notch | subcarrier<br>frequency = 57 kHz  | –    | 83    | –     | dB   |
|                    |  | unmodulated   | –    | 96    | –     | dB   |
| $\alpha_{76}$      | carrier and harmonic<br>suppression for<br>19 kHz, including notch | subcarrier<br>frequency = 76 kHz  | –    | 84    | –     | dB   |
|                    |  | unmodulated   | –    | 94    | –     | dB   |
| $IM_{\alpha 10}$   | intermodulation  | $f_{mod} = 10$ kHz; $f_{spur} = 1$ kHz  | 77   | –     | –     | dB   |
| $IM_{\alpha 13}$   | intermodulation  | $f_{mod} = 13$ kHz; $f_{spur} = 1$ kHz  | 76   | –     | –     | dB   |
| $\alpha_{57(VF)}$  | traffic radio (Verkehrs<br>Warnfunk) suppression                   | $f = 57$ kHz  | –    | 110   | –     | dB   |
| $\alpha_{67(SCA)}$ | Subsidiary<br>Communication<br>Authority (SCA)<br>suppression      | $f = 67$ kHz  | –    | 110   | –     | dB   |

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| SYMBOL  | PARAMETER  | CONDITIONS   | MIN. | TYP. | MAX. | UNIT |
|---|--|--|------|------|------|------|
| $\alpha_{114}$  | adjacent channel suppression                                   | $f = 114 \text{ kHz}$  | –    | 110  | –    | dB   |
| $\alpha_{190}$  | adjacent channel suppression                                   | $f = 190 \text{ kHz}$  | –    | 110  | –    | dB   |
| $V_{th(pilot)(rms)}$  | pilot threshold voltage (RMS value) at pin DSPOUT1             | stereo 'on', AD input selection switch position '110'  | –    | 35.5 | –    | mV   |
|   |  | stereo 'off', AD input selection switch position '110'   | –    | 35.4 | –    | mV   |
| hys   | hysteresis of $V_{th(pilot)(rms)}$                             |  | –    | 0    | –    | dB   |
| $f_{i(FMMPX)}$  | input frequency of the FMMPX input                             | –3 dB; AD via bitstream test output  | 0    | –    | 55   | kHz  |
| $\alpha_{cs}$   | FM-stereo channel separation                                   | $f_i = 1 \text{ kHz}$  | 40   | 45   | –    | dB   |
|   |  | $f_i = 10 \text{ kHz}$   | 25   | 30   | –    | dB   |
| $f_{res(FM)}$   | audio frequency response FM                                    | at –3 dB via DSP at DAC output   | 17   | –    | –    | kHz  |
| $\Delta G_{L-R}$  | overall left/right gain unbalance (TAPE, CD, FM and AM inputs) |  | –    | –    | 0.5  | dB   |
| $\alpha_{cs(TAPE,CD)}$  | channel separation (TAPE and CD inputs)                        | $f_i = 1 \text{ kHz}$  | 70   | 75   | –    | dB   |
|   |  | $f_i = 10 \text{ kHz}$   | 65   | 70   | –    | dB   |
| $f_{res(TAPE,CD)}$  | response frequency (TAPE and CD inputs)                        | $f_s = 38 \text{ kHz}$ ; at –3 dB  | 18   | –    | –    | kHz  |
| $\alpha_{ct}$   | crosstalk between inputs                                       | $f_i = 1 \text{ kHz}$  | 65   | –    | –    | dB   |
|   |  | $f_i = 15 \text{ kHz}$   | 50   | –    | –    | dB   |
| $PSRR_{MPX/RDS}$  | power supply ripple rejection MPX and RDS ADCs                 | output via I <sup>2</sup> S-bus; ADC input short-circuited; $f_{ripple} = 1 \text{ kHz}$ ; $V_{ripple} = 100 \text{ mV (peak)}$ ; $C_{VREFAD} = 22 \mu\text{F}$ ; $C_{VDACP} = 10 \mu\text{F}$ | 35   | 45   | –    | dB   |
| $PSRR_{LAD}$  | power supply ripple rejection level-ADC                        | output via DAC; ADC input short-circuited; $f_{ripple} = 1 \text{ kHz}$ ; $V_{ripple} = 100 \text{ mV (peak)}$ ; $C_{VREFAD} = 22 \mu\text{F}$   | 29   | 39   | –    | dB   |
| $CMRR_{CD}$   | common-mode rejection ratio for CD input mode                  | $R_{CDGND} = 1 \text{ M}\Omega$ ; resistance of CD player ground cable < 1 k $\Omega$ ; $f_i = 1 \text{ kHz}$  | 60   | –    | –    | dB   |
| <b>AC characteristics RDS input; <math>T_{amb} = 25 \text{ }^\circ\text{C}</math></b> |  |  |      |      |      |      |
| $V_{i(con)(max)(rms)}$  | maximum conversion input level (RMS value)                     | THD < 1%   | 0.6  | 0.66 | –    | V    |

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| SYMBOL  | PARAMETER   | CONDITIONS  | MIN.                  | TYP.                 | MAX.                  | UNIT                              |
|---|---|---|-----------------------|----------------------|-----------------------|-----------------------------------|
| $R_{i(\text{FMRDS})}$   | input resistance<br>FMRDS input                       |   | 44                    | –                    | 164                   | k $\Omega$                        |
| $\text{THD}_{\text{FMRDS}}$   | total harmonic<br>distortion RDS ADC                  | $f_c = 57$ kHz  | –60                   | –67                  | –                     | dB                                |
| $\text{S/N}_{\text{FMRDS}}$   | signal-to-noise ratio<br>RDS ADC                      | 6 kHz bandwidth;<br>$f_c = 57$ kHz;<br>0 dB reference = 0.55 V<br>(RMS); note 1 | 54                    | –                    | –                     | dB                                |
| $\alpha_{\text{pilot}}$   | pilot attenuation RDS                                 |   | 50                    | –                    | –                     | dB                                |
| $\alpha$  | nearby selectivity RDS                                | neighbouring channel at<br>200 kHz distance                                     | 61                    | –                    | –                     | dB                                |
| $\alpha_{n(\text{ADC})}$  | RDS ADC noise<br>attenuation                          |   | 70                    | –                    | –                     | dB                                |
| $V_{\text{ripple}(\text{RDS})}$   | ripple voltage RDS<br>pass band                       | 2.4 kHz bandwidth   | –                     | –                    | 0.5                   | dB                                |
| $\alpha_{\text{mux}(\text{RDS})}$   | multiplex attenuation<br>RDS                          | mono  | 70                    | –                    | –                     | dB                                |
|   |   | stereo  | 40                    | –                    | –                     | dB                                |
| $\Delta f_{\text{osc}}$   | allowable frequency<br>deviation of the 57 kHz<br>RDS | maximum crystal<br>resonance frequency<br>deviation of 100 ppm                  | –                     | –                    | 6                     | Hz                                |
| <b>Analog level inputs (AML and FML); <math>T_{\text{amb}} = 25</math> °C; <math>V_{\text{DDA1}} = 3.3</math> V</b> |   |   |                       |                      |                       |                                   |
| $\text{S/N}_{\text{LAD}}$   | signal-to-noise ratio of<br>level-ADC                 | 0 to 29 kHz bandwidth;<br>maximum input level;<br>unweighted                    | 48                    | 54                   | –                     | dB                                |
| $R_i$   | input resistance                                      |   | 1.5                   | –                    | 2.2                   | M $\Omega$                        |
| $V_{i(\text{fs})}(\text{LAD})$  | full-scale level-ADC<br>input voltage                 |   | 0                     | –                    | $V_{\text{DDA1}}$     | V                                 |
| $V_{\text{IO}}$   | DC offset voltage                                     |   | –                     | –                    | 60                    | mV                                |
| $\alpha$  | decimation filter<br>attenuation                      |   | 20                    | –                    | –                     | $\frac{\text{dB}}{\text{decade}}$ |
| $f_{\text{co}(\text{PB})}$  | pass band cut-off<br>frequency                        | at –3 dB and DCS<br>clock = 9.728 MHz   | –                     | 29                   | –                     | kHz                               |
| $f_{\text{sr}}$   | sample rate frequency<br>after decimation             | DCS clock = 9.728 MHz   | –                     | 38                   | –                     | kHz                               |
| <b>Analog outputs; <math>T_{\text{amb}} = 25</math> °C; <math>V_{\text{DDA2}} = 3.3</math> V</b>                    |   |   |                       |                      |                       |                                   |
| $V_{\text{VREFDA}}$   | voltage at pin VREFDA                                 |   | $0.47V_{\text{DDA2}}$ | $0.5V_{\text{DDA2}}$ | $0.53V_{\text{DDA2}}$ | V                                 |
| $Z_{\text{VREFDA}}$   | impedance at<br>pin VREFDA                            | with respect to pin $V_{\text{DDA2}}$   | –                     | 40                   | –                     | k $\Omega$                        |
|   |   | with respect to pin $V_{\text{SSA2}}$   | –                     | 40                   | –                     | k $\Omega$                        |
| $V_o$   | output voltage of<br>operational amplifiers           | maximum I <sup>2</sup> S-bus signal<br>(RMS); $R_L > 5$ k $\Omega$ (AC)         | 0.65                  | 0.75                 | 0.85                  | V                                 |
| $V_{O(\text{av})}$  | average DC output<br>voltage                          | $R_L > 5$ k $\Omega$ (AC)   | 1.5                   | 1.65                 | 1.8                   | V                                 |

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| SYMBOL   | PARAMETER   | CONDITIONS  | MIN.         | TYP.     | MAX.         | UNIT       |
|--|---|---|--------------|----------|--------------|------------|
| $I_{pu(POM)}$  | pull-up current to $V_{DDA2}$ from pin POM                    | voltage at pin POM $< 0.6$ V  | 3.3          | –        | 5            | $\mu$ A    |
|  |   | voltage at pin POM $> 0.8$ V  | 50           | –        | 90           | $\mu$ A    |
| $PSRR_{QDAC}$  | power supply ripple rejection of QDAC                         | input via I <sup>2</sup> S-bus;<br>$f_{ripple} = 1$ kHz;<br>$V_{ripple} = 100$ mV (p-p);<br>$C_{VREFDA} = 22$ $\mu$ F | 45           | 60       | –            | dB         |
| $\Delta I_{O(QDAC)(max)}$                                | maximum deviation in output level of the QDAC current outputs | full-scale output; with respect to the average of the 4 current outputs   | –            | –        | $\pm 4.47$   | %          |
|  |   |   | –            | –        | $\pm 0.38$   | dB         |
| $\alpha_{ct}$  | crosstalk between all outputs in the audio band               | one output digital silence, three maximum volume  | –            | –        | –69          | dB         |
| $I_{O(sc)}$  | output short-circuit current                                  | output short-circuited to ground  | –            | –        | 20           | mA         |
| $RES_{DAC}$  | DAC resolution  |   | –            | 18       | –            | bits       |
| (THD + N)/S  | total harmonic distortion-plus-noise to signal ratio          | $f = 1$ kHz;<br>$V_o = 0.72$ V (RMS);<br>$R_L > 5$ k $\Omega$ (AC);<br>A-weighted                                     | –            | –75      | –65          | dBA        |
| DR   | dynamic range   | output signal –60 dB at 1 kHz;<br>0 dB reference = 0.77 V (RMS); A-weighted   | 92           | 102      | –            | dBA        |
| DS   | digital silence   | $f = 20$ Hz to 17 kHz;<br>reference $V_o = 0.77$ V (RMS); A-weighted  | –            | 102      | 108          | dBA        |
| $V_{no(DS)(rms)}$  | digital silence noise output voltage (RMS value)              |   | –            | 3        | 8            | $\mu$ V    |
| IM   | intermodulation distortion/comparator                         | $f = 60$ Hz and 7 kHz; ratio 4  | –            | –70      | –55          | dB         |
| $f_{s(max)}$   | maximum sample frequency                                      |   | 48           | –        | –            | kHz        |
| B  | bandwidth DAC   | at –3 dB  | –            | $0.5f_s$ | –            | Hz         |
| $C_L$  | load capacitance on DAC voltage outputs                       |   | –            | –        | 2.5          | nF         |
| $R_L$  | load resistance on DAC voltage outputs                        |   | 2            | –        | –            | k $\Omega$ |
| <b>I<sup>2</sup>S-bus inputs and outputs; see Fig.12</b> |   |   |              |          |              |            |
| $T_{cy}$   | bit clock cycle time  |   | 50           | –        | –            | ns         |
| $t_r$  | rise time   |   | –            | –        | $0.15T_{cy}$ | ns         |
| $t_f$  | fall time   |   | –            | –        | $0.15T_{cy}$ | ns         |
| $t_{BCK(H)}$   | bit clock HIGH time   |   | $0.35T_{cy}$ | –        | –            | ns         |
| $t_{BCK(L)}$   | bit clock LOW time  |   | $0.35T_{cy}$ | –        | –            | ns         |

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| SYMBOL  | PARAMETER                          | CONDITIONS                                 | MIN.        | TYP.    | MAX.         | UNIT    |
|---|------------------------------------|--|-------------|---------|--------------|---------|
| $t_{su(D)}$                                     | data set-up time                   |  | $0.2T_{cy}$ | –       | –            | ns      |
| $t_{h(D)}$                                      | data hold time                     |  | $0.2T_{cy}$ | –       | –            | ns      |
| $t_{d(D)}$                                      | data delay time                    |  | –           | –       | $0.15T_{cy}$ | ns      |
| $t_{su(WS)}$                                    | word select set-up time            |  | $0.2T_{cy}$ | –       | –            | ns      |
| $t_{h(WS)}$                                     | word select hold time              |  | $0.2T_{cy}$ | –       | –            | ns      |
| <b>RDS interface timing; see Figs 10 and 11</b> |                                    |  |             |         |              |         |
| $f_{RDCLK}$                                     | nominal RDS clock frequency        |  | –           | 1 187.5 | –            | Hz      |
| $t_{su}$  | clock set-up time                  | direct output mode                         | 100         | –       | –            | $\mu s$ |
| $T_{cy}$  | cycle time                         | direct output mode                         | –           | 842     | –            | $\mu s$ |
|   |                                    | buffer mode                                | 2           | –       | –            | $\mu s$ |
| $t_{HC}$  | clock HIGH time                    | direct output mode                         | 220         | –       | 640          | $\mu s$ |
|   |                                    | buffer mode                                | 1           | –       | –            | $\mu s$ |
| $t_{LC}$  | clock LOW time                     | direct output mode                         | 220         | –       | 640          | $\mu s$ |
|   |                                    | buffer mode                                | 1           | –       | –            | $\mu s$ |
| $t_h$   | data output hold time              | direct output mode                         | 100         | –       | –            | $\mu s$ |
| $t_w$   | wait time                          | buffer mode                                | 1           | –       | –            | $\mu s$ |
| $f_{i(clk)(ext)}$                               | input frequency external RDS clock | buffer mode                                | –           | –       | 22           | MHz     |
| <b>Oscillator</b>                               |                                    |  |             |         |              |         |
| $f_{xtal}$                                      | crystal frequency                  |  | –           | 11.2896 | –            | MHz     |
| $f_{clk(DSP)}$                                  | clock frequency DSP core           |  | 27.1656     | –       | –            | MHz     |
| $\alpha_f$                                      | spurious frequency attenuation     |  | 20          | –       | –            | dB      |
| $V_{xtal}$                                      | voltage across the crystal         |  | –           | 3       | –            | V       |
| $g_m$   | transconductance                   | at start-up                                | 10.5        | 19      | 32           | mS      |
|   |                                    | in operating range                         | 3.6         | –       | 38           | mS      |
| $C_L$   | load capacitance                   |  | –           | 15      | –            | pF      |
| $N_{cy(su)}$                                    | number of cycles in start-up time  | depends on quality of the external crystal | –           | 1 000   | –            | cycles  |
| $P_{xtal}$                                      | crystal drive power level          | at oscillation                             | –           | 0.4     | 0.5          | mW      |
| $V_{i(clk)(ext)}$                               | external clock input voltage       | in slave mode                              | 3           | 3.3     | 5            | V       |

**Note**

1. FMRDS and FMMPX input sensitivity setting '000' (see Table 17).



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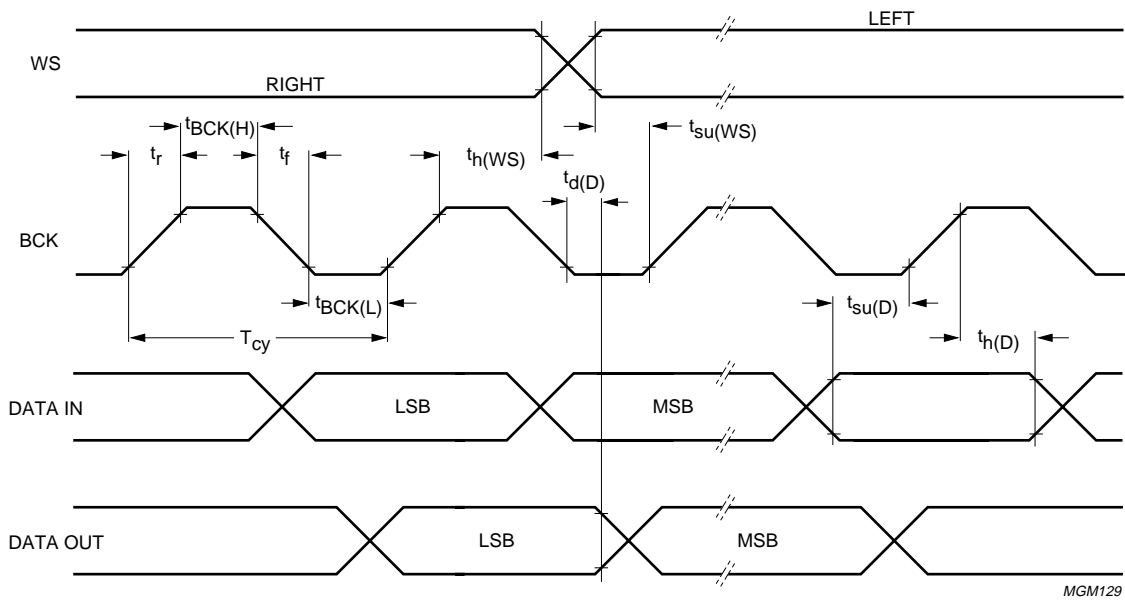


Fig.12 Timing of the digital audio data in- and outputs.

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12 I<sup>2</sup>C-BUS INTERFACE AND PROGRAMMING

12.1 I<sup>2</sup>C-bus interface

12.1.1 CHARACTERISTICS OF THE I<sup>2</sup>C-BUS

The I<sup>2</sup>C-bus is used for 2-way, 2-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to V<sub>DD</sub> via a pull-up resistor when connected to the output stages of a microcontroller. For a 400 kHz clock frequency the recommendations of Philips Semiconductors for this type of bus must be followed e.g. up to loads of 200 pF at the bus a pull-up resistor can be used; loads between 200 to 400 pF need a current source or switched resistor. Data transfer can only be initiated when the bus is not busy.

12.1.2 BIT TRANSFER

One data bit is transferred during each clock pulse; see Fig.13. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as control signals. The maximum clock frequency is 400 kHz. To be able to run on this high frequency all the I/Os connected to this bus must be designed for this high speed according to the Philips specification.

12.1.3 START AND STOP CONDITIONS

Both data and clock line will remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line while the clock is HIGH is defined as a START condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as a STOP condition (P); see Fig.14.

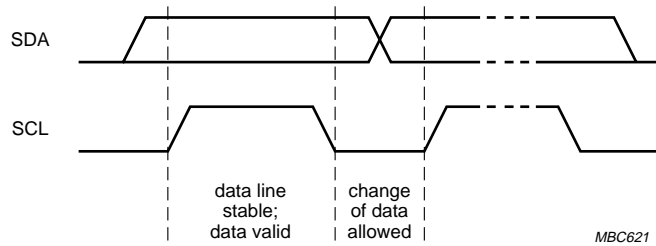


Fig.13 Bit transfer on the I<sup>2</sup>C-bus.

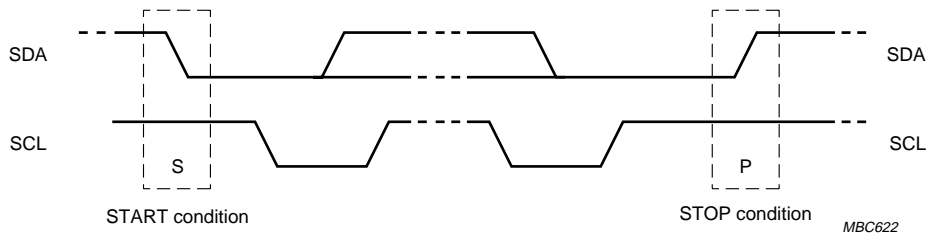


Fig.14 START and STOP condition.

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#### 12.1.4 DATA TRANSFER

A device generating a message is a 'transmitter', a device receiving a message is the 'receiver'. The device that controls the message is the 'master' and the devices which are controlled by the master are the 'slaves'; see Fig.15.

### 12.1.5 ACKNOWLEDGE

The number of data bits transferred between the START and STOP conditions from the transmitter to receiver is not limited. Each byte of eight bits is followed by one acknowledge bit. At the acknowledge bit the data line is released by the master and the master generates an extra acknowledge related clock pulse. A slave receiver, which

is addressed, must generate an acknowledge after the reception of each byte. Also a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse. Set-up and hold times must be taken into account. A master receiver must signal an 'end of data' to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a STOP condition; see Fig.16.

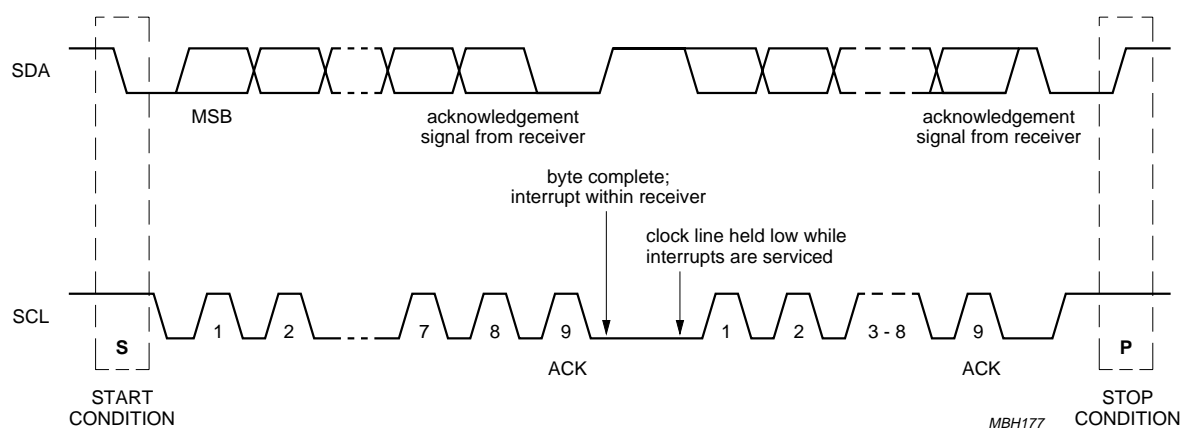


Fig.15 Data transfer on the I<sup>2</sup>C-bus.

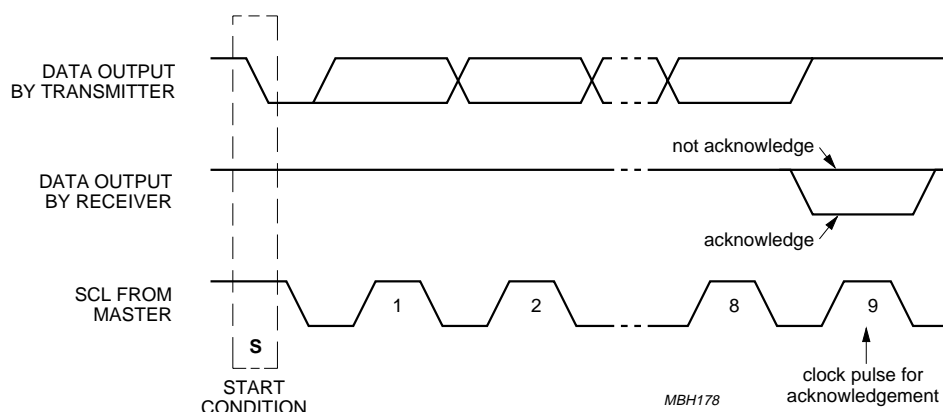


Fig.16 Acknowledge on the I<sup>2</sup>C-bus.

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12.2 I<sup>2</sup>C-bus protocol

12.2.1 ADDRESSING

Before any data is transmitted on the I<sup>2</sup>C-bus, the device that should respond is addressed first. The addressing is always done with the first byte transmitted after the START procedure.

12.2.2 SLAVE ADDRESS

The SAA7705H acts as a slave receiver or a slave transmitter. Therefore, the clock signal SCL is only an input signal. The data signal SDA is a bidirectional line. The slave address is shown in Table 3.

Table 3 Slave address

| MSB |   |   |   |   |   |    | LSB |
|-----|---|---|---|---|---|----|-----|
| 0   | 0 | 1 | 1 | 1 | 0 | A0 | R/W |

The sub-address bit A0 corresponds to the hardware address pin A0 which allows the device to have 2 different addresses. The A0 input is also used in the test mode as a serial input of the test control block.

12.2.3 WRITE CYCLES

The I<sup>2</sup>C-bus configuration for a write cycle is shown in Fig.17. The write cycle is used to write the bytes to control the DCS block, the PLL for the DSP clock generation, the IAC settings, the AD volume control settings, the analog input selection, the format of the I<sup>2</sup>S-bus and some other settings. More details can be found in the I<sup>2</sup>C-bus memory map (see Table 5).

The data length is 2 or 3 bytes depending on the accessed memory. If the Y-memory is addressed the data length is 2 bytes, in case of the X-memory the length is 3 bytes. The slave receiver detects the address and adjusts the number of bytes accordingly.

12.2.4 READ CYCLES

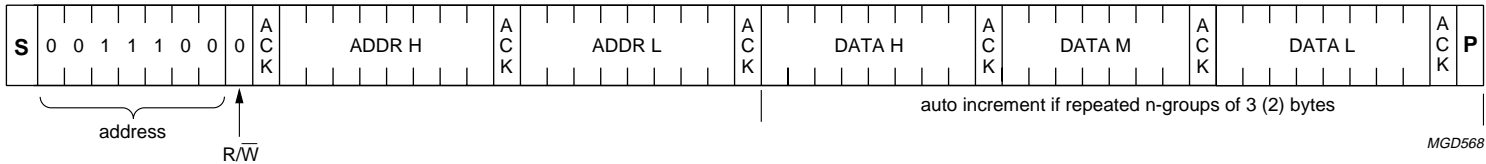
The I<sup>2</sup>C-bus configuration for a read cycle is shown in Fig.18. The read cycle is used to read the data values from XRAM or YRAM. The master starts with a START condition (S), the DSP address '0011100' and a logic 0 (write) for the read/write bit. This is followed by an acknowledge of the SAA7705H. Then the master writes the high memory address (ADDR H) and low memory address (ADDR L) where the reading of the memory content of the SAA7705H must start. The SAA7705H acknowledges these addresses both.

The master generates a repeated START and again the SAA7705H address '0011100' but this time followed by a logic 1 (read) of the read/write bit. From this moment on the SAA7705H will send the memory content in groups of 2 (Y-memory) or 3 (X-memory) bytes to the I<sup>2</sup>C-bus, each time acknowledged by the master. The master stops this cycle by generating a negative acknowledge, then the SAA7705H frees the I<sup>2</sup>C-bus and the master can generate a STOP condition.

The data is transferred from the DSP register to the I<sup>2</sup>C-bus register at execution of the MPI instruction in the DSP program. Therefore at least once every DSP cycle an MPI instruction should be added.

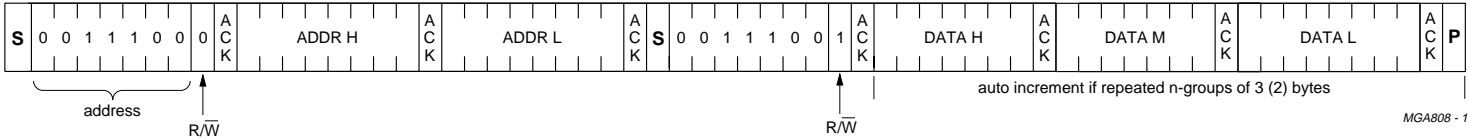
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S = START condition.  
ACK = acknowledge from DSP (SDA LOW).  
ADDR H and ADDR L = address DSP register.  
DATA H, DATA M and DATA L = data of XRAM or registers.  
DATA H and DATA M = data of YRAM.  
P = STOP condition.

Fig.17 Master transmitter writes to the DSP registers.

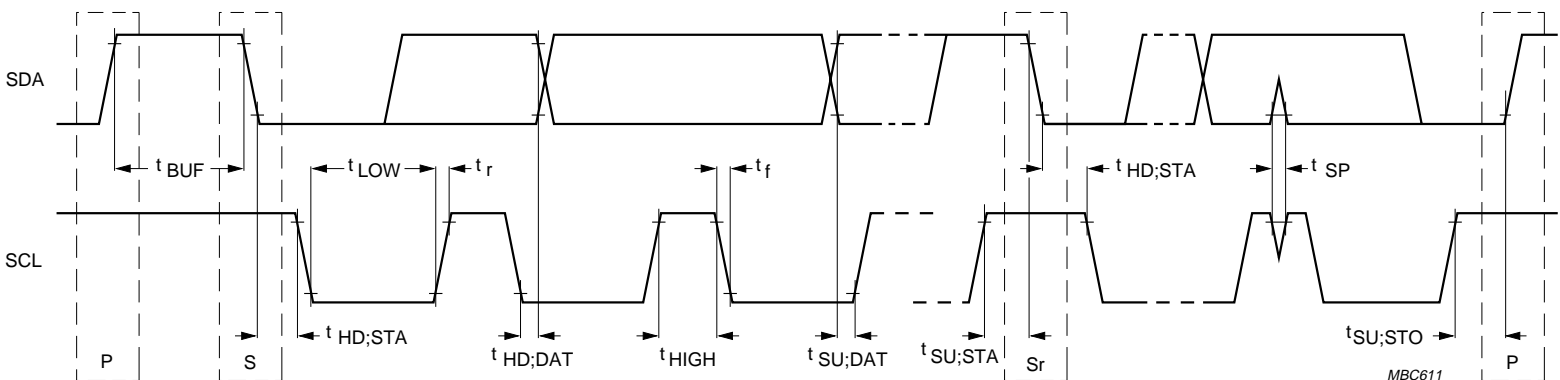


S = START condition.  
ACK = acknowledge from DSP (SDA LOW).  
ADDR H and ADDR L = address DSP register.  
DATA H, DATA M and DATA L = data of XRAM or registers.  
DATA H and DATA M = data of YRAM.  
P = STOP condition.

Fig.18 Master transmitter reads from the DSP registers.

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Fig.19 Definition of timing on the I<sup>2</sup>C-bus.**Table 4** Timing fast I<sup>2</sup>C-bus (see Fig.19)

| SYMBOL              | PARAMETER   | CONDITIONS           | STANDARD I <sup>2</sup> C-BUS |      | FAST MODE I <sup>2</sup> C-BUS |      | UNIT |
|---------------------|---|----------------------|-------------------------------|------|--------------------------------|------|------|
|                     |   |                      | MIN.                          | MAX. | MIN.                           | MAX. |      |
| f <sub>SCL</sub>    | SCL clock frequency   |                      | 0                             | 100  | 0                              | 400  | kHz  |
| t <sub>BUF</sub>    | bus free time between a STOP and START condition  |                      | 4.7                           | –    | 1.3                            | –    | μs   |
| t <sub>HD;STA</sub> | hold time (repeated) START condition; after this period, the first clock pulse is generated |                      | 4.0                           | –    | 0.6                            | –    | μs   |
| t <sub>LOW</sub>    | SCL LOW period  |                      | 4.7                           | –    | 1.3                            | –    | μs   |
| t <sub>HIGH</sub>   | SCL HIGH period   |                      | 4.0                           | –    | 0.6                            | –    | μs   |
| t <sub>SU;STA</sub> | set-up time for a repeated START condition  |                      | 4.7                           | –    | 0.6                            | –    | μs   |
| t <sub>HD;DAT</sub> | DATA hold time  |                      | 0                             | –    | 0                              | 0.9  | μs   |
| t <sub>SU;DAT</sub> | DATA set-up time  |                      | 250                           | –    | 100                            | –    | μs   |
| t <sub>r</sub>      | rise time of both SDA and SCL signals   | C <sub>b</sub> in pF | –                             | 1000 | 20 + 0.1C <sub>b</sub>         | 300  | μs   |
| t <sub>f</sub>      | fall time of both SDA and SCL signals   | C <sub>b</sub> in pF | –                             | 300  | 20 + 0.1C <sub>b</sub>         | 300  | μs   |
| t <sub>SU;STO</sub> | set-up time for STOP condition  |                      | 4.0                           | –    | 0.6                            | –    | μs   |
| C <sub>b</sub>      | capacitive load for each bus line   |                      | –                             | 400  | –                              | 400  | pF   |
| t <sub>SP</sub>     | pulse width of spikes to be suppressed by input filter                                      |                      | not applicable                |      | 0                              | 50   | ns   |

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**12.3 Memory map specification and register overview**

The SAA7705H memory map contains all defined bits. The map is split up in two different sections: the hardware memory registers and the RAM definitions. In Table 5 the memory map is depicted. Table 6 shows the detailed memory map locations.

**Table 5** Memory map

| ADDRESS        | FUNCTION            | SIZE            |
|----------------|---------------------|-----------------|
| 9C00H to 9FFFH | reserved            | 1 024 × 32 bits |
| 9000H to 9BFFH | not used            |                 |
| 8000H to 8FFFH | reserved            | 4 096 × 28 bits |
| 1000H to 7FFFH | not used            |                 |
| 0FF9H to 0FFFH | DSP core            | 7 × 16 bits     |
| 0FF4H to 0FF8H | reserved            | 5 × 16 bits     |
| 0FF3H          | RDS                 | 1 × 16 bits     |
| 0FEEH to 0FF2H | reserved            | 5 × 16 bits     |
| 0FA8H to 0FEDH | not used            |                 |
| 0F80H to 0FA7H | equalizer           | 40 × 16 bits    |
| 0B30H to 0F7FH | not used            |                 |
| 0AFFH to 0B2FH | reserved            | 49 × 16 bits    |
| 0AC0H to 0AFEH | not used            |                 |
| 0A80H to 0ABFH | reserved            | 65 × 16 bits    |
| 0A40H to 0A7FH | not used            |                 |
| 0A00H to 0A3FH | reserved            | 65 × 16 bits    |
| 0980H to 09FFH | reserved YRAM space |                 |
| 0800H to 097FH | YRAM                | 384 × 12 bits   |
| 0200H to 07FFH | not used            |                 |
| 0180H to 01FFH | reserved XRAM space |                 |
| 0000H to 017FH | XRAM                | 384 × 18 bits   |

**Table 6** Register overview

| ADDRESS       | NAME     | DESCRIPTION                             |
|---------------|----------|---|
| <b>EPICS6</b> |          |   |
| 0FFFH         | DCSCTR   | DCS control register (see Table 7)      |
| 0FFEH         | DCSDIV   | DCS divide register (see Table 8)       |
| 0FFDH         | AD       | AD register (see Table 9)               |
| 0FFCH         | LEVELIAC | IAC level register (see Table 10)       |
| 0FFBH         | IAC      | IAC register (see Table 11)             |
| 0FFAH         | SEL      | Input selection register (see Table 12) |
| 0FF9H         | HOST     | Host register (see Table 13)            |
| <b>RDS</b>    |          |   |
| 0FF3H         | RDSCTR   | RDS control register (see Table 14)     |

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## 12.4 Register description

**Table 7** DCSCCTR register (address 0FFFH)

| NAME          | SIZE (BITS) | DESCRIPTION  | DEFAULT             | BIT POSITION |
|---------------|-------------|--|---------------------|--------------|
| CLK-ISN-ONOFF | 1           | ISN clock<br>1: off<br>0: on                           | 1 (off)             | 15           |
| PLL-DIV       | 4           | PLL clock division factor (see Table 15)               | 1010 (154)          | 14 to 11     |
| LOOPO-ONOFF   | 1           | Loopo<br>1: on<br>0: off                               | 0 (off)             | 10           |
| GAIN-HL       | 1           | variable loop-gain stereo decoder<br>1: high<br>0: low | 1 (high)            | 9            |
| LOCKED-PRESET | 1           | DCS clock<br>1: locked<br>0: preset                    | 1 (locked)          | 8            |
| F1-COEF       | 4           | coarse division factor F1 (see Table 16)               | 0010 (F1 = 11)      | 7 to 4       |
| F0-COEF       | 4           | coarse division factor F0 (see Table 16)               | 0011<br>(F0 = 11.5) | 3 to 0       |

**Table 8** DCSDIV register (address 0FFEh)

| NAME     | SIZE (BITS) | DESCRIPTION                      | DEFAULT | BIT POSITION |
|----------|-------------|----------------------------------|---------|--------------|
| DCS-COEF | 16          | Sigma-Delta modulator V (note 1) | 28EDH   | 15 to 0      |

**Note**

1. DCS-COEF can be calculated by the multiplication  $V \times 2^{15}$  and then convert this decimal value to hexadecimal.



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**Table 9** AD register (address 0FFDH)

| NAME      | SIZE (BITS) | DESCRIPTION   | DEFAULT           | BIT POSITION |
|-----------|-------------|---|-------------------|--------------|
| LDEF      | 3           | always in position 000  | 000               | 15 to 13     |
| TWO-FOUR  | 1           | equalizer configuration<br>1: two channels<br>0: four channels      | 0 (four channels) | 12           |
| DSPTURBO  | 1           | PLL output frequency<br>1: double<br>0: no doubling                 | 0 (no doubling)   | 11           |
| –         | 4           | reserved  | –                 | 10 to 7      |
| VOLFM     | 3           | input sensitivity FMMPX input (see Table 17)                        | 110 (200 mV)      | 6, 5 and 4   |
| VOLRDS    | 3           | input sensitivity FMRDS input (see Table 17)                        | 110 (200 mV)      | 3, 2 and 1   |
| SELTWOTUN | 1           | select one- or two-tuner operation<br>1: two tuners<br>0: one tuner | 0 (one tuner)     | 0            |

**Table 10** LEVELIAC register (address 0FFCH)

| NAME                | SIZE (BITS) | DESCRIPTION   | DEFAULT         | BIT POSITION |
|---------------------|-------------|---|-----------------|--------------|
| LEV-EN-DYN-IAC      | 1           | FM frequency sweep dependent IAC<br>1: enable<br>0: disable             | 0 (disable)     | 15           |
| LEV-DYN-IAC-DEV     | 2           | deviation threshold frequency setting of the dynamic IAC (see Table 18) | 00 (50 kHz)     | 14 and 13    |
| –                   | 5           | not used  | –               | 12 to 8      |
| LEV-IAC-STRETCH     | 2           | level-IAC stretch time (see Table 19)                                   | 10 (13 periods) | 7 and 6      |
| LEV-IAC-FEEDFORWARD | 2           | level-IAC deviation feed-forward factor (see Table 20)                  | 00 (–2 periods) | 5 and 4      |
| LEV-IAC-THRESHOLD   | 4           | level-IAC threshold settings (see Table 21)                             | 0000 (off)      | 3 to 0       |

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**Table 11** IAC register (address 0FFBH)

| NAME        | SIZE (BITS) | DESCRIPTION  | DEFAULT                        | BIT POSITION |
|-------------|-------------|--|--------------------------------|--------------|
| IACTRIGGER  | 1           | input selection for IAC triggering<br>1: IAC output<br>0: DSPOUT2 output | 0 (DSPOUT2)                    | 15           |
| —           | 3           | not used   |                                | 14 to 12     |
| AGC         | 1           | AGC set point<br>1: $\frac{1}{256}$<br>0: $\frac{1}{128}$                | 1 $\left(\frac{1}{256}\right)$ | 11           |
| MPXDELAY    | 2           | IAC delay settings MPX (see Table 22)                                    | 01 (5 periods)                 | 10 and 9     |
| SUPPRESSION | 3           | IAC stretch time suppression (see Table 23)                              | 011 (2 samples)                | 8, 7 and 6   |
| FEEDFORWARD | 3           | IAC deviation feed-forward factor (see Table 24)                         | 101 (0.00781)                  | 5, 4 and 3   |
| THRESHOLD   | 3           | IAC threshold sensitivity (see Table 25)                                 | 101 (0.031)                    | 2, 1 and 0   |

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**Table 12** SEL register (address 0FFAH)

| NAME         | SIZE (BITS) | DESCRIPTION  | DEFAULT                  | BIT POSITION |
|--------------|-------------|--|--------------------------|--------------|
| ADC-BWSWITCH | 1           | processing base SCAD1, SCAD2 and LAD<br>1: 44.1 kHz<br>0: 38 kHz                                       | 0 (38 kHz)               | 15           |
| —            | 1           | not used   |                          | 14           |
| INVHOSTWS    | 1           | word select<br>1: inverting<br>0: non-inverting  | 0 (non-inverting)        | 13           |
| NSDEC        | 1           | select noise detector<br>1: ratio 1 : 8<br>0: ratio 1 : 4  | 1 (1 : 8)                | 12           |
| ADCSRC       | 1           | compensation switch for Audio-AD   | 0 (Audio-AD, required)   | 11           |
| —            | 1           | reserved   | —                        | 10           |
| DCOFFSET     | 1           | DC offset filter<br>1: off<br>0: on  | 0 (on)                   | 9            |
| BYPASSPLL    | 1           | clock oscillator signal handling by PLL<br>1: PLL by-passed<br>0: PLL active                           | 0 (PLL active)           | 8            |
| DEF          | 1           | selection<br>1: 19 kHz (microphone input and compensation filter)<br>0: 29 kHz (level filter position) | 0 (29 kHz)               | 7            |
| WIDE-NARROW  | 1           | selection<br>1: audio data<br>0: audio + RDS info  | 1 (audio data, required) | 6            |
| LEVAM-FM     | 1           | select input for level detector<br>1: AM level (pin AML)<br>0: FM level (pin FML)                      | 0 (FM level)             | 5            |
| —            | 1           | reserved   | —                        | 4            |
| CD-TAPE      | 1           | select audio input<br>1: CD<br>0: TAPE   | 1 (CD)                   | 3            |
| AM-TAPE      | 1           | select audio input<br>1: AM<br>0: TAPE   | 0 (TAPE)                 | 2            |
| AUX-FM       | 1           | select audio input<br>1: CD left<br>0: FM  | 0 (FM)                   | 1            |
| —            | 1           | reserved   | —                        | 0            |

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**Table 13** HOST register (address 0FF9H)

| NAME           | SIZE (BITS) | DESCRIPTION  | DEFAULT                                      | BIT POSITION |
|----------------|-------------|--|--|--------------|
| CLOOP-MODE     | 3           | cloop mode (see Table 27)                                | 110 (WS 50% duty cycle + BCLK/4)             | 15 to 13     |
| ENHOSTIO       | 1           | external I <sup>2</sup> S-bus<br>1: enable<br>0: disable | 0 (disable)                                  | 12           |
| HOST-IO-FORMAT | 2           | host input/output data format (see Table 28)             | 00 (standard I <sup>2</sup> S-bus, required) | 11 and 10    |
| AUDIO-FORMAT   | 3           | audio register data format (see Table 29)                | 000 (ISN)                                    | 9, 8 and 7   |
| AUDIO-SOURCE   | 2           | audio selection register (see Table 30)                  | 01 (ISN)                                     | 6 and 5      |
| —              | 5           | reserved   | —  | 4 to 0       |

**Table 14** RDSCTR register (address 0FF3H)

| NAME      | SIZE (BITS) | DESCRIPTION  | DEFAULT        | BIT POSITION |
|-----------|-------------|--|----------------|--------------|
| —         | 7           | reserved   | —              | 15 to 9      |
| RDS-CLKIN | 1           | select output for RDS<br>1: buffered RDS with RDS clock input<br>0: RDS output | 0 (RDS output) | 8            |
| —         | 8           | reserved   | —              | 7 to 0       |

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## 12.5 Detailed register description

Table 15 PLL clock division factor (PLL-DIV bits)

| PLL-DIV |        |        |        | PLL CLOCK DIVISION FACTOR |                          |
|---------|--------|--------|--------|---------------------------|--------------------------|
| BIT 14  | BIT 13 | BIT 12 | BIT 11 | dsp-turbo = 0             | dsp-turbo = 1 (not used) |
| 0       | 0      | 0      | 0      | 93                        | 186                      |
| 0       | 0      | 0      | 1      | 99                        | 198                      |
| 0       | 0      | 1      | 0      | 106                       | 106                      |
| 0       | 0      | 1      | 1      | 113                       | 212                      |
| 0       | 1      | 0      | 0      | 121                       | 242                      |
| 0       | 1      | 0      | 1      | 126                       | 252                      |
| 0       | 1      | 1      | 0      | 132                       | 264                      |
| 0       | 1      | 1      | 1      | 137                       | 274                      |
| 1       | 0      | 0      | 0      | 143                       | 286                      |
| 1       | 0      | 0      | 1      | 148                       | 296                      |
| 1       | 0      | 1      | 0      | 154 (default)             | 308                      |
| 1       | 0      | 1      | 1      | 159                       | 318                      |
| 1       | 1      | 0      | 0      | 165                       | 330                      |
| 1       | 1      | 0      | 1      | 170                       | 340                      |
| 1       | 1      | 1      | 0      | 176                       | 352                      |
| 1       | 1      | 1      | 1      | 181                       | 362                      |

Table 16 Representation of division factors F0 and F1

| F0-COEF/F1-COEF |         |         |         |           | DIVISION FACTOR<br>F0/F1 |
|-----------------|---------|---------|---------|-----------|--------------------------|
| BIT 3/7         | BIT 2/6 | BIT 1/5 | BIT 0/4 | HEX-VALUE |                          |
| 1               | 0       | 0       | 0       | 8H        | 6                        |
| 1               | 0       | 0       | 1       | 9H        | 6.5                      |
| 1               | 0       | 1       | 0       | AH        | 7                        |
| 1               | 0       | 1       | 1       | BH        | 7.5                      |
| 1               | 1       | 0       | 0       | CH        | 8                        |
| 1               | 1       | 0       | 1       | DH        | 8.5                      |
| 1               | 1       | 1       | 0       | EH        | 9                        |
| 1               | 1       | 1       | 1       | FH        | 9.5                      |
| 0               | 0       | 0       | 0       | 0H        | 10                       |
| 0               | 0       | 0       | 1       | 1H        | 10.5                     |
| 0               | 0       | 1       | 0       | 2H        | 11 (default F1)          |
| 0               | 0       | 1       | 1       | 3H        | 11.5 (default F0)        |
| 0               | 1       | 0       | 0       | 4H        | 12                       |
| 0               | 1       | 0       | 1       | 5H        | 12.5                     |
| 0               | 1       | 1       | 0       | 6H        | 13                       |
| 0               | 1       | 1       | 1       | 7H        | 13.5                     |

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**Table 17** Volume control of the FMMPX and FMRDS input by the AD register.

| VOLFM/VOLRDS |         |         | FMMPX/FMRDS INPUTS        |                         |                                  |
|--------------|---------|---------|---------------------------|-------------------------|----------------------------------|
|              |         |         | INPUT VOLTAGE             |                         | INPUT IMPEDANCE<br>(k $\Omega$ ) |
| BIT 3/6      | BIT 2/5 | BIT 1/4 | AT 22.5 kHz SWEEP<br>(mV) | FOR 0 dB AT DSP<br>(mV) |                                  |
| 0            | 0       | 0       | 65                        | 410                     | 137                              |
| 0            | 0       | 1       | 78                        | 493                     | 103                              |
| 0            | 1       | 0       | 93                        | 587                     | 84.8                             |
| 0            | 1       | 1       | 111                       | 700                     | 74                               |
| 1            | 0       | 0       | 132                       | 833                     | 67                               |
| 1            | 0       | 1       | 158                       | 1000                    | 62                               |
| 1            | 1       | 0       | 188 (default)             | 1188 (default)          | 58.4 (default)                   |
| 1            | 1       | 1       | 225                       | 1387                    | 56                               |

**Table 18** Dynamic IAC deviation threshold

| LEV-DYN-IAC-DEV |        | DEVIATION<br>(kHz) |
|-----------------|--------|--------------------|
| BIT 14          | BIT 13 |                    |
| 0               | 0      | 43 (default)       |
| 0               | 1      | 48.5               |
| 1               | 0      | 58                 |
| 1               | 1      | 65                 |

**Table 19** IAC-level stretch time

| LEV-IAC-STRETCH |       | PULSE LENGTH ON SINGLE TRIGGER IN PERIODS OF 304 kHz |
|-----------------|-------|--|
| BIT 7           | BIT 6 |  |
| 0               | 0     | 9  |
| 0               | 1     | 11 (default)   |
| 1               | 0     | 13   |
| 1               | 1     | 15   |

**Table 20** IAC-level deviation feed-forward factor

| LEV-IAC-FEEDFORWARD |       | DELAY (DECIMAL VALUE) IN PERIODS OF 304 kHz |
|---------------------|-------|---|
| BIT 5               | BIT 4 |   |
| 0                   | 0     | -2 (default)                                |
| 0                   | 1     | -1  |
| 1                   | 0     | 0   |
| 1                   | 1     | 1   |

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**Table 21** Level IAC threshold settings

| LEVEL-IAC-THRESHOLD |       |       |       | THRESHOLD               |              |
|---------------------|-------|-------|-------|-------------------------|--------------|
| BIT 3               | BIT 2 | BIT 1 | BIT 0 | DECIMAL VALUE           | BINARY VALUE |
| 0                   | 0     | 0     | 0     | level-IAC off (default) |              |
| 0                   | 0     | 0     | 1     | 0.02                    | 0.0000010    |
| 0                   | 0     | 1     | 0     | 0.025                   | 0.0000011    |
| 0                   | 0     | 1     | 1     | 0.0316                  | 0.0000100    |
| 0                   | 1     | 0     | 0     | 0.04                    | 0.0000101    |
| 0                   | 1     | 0     | 1     | 0.05                    | 0.0000110    |
| 0                   | 1     | 1     | 0     | 0.063                   | 0.0001000    |
| 0                   | 1     | 1     | 1     | 0.08                    | 0.0001010    |
| 1                   | 0     | 0     | 0     | 0.1                     | 0.0001101    |
| 1                   | 0     | 0     | 1     | 0.126                   | 0.0010000    |
| 1                   | 0     | 1     | 0     | 0.16                    | 0.0010100    |
| 1                   | 0     | 1     | 1     | 0.2                     | 0.0011010    |
| 1                   | 1     | 0     | 0     | 0.25                    | 0.0100000    |
| 1                   | 1     | 0     | 1     | 0.316                   | 0.0101000    |
| 1                   | 1     | 1     | 0     | 0.4                     | 0.0110100    |
| 1                   | 1     | 1     | 1     | 0.5                     | 0.1000000    |

**Table 22** IAC delay settings MPX

| MPX-DELAY |       | DELAY (DECIMAL VALUE) IN PERIODS OF 304 kHz |
|-----------|-------|---|
| BIT 10    | BIT 9 |   |
| 1         | 0     | 2   |
| 1         | 1     | 3   |
| 0         | 0     | 4   |
| 0         | 1     | 5 (default)                                 |

**Table 23** IAC stretch time suppression

| SUPPRESSION |       |       | STRETCH TIME SUPPRESSION       |                             |
|-------------|-------|-------|--------------------------------|-----------------------------|
| BIT 8       | BIT 7 | BIT 6 | PULSE LENGTH ON SINGLE TRIGGER | STRETCH (NUMBER OF SAMPLES) |
| 1           | 0     | 1     | 0                              | not applicable              |
| 1           | 0     | 0     | 1                              | 0                           |
| 1           | 1     | 1     | 2                              | 1                           |
| 1           | 1     | 0     | 3                              | 2                           |
| 0           | 0     | 1     | 4                              | 3                           |
| 0           | 0     | 0     | 5                              | 4                           |
| 0           | 1     | 1     | 6                              | 5 (default)                 |
| 0           | 1     | 0     | 7                              | 6                           |

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**Table 24** IAC deviation feed-forward factor

| FEEDFORWARD |       |       | FACTOR            |                |
|-------------|-------|-------|-------------------|----------------|
| BIT 5       | BIT 4 | BIT 3 | DECIMAL VALUE     | BINARY VALUE   |
| 0           | 1     | 1     | 0.00146           | 0.000000000110 |
| 0           | 1     | 0     | 0.00195           | 0.000000001000 |
| 0           | 0     | 1     | 0.00293           | 0.000000001100 |
| 0           | 0     | 0     | 0.00391           | 0.000000010000 |
| 1           | 1     | 1     | 0.00586           | 0.000000011000 |
| 1           | 1     | 0     | 0.00781           | 0.000000100000 |
| 1           | 0     | 1     | 0.01172 (default) | 0.000000110000 |
| 1           | 0     | 0     | 0.00000           | 0.000000000000 |

**Table 25** IAC threshold sensitivity

| DYN-IAC-DEV |       |       | THRESHOLD       |                |
|-------------|-------|-------|-----------------|----------------|
| BIT 2       | BIT 1 | BIT 0 | DECIMAL VALUE   | BINARY VALUE   |
| 1           | 0     | 0     | 0.027           | 0.000001110000 |
| 1           | 0     | 1     | 0.031 (default) | 0.000010000000 |
| 1           | 1     | 0     | 0.038           | 0.000010011100 |
| 1           | 1     | 1     | 0.047           | 0.000011000000 |
| 0           | 0     | 0     | 0.055           | 0.000011100000 |
| 0           | 0     | 1     | 0.063           | 0.000100000000 |
| 0           | 1     | 0     | 0.074           | 0.000100110000 |
| 0           | 1     | 1     | 0.085           | 0.000101100000 |



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**Table 26** Analog input selection; notes 1 and 2

| MODE                      | AM-TAPE          | AUX-FM           | CD-TAPE          | SELTWOTUN        | LEVAM-FM         |
|---------------------------|------------------|------------------|------------------|------------------|------------------|
| FMMPX one tuner mode      | X <sup>(3)</sup> | 0                | 1                | 0                | 0                |
| FMMPX two tuner mode      | X <sup>(3)</sup> | 0                | 1                | 1                | 0                |
| AM                        | 1                | X <sup>(3)</sup> | 0                | X <sup>(3)</sup> | 1                |
| CD-ANALOG                 | X <sup>(3)</sup> | 1                | 1                | X <sup>(3)</sup> | X <sup>(3)</sup> |
| MICROPHONE <sup>(4)</sup> | X <sup>(3)</sup> | X <sup>(3)</sup> | X <sup>(3)</sup> | X <sup>(3)</sup> | 1                |
| TAPE                      | 0                | X <sup>(3)</sup> | 0                | X <sup>(3)</sup> | X <sup>(3)</sup> |

**Notes**

1. It is assumed that the AM level input is used for AM reception and the FM level input for FM reception. It is, however, also possible to have a combined AM and FM level output from the tuner. In that case the FM level input should be used and the LEVAM-FM should remain logic 0.
2. In all the positions it is assumed that pin SELFR is LOW.
3. X = don't care.
4. In the MICROPHONE position it is assumed that the microphone is connected to the AML input. When using a microphone the bandwidth of the level decimation path is limited to 19 kHz. In all other cases the bandwidth is 29 kHz. At the same time the I<sup>2</sup>C-bus bit DEF of the SEL register must be put in the 'voice' = logic 1 position.

**Table 27** Cloop mode settings

| CLOOP-MODE       |        |        | OUTPUT                      |
|------------------|--------|--------|-----------------------------|
| BIT 15           | BIT 14 | BIT 13 |                             |
| Word select (WS) |        |        |                             |
| 0                | –      | –      | bypass WS                   |
| 1                | –      | –      | WS 50% duty-cycle (default) |
| Bit clock (BCLK) |        |        |                             |
| –                | 0      | 0      | bypass BCLK                 |
| –                | 0      | 1      | divide BCLK by 2            |
| –                | 1      | 0      | divide BCLK by 4 (default)  |
| –                | 1      | 1      | divide BCLK by 8            |

**Table 28** Host input/output data format

| HOST-IO-FORMAT |        | OUTPUT                                  |
|----------------|--------|---|
| BIT 11         | BIT 10 |   |
| 0              | 0      | standard I <sup>2</sup> S-bus (default) |
| 0              | 1      | LSB-justified, 16 bits                  |
| 1              | 0      | LSB-justified, 18 bits                  |
| 1              | 1      | LSB-justified, 20 bits                  |

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**Table 29** Audio register data format

| AUDIO-FORMAT |       |       | OUTPUT                        |
|--------------|-------|-------|-------------------------------|
| BIT 9        | BIT 8 | BIT 7 |                               |
| 0            | 0     | 0     | ISN, LSB first (default)      |
| –            | 0     | 1     | LSB-justified, 16 bits        |
| –            | 1     | 0     | LSB-justified, 18 bits        |
| –            | 1     | 1     | LSB-justified, 20 bits        |
| 1            | 0     | 0     | standard I <sup>2</sup> S-bus |

**Table 30** Audio selection register

| AUDIO-SOURCE |       | OUTPUT                        |
|--------------|-------|-------------------------------|
| BIT 6        | BIT 5 |                               |
| 0            | 0     | Audio-AD                      |
| 0            | 1     | ISN L + R and R – L (default) |
| 1            | 0     | external CD1                  |
| 1            | 1     | external CD2                  |

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## 13 APPLICATION INFORMATION

The application diagram shown in Figs 21 and 22 must be considered as one of the examples of a (limited) application of the chip e.g. in this case the I<sup>2</sup>S-bus inputs of the CD1 and CD2 are not used. For the real application set-up the information of the application report and application support by Philips is necessary on issues such as EMC, kappa reduction of the package, DSP program, etc.

## 13.1 Software description

The use and description of the software features of the SAA7705H is described in the separate manual:

*"USER MANUAL SAA7705H, report no. NBA/AN9704, Version 2.1, Author G. Willighagen"*

Further information about the programming of the EPICS6 DSP core is available in *"EPICS6 Programmer's Guide, version 1.3, July 3 1997, Author Ron Schiffelers, CIC development Nijmegen"*

The availability of a programmer's guide does not mean that the normal procedure enables the customer to develop their own DSP software.

## 13.2 Power supply connection and EMC

The digital part of the chip has in total 7 positive supply line connections and 7 ground connections. To minimise radiation the chip should be put on a double layer Printed-Circuit Board (PCB) with on one side a large ground plane. The ground supply lines should have a short connection to this ground plane. A coil and capacitor network in the positive supply line can be used as high frequency filter.

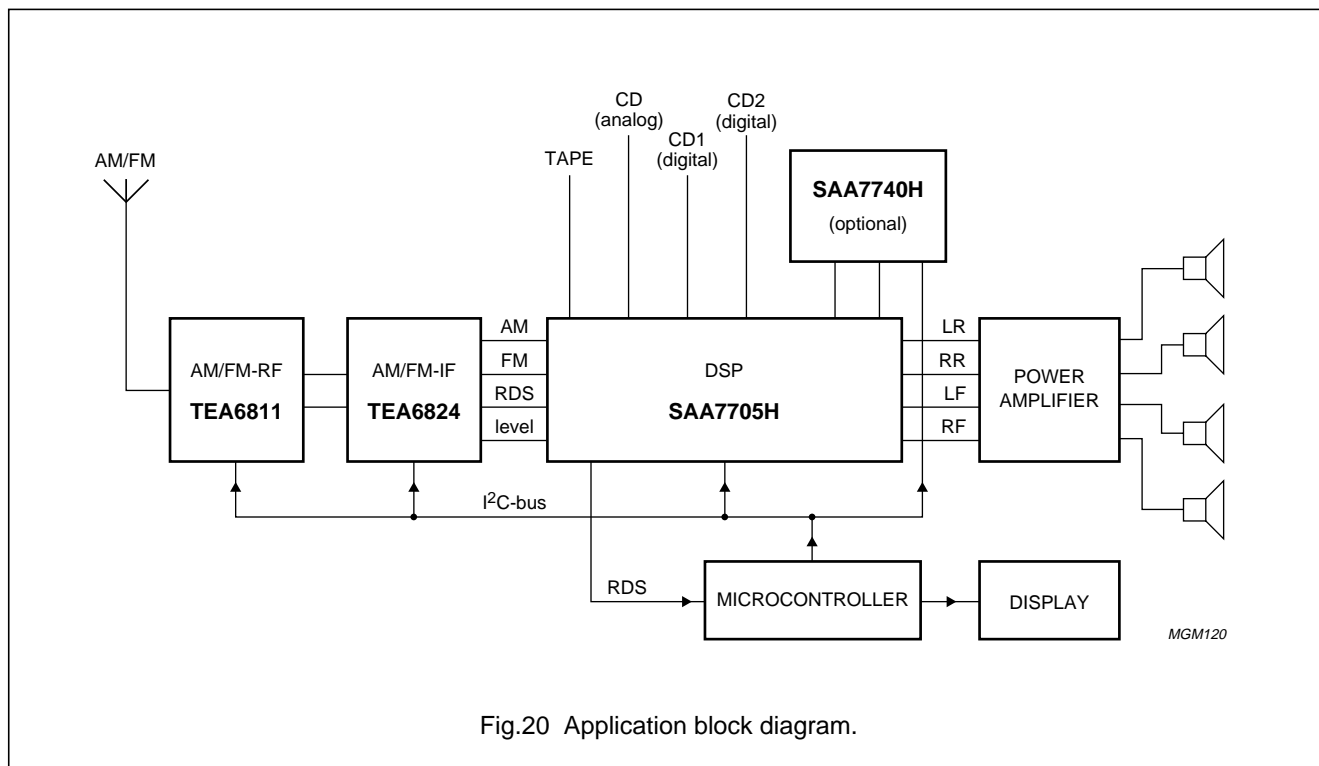


Fig.20 Application block diagram.

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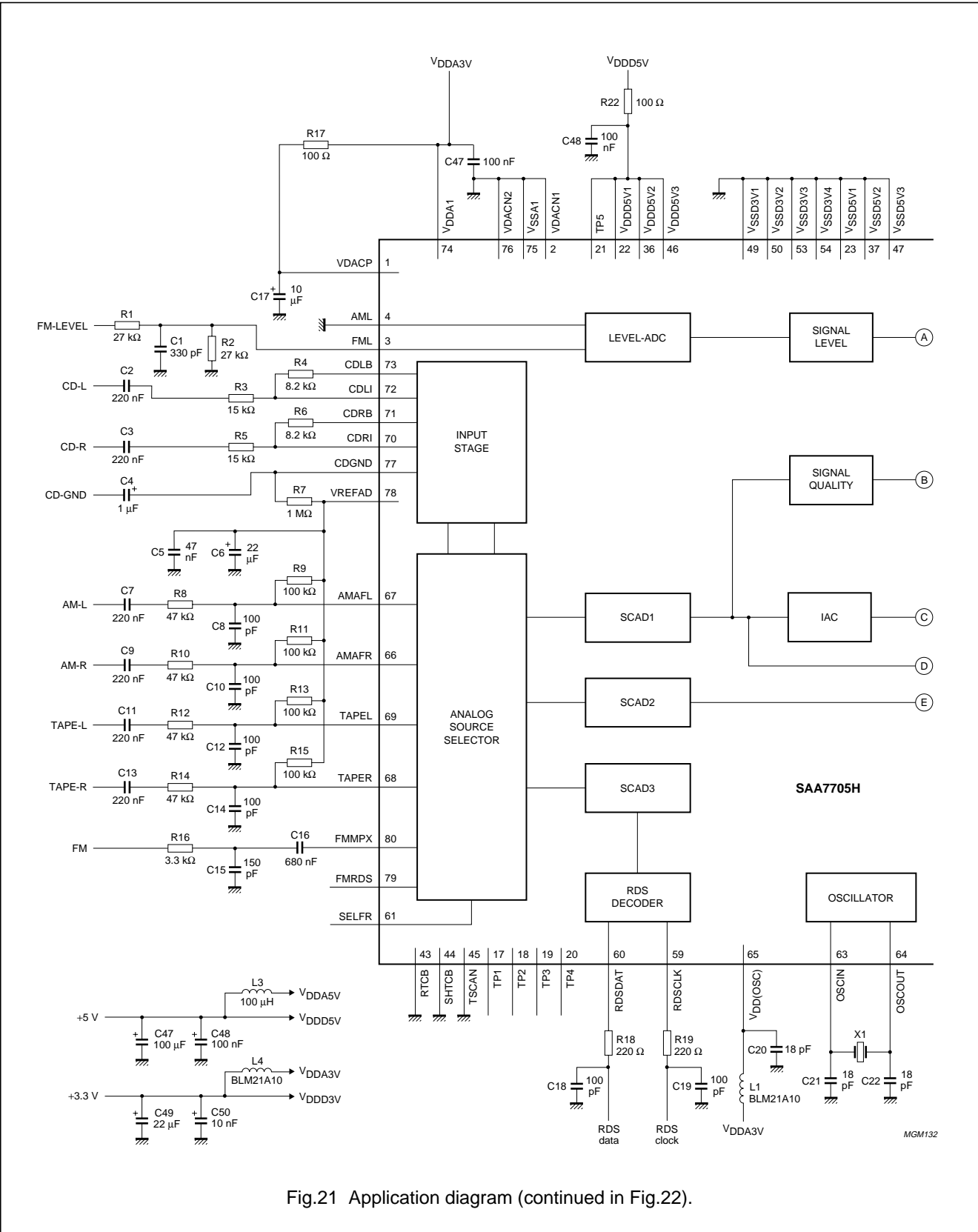


Fig.21 Application diagram (continued in Fig.22).

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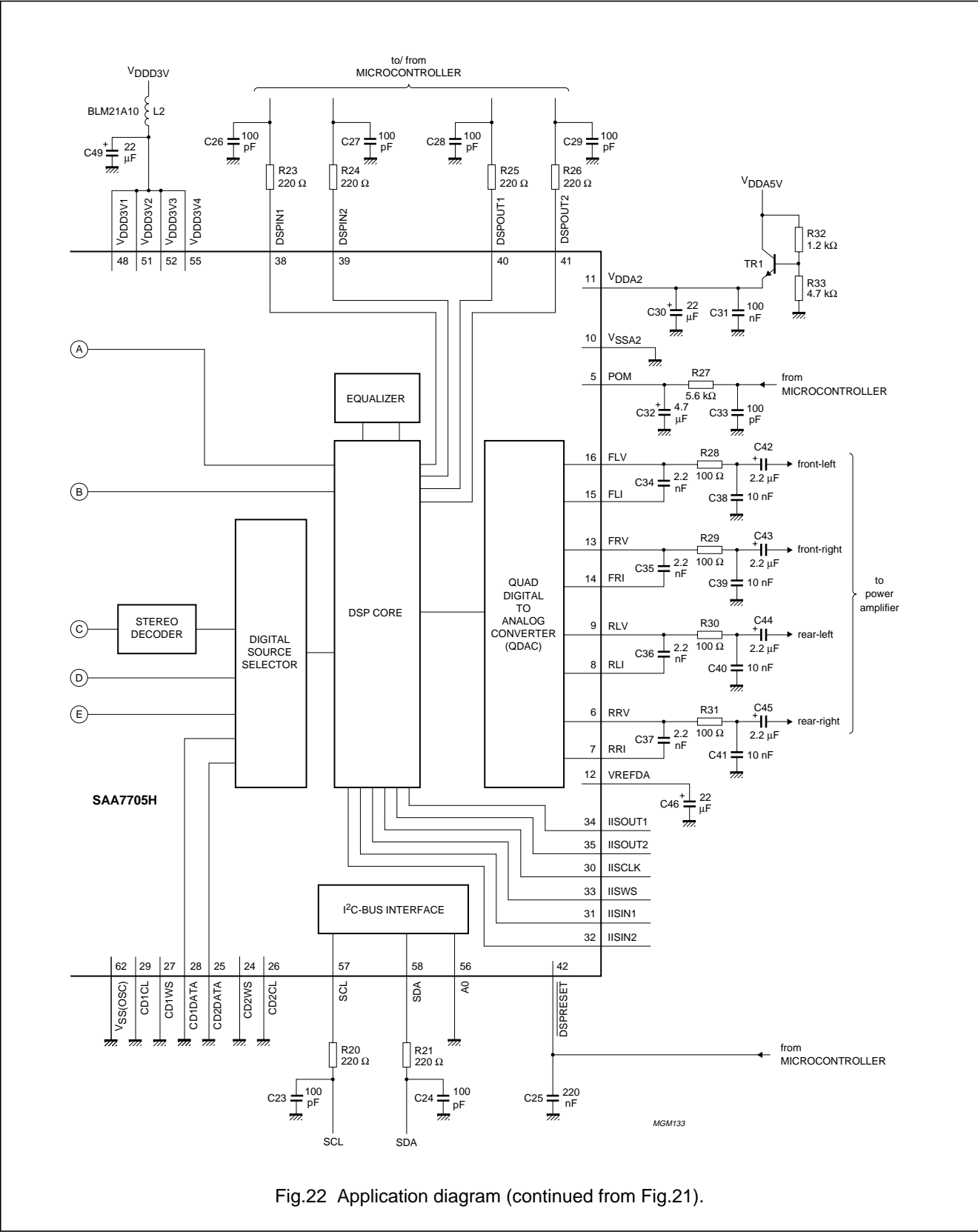


Fig.22 Application diagram (continued from Fig.21).

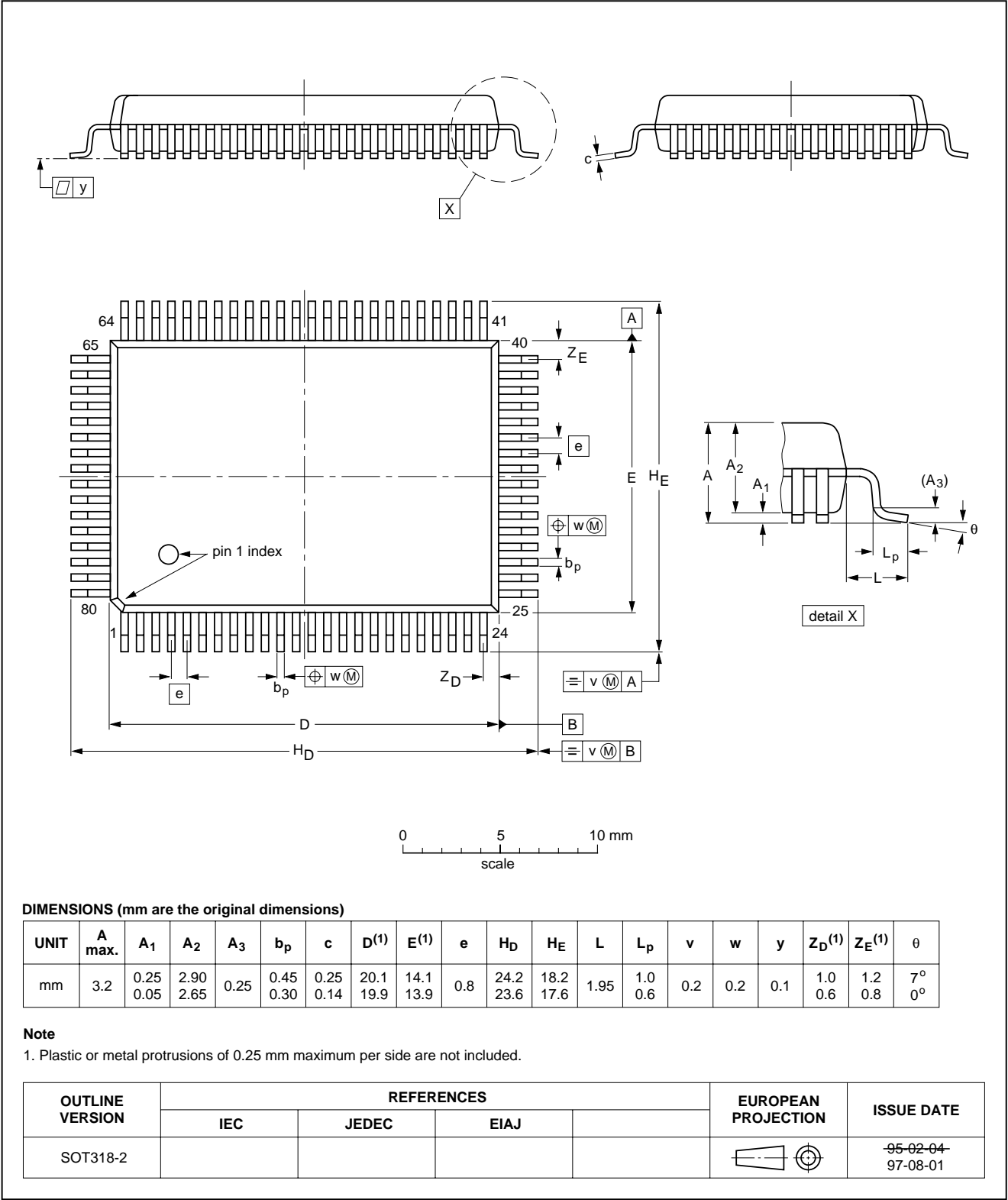
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14 PACKAGE OUTLINE

QFP80: plastic quad flat package; 80 leads (lead length 1.95 mm); body 14 x 20 x 2.8 mm

SOT318-2



## Car radio Digital Signal Processor (DSP)

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### 15 SOLDERING

#### 15.1 Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering is not always suitable for surface mount ICs, or for printed-circuit boards with high population densities. In these situations reflow soldering is often used.

#### 15.2 Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, infrared/convection heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferably be kept below 230 °C.

#### 15.3 Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

The footprint must incorporate solder thieves at the downstream end.

- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

#### 15.4 Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

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## 15.5 Suitability of surface mount IC packages for wave and reflow soldering methods

| PACKAGE                         | SOLDERING METHOD                  |                       |
|---------------------------------|-----------------------------------|-----------------------|
|                                 | WAVE                              | REFLOW <sup>(1)</sup> |
| BGA, SQFP                       | not suitable                      | suitable              |
| HLQFP, HSQFP, HSOP, HTSSOP, SMS | not suitable <sup>(2)</sup>       | suitable              |
| PLCC <sup>(3)</sup> , SO, SOJ   | suitable                          | suitable              |
| LQFP, QFP, TQFP                 | not recommended <sup>(3)(4)</sup> | suitable              |
| SSOP, TSSOP, VSO                | not recommended <sup>(5)</sup>    | suitable              |

**Notes**

1. All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *"Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods"*.
2. These packages are not suitable for wave soldering as a solder joint between the printed-circuit board and heatsink (at bottom version) can not be achieved, and as solder may stick to the heatsink (on top version).
3. If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
4. Wave soldering is only suitable for LQFP, TQFP and QFP packages with a pitch (e) equal to or larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
5. Wave soldering is only suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.



## Car radio Digital Signal Processor (DSP)

SAA7705H

**16 DEFINITIONS**

| <b>Data sheet status</b>  |   |
|---|---|
| Objective specification   | This data sheet contains target or goal specifications for product development.       |
| Preliminary specification   | This data sheet contains preliminary data; supplementary data may be published later. |
| Product specification   | This data sheet contains final product specifications.                                |
| <b>Limiting values</b>  |   |
| Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability. |   |
| <b>Application information</b>  |   |
| Where application information is given, it is advisory and does not form part of the specification.   |   |

**17 LIFE SUPPORT APPLICATIONS**

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.

**18 PURCHASE OF PHILIPS I<sup>2</sup>C COMPONENTS**

Purchase of Philips I<sup>2</sup>C components conveys a license under the Philips' I<sup>2</sup>C patent to use the components in the I<sup>2</sup>C system provided the system conforms to the I<sup>2</sup>C specification defined by Philips. This specification can be ordered using the code 9398 393 40011.

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Car radio Digital Signal Processor (DSP)

SAA7705H

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**NOTES**

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Car radio Digital Signal Processor (DSP)

SAA7705H

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**NOTES**

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