CAT24FC02

2-kb I²C Serial EEPROM

FEATURES

- 400 kHz (2.5 V) I²C bus compatible
- 2.5 to 5.5 volt operation
- Low power CMOS technology
- 16-byte page write buffer
- Industrial and extended temperature ranges
- Self-timed write cycle with auto-clear
- 1,000,000 program/erase cycles
- 100 year data retention
- 8-pin DIP, SOIC, TSSOP and MSOP packages - "Green" package option available
- 256 x 8 memory organization
- Hardware write protect

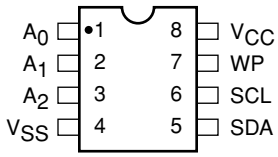
DESCRIPTION

The CAT24FC02 is a 2-kb Serial CMOS EEPROM internally organized as 256 words of 8 bits each. Catalyst's advanced CMOS technology substantially reduces device power requirements.

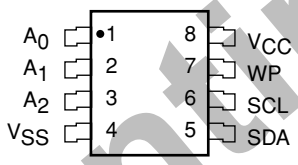
The CAT24FC02 features a 16-byte page write buffer. The device operates via the I²C bus serial interface and is available in 8-pin DIP, SOIC, TSSOP and MSOP packages.

PIN CONFIGURATION

DIP Package (P, L, GL)

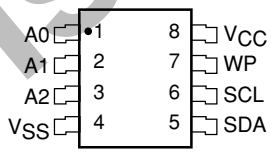


SOIC Package (J, W, GW)



TSSOP Package (U, Y, GY)

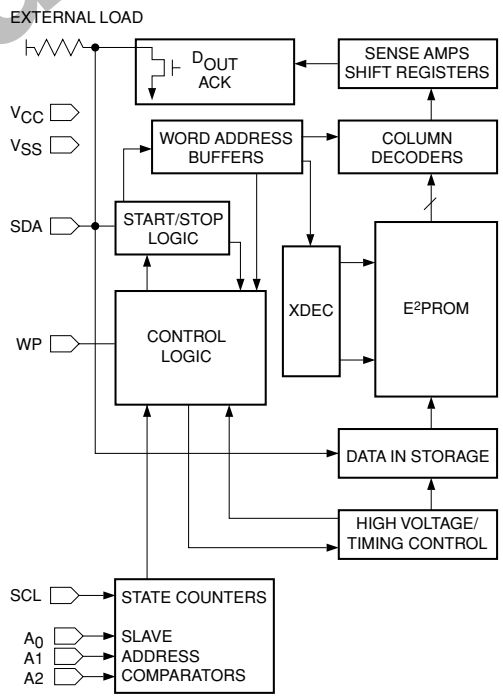
MSOP Package (R, Z, GZ)



PIN FUNCTIONS

Pin Name	Function
A0, A1, A2	Device Address Inputs
SDA	Serial Data/Address
SCL	Serial Clock
WP	Write Protect
V_{CC}	2.5 V to 5.5 V Power Supply
V_{SS}	Ground

BLOCK DIAGRAM



* Catalyst Semiconductor is licensed by Philips Corporation to carry the I²C Bus Protocol.

Doc. No. 1045, Rev. G

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias –55°C to +125°C

Storage Temperature ..... –65°C to +150°C

Voltage on Any Pin with Respect to Ground(1) .....–2.0 V to V_{CC} + 2.0 V

V_{CC} with Respect to Ground ..... –2.0 V to +7.0 V

Package Power Dissipation Capability (T_A = 25°C) ..... 1.0 W

Lead Soldering Temperature (10 seconds) ..... 300°C

Output Short Circuit Current(2) ..... 100 mA

*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions outside of those listed in the operational sections of this specification is not implied. Exposure to any absolute maximum rating for extended periods may affect device performance and reliability.

RELIABILITY CHARACTERISTICS (3)

Symbol	Parameter	Min	Typ	Max	Units
N_{END}	Endurance	1,000,000			Cycles/Byte
T_{DR}	Data Retention	100			Years
V_{ZAP}	ESD Susceptibility	4000			Volts
I_{LTH}(4)	Latch-up	100			mA

D.C. OPERATING CHARACTERISTICS

V_{CC} = 2.5 V to 5.5 V, unless otherwise specified.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
I_{CC}	Power Supply Current (Read)	f_{SCL} = 400 kHz			1	mA
I_{CC}	Power Supply Current (Write)	f_{SCL} = 400 kHz			3	mA
I_{SB}(5)	Standby Current (V_{CC} = 5.0 V)	V_{IN} = GND or V_{CC}			1	µA
I_{LI}	Input Leakage Current	V_{IN} = GND to V_{CC}			1	µA
I_{LO}	Output Leakage Current	V_{OUT} = GND to V_{CC}			1	µA
V_{IL}	Input Low Voltage		–1		V_{CC} x 0.3	V
V_{IH}	Input High Voltage		V_{CC} x 0.7		V_{CC} + 1.0	V
V_{OL}	Output Low Voltage (V_{CC} = 3.0 V)	I_{OL} = 3 mA			0.4	V

CAPACITANCE T_A = 25°C, f = 400 kHz, V_{CC} = 5 V

Symbol	Test	Conditions	Min	Typ	Max	Units
$C_{I/O}$(3)	Input/Output Capacitance (SDA)	$V_{I/O}$ = 0 V			8	pF
C_{IN}(3)	Input Capacitance (other pins)	V_{IN} = 0 V			6	pF

Note:

(1) The minimum DC input voltage is –0.5 V. During transitions, inputs may undershoot to –2.0 V for periods of less than 20 ns. Maximum DC voltage on output pins is V_{CC} + 0.5 V, which may overshoot to V_{CC} + 2.0 V for periods of less than 20 ns.

(2) Output shorted for no more than one second. No more than one output shorted at a time.

(3) These parameters are tested initially and after a design or process change that affects the parameter according to appropriate AEC-Q100 and JEDEC test methods.

(4) Latch-up protection is provided for stresses up to 100 mA on address and data pins from –1.0 V to V_{CC} + 1.0 V.

(5) Maximum standby current (I_{SB}) = 10µA for the Extended Automotive temperature range.

A.C. CHARACTERISTICS

V_{CC} = 2.5 V to 5.5 V, unless otherwise specified.

Read & Write Cycle Limits

Symbol	Parameter	2.5 V - 5.5 V		Units
		Min	Max	
F_{SCL}	Clock Frequency	0	400	kHz
T_I(1)	Noise Suppression Time Constant at SCL, SDA Inputs		100	ns
t_{AA}	SCL Low to SDA Data Out and ACK Out		900	ns
t_{BUF}(1)	Time the Bus Must be Free Before a New Transmission Can Start	1300		ns
$t_{HD:STA}$	Start Condition Hold Time	600		ns
t_{LOW}	Clock Low Period	1300		ns
t_{HIGH}	Clock High Period	600		ns
$t_{SU:STA}$	Start Condition Setup Time (for a Repeated Start Condition)	600		ns
$t_{HD:DAT}$	Data In Hold Time	0		ns
$t_{SU:DAT}$	Data In Setup Time	100		ns
t_R(1)	SDA and SCL Rise Time		300	ns
t_F(1)	SDA and SCL Fall Time		300	ns
$t_{SU:STO}$	Stop Condition Setup Time	600		ns
t_{DH}	Data Out Hold Time	100		ns

Power-Up Timing(1)(2)

Symbol	Parameter	Min	Typ	Max	Units
t_{PUR}	Power-up to Read Operation			1	ms
t_{PUW}	Power-up to Write Operation			1	ms

Write Cycle Limits

Symbol	Parameter	Min	Typ	Max	Units
t_{WR}	Write Cycle Time			5	ms

The write cycle time is the time from a valid stop condition of a write sequence to the end of the internal program/erase cycle. During the write cycle, the bus interface circuits are disabled, SDA is allowed to remain high, and the device does not respond to its slave address.

Note:
(1) This parameter is tested initially and after a design or process change that affects the parameter.
(2) t_{PUR} and t_{PUW} are the delays required from the time V_{CC} is stable until the specified operation can be initiated.

FUNCTIONAL DESCRIPTION

The CAT24FC02 supports the I^2C Bus data transmission protocol. This Inter-Integrated Circuit Bus protocol defines any device that sends data to the bus to be a transmitter and any device receiving data to be a receiver. Data transfer is controlled by the Master device which generates the serial clock and all START and STOP conditions for bus access. The CAT24FC02 operates as a Slave device. Both the Master and Slave devices can operate as either transmitter or receiver, but the Master device controls which mode is activated. A maximum of 8 devices may be connected to the bus as determined by the device address inputs A0, A1, and A2.

PIN DESCRIPTIONS

SCL: Serial Clock
The CAT24FC02 serial clock input pin is used to clock all data transfers into or out of the device. This is an input pin.

SDA: Serial Data/Address
The CAT24FC02 bidirectional serial data/address pin is used to transfer data into and out of the device. The SDA pin is an open drain output and can be wire-ORed with other open drain or open collector outputs.

A0, A1, A2: Device Address Inputs
These inputs set device address when cascading multiple devices. A maximum of eight devices can be cascaded when using the device.

WP: Write Protect

This input, when tied to GND, allows write operations to the entire memory. For CAT24FC02 when this pin is tied to V_{CC}, the entire array of memory is write protected. When left floating, memory is unprotected.

Figure 1. Bus Timing

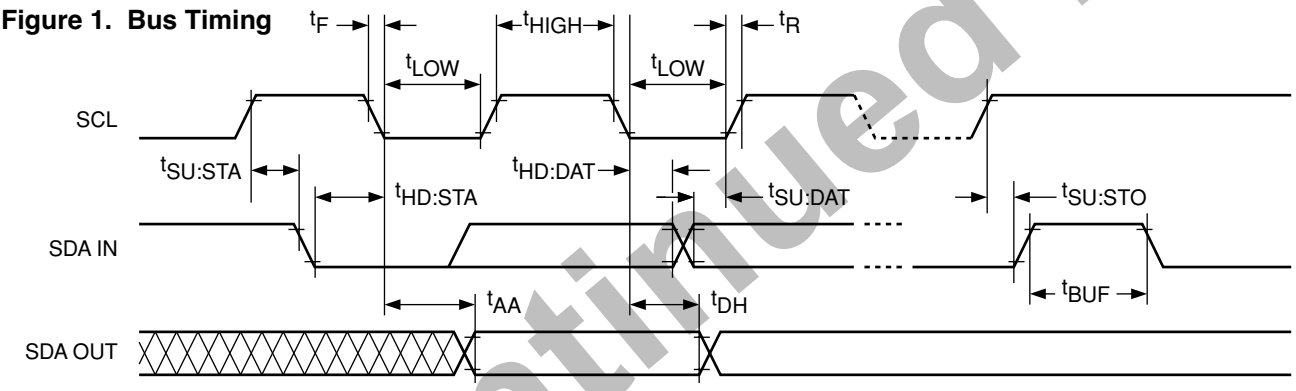


Figure 2. Write Cycle Timing

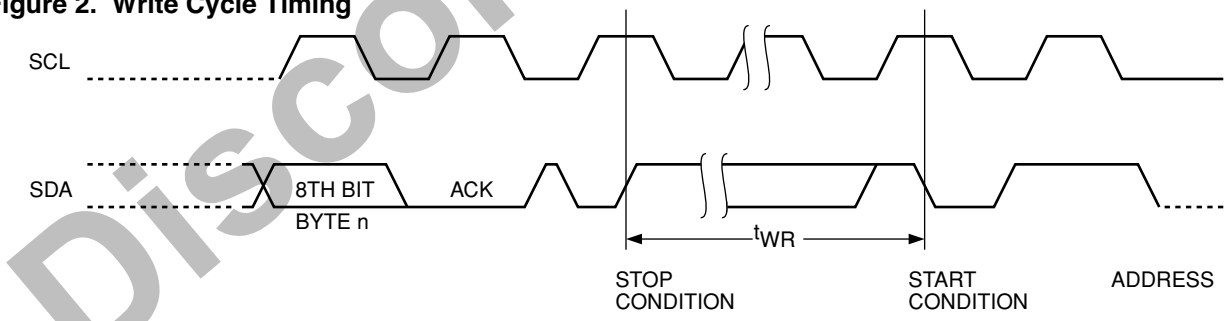
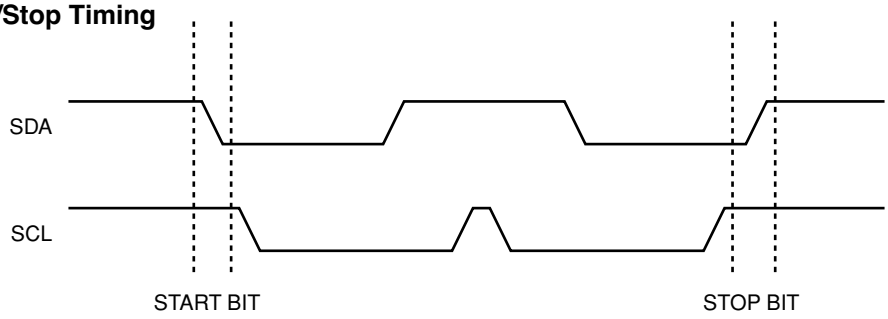


Figure 3. Start/Stop Timing



I²C BUS PROTOCOL

The following defines the features of the I²C bus protocol:

(1) Data transfer may be initiated only when the bus is not busy.

(2) During a data transfer, the data line must remain stable whenever the clock line is high. Any changes in the data line while the clock line is high will be interpreted as a START or STOP condition.

START Condition

The START Condition precedes all commands to the device, and is defined as a HIGH to LOW transition of SDA when SCL is HIGH. The CAT24FC02 monitors the SDA and SCL lines and will not respond until this condition is met.

STOP Condition

A LOW to HIGH transition of SDA when SCL is HIGH determines the STOP condition. All operations must end with a STOP condition.

DEVICE ADDRESSING

The Master begins a transmission by sending a START condition. The Master then sends the address of the particular slave device it is requesting. The four most significant bits of the 8-bit slave address are fixed as 1010 for the CAT24FC02 (see Fig. 5). The next three significant bits (A2, A1, A0) are the device address bits and define which device the Master is accessing. Up to eight CAT24FC02 may be individually addressed by the system. The last bit of the slave address specifies whether a Read or Write operation is to be performed. When this bit is set to 1, a Read operation is selected, and when set to 0, a Write operation is selected.

After the Master sends a START condition and the slave address byte, the CAT24FC02 monitors the bus and responds with an acknowledge (on the SDA line) when its address matches the transmitted slave address. The CAT24FC02 then performs a Read or a Write operation depending on the state of the R/$\overline{W}$ bit.

Acknowledge

After a successful data transfer, each receiving device is required to generate an acknowledge. The Acknowledging device pulls down the SDA line during the ninth clock cycle, signaling that it received the 8 bits of data.

The CAT24FC02 responds with an acknowledge after receiving a START condition and its slave address. If the device has been selected along with a write operation, it responds with an acknowledge after receiving each byte.

When the CAT24FC02 begins a READ mode, it transmits 8 bits of data, releases the SDA line, and monitors the line for an acknowledge. Once it receives this acknowledge, the CAT24FC02 will continue to transmit data. If no acknowledge is sent by the Master, the device terminates data transmission and waits for a STOP condition.

Figure 4. Acknowledge Timing

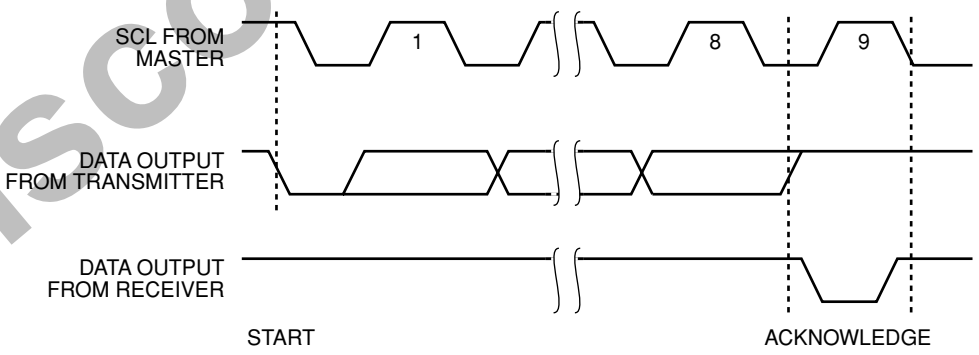
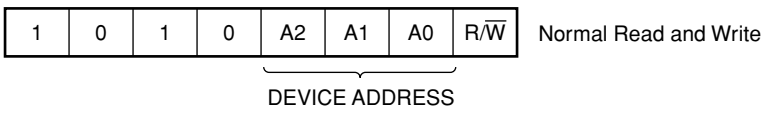


Figure 5. Slave Address Bits



WRITE OPERATIONS

Byte Write

In the Byte Write mode, the Master device sends the START condition and the slave address information (with the R/$\overline{W}$ bit set to zero) to the Slave device. After the Slave generates an acknowledge, the Master sends the byte address that is to be written into the address pointer of the CAT24FC02. After receiving another acknowledge from the Slave, the Master device transmits the data byte to be written into the addressed memory location. The CAT24FC02 acknowledges once more and the Master generates the STOP condition, at which time the device begins its internal programming to nonvolatile memory. While this internal cycle is in progress, the device will not respond to any request from the Master device.

Page Write

The CAT24FC02 writes up to 16 bytes of data in a single write cycle, using the Page Write operation. The Page Write operation is initiated in the same manner as the Byte Write operation, however instead of terminating after the initial word is transmitted, the Master is allowed to send up to 15 additional bytes. After each byte has been transmitted the CAT24FC02 will respond with an acknowledge, and internally increment the low order address bits by one. The high order bits remain unchanged.

If the Master transmits more than 16 bytes prior to sending the STOP condition, the address counter 'wraps around', and previously transmitted data will be overwritten.

Once all 16 bytes are received and the STOP condition has been sent by the Master, the internal programming cycle begins. At this point all received data is written to the CAT24FC02 in a single write cycle.

Acknowledge Polling

The disabling of the inputs can be used to take advantage of the typical write cycle time. Once the stop condition is issued to indicate the end of the host's write operation, the CAT24FC02 initiates the internal write cycle. ACK polling can be initiated immediately. This involves issuing the start condition followed by the slave address for a write operation. If the CAT24FC02 is still busy with the write operation, no ACK will be returned. If the CAT24FC02 has completed the write operation, an ACK will be returned and the host can then proceed with the next read or write operation.

WRITE PROTECTION

The CAT24FC02 is designed with a hardware protect pin that enables the user to protect the entire memory. Thehardware protection feature of the CAT24FC02 is designed into the part to provide added flexibility to the design engineers. The write protection feature of CAT24FC02 allows the user to protect against inadvertent programming of the memory array. If the WP pin is tied to Vcc, the entire memory array is protected and becomes read only. The entire memory becomes write protected regardless of whether the write protect register has been written or not. When WP pin is tied to Vcc, the user cannot program the write protect register. If the WP pin is left floating or tied to Vss, the device can be written into.

Figure 6. Byte Write Timing

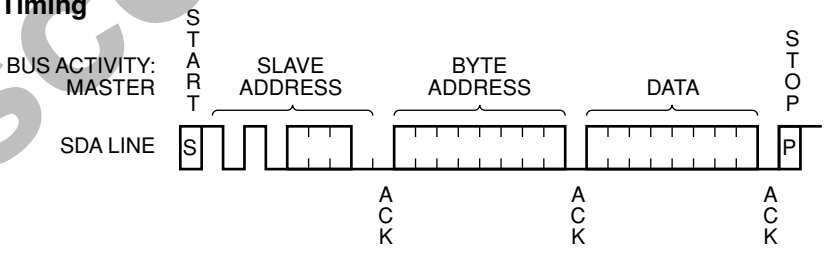
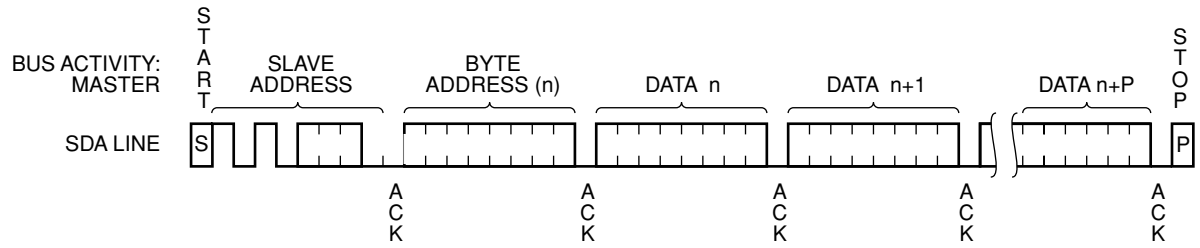


Figure 7. Page Write Timing



NOTE: IN THIS EXAMPLE n = XXXX 0000(B); X = 1 or 0

Read Operations

The READ operation for the CAT24FC02 is initiated in the same manner as the write operation with the one exception that the R/$\overline{W}$ bit is set to a one. Three different READ operations are possible: Immediate Address READ, Selective READ and Sequential READ.

Immediate Address Read

The CAT24FC02 address counter contains the address of the last byte accessed, incremented by one. In other words, if the last READ or WRITE access was to address N, the READ immediately following would access data from address N + 1. If N = 255, the counter will 'wrap around' to address 0 and continue to clock out data. After the CAT24FC02 receives its slave address information (with the R/$\overline{W}$ bit set to one), it issues an acknowledge, then transmits the 8-bit byte requested. The master device does not send an acknowledge but will generate a STOP condition.

Selective Read

Selective READ operations allow the Master device to select at random any memory location for a READ operation. The Master device first performs a 'dummy' write operation by sending the START condition, slave address and byte address of the location it wishes to read. After the CAT24FC02 acknowledge the word address, the Master device resends the START condition and the slave address, this time with the R/$\overline{W}$ bit set to one. The CAT24FC02 then responds with its acknowledge and sends the 8-bit byte requested. The master device does not send an acknowledge but will generate a STOP condition.

Sequential Read

The Sequential READ operation can be initiated by either the Immediate Address READ or Selective READ operations. After the CAT24FC02 sends the initial 8-bit data requested, the Master will respond with an acknowledge which tells the device it requires more data. The CAT24FC02 will continue to output a byte for each acknowledge sent by the Master. The operation will terminate operation when the Master fails to respond with an acknowledge, thus sending the STOP condition.

The data being transmitted from the CAT24FC02 is outputted sequentially with data from address N followed by data from address N + 1. The READ operation address counter increments all of the CAT24FC02 address bits so that the entire memory array can be read during one operation. If more than the 256 bytes are read out, the counter will "wrap around" and continue to clock out data bytes.

Figure 8. Immediate Address Read Timing

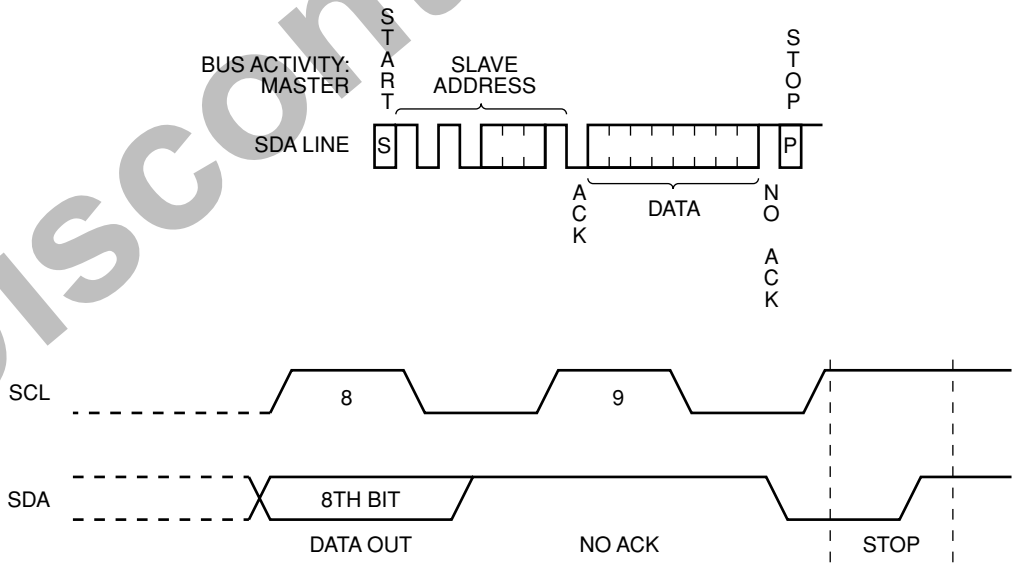


Figure 9. Selective Read Timing

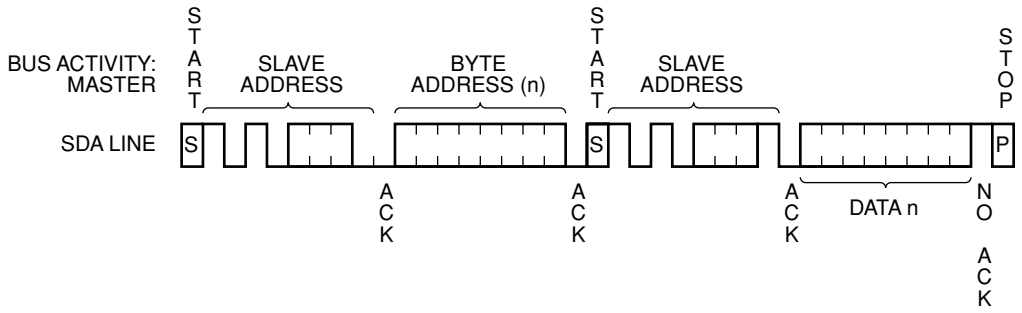
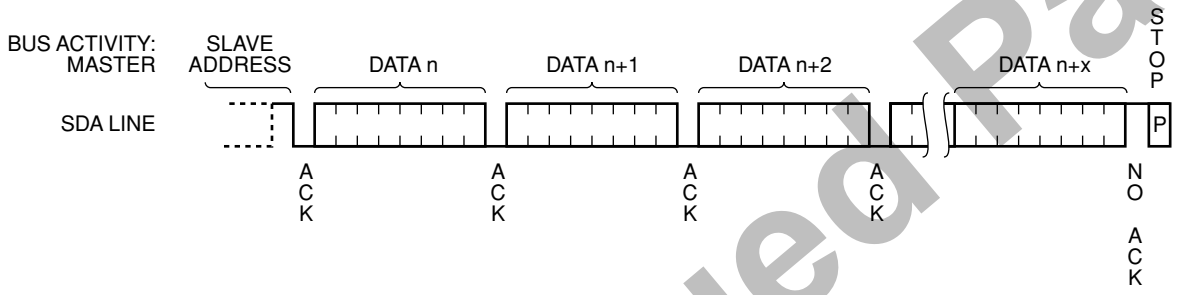
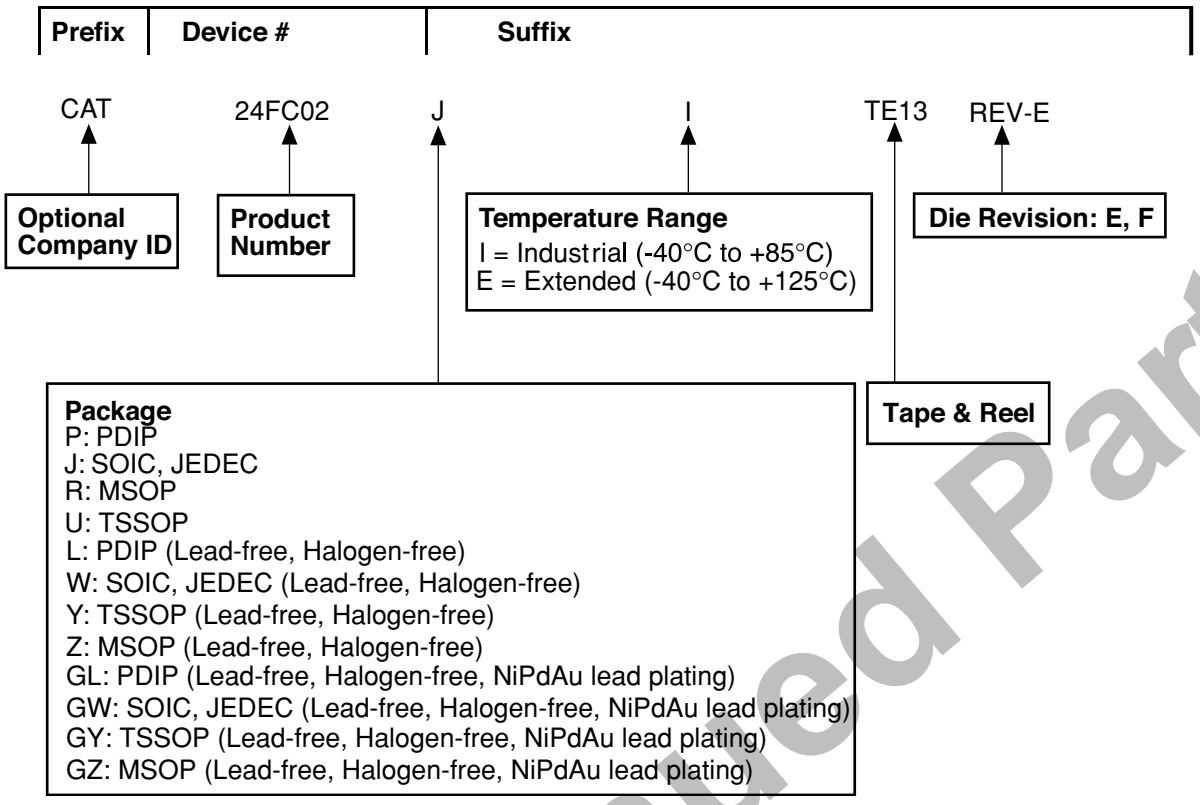


Figure 10. Sequential Read Timing



ORDERING INFORMATION



Notes:
(1) The device used in the above example is a CAT24FC02JI-TE13 REV-E (SOIC, Industrial Temperature, 2.5 Volt to 5.5 Volt Operating Voltage, Tape & Reel)

REVISION HISTORY

Date	Revision	Comments
03/01/04	A	Initial Issue
05/15/04	B	D.C. Operating Characteristics Write Cycle Limits Update Ordering Information Update Revision History Update Rev Number
06/07/04	C	Update Write Cycle Limits
7/27/2004	D	Updated notes on page 2
1/27/2005	E	Added Die Revision E in Ordering Information
03/23/2005	F	Updated Features Updated Description Updated Pin Function Updated Reliability Characteristics Updated Operating Characteristics Updated A.C. Characteristics Updated Ordering Information
08/02/2005	G	Update Pin Configuration Update Ordering Information

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