# SN54HC112, SN74HC112
# DUAL J-K NEGATIVE-EDGE-TRIGGERED FLIP-FLOPS WITH CLEAR AND PRESET

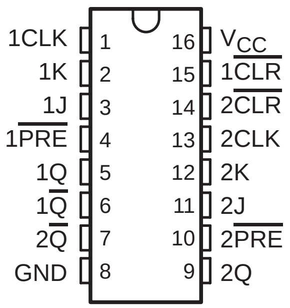
SCLS099F − DECEMBER 1982 − REVISED SEPTEMBER 2003

- **Wide Operating Voltage Range of 2 V to 6 V**
- **Outputs Can Drive Up To 10 LSTTL Loads**
- **Low Power Consumption, 40-µA Max $I_{CC}$**
- **Typical $t_{pd}$ = 13 ns**
- **±4-mA Output Drive at 5 V**
- **Low Input Current of 1 µA Max**

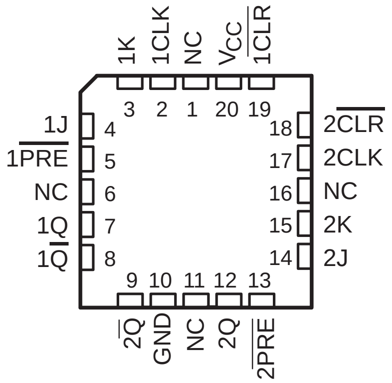
## description/ordering information

The ’HC112 devices contain two independent J-K negative-edge-triggered flip-flops. A low level at the preset ($\overline{\text{PRE}}$) or clear ($\overline{\text{CLR}}$) inputs sets or resets the outputs, regardless of the levels of the other inputs. When $\overline{\text{PRE}}$ and $\overline{\text{CLR}}$ are inactive (high), data at the J and K inputs meeting the setup time requirements are transferred to the outputs on the negative-going edge of the clock (CLK) pulse. Clock triggering occurs at a voltage level and is not directly related to the fall time of the CLK pulse. Following the hold-time interval, data at the J and K inputs may be changed without affecting the levels at the outputs. These versatile flip-flops perform as toggle flip-flops by tying J and K high.

**SN54HC112 . . . J OR W PACKAGE**
**SN74HC112 . . . D OR N PACKAGE**
**(TOP VIEW)**



**SN54HC112 . . . FK PACKAGE**
**(TOP VIEW)**



NC − No internal connection

**ORDERING INFORMATION**

| $T_A$ | PACKAGE† | | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|---|---|---|---|---|
| −40°C to 85°C | PDIP − N | Tube of 25 | SN74HC112N | SN74HC112N |
| | SOIC − D | Tube of 40 | SN74HC112D | HC112 |
| | | Reel of 2500 | SN74HC112DR | |
| | | Reel of 250 | SN74HC112DT | |
| −55°C to 125°C | CDIP − J | Tube of 25 | SNJ54HC112J | SNJ54HC112J |
| | CFP − W | Tube of 150 | SNJ54HC112W | SNJ54HC112W |
| | LCCC − FK | Tube of 55 | SNJ54HC112FK | SNJ54HC112FK |

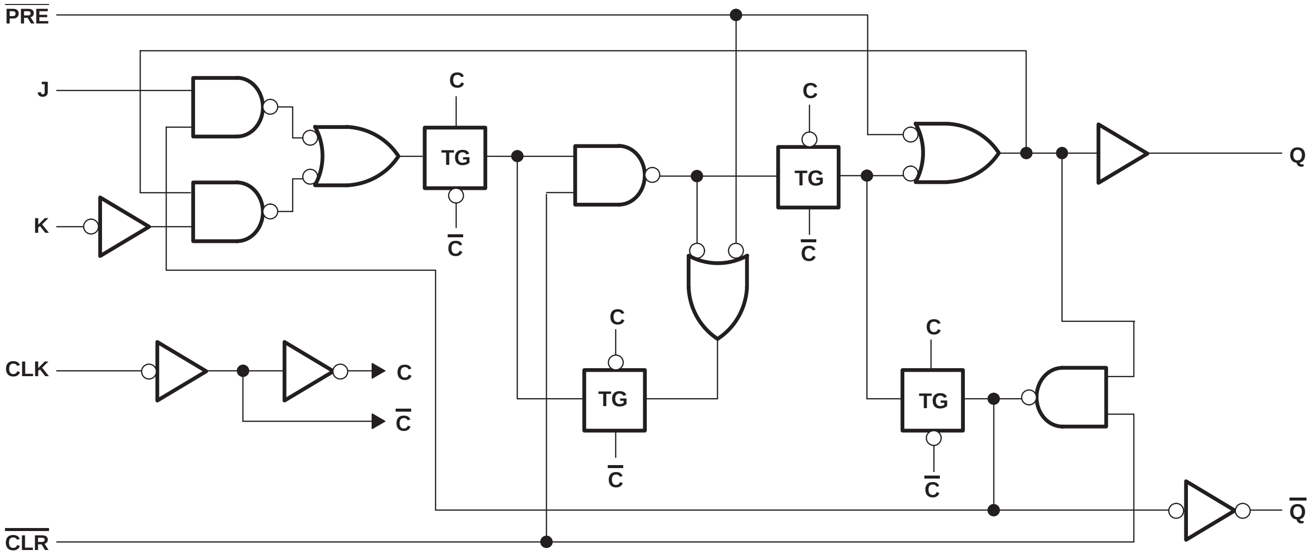
† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

**FUNCTION TABLE**

| INPUTS | | | | | OUTPUTS | |
|---|---|---|---|---|---|---|
| $\overline{PRE}$ | $\overline{CLR}$ | CLK | J | K | Q | $\overline{Q}$ |
| L | H | X | X | X | H | L |
| H | L | X | X | X | L | H |
| L | L | X | X | X | H† | H† |
| H | H | ↓ | L | L | $Q_0$ | $\overline{Q}_0$ |
| H | H | ↓ | H | L | H | L |
| H | H | ↓ | L | H | L | H |
| H | H | ↓ | H | H | Toggle | |
| H | H | H | X | X | $Q_0$ | $\overline{Q}_0$ |

† This configuration is nonstable; that is, it does not persist when either $\overline{PRE}$ or $\overline{CLR}$ returns to its inactive (high) level.

### logic diagram, each flip-flop (positive logic)



## absolute maximum ratings over operating free-air temperature range[†]

| | | |
|---|---|---|
| Supply voltage range, $V_{CC}$ | | −0.5 V to 7 V |
| Input clamp current, $I_{IK}$ ($V_I < 0$ or $V_I > V_{CC}$) (see Note 1) | | ±20 mA |
| Output clamp current, $I_{OK}$ ($V_O < 0$ or $V_O > V_{CC}$) (see Note 1) | | ±20 mA |
| Continuous output current, $I_O$ ($V_O = 0$ to $V_{CC}$) | | ±25 mA |
| Continuous current through $V_{CC}$ or GND | | ±50 mA |
| Package thermal impedance, $\theta_{JA}$ (see Note 2): | D package | 73°C/W |
| | N package | 67°C/W |
| Storage temperature range, $T_{stg}$ | | −65°C to 150°C |

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

## recommended operating conditions (see Note 3)

| | | | SN54HC112 | | | SN74HC112 | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | **MIN** | **NOM** | **MAX** | **MIN** | **NOM** | **MAX** | |
| $V_{CC}$ | Supply voltage | | 2 | 5 | 6 | 2 | 5 | 6 | V |
| $V_{IH}$ | High-level input voltage | $V_{CC} = 2$ V | 1.5 | | | 1.5 | | | V |
| | | $V_{CC} = 4.5$ V | 3.15 | | | 3.15 | | | |
| | | $V_{CC} = 6$ V | 4.2 | | | 4.2 | | | |
| $V_{IL}$ | Low-level input voltage | $V_{CC} = 2$ V | | | 0.5 | | | 0.5 | V |
| | | $V_{CC} = 4.5$ V | | | 1.35 | | | 1.35 | |
| | | $V_{CC} = 6$ V | | | 1.8 | | | 1.8 | |
| $V_I$ | Input voltage | | 0 | | $V_{CC}$ | 0 | | $V_{CC}$ | V |
| $V_O$ | Output voltage | | 0 | | $V_{CC}$ | 0 | | $V_{CC}$ | V |
| $t_t$[‡] | Input transition (rise and fall) time | $V_{CC} = 2$ V | | | 1000 | | | 1000 | ns |
| | | $V_{CC} = 4.5$ V | | | 500 | | | 500 | |
| | | $V_{CC} = 6$ V | | | 400 | | | 400 | |
| $T_A$ | Operating free-air temperature | | −55 | | 125 | −40 | | 85 | °C |

[‡] If this device is used in the threshold region (from $V_{IL}$max = 0.5 V to $V_{IH}$min = 1.5 V), there is a potential to go into the wrong state from induced grounding, causing double clocking. Operating with the inputs at $t_t = 1000$ ns and $V_{CC} = 2$ V does not damage the device; however, functionally, the CLK inputs are not ensured while in the shift, count, or toggle operating modes.

NOTE 3: All unused inputs of the device must be held at $V_{CC}$ or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | | $V_{CC}$ | $T_A$ = 25°C | | | SN54HC112 | | SN74HC112 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $V_{OH}$ | $V_I = V_{IH}$ or $V_{IL}$ | $I_{OH}$ = −20 µA | 2 V | 1.9 | 1.998 | | 1.9 | | 1.9 | | V |
| | | | 4.5 V | 4.4 | 4.499 | | 4.4 | | 4.4 | | |
| | | | 6 V | 5.9 | 5.999 | | 5.9 | | 5.9 | | |
| | | $I_{OH}$ = −4 mA | 4.5 V | 3.98 | 4.3 | | 3.7 | | 3.84 | | |
| | | $I_{OH}$ = −5.2 mA | 6 V | 5.48 | 5.8 | | 5.2 | | 5.34 | | |
| $V_{OL}$ | $V_I = V_{IH}$ or $V_{IL}$ | $I_{OL}$ = 20 µA | 2 V | | 0.002 | 0.1 | | 0.1 | | 0.1 | V |
| | | | 4.5 V | | 0.001 | 0.1 | | 0.1 | | 0.1 | |
| | | | 6 V | | 0.001 | 0.1 | | 0.1 | | 0.1 | |
| | | $I_{OL}$ = 4 mA | 4.5 V | | 0.17 | 0.26 | | 0.4 | | 0.33 | |
| | | $I_{OL}$ = 5.2 mA | 6 V | | 0.15 | 0.26 | | 0.4 | | 0.33 | |
| $I_I$ | $V_I = V_{CC}$ or 0 | | 6 V | | ±0.1 | ±100 | | ±1000 | | ±1000 | nA |
| $I_{CC}$ | $V_I = V_{CC}$ or 0, | $I_O$ = 0 | 6 V | | | 4 | | 80 | | 40 | µA |
| $C_i$ | | | 2 V to 6 V | | 3 | 10 | | 10 | | 10 | pF |

## timing requirements over recommended operating free-air temperature range (unless otherwise noted)

| | | | $V_{CC}$ | $T_A$ = 25°C | | SN54HC112 | | SN74HC112 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | MAX | MIN | MAX | MIN | MAX | |
| $f_{clock}$ | Clock frequency | | 2 V | | 5 | | 3.4 | | 4 | MHz |
| | | | 4.5 V | | 25 | | 17 | | 20 | |
| | | | 6 V | | 29 | | 20 | | 24 | |
| $t_w$ | Pulse duration | $\overline{PRE}$ or $\overline{CLR}$ low | 2 V | 100 | | 150 | | 125 | | ns |
| | | | 4.5 V | 20 | | 30 | | 25 | | |
| | | | 6 V | 17 | | 25 | | 21 | | |
| | | CLK high or low | 2 V | 100 | | 150 | | 125 | | |
| | | | 4.5 V | 20 | | 30 | | 25 | | |
| | | | 6 V | 17 | | 25 | | 21 | | |
| $t_{su}$ | Setup time before CLK↓ | Data (J, K) | 2 V | 100 | | 150 | | 125 | | ns |
| | | | 4.5 V | 20 | | 30 | | 25 | | |
| | | | 6 V | 17 | | 25 | | 21 | | |
| | | $\overline{PRE}$ or $\overline{CLR}$ inactive | 2 V | 100 | | 150 | | 125 | | |
| | | | 4.5 V | 20 | | 30 | | 25 | | |
| | | | 6 V | 17 | | 25 | | 21 | | |
| $t_h$ | Hold time, data after CLK↓ | | 2 V | 0 | | 0 | | 0 | | ns |
| | | | 4.5 V | 0 | | 0 | | 0 | | |
| | | | 6 V | 0 | | 0 | | 0 | | |

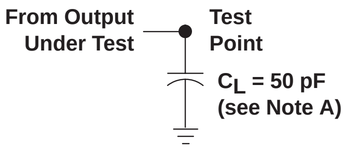
## switching characteristics over recommended operating free-air temperature range, $C_L$ = 50 pF (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC}$ | $T_A$ = 25°C |  |  | SN54HC112 |  | SN74HC112 |  | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
|  |  |  |  | MIN | TYP | MAX | MIN | MAX | MIN | MAX |  |
| $f_{max}$ |  |  | 2 V | 5 | 10 |  | 3.4 |  | 4 |  | MHz |
|  |  |  | 4.5 V | 25 | 50 |  | 17 |  | 20 |  |  |
|  |  |  | 6 V | 29 | 60 |  | 20 |  | 24 |  |  |
| $t_{pd}$ | $\overline{PRE}$ or $\overline{CLR}$ | Q or $\overline{Q}$ | 2 V |  | 54 | 165 |  | 245 |  | 205 | ns |
|  |  |  | 4.5 V |  | 16 | 33 |  | 49 |  | 41 |  |
|  |  |  | 6 V |  | 13 | 28 |  | 42 |  | 35 |  |
|  | CLK | Q or $\overline{Q}$ | 2 V |  | 56 | 125 |  | 185 |  | 155 |  |
|  |  |  | 4.5 V |  | 16 | 25 |  | 37 |  | 31 |  |
|  |  |  | 6 V |  | 13 | 21 |  | 31 |  | 26 |  |
| $t_t$ |  | Q or $\overline{Q}$ | 2 V |  | 29 | 75 |  | 110 |  | 95 | ns |
|  |  |  | 4.5 V |  | 9 | 15 |  | 22 |  | 19 |  |
|  |  |  | 6 V |  | 8 | 13 |  | 19 |  | 16 |  |

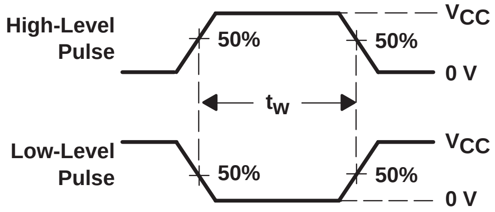
## operating characteristics, $T_A$ = 25°C

| PARAMETER |  | TEST CONDITIONS | TYP | UNIT |
|---|---|---|---|---|
| $C_{pd}$ | Power dissipation capacitance | No load | 35 | pF |

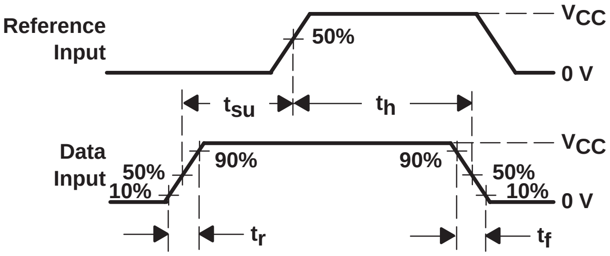
## PARAMETER MEASUREMENT INFORMATION



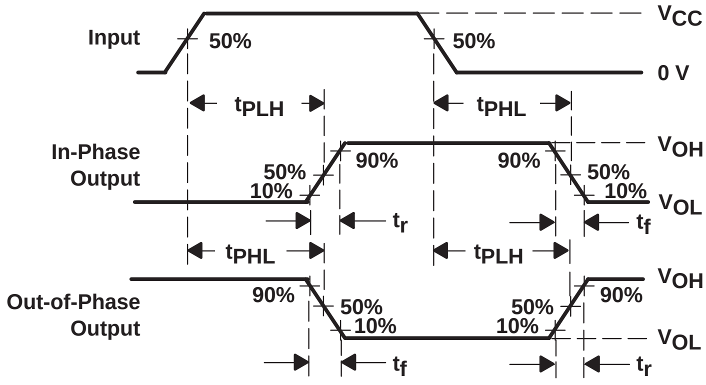
**LOAD CIRCUIT**



**VOLTAGE WAVEFORMS**
**PULSE DURATIONS**



**VOLTAGE WAVEFORMS**
**SETUP AND HOLD AND INPUT RISE AND FALL TIMES**



**VOLTAGE WAVEFORMS**
**PROPAGATION DELAY AND OUTPUT TRANSITION TIMES**

NOTES:
- A. $C_L$ includes probe and test-fixture capacitance.
- B. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, $Z_O$ = 50 Ω, $t_r$ = 6 ns, $t_f$ = 6 ns.
- C. For clock inputs, $f_{max}$ is measured when the input duty cycle is 50%.
- D. The outputs are measured one at a time with one input transition per measurement.
- E. $t_{PLH}$ and $t_{PHL}$ are the same as $t_{pd}$.

**Figure 1. Load Circuit and Voltage Waveforms**

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 84088012A | ACTIVE | LCCC | FK | 20 | 1 | TBD | POST-PLATE | N / A for Pkg Type | -55 to 125 | 84088012A<br>SNJ54HC<br>112FK | Samples |
| 8408801EA | ACTIVE | CDIP | J | 16 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | 8408801EA<br>SNJ54HC112J | Samples |
| 8408801FA | ACTIVE | CFP | W | 16 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | 8408801FA<br>SNJ54HC112W | Samples |
| JM38510/65305BEA | ACTIVE | CDIP | J | 16 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | JM38510/<br>65305BEA | Samples |
| M38510/65305BEA | ACTIVE | CDIP | J | 16 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | JM38510/<br>65305BEA | Samples |
| SN54HC112J | ACTIVE | CDIP | J | 16 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | SN54HC112J | Samples |
| SN74HC112D | ACTIVE | SOIC | D | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | HC112 | Samples |
| SN74HC112DE4 | ACTIVE | SOIC | D | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | HC112 | Samples |
| SN74HC112DG4 | ACTIVE | SOIC | D | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | HC112 | Samples |
| SN74HC112DR | ACTIVE | SOIC | D | 16 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | HC112 | Samples |
| SN74HC112DRE4 | ACTIVE | SOIC | D | 16 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | HC112 | Samples |
| SN74HC112DRG4 | ACTIVE | SOIC | D | 16 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | HC112 | Samples |
| SN74HC112DT | ACTIVE | SOIC | D | 16 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | HC112 | Samples |
| SN74HC112DTE4 | ACTIVE | SOIC | D | 16 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | HC112 | Samples |
| SN74HC112DTG4 | ACTIVE | SOIC | D | 16 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | HC112 | Samples |
| SN74HC112N | ACTIVE | PDIP | N | 16 | 25 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | -40 to 85 | SN74HC112N | Samples |
| SN74HC112N3 | OBSOLETE | PDIP | N | 16 |  | TBD | Call TI | Call TI | -40 to 85 |  |  |

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| SN74HC112NE4 | ACTIVE | PDIP | N | 16 | 25 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | -40 to 85 | SN74HC112N | Samples |
| SNJ54HC112FK | ACTIVE | LCCC | FK | 20 | 1 | TBD | POST-PLATE | N / A for Pkg Type | -55 to 125 | 84088012A<br>SNJ54HC<br>112FK | Samples |
| SNJ54HC112J | ACTIVE | CDIP | J | 16 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | 8408801EA<br>SNJ54HC112J | Samples |
| SNJ54HC112W | ACTIVE | CFP | W | 16 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | 8408801FA<br>SNJ54HC112W | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

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**OTHER QUALIFIED VERSIONS OF SN54HC112, SN74HC112 :**

- Catalog: SN74HC112

- Military: SN54HC112

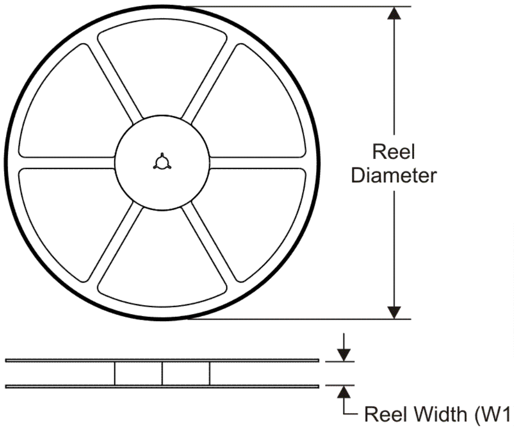
NOTE: Qualified Version Definitions:

  - Catalog - TI's standard catalog product

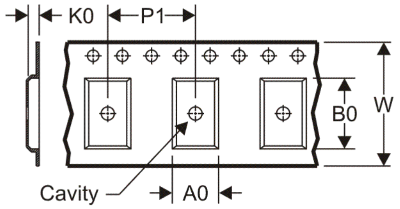
  - Military - QML certified for Military and Defense Applications

## TAPE AND REEL INFORMATION

### REEL DIMENSIONS

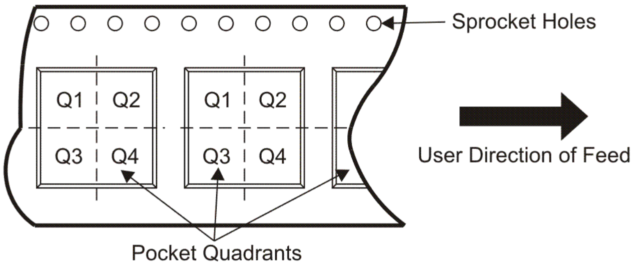


### TAPE DIMENSIONS



| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

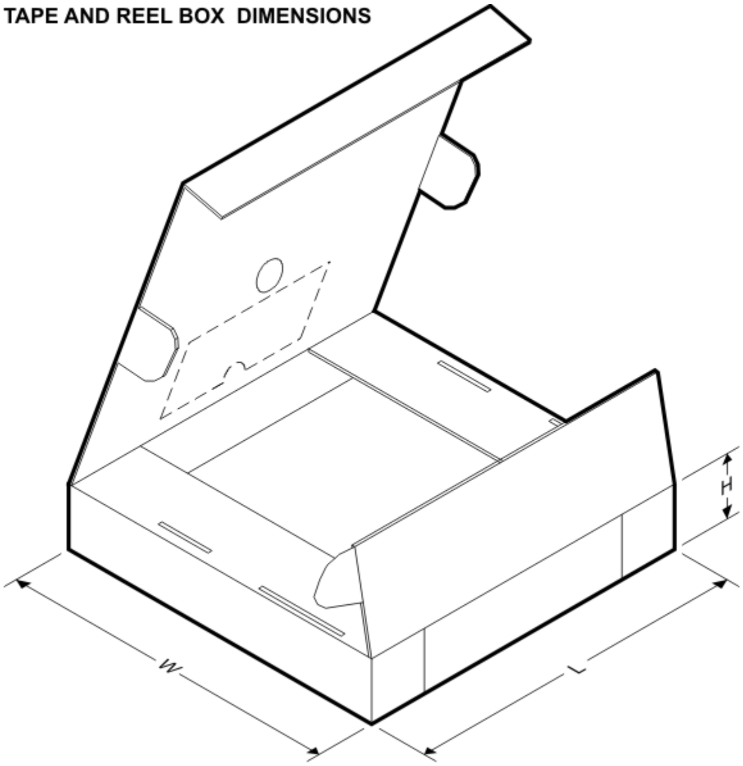
### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| SN74HC112DR | SOIC | D | 16 | 2500 | 330.0 | 16.4 | 6.5 | 10.3 | 2.1 | 8.0 | 16.0 | Q1 |

## TAPE AND REEL BOX DIMENSIONS



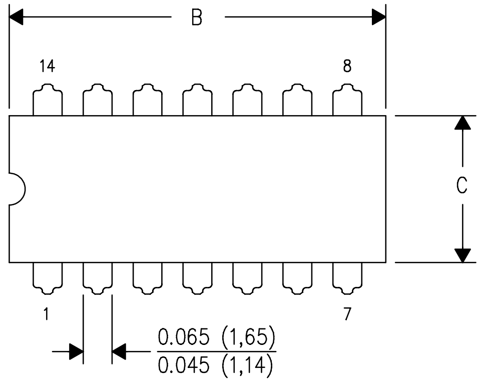
*All dimensions are nominal

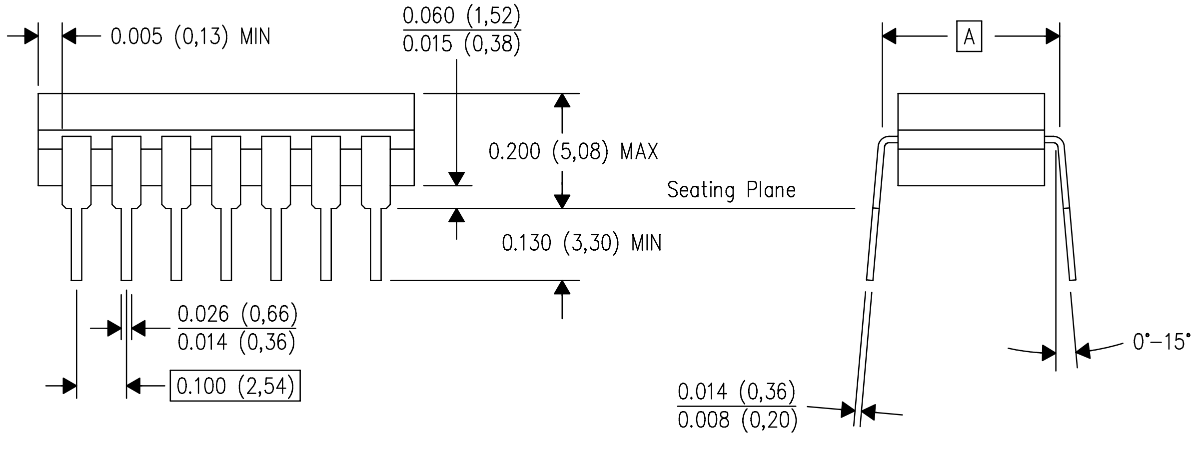
| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| SN74HC112DR | SOIC | D | 16 | 2500 | 333.2 | 345.9 | 28.6 |

## J (R-GDIP-T**) CERAMIC DUAL IN-LINE PACKAGE

14 LEADS SHOWN

| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---|---|---|---|---|
| A | 0.300<br>(7,62)<br>BSC | 0.300<br>(7,62)<br>BSC | 0.300<br>(7,62)<br>BSC | 0.300<br>(7,62)<br>BSC |
| B MAX | 0.785<br>(19,94) | .840<br>(21,34) | 0.960<br>(24,38) | 1.060<br>(26,92) |
| B MIN | —— | —— | —— | —— |
| C MAX | 0.300<br>(7,62) | 0.300<br>(7,62) | 0.310<br>(7,87) | 0.300<br>(7,62) |
| C MIN | 0.245<br>(6,22) | 0.245<br>(6,22) | 0.220<br>(5,59) | 0.245<br>(6,22) |

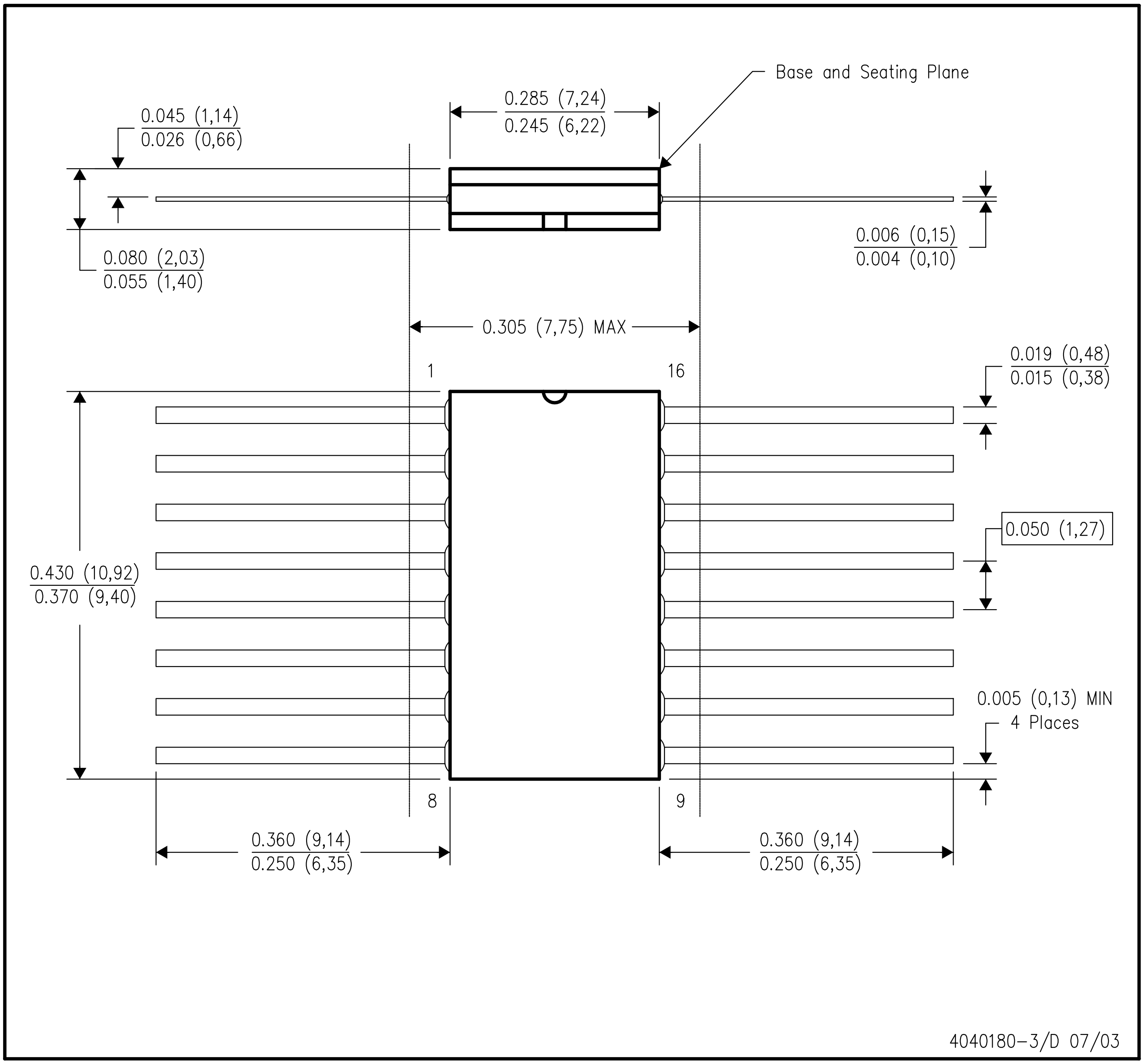




4040083/F 03/03

NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package is hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
- E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

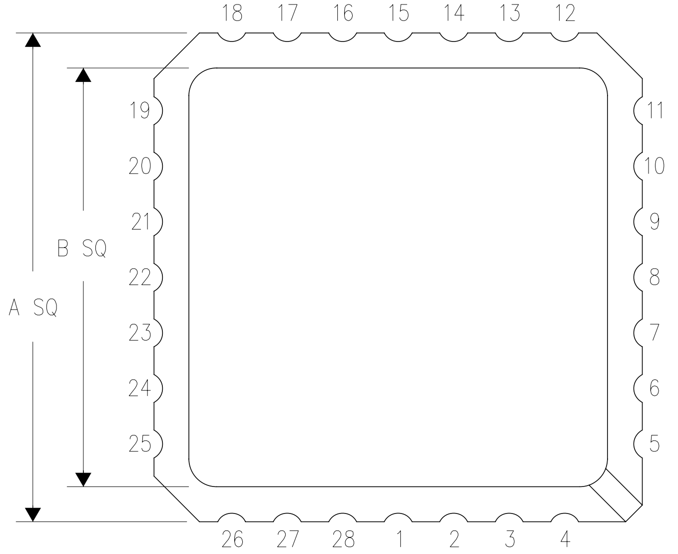
## W (R–GDFP–F16) CERAMIC DUAL FLATPACK



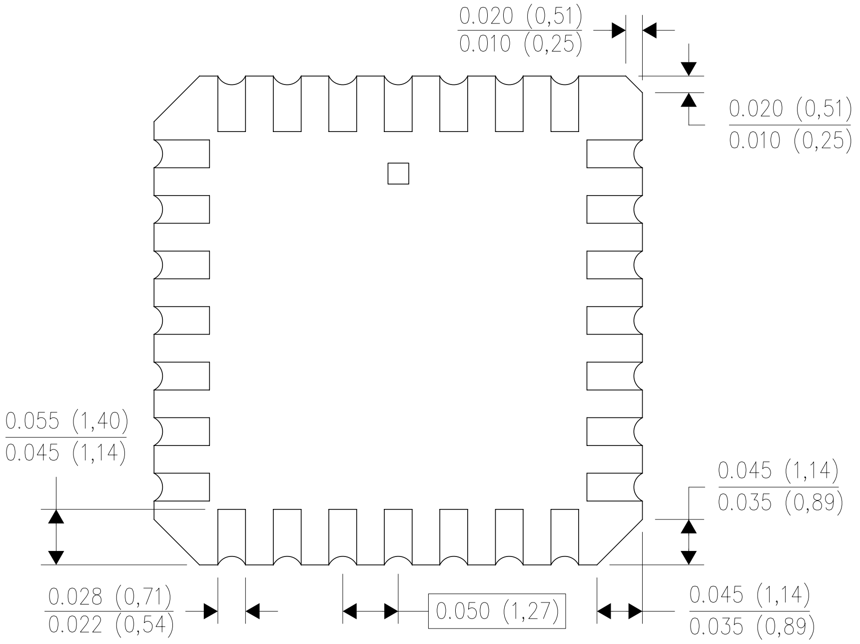
NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only.
- E. Falls within MIL STD 1835 GDFP1–F16 and JEDEC MO–092AC

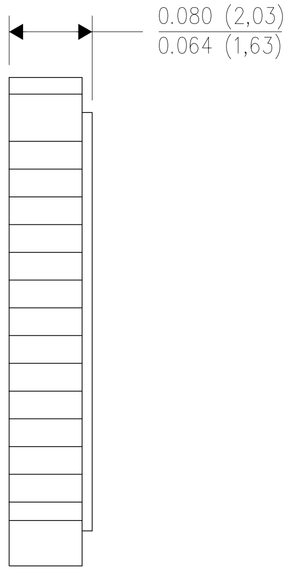
## FK (S-CQCC-N**) LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



| NO. OF TERMINALS ** | A | | B | |
|---|---|---|---|---|
| | MIN | MAX | MIN | MAX |
| 20 | 0.342 (8,69) | 0.358 (9,09) | 0.307 (7,80) | 0.358 (9,09) |
| 28 | 0.442 (11,23) | 0.458 (11,63) | 0.406 (10,31) | 0.458 (11,63) |
| 44 | 0.640 (16,26) | 0.660 (16,76) | 0.495 (12,58) | 0.560 (14,22) |
| 52 | 0.740 (18,78) | 0.761 (19,32) | 0.495 (12,58) | 0.560 (14,22) |
| 68 | 0.938 (23,83) | 0.962 (24,43) | 0.850 (21,6) | 0.858 (21,8) |
| 84 | 1.141 (28,99) | 1.165 (29,59) | 1.047 (26,6) | 1.063 (27,0) |



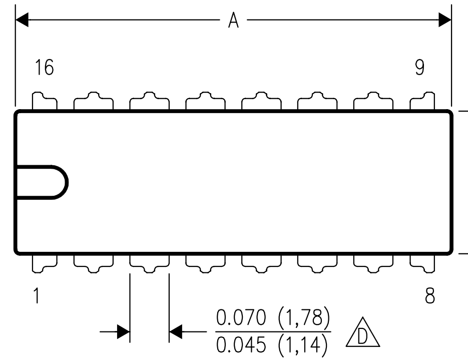


4040140/D 01/11

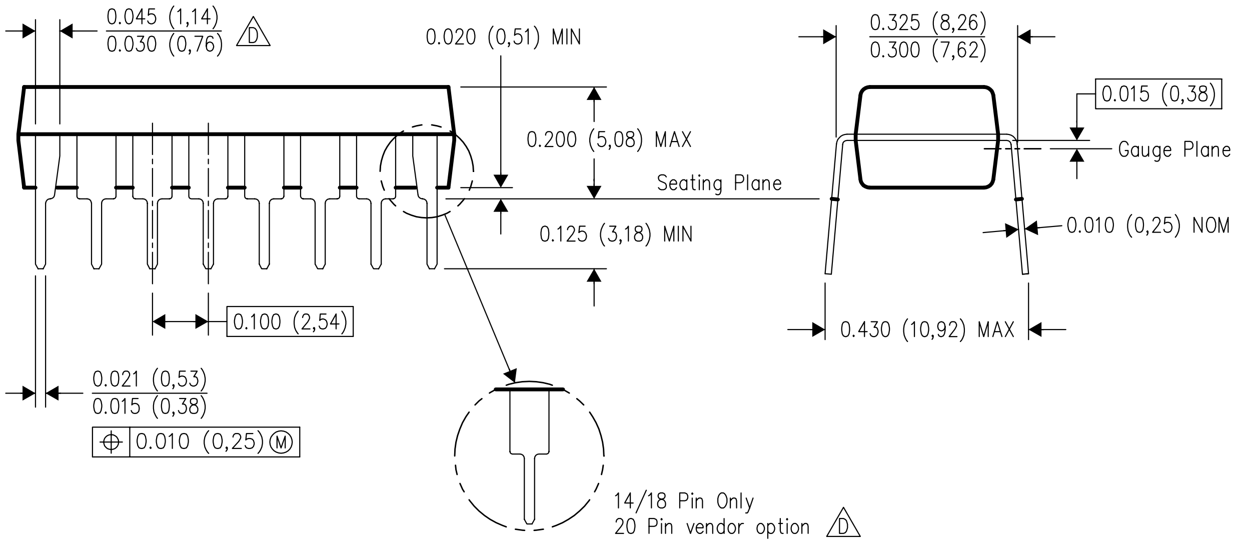
NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a metal lid.
- D. Falls within JEDEC MS-004

## N (R-PDIP-T**) PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



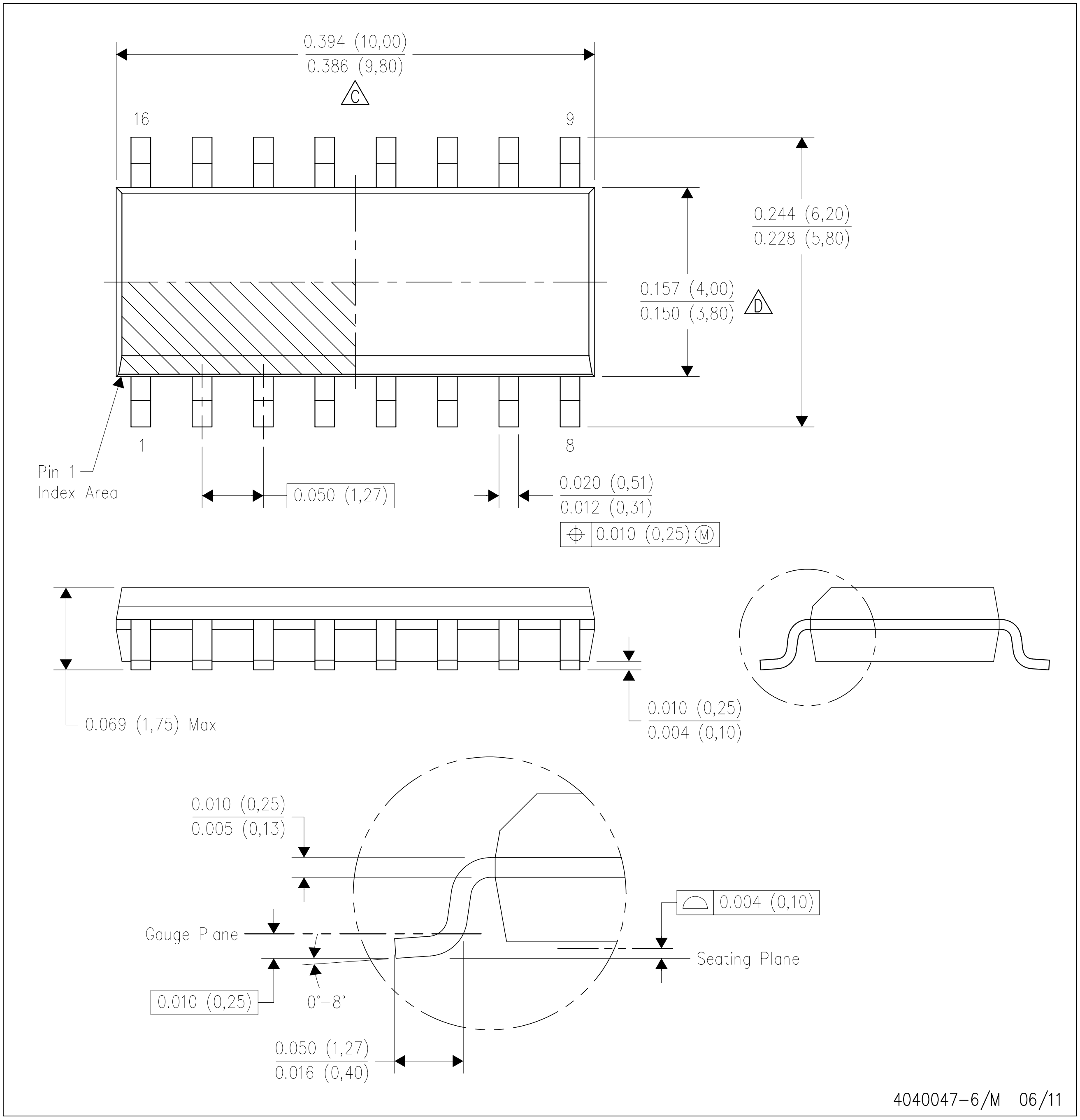
| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---|---|---|---|---|
| A MAX | 0.775<br>(19,69) | 0.775<br>(19,69) | 0.920<br>(23,37) | 1.060<br>(26,92) |
| A MIN | 0.745<br>(18,92) | 0.745<br>(18,92) | 0.850<br>(21,59) | 0.940<br>(23,88) |
| △C MS-001 VARIATION | AA | BB | AC | AD |



4040049/E 12/2002

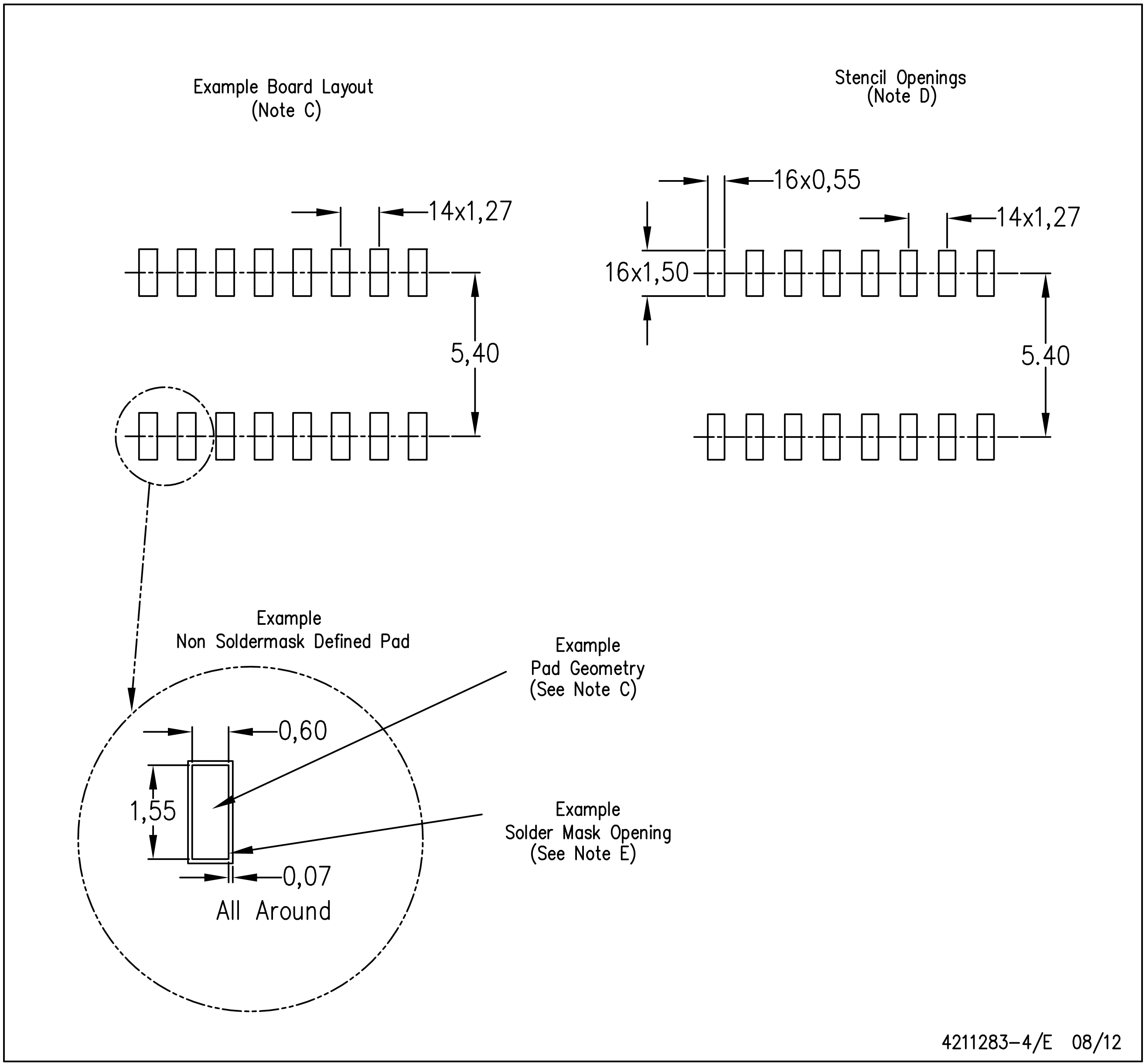
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
△C Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
△D The 20 pin end lead shoulder width is a vendor option, either half or full width.

## D (R-PDSO-G16) PLASTIC SMALL OUTLINE



NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AC.

D (R-PDSO-G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC-7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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