4-Channel Buck-Boost White LED Driver for up to 32 LEDs

BD81A34MUV-M

Under development

●General Description

BD81A34MUV-M is a white LED driver with the capability of withstanding high input voltage (40V Max).
This driver has 4ch constant-current drivers integrated in 1-chip, which each channel can draw up to 120mA Max, so that high brightness LED driving can be realized.
Furthermore, a current-mode buck-boost DC/DC controller is also integrated to achieve stable operation against unstable car-battery voltage input and also to remove the constraint of the number of LEDs in series connection.
The brightness can be controlled by PWM techniques.

●Features

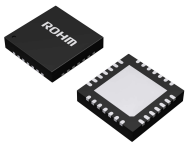
- Integrated buck-boost current-mode DC/DC controller
- Four integrated LED current driver channels (120 mA Max. each channel)
- PWM Light Modulation
- DCDC external synchronization
- Built-in protection functions (UVLO, OVP, TSD, OCP, SCP)
- Abnormal status detection function (OPEN/ SHORT)
- Integrated VOUT discharge function

●Key Specifications

Power supply voltage	4.5 to 35 [V]
LED output current accuracy	±3.0 % @50mA
Oscillation frequency	200 to 2200 kHz
Operating temperature range	-40 to 125 ℃
PWM Minimum pulse width	1usec
LED Maximum output current	120mA/ch

●Packages

	W × L × H
VQFN28SV5050	5.0 ㎜×5.0 ㎜×1.0 ㎜



VQFN28SV5050

●Applications

For display audio, Small and medium-sized Type LCD panel

●Typical Application Circuits

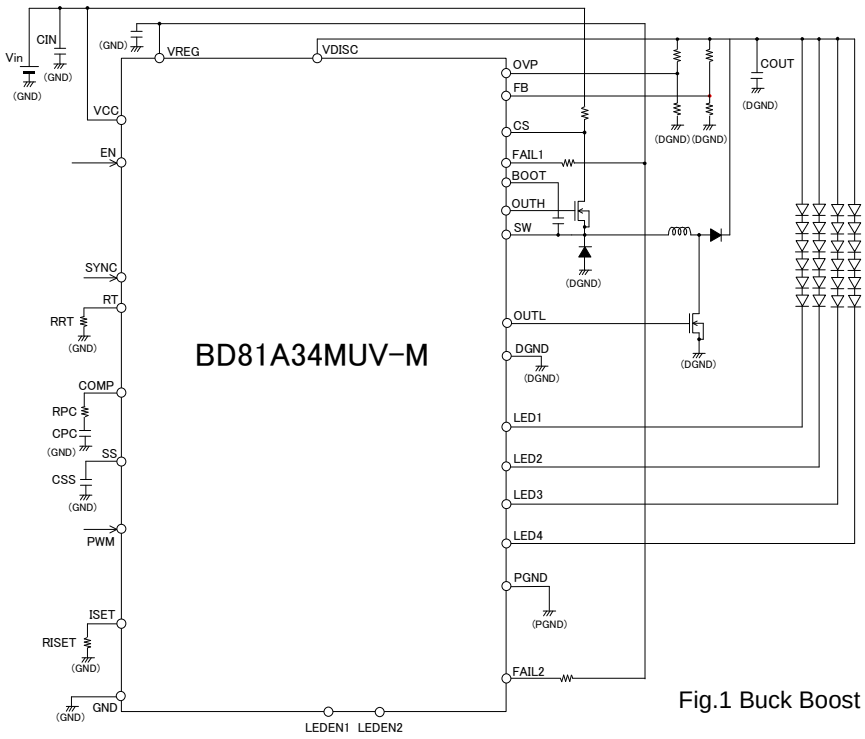


Fig.1 Buck Boost application circuit

○Product structure：Silicon monolithic integrated circuit
○This product is not designed protection against radioactive rays.

●Pin Configuration

VQFN28SV5050 (Top view)

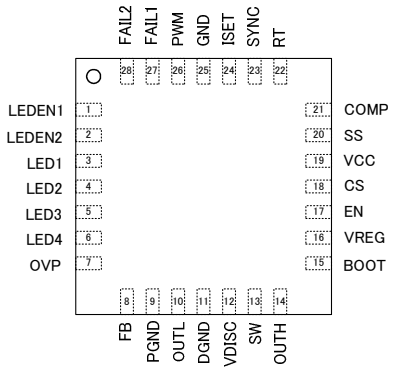


Fig.2 Pin configuration

●Pin Description

VQFN28 SV5050	Symbol	Function
1	LEDEN1	LED output enable input 1
2	LEDEN2	LED output enable input 2
3	LED1	LED output 1
4	LED2	LED output 2
5	LED3	LED output 3
6	LED4	LED output 4
7	OVP	Over voltage detection input
8	FB	FB voltage detection input
9	PGND	LED output GND
10	OUTL	Low-side MOSFET Gate output
11	DGND	DCDC output GND
12	VDISC	VOUT discharge signal
13	SW	High-side external MOSFET Source pin
14	OUTH	High-side external MOSFET Gate output
15	BOOT	High-side external MOSFET power supply pin
16	VREG	Internal reference voltage output
17	EN	Enable input
18	CS	DC/DC current sence pin
19	Vcc	Input power supply
20	SS	Soft start time-setting capacitance input
21	COMP	Error amplifier output
22	RT	Oscillation frequency-setting resistance input
23	SYNC	External synchronization signal input
24	ISET	LED output current-setting resistance input
25	GND	Small-signal GND
26	PWM	PWM light modulation input
27	FAIL1	Failure signal output
28	FAIL2	Failure signal output

●Block Diagram

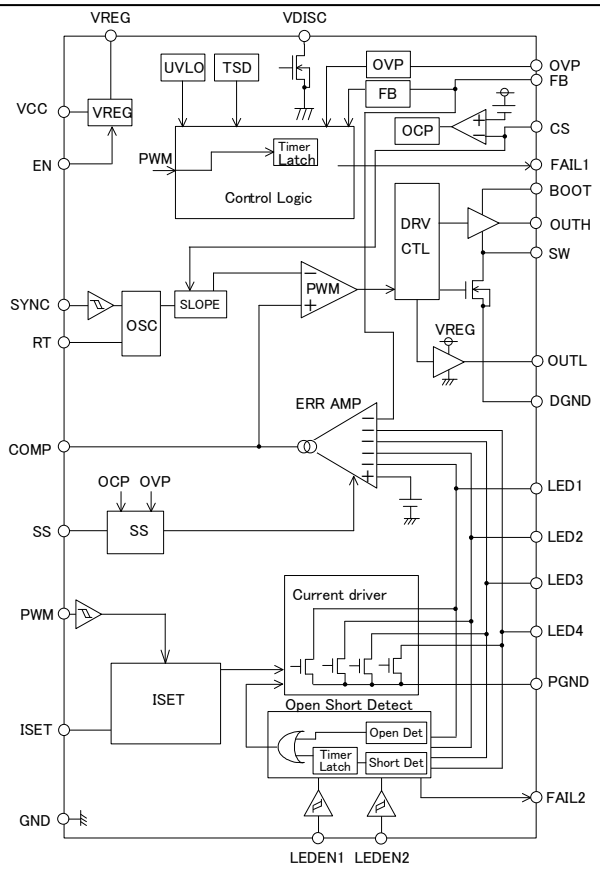


Fig.3 Internal block circuit

● **Absolute Maximum ratings** (Ta=25℃)

Parameter	Symbol	Rating	Unit
Power supply voltage	Vcc	40	V
BOOT ,OUTH Voltage	VBOOT, VOUTH	45	V
SW,CS,OUTL Voltage	VSW, VCS	40	V
BOOT-SW Voltage	VBOOT-SW	7	V
LED output, VDISC voltage	VLED1,2,3,4, VVDISC	40	V
VREG, OVP, FAIL1, FAIL2, LEDEN1, LEDEN2 ISET, PWM, SS, COMP, RT, SYNC, EN, OUTL Voltage	VVREG, VOVP, VFAIL1, VFAIL2, VLEDEN1, VLEDEN2, VISET, VPWM, VSS, VCOMP, VRT, VSYNC, VEN, VFB,VOUTL	-0.3～7 < Vcc	V
Power Consumption	Pd	1.45 ※1	W
Operating temperature range	Topr	-40～+125	℃
Storage temperature range	Tstg	-55～+150	℃
LED Maximum output current	ILED	120 ※2 ※3	mA
Junction temperature	TjMax	150	℃

※1 IC mounted on glass epoxy board measuring 70mm×70mm×1.6mm, power dissipated at a rate of 11.6mw/℃ at temperatures above 25℃.

※2 Dispersion figures for LED Maximum output current and V_F are correlated. Please refer to data on separate sheet.

※3 Amount of current per channel.

● **Operating conditions** (Ta=25℃)

Parameter	Symbol	Limits	Unit
Power supply voltage	Vcc	4.5～35	V
Oscillating frequency range	FOSC	200～2200	kHz
External synchronization frequency range ※4 ※5	FSYNC	fosc～2200	kHz
External synchronization pulse duty range	FSDUTY	40～60	%

※4 Connect SYNC to GND or OPEN when not using external frequency synchronization.

※5 Do not switch between internal and external synchronization when an external synchronization signal is input to the device.

●**Electrical Characteristics** (unless otherwise specified, Vcc=12V Ta=25℃)

Parameter	Symbol	Target value			Unit	Conditions
		Min	Typ	Max.		
Circuit current	ICC	-	-	10	mA	EN=High, SYNC=High, RT=OPEN, PWM=Low, ISET=OPEN, CIN=10μF
Standby current	IST	-	-	10	μA	EN=Low
[VREG Block (VREG)]						
Reference voltage	VREG	4.5	5	5.5	V	IREG=-5mA, CREG=2.2μF
[OUTH Block]						
OUTH high-side ON resistance	RONHH	1.5	3.5	7.0	Ω	ION=-10mA
OUTH low-side ON resistance	RONHL	1.0	2.5	5.0	Ω	ION=10mA
Over-current protection operating voltage	VOLIMIT	Vcc-0.66	Vcc -0.6	Vcc -0.54	V	
[OUTL Block]						
OUTL high-side ON resistance	RONLH	1.5	5.0	10.0	Ω	ION=-10mA
OUTL low-side ON resistance	RONLL	1.0	2.5	5.0	Ω	ION=10mA
[SW Block]						
SW low -side ON resistance	RON_SW	5.0	10.0	15.0	Ω	ION_SW=10mA
[Error Amplifie Block]						
LED voltage	VLED	0.9	1.0	1.1	V	
COMP sink current	ICOMPSINK	20	80	160	μA	VLED=2V, VCOMP=1V
COMP source current	ICOMP SOURCE	-160	-80	-20	μA	VLED=0V, VCOMP=1V
[Oscillator Block]						
Oscillating frequency	FOSC1	285	300	315	kHz	RT=27kΩ
Oscillating frequency	FOSC2	1800	2000	2200	kHz	RT=3.9kΩ
[OVP Block]						
Over-voltage detection reference voltage	VOVP	1.9	2.0	2.1	V	VOVP=Sweep up
OVP hysteresis width	VOHYS	0.45	0.55	0.65	V	VOVP=Sweep down
SCP Latch OFF Delay Time	TSCP	70	100	130	ms	RT=27kΩ
[FB Block]						
FB detection reference voltage	VFB	0.9	1.0	1.1	V	VFB=Sweep up
FB hysteresis width	VFBHYS	0.33	0.43	0.53	V	VFB=Sweep down
[UVLO Block]						
UVLO voltage	VUVLO	3.2	3.5	3.8	V	Vcc : Sweep down
UVLO hysteresis width	VUHYS	250	500	750	mV	Vcc :Sweep up,VREG>3.5V

[LED Output Block]						
LED current relative dispersion	⊿ILED1	-3	-	+3	%	ILED=50mA, ΔILED1=(ILED/ILED_AVG-1) ×100
LED current absolute dispersion	⊿ILED2	-3	-	+3	%	ILED=50mA, ΔILED2=(ILED/50mA-1)×100
ISET voltage	VISET	0.9	1.0	1.1	V	RISET=100kΩ
PWM Minimum pulse width	TMin	1	-	-	μs	FPWM=150Hz, ILED=100mA
PWM Maximum duty	DMax	-	-	100	%	FPWM=150Hz, ILED=50mA
PWM frequency	FPWM	-	-	20	kHz	Duty=2%, ILED=50mA
Open detection voltage	VOPEN	0.2	0.3	0.4	V	VLED= Sweep down
LED Short detection Voltage	VSHORT	4.2	4.5	4.8	V	VLED= Sweep up
LED Short Latch OFF Delay Time	TSHORT	70	100	130	ms	RT=27kΩ
PWM Latch OFF Delay Time	TPWM	70	100	130	ms	RT=27kΩ
[Logic Inputs (EN, SYNC, PWM, LEDEN1, LEDEN2)]						
Input High voltage	VINH	2.1	-	5.5	V	
Input Low voltage	VINL	GND	-	0.8	V	
Input current	IIN	25	50	100	μA	VIN=5V(EN,SYNC,PWM, LEDEN1, LEDEN2)
[FAIL Output (open drain)]						
FAIL Low voltage	VOL	-	0.1	0.2	V	IOL=0.1mA

● **Reference data** (unless otherwise specified, Ta=25℃)

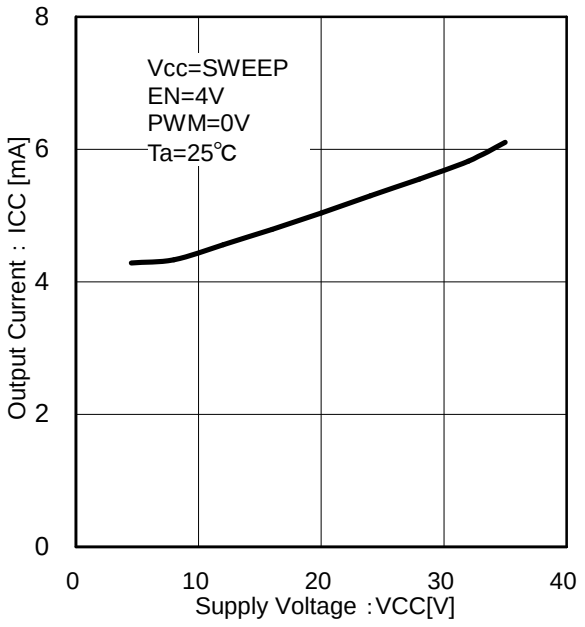


Fig.4 Circuit Current
(Switching OFF)

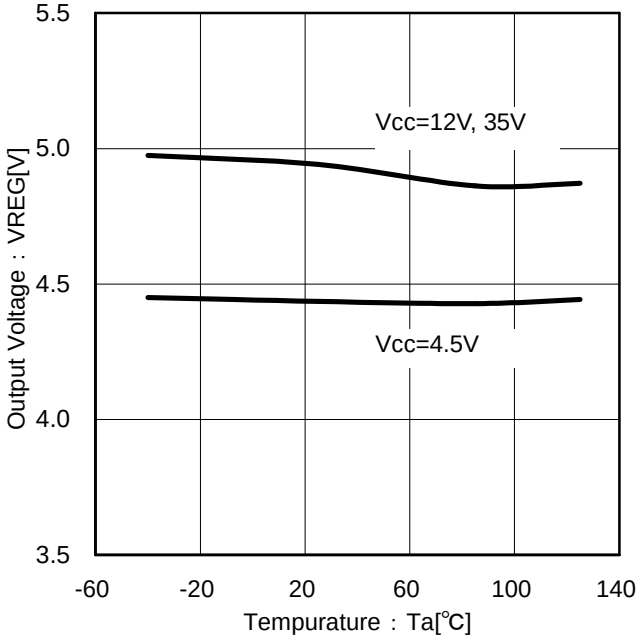


Fig.5 VREG temperature characteristic

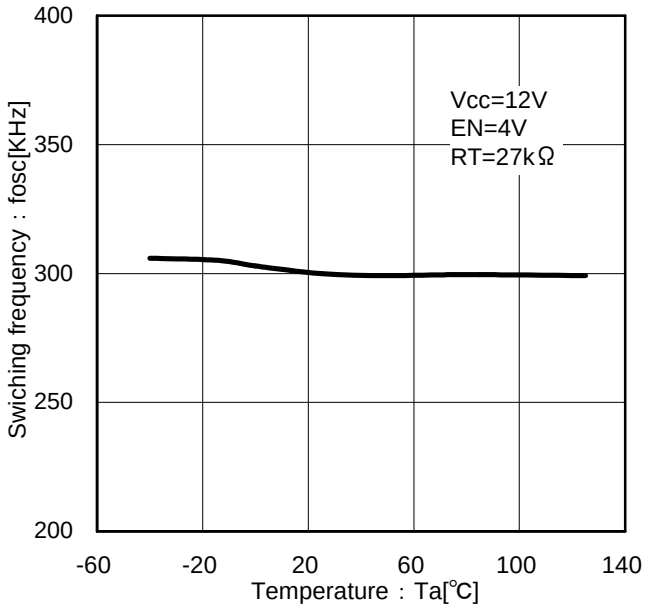


Fig.6 OSC temperature characteristic
(@ 300 kHz)

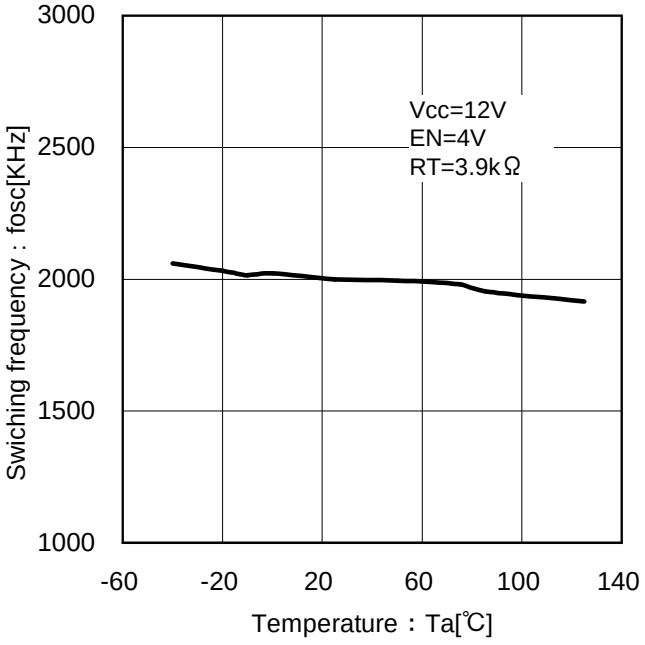


Fig.7 OSC temperature characteristic
(@ 2000 kHz)

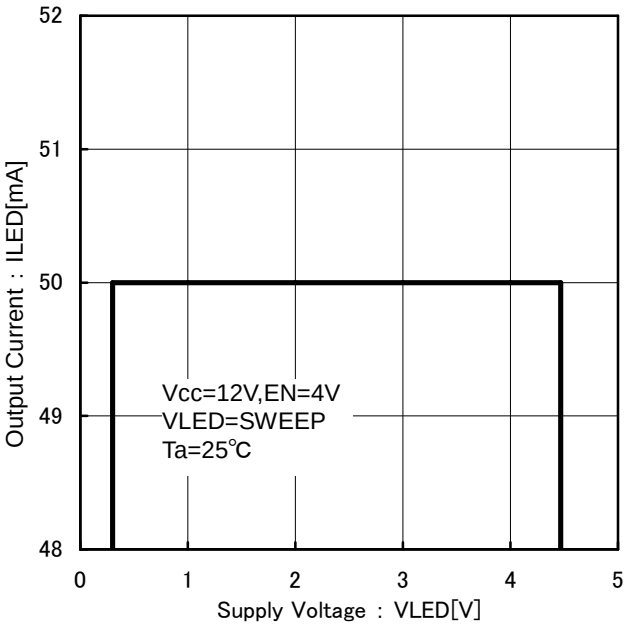


Fig.8 VLED vs ILED

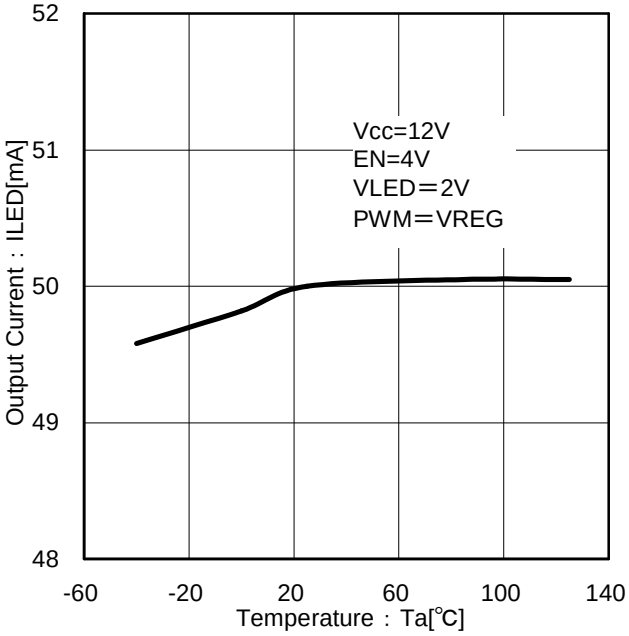


Fig.9 ILED temperature characteristic

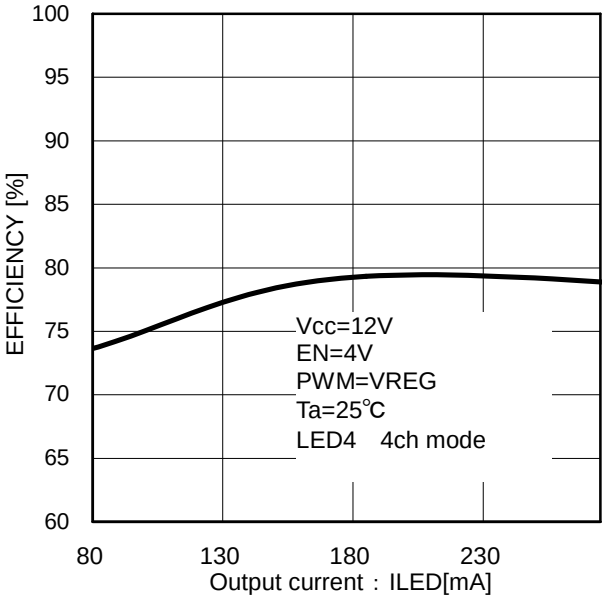


Fig.10 Efficiency (Buck-boost application)

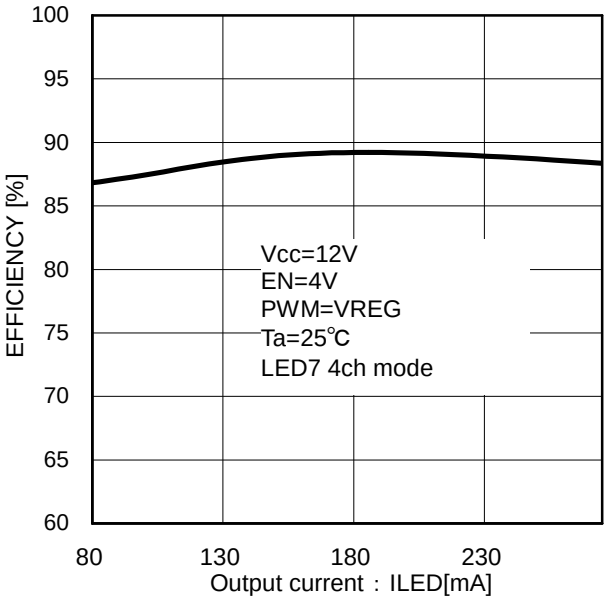


Fig.11 Efficiency (Boost application)

● **Description of Blocks**

1. **Voltage reference (VREG)**

5V (Typ.) is generated from the Vcc input voltage when the enable pin is set HI. This voltage is used to power internal circuitry, as well as the voltage source for device pins that need to be fixed to a logical HI.

UVLO protection is integrated into the VREG pin. The voltage regulation circuitry operates uninterrupted for VREG voltages Vcc>4.0V (Typ.) and VREG>3.5V(Typ.), but if output voltage drops to Vcc<3.5V(Typ.) or VREG<2.0V(Typ.) UVLO engages and turns the IC off.

Connect a capacitor (Creg=2.2～10μF) to the VREG terminal for phase compensation. Operation may become unstable if Creg is not connected.

2. Constant-current LED drivers

Table1 LED voltage

LED EN		LED			
〈1〉	〈2〉	1	2	3	4
L	L	ON	ON	ON	ON
H	L	ON	ON	ON	OFF
L	H	ON	ON	OFF	OFF
H	H	ON	OFF	OFF	OFF

If less than four constant-current drivers are used, unused channels should be switched off via the LEDEN1 and LEDEN2 pin configuration. The truth table for these pins is shown above. If a driver output is enabled but not used (i.e. left open), the IC's open circuit-detection circuitry will operate. Please keep the unused pins open. The LEDEN terMinals are pulled down internally in the IC, so if left open, the IC will recognize them as logic LOW. However, they should be connected directly to VREG or fixed to a logic HI when in use.

(1)**Output current setting**

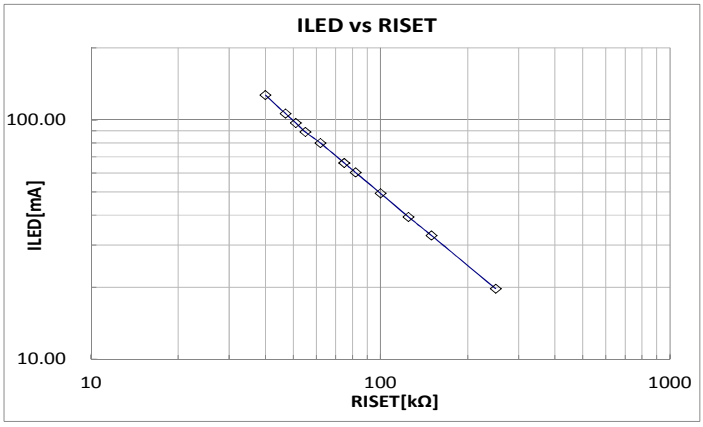


Fig.12 RISET vs ILED

LED current is computed via the following equation. GAIN is a constant decided in the circuit.

ILED[mA]= (1.0V / RISET[kΩ]) x GAIN [A] ：GAIN=5000(Typ.)

(2)**PWM intensity control**

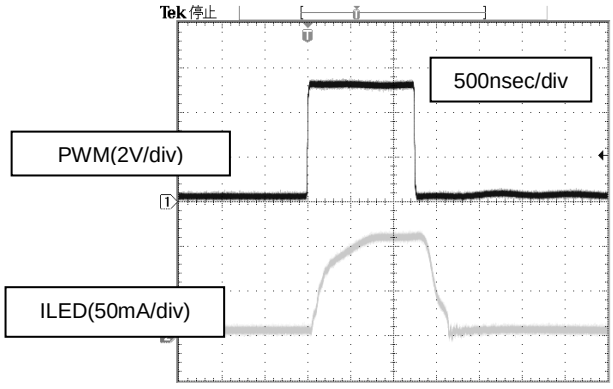


Fig.13 PWM=150Hz, Duty=0.02% ILED wave form

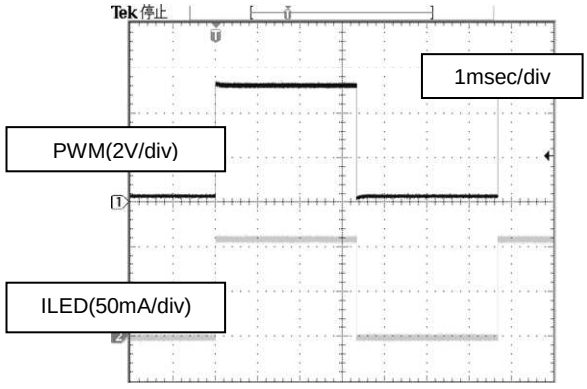


Fig.14 PWM=150Hz, Duty=50.0% ILED wave form

In PWM intensity control mode, the ON/OFF state of each current driver is controlled directly by the input signal on the PWM pin; thus, the duty ratio of the input signal on the PWM pin equals the duty ratio of the LED current. When not controlling intensity via PWM, fix the PWM terminal to a high voltage. Output light intensity is greatest at 100% input.

3. **Buck-Boost DC/DC controller**

(1)**Number of LEDs in series connection**

Output voltage of the DCDC converter is controlled such that the forward voltage over each of the LEDs on the output is set to 1.0V (Typ.). DCDC operation is performed only when the LED output is operating. When two or more LED outputs are operating simultaneously, the LED voltage output is held at 1.0V (Typ.) per LED over the column of LEDs with the highest VF value. The voltages of other LED outputs are increased only in relation to the fluctuation of voltage over this column. Consideration should be given to the change in power dissipation due to variations in VF of the LEDs. Please deterMine the allowable Maximum VF variance of the total LEDs in series by using the description as shown below:

VF variation allowable voltage 3.5V(Typ.)= short detecting voltage 4.5V(Typ.)－LED control voltage 1.0V(Typ.)

The number of LEDs that can be connected in series is limited due to the open-circuit protection circuit, which engages at 85% of the set OVP voltage. Therefore, the Maximum output voltage of the under normal operation becomes

34 V (= **40** V x **0.85**, where (**34** V – **1.1** V) / **VF** > **N** [Maximum number of LEDs in series]).

(2) **Over-voltage protection circuit (OVP)**

The output of the DCDC converter should be connected to the OVP pin via a voltage divider. In deterMining an appropriate trigger voltage of for OVP function, consider the total number of LEDs in series and the Maximum variation in VF. Also, bear in Mind that LED Open Detection is triggered at 0.85 x OVP trigger voltage.

If the OVP function engages, it will not release unless the DCDC voltage drops to 72.5% of the OVP trigger voltage. For example, if ROVP1 (GND side), ROVP2 (output voltage side), and DCDC voltage VOUT are conditions for OVP, then:

VOUT[V] ≥ (**ROVP1[kΩ]** + **ROVP2[kΩ]**) / **ROVP1[kΩ]** x **2.0** V.

OVP will engage when **VOUT** > **32** V if **ROVP1** = **22** kΩ and **ROVP2** = **330** kΩ.

(3) **Buck-boost DC/DC converter oscillation frequency (Fosc)**

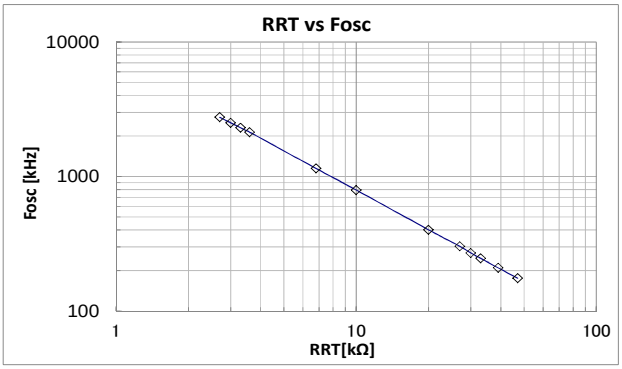


Fig.15 RRT VS Fosc

The regulator's internal triangular wave oscillation frequency can be set via a resistor connected to the RT pin (pin 4). This resistor deterMines the charge/discharge current to the internal capacitor, thereby changing the oscillating frequency. Refer to the above graph and following expression when setting RT.

$$Fosc[kHz] = (81\times10^{5} / RRT\ [k\Omega]) \times \alpha$$

81×10^5 is constant value in IC (+-5%) and α is adjustment factor.

(RT :α = 43kΩ: 1.01, 27kΩ: 1.00 , 18kΩ: 0.99, 10 kΩ: 0.98, 4.7kΩ: 0.97, 3.9kΩ: 0.96)

A resistor in the range of 3 kΩ～33 kΩ is recommended. Settings that deviate from the frequency range shown below may cause switching to stop, and proper operation cannot be guaranteed.

(4) **External DC/DC converter oscillating frequency synchronization (FSYNC)**

Do not switch from external to internal oscillation of the DC/DC converter if an external synchronization signal is present on the SYNC pin. When the signal on the SYNC terminal is switched from high to low, a delay of about 30 µS (Typ.) occurs before the internal oscillation circuitry starts to operate (only the rising edge of the input clock signal on the SYNC terminal is recognized). Moreover, if external input frequency is less than the internal oscillation frequency, the internal oscillator will engage after the above-mentioned 30 µS (Typ.) delay; thus, do not input a synchronization signal with a frequency less than the internal oscillation frequency.

(5)**Soft Start Function**

The soft-start (SS) limits the current and slows the rise-time of the output voltage during the start-up, and hence leads to prevention of the overshoot of the output voltage and the inrush current. If you don't use soft-start function, please set SS terminal open. About SS time calculation, please refer P.15.

4. **LED Short Detection**

Table2 Detecting condition and operation after detect about each protection

Protection	Detecting Condition		Operation after detect
	[Detect]	[Release]	
UVLO	Vcc<3.5V or VREG<2.0V	Vcc>4.0V and VREG>3.5V	All blocks (but except VREG) shut down
TSD	Tj>175℃	Tj<150℃	All blocks (but except VREG) shut down
OVP	VOVP>2.0V	VOVP<1.45V	SS discharged
OCP	VCS≦Vcc-0.6V	VCS>Vcc-0.6V	SS discharged
SCP	VLED<0.3V or VFB<0.57V (100ms delay 300kHz)	EN or UVLO	Counter starts and then latches off all blocks (but except VREG)
LED open	VLED<0.3V & VOVP>1.7V	EN or UVLO	The only detected channel latches off
LED short	VLED>4.5V (100ms delay 300kHz)	EN or UVLO	The only detected channel latches off (after the counter sets)

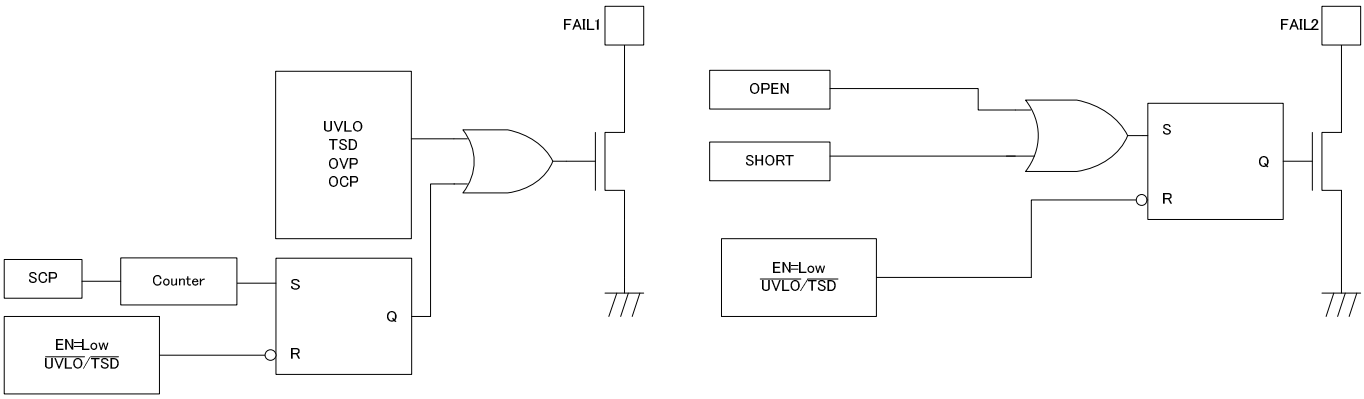


Fig.16 Protection flag output part block diagram

The operating status of the built-in protection circuitry is propagated to FAIL1 and FAIL2 pins (open-drain outputs). FAIL1 becomes low when UVLO, TSD, OVP, OCP, or SCP protection is engaged, whereas FAIL2 becomes low when open or short LED is detected. The recommend circuit is FAIL1 and FAIL2 terminal pullup to VREG. When pullup FAIL1 and FAIL2 to external voltage, please be attentive FAIL1 and FAIL2 current (IFAIL) at EN=Low.

IFAIL[mA]=(VFAIL[V]-Vf[V]) / RFAIL VFAIL : External voltage RFAIL : pull up resisiter

●Operation of the Protection Circuitry

(1)Under-Voltage Lock Out (UVLO)

The UVLO shuts down all the circuits other than REG when Vcc<3.5V(Typ.) or VREG<2.0V(Typ.)

(2)Thermal Shut Down (TSD)

The TSD shuts down all the circuits other than REG when the Tj reaches 175℃ (Typ), and releases when the Tj becomes below 150℃ (Typ).

(3)Over Current Protection (OCP)

The OCP detects the current through the power-FET by monitoring the voltage of the high-side resistor, and activates when the CS voltage becomes less than Vcc-0.6V (Typ).
When the OCP is activated, the external capacitor of the SS pin becomes discharged and the switching operation of the DCDC turns off.

(4) Over Voltage Protection (OVP)

The output voltage of the DCDC is detected with the OVP-pin voltage, and the protection activates when the OVP-pin voltage becomes greater than 2.0V (Typ).
When the OVP is activated, the external capacitor of the SS pin becomes discharged and the switching operation of the DCDC turns off.

(5)Short Circuit Protection (SCP)

When the LED-pin voltage becomes less than 0.3V (Typ), the internal counter starts operating and latches off the circuit approximately after 100ms (when FOSC = 300kHz). If the LED-pin voltage becomes over 0.3V before 100ms, then the counter resets.

When the LED anode (i.e. DCDC output voltage) is shorted to ground, then the LED current becomes off and the LED-pin voltage becomes low. Furthermore, the LED current also becomes off when the LED cathode is shorted to ground. Hence in summary, the SCP works with both cases of the LED anode and the cathode being shorted.

(6)LED Open Detection

When the LED-pin voltage ≤ 0.3V (Typ) as well as OVP-pin voltage ≥ 1.7V (Typ) simultaneously, the device detects as LED open and latches off that particular channel.

(7)PWM Low detection circuit

Built-in counter operation is begun after EN=High and PWM=Low. After 32770 clk, all blocks (but except VREG) shut down. If PWM=High, the PWM Low detection released and return the nomal operation.

(8) Circuit of discharge Vout (VDISC terminal)

Restarting DC/DC must be operated after discharging Vout. If using only pull-down resistance as setting OVP for discharging, it takes a lot time for discharging Vout. Therefore this product has functionality of circuit for discharge. By VDISC terminal is connected to output of DCDC , the output can be discharged when DCCD circuit become OFF (with EN changing high to low or detection of protect).

The formulas of discharge time as Tdisc are as follows

Tdisc[sec](Typ.) = Cout[F] × Vout[V] / 0.33 Tdisc : Time of discharge DCDC output

Tdisc[sec](Max.) = Cout[F] × Vout[V] / 0.192 Cout : Capacitance of DC/DC output

Shown by formula, It takes a time of Tdisc for discharging Vout.

When restating DC/DC with using EN, please keep more time of Tdisc after DCDC becomes off.

On the configure of Boost DC/DC application, constant current goes through Vcc→inductor→diode→VDISC by VDISC connected to DC/DC output.

This constant current causes at stand-by mode. Fig.17 shows the relation between VCC and ICC (stand-by) by using VDISC at Boost application. It is necessary for reducing stand-by current to use Boost-buck or add High-side VCC switch controlled by EN at Vcc side.

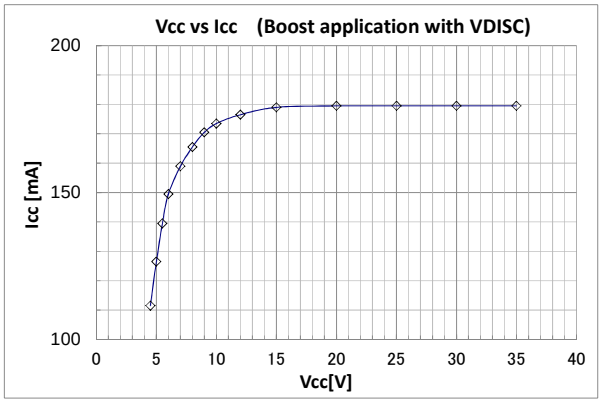


Fig.17 Vcc vs Stand-by current (Boost DC/DC with using VDISC)

(9)LED Short detection

The internal counter starts operating, and approximately after 100ms (when Fosc = 300kHz) the only detected channel (as LED short) latches off. With the PWM brightness control, the detecting operation is processed only when PWM = High. If the condition of the detection operation is released before 100ms (when Fosc = 300kHz), then the internal counter resets. The counter frequency is the DCDC switching frequency determined by the RT. The latch proceeds at the count of 32770.

●**Timing Chart**

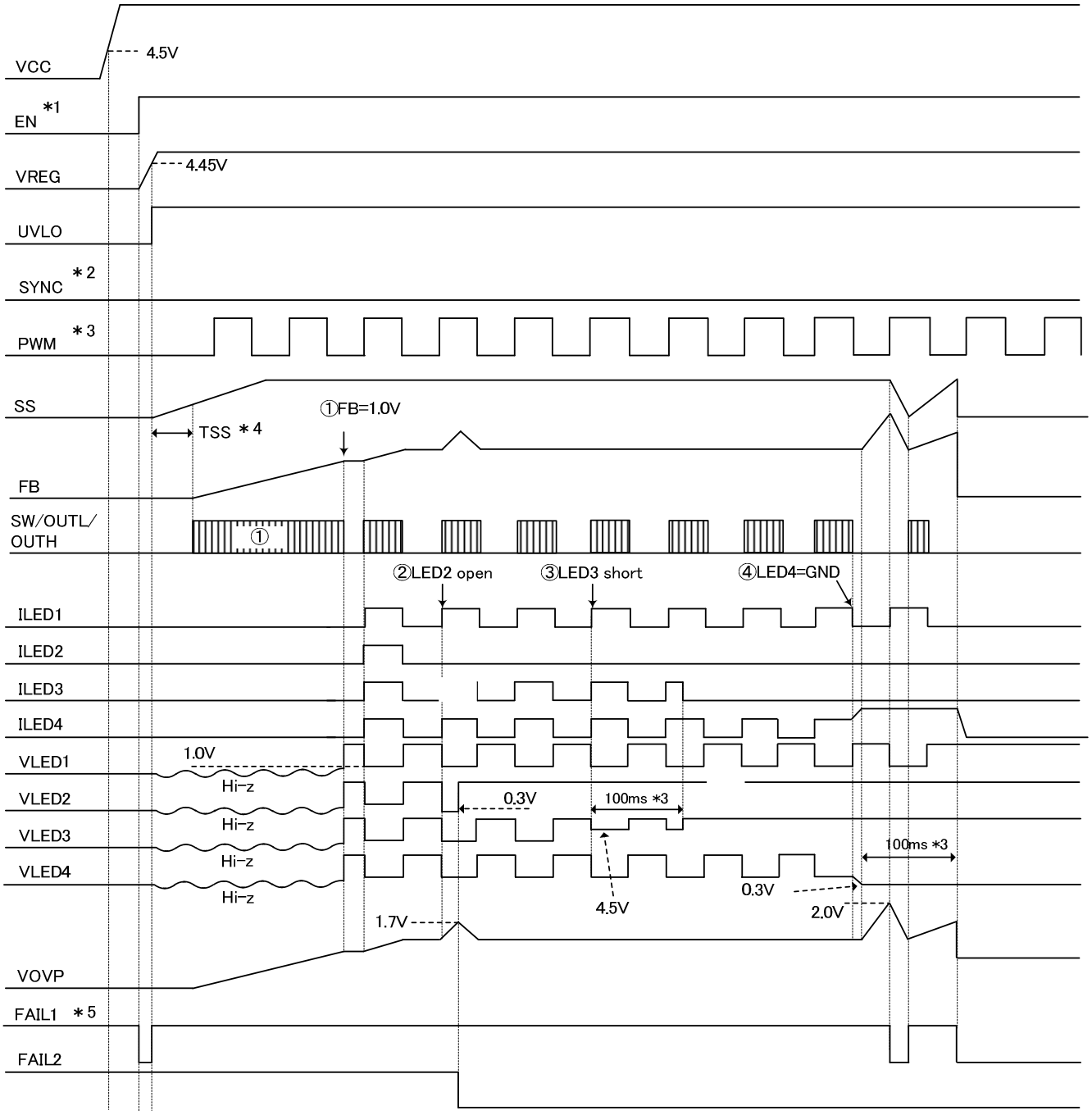


Fig.18 Protection Sequence timing Chart

＊1 Turn on the EN after the Vcc is on
Turn on the PWM and SYNC after VREG≧4.45V.

＊2 The order of turning on PWM and SYNC is arbitrary.

＊3 Aprox 100ms of delay when Fosc = 300kHz

＊4 It is the timing chart that Fail is pull-up in an external voltage.

*5 fail terminal is pulled-up to external power supply.

① During FB<1.0V、DCDC is switching without PWM input (called Pre-Boost)。When FB reaches to FB≧1.0V, Pre-Boost finishes。

② LED2 is open mode.VLED2<0.3V VOVP and > detects 1.7V, and LED2 is turned off. →FAIL2 becomes Low.

③ LED3 is short mode.VLED3>4.5V is detected, and LED3 after about 100ms is turned off.

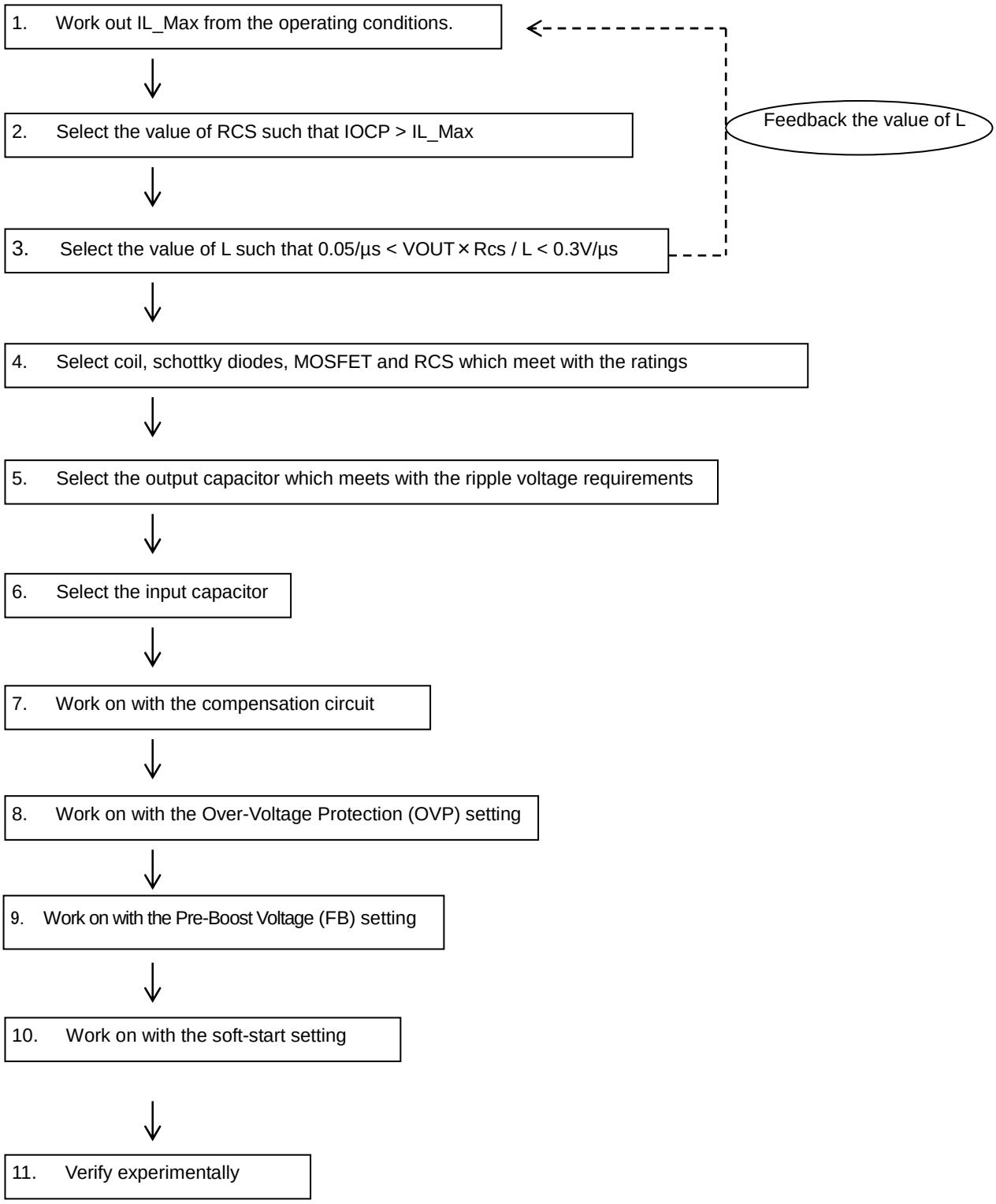
④ VLED4 is GND- shorted.

④-1 The output voltage lifts, and OVP is detected with VOVP>2.0V.
→SS pulling out
→FAIL1 becomes Low.

④-2 Shutdown after about 100ms when LED4<0.3V is detected.

●**Procedure for external components selection**

Follow the steps as shown below for selecting the external components



1. Computation of the Input Peak Current and IL_Max

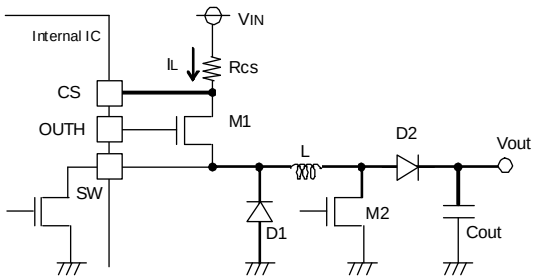


Fig.19 Output application circuit diagram

① Calculation of the Maximum output voltage (Vout_Max)
To calculate the Vout_Max, it is necessary to take into account of the VF variation and the number of LED connection in series.

Vout_Max = (VF + ΔVF) × N + 1.1V

Vout_Max [V] : Output voltage Max VF[V] : LED VF Voltage
ΔVF : LED VF Voltage vary N : LED cascade

② Calculation of the Max output current Iout_Max

Iout_Max = ILED × 1.03 × M

Iout_Max[A] : Input peak current Max
ILED[A] : Output current by 1ch M : LED parallel

③Calculation of the Max input peak current IL_Max

IL_Max = IL_AVG + 1/2ΔIL
IL_AVG = (VIN + Vout_Max) × Iout_Max / (n × VIN)

$$\Delta IL = \frac{VIN}{L} \times \frac{1}{Fosc} \times \frac{Vout}{VIN+Vout}$$

IL_Max[A] : Input peak current Max
IL_AVG[A] : Input average current Max
IL[A] : Input current sweep width
VIN[V] : Input voltage n : efficiency
L[H] : Coil value Fosc : Switching frequency

・The worst case scenario for VIN is when it is at the Minimum, and thus the Minimum value should be applied in the equation.

・The L value of 2.2 ~ 47μH is recommended. The current-mode Type of DC/DC conversion is adopted for BD81A14EFV-M, which is optimized with the use of the recommended L value in the design stage. This recommendation is based upon the efficiency as well as the stability. The L values outside this recommended range may cause irregular switching waveform and hence deteriorate stable operation.

・n (efficiency) is approximately 80%

2. The setting of over-current protection

Choose Rcs with the use of the equation

Vocp_Min[V] (=0.54V) / Rcs[Ω] > IL_Max[A]

3. The selection of the L

In order to achieve stable operation of the current-mode DC/DC converter, we recommend selecting the L value in the range indicated below:

$$0.05\ [V/\mu s] < \frac{Vout[V] \times Rcs[\Omega]}{L[\mu H]} < 0.3\ [V/\mu s]$$

When investigating the margin, it is worth noting that the L value may vary by approximately ±30%.

The smaller $\frac{Vout \times Rcs}{L}$ allows stability improvement but slows down the response time.

4. Selection of coil L, diode D1 and D2, MOSFET M1 and M2, and Rcs

	Current rating	Voltage rating	Heat loss
Coil L	> IL_Max	—	
Diode D1	> Iocp	> VIN_Max	
Diode D2	> Iocp	> Vout	
MOSFET M1	> Iocp	> VIN_Max	
MOSFET M2	> Iocp	> Vout	
Rcs	—	—	> $Iocp^2$ × Rcs

※ Allow some margin, such as the tolerance of the external components, when selecting.

※ In order to achieve fast switching, choose the MOSFETs with the smaller gate-capacitance.

5. Selection of the output capacitor

Select the output capacitor Cout based on the requirement of the ripple voltage Vpp.

$$Vpp[V] = \frac{Iout[A]}{Cout[F]} \times \frac{Vout[V]}{Vout[V]+VIN[V]} \times \frac{1}{Fosc[Hz]} + \Delta IL[A] \times RESR[\Omega]$$

Choose Cout that allows the Vpp to settle within the requirement. Allow some margin also, such as the tolerance of the external components.

6. Selection of the input capacitor

A capacitor at the input is also required as the peak current flows between the input and the output in DC/DC conversion. We recommend an input capacitor greater than 10µF with the ESR smaller than 100mΩ. The input capacitor outside of our recommendation may cause large ripple voltage at the input and hence lead to malfunction.

7. Phase Compensation Guidelines

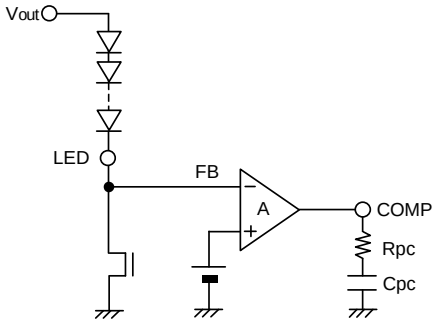


Fig.20 COMP part application circuit diagram

In general, the negative feedback loop is stable when the following condition is met

- Overall gain of 1 (0dB) with a phase lag of less than 150º (i.e., a phase margin of 30º or more)
- The switching frequency more than unity gain frequency (frequency at gain 0dB) of 1/10.

※ R_L is the load impedance. (R_L = VOUT / IOUT)

The key for achieving stability is to place fz near to the unity gain frequency.

$$\text{Phase-lead} \quad fz[Hz] = \frac{1}{2\pi Cpc[F]Rpc[\Omega]} \ [Hz]$$

$$\text{Phase-lag} \quad fp1[Hz] = \frac{1}{2\pi R_L Cout} \ [Hz]$$

Good stability would be obtained when the fz is set between 1kHz～10kHz.

In buck-boost applications, Right-Hand-Plane (RHP) Zero exists. This Zero has zero characteristic for gain and pole characteristic in terms of phase. As this Zero would cause instability when it is in the control loop, so it is necessary to keep RHP frequency more than GBW frequency.

$$fRHP[Hz] = \frac{Vout[V] \times \{VIN[V]/(Vout[V]+VIN[V])\}^2}{2\pi I_{LOAD}[A]L\,[H]}$$

I_{LOAD}: MAXIMUM LOAD CURRENT

It is important to keep in Mind that these are very loose guidelines, and adjustments may have to be made to ensure stability in the actual circuitry. It is also important to note that stability characteristics can change greatly depending on factors such as substrate layout and load conditions. Therefore, when designing for mass-production, stability should be thoroughly investigated and confirmed in the actual physical design.

8. Setting of the over-voltage protection

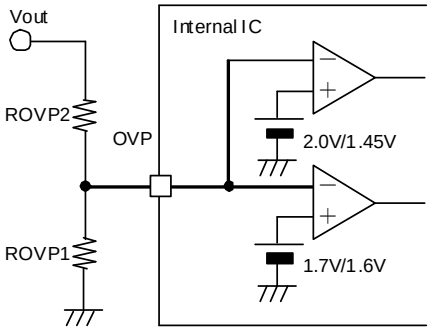


Fig.21 OVP part application circuit diagram

* We recommend setting the over-voltage protection Vovp 1.2V to 1.5V greater than Vout which is adjusted by the number of LEDs in series connection. Less than 1.2V may cause unexpected detection of the LED open and short during the PWM brightness control. For the Vovp greater than 1.5V, the LED short detection may become invalid.

9. Setting of Pre-Boost (FB)

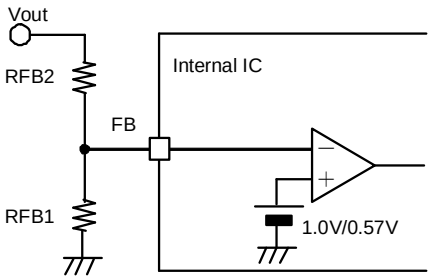


Fig.22 FB part application circuit diagram

DC/DC is FB terminal detects below 1.0V
During FB terminal is below 1.0V that means the detection that output voltage has not boosted to setting voltage.
DC/DC is switching without regarding PWM for fast start-up of DC/DC during FB is below 1.0V. This condition is called “Pre-boost”.
Therefore the voltage of divided resistance at minimum condition (LED VF minimum) should be over VFB(1.1V max) for operating normal switching DC/DC (not Pre-boost).

RFB1、RFB2 resistances are set as follows

Vout (Min.) × (RFB1/(RFB1+RFB2)) > VFB(Max.) ・・・(2)

Vout：DCDC output Voltage、 VFB：FB detection voltage

For example1) In case of 8 strings LEDs Vf=3.2V±0.3VLED

Vout (Min.) = 0.9V (LED regulated min Voltage) + (3.2V – 0.3V) × 8 = 24.1V
FB detection voltage for Pre-boost : VFB (Max.) = 1.1V
When deciding RFB1=20kΩ → getting RFB2 < 418.2kΩ referring to (2)
The detection of pre-Boost voltage is 21.9V (typ)

For example2) In case of 4 strings LEDs Vf=3.2V±0.3VLED

Vout (Min.) = 0.9V (LED regulated min Voltage) + (3.2V – 0.3V) × 4 = 12.5V
FB detection voltage for Pre-boost : VFB (Max.) = 1.1V
When deciding RFB1=20kΩ → getting RFB2 < 207.3kΩ referring to (2)
The detection of pre-Boost voltage is 11.4V (typ)

10. Setting of the soft-start

The soft-start allows Minimization of the coil current as well as the overshoot of the output voltage at the start-up.

For the capacitance we recommend in the range of 0.001 to 0.1uF. For the capacitance less than 0.001uF may cause overshoot of the output voltage. For the capacitance greater than 0.1uF may cause massive reverse current through the parasitic elements of the IC and damage the whole device. In case it is necessary to use the capacitance greater than 0.1uF, ensure to have a reverse current protection diode at the Vcc or a bypass diode placed between the SS-pin and the Vcc.

Soft-start time (The time of EN input and PWM input to DCDC switching start) TSS (Typ.)

TSS[sec] = CSS[F]X0.7[V] / 5[uA] CSS: The capacitance at the SS-pin

There is the possibility of SCP error detection hang on CSS setting and Oscillating frequency setting.
Please check the following condition.

Trise[sec] = CSS[F] X V1[V] / Iss[A]
Trise : DCDC start up time, V1 : IC constant voltage(Max 2.5V), Iss : SS source current(Min 2.0uA)
Tscp[sec] = 32770 X (1/Fosc)[Hz]
Tscp : SCP Latch OFF Delay Time, Fosc : Oscillating frequency
SCP error detection avoid condition : Trise < Tscp

11. Verification of the operation by taking measurements
The overall characteristic may change by load current, input voltage, output voltage, inductance, load capacitance, switching frequency, and the PCB layout. We strongly recommend verifying your design by taking the actual measurements.

●**Recommended operating range**

The following data is recommended operating range of BD81A14EFV-M (Vcc vs Vout). Please use above the border line.
The following data is reference data in Rohm evaluation board. So please check the behavior of practice board and use this IC.

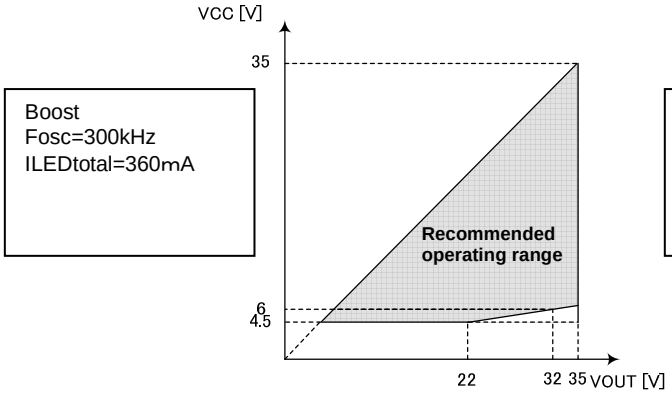


Fig.23 Boost operating range (1)

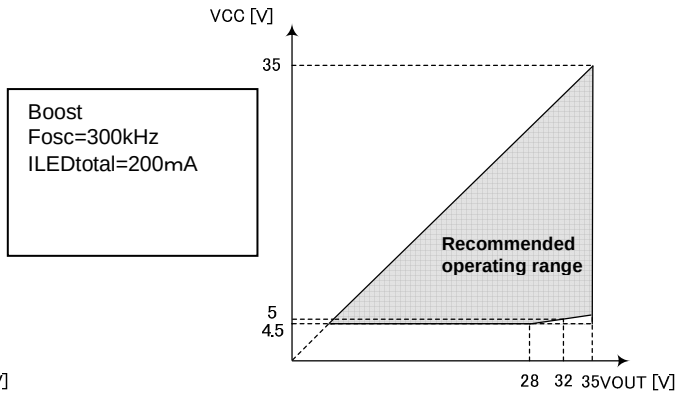


Fig.24 Boost operating range (2)

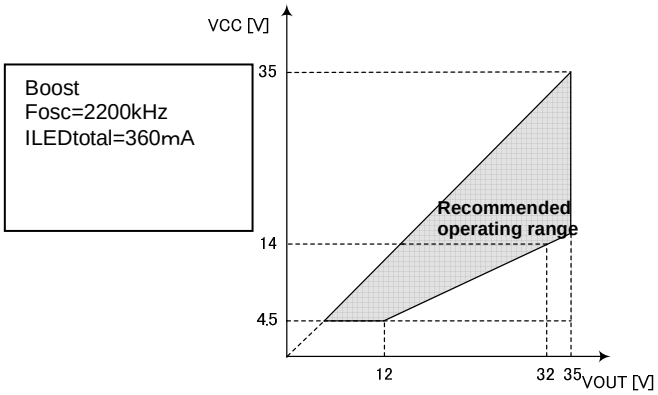


Fig.25 Boost operating range (3)

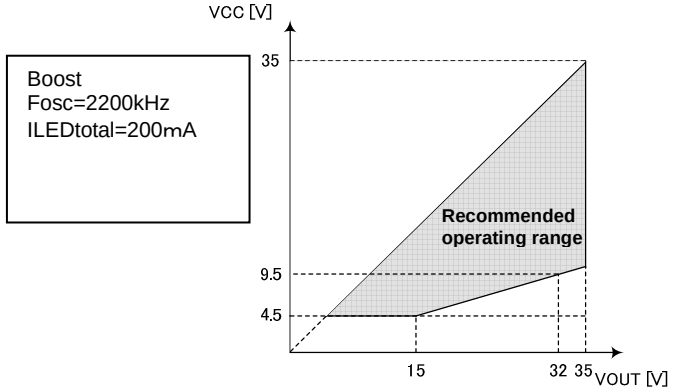


Fig.26 Boost operating range (4)

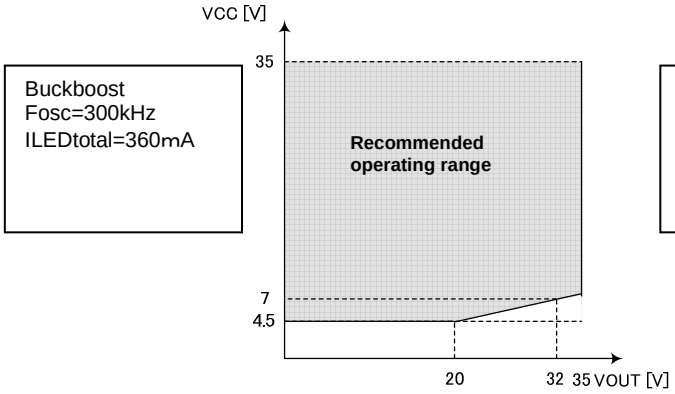


Fig.27 Buckboost operating range (1)

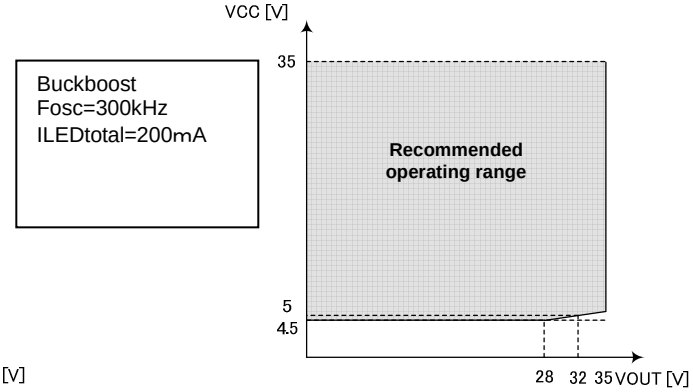


Fig.28 Buckboost operating range (2)

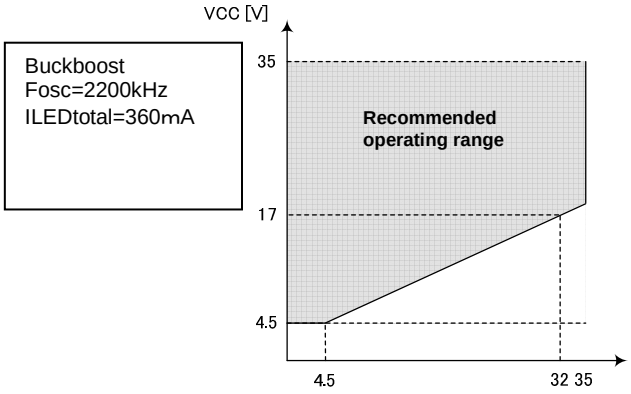


Fig.29 Buckboost operating range (3)

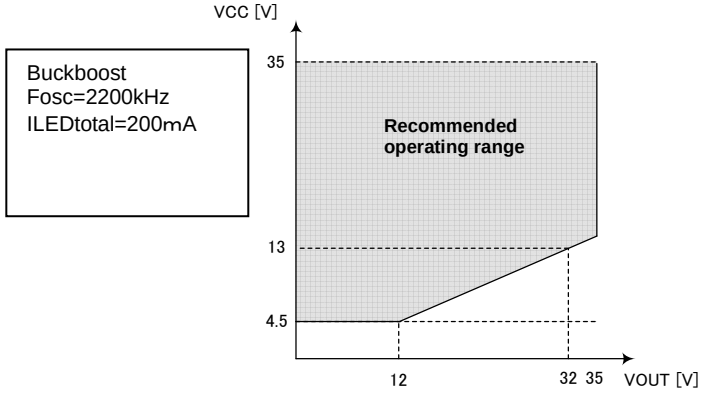


Fig.30 Buckboost operating range (4)

●PCB application circuit diagram

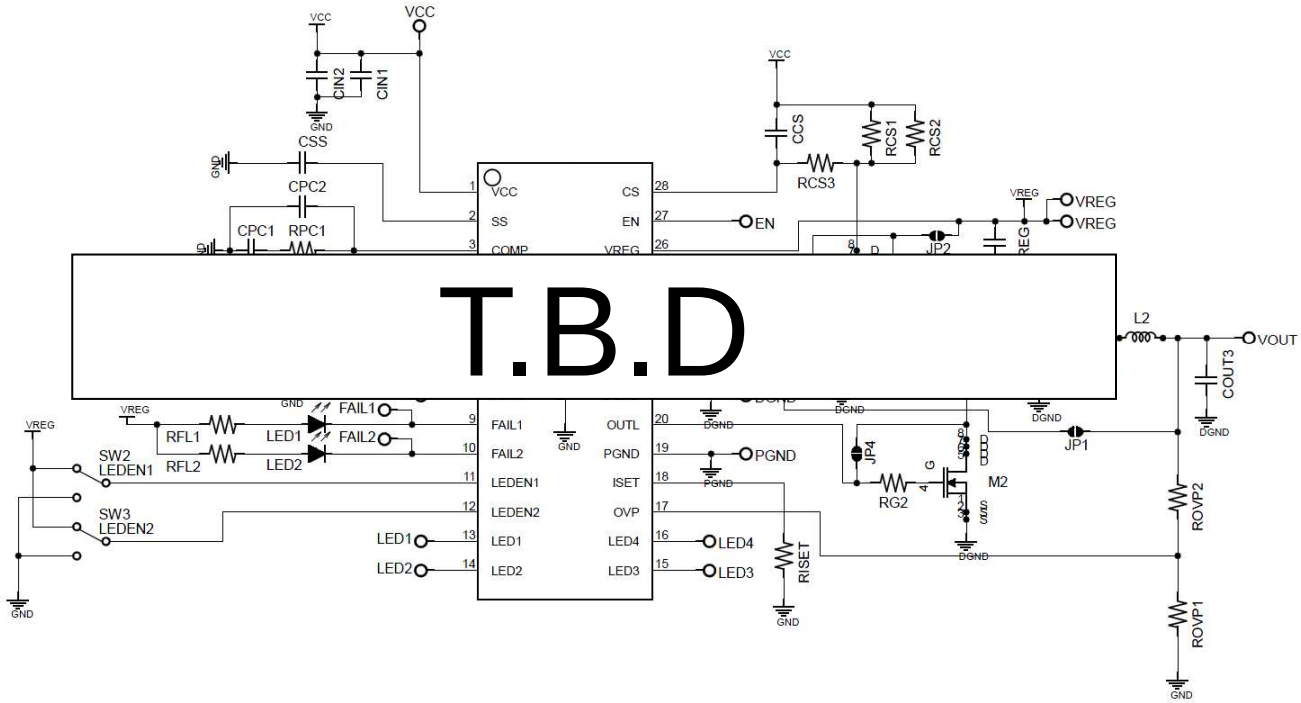


Fig.31 PCB application circuit diagram

- The RRT resister should be mounted as close as possible to the RT pin.
- The coupling capacitors CVcc and CREG should be mounted as close as possible to the IC's pins.
- Large currents may pass through DGND and PGND, so each should have its own low-impedance routing to the system ground.
- Noise should be Minimized as much as possible on pins PWM, ISET, RT and COMP.
- PWM, OUTH, OUTL, SW, SYNC and LED1-4 carry switching signals, so ensure during layout that surrounding traces are not affected by crosstalk.
- VQFN28SV505 package has heat dissipation PAD behind it. The dissipation PAD needs to be connected to PCB with solder.
- Capacitance of LED1～LED4 terminals should be reduced to eliminate flickering at starting DC/DC without PWM.
  If the flickering occurs despite reduce capacitance, start-up sequence should be changed as follows to avoid flickering.
  1. Input SYNC = High
  2. Input EN =High and PWM after SYNC is high.
  3. Input SYNC = Low →DC/DC starts-up when SYNC becoming High to Low.

● **Application Board Diagram**

When using it as Step-up DCDC converter

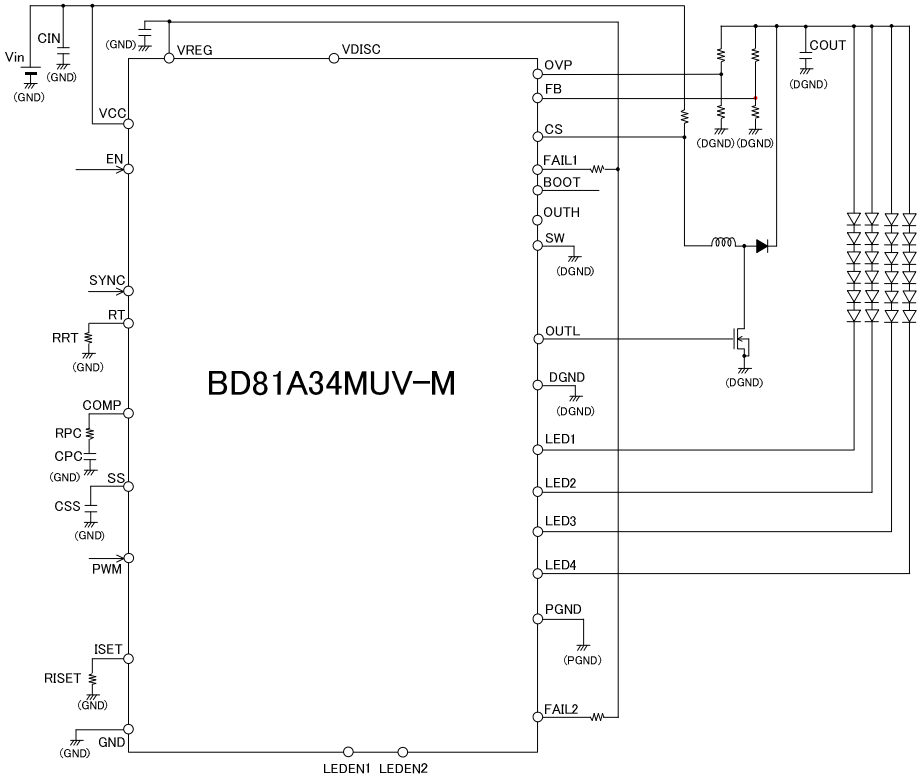


Fig.32 Step-up application circuit diagram

When using it as Step-down DCDC converter

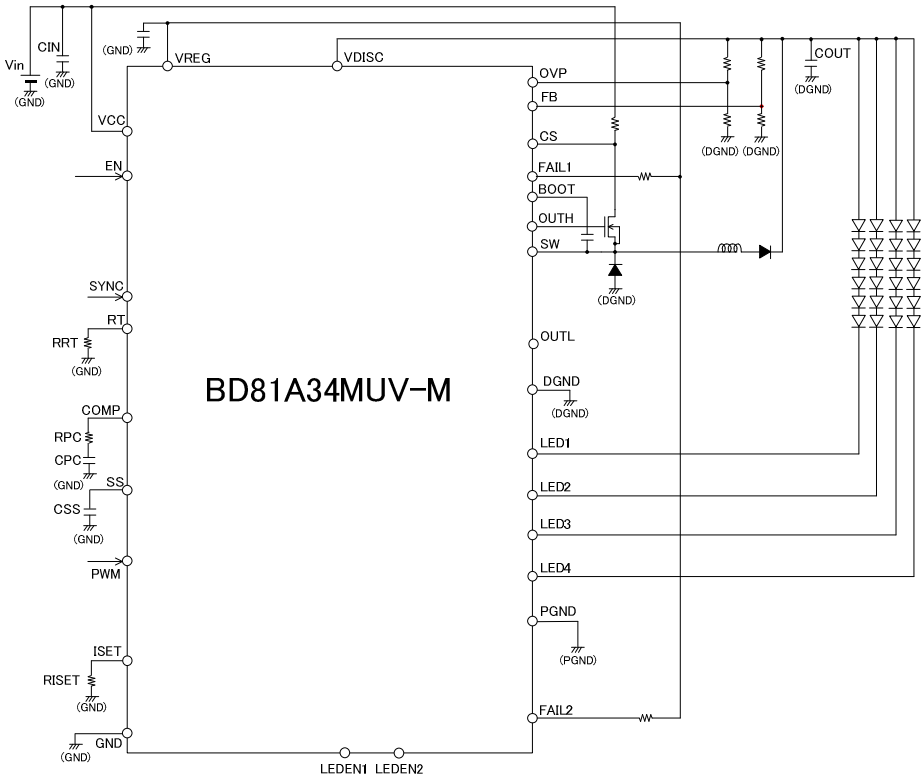


Fig.33 Step-down application circuit diagram

Note：When VOUT and the LED terminal are shorted to GND, the overcurrent from VIN cannot be obstructed when using it as stated above as the Step-up DCDC converter. Therefore, please do measures of the insertion of the fuse between Vcc and RCS etc.

●PCB board external part list

serial No.	component name	component value	product name	Manufacturer
1	CIN1	10μF	GRM31CB31E106KA75B	murata
2	CIN2	–	–	–
3	CPC1	0.1μF	GRM188B31H104KA92	murata
4	CPC2	–	–	–
5	RPC1	510Ω	MCR03 Series	Rohm
6	CSS	0.01μF	GRM188B31H103KA92	murata
7	RRT	27kΩ	MCR03 Series	Rohm
8	RFL1	100kΩ	MCR03 Series	Rohm
9	RFL2	100kΩ	MCR03 Series	Rohm
10	CCS	–	–	–
11	RCS1	620mΩ	MCR100 Series	Rohm
12	RCS2	620mΩ	MCR100 Series	Rohm
13	RCS3	0Ω	–	–
14	CREG	2.2μF	GRM188B31A225KE33	murata
15	CPC3	0.1μF	GRM188B31H104KA92	murata
16	M1	–	RSH070N05	Rohm
17	M2	–	RSH070N05	Rohm
18	D1	–	RB050L-40	Rohm
19	D2	–	RF201L2S	Rohm
20	L1	33μH	SLF10145T-330M1R6-H	TDK
21	L2	-	–	–
22	COUT1	10μF	GRM31CB31E106KA75B	murata
23	COUT2	10μF	GRM31CB31E106KA75B	murata
24	COUT3	-	–	–
25	ROVP1	30kΩ	MCR03 Series	Rohm
26	ROVP2	360kΩ	MCR03 Series	Rohm
27	RISET	100kΩ	MCR03 Series	Rohm
28	RG1	0Ω	–	–
29	RG2	0Ω	–	–
30	LED1	0Ω	–	Rohm
31	LED2	0Ω	–	Rohm
32	JP1	0Ω	–	–
33	JP2	–	–	–
34	JP3	0Ω	–	–
35	JP4	–	–	–
36	JP5	–	–	–
37	RFB1	30kΩ	MCR03 Series	Rohm
38	RFB2	360kΩ	MCR03 Series	Rohm

● **Power Dissipation Calculation**

Pc	=	Icc×Vcc	・・・①Power of circuit
	＋	Ciss1×VREG×Fsw×VREG	・・・②Boost FET drive power
	＋	Ciss2×VREG×Fsw×VREG	・・・③Buck FET drive power
	＋	{ VLED×M + △Vf×(M-1) }×ILED	・・・④Power of current driver

IL_AVG =	(Vcc+Vout)/Vcc×Iout/n	・・・⑤Inductance average current
IFET=	IL_AVG×Vout/(Vcc+Vout)	・・・⑥Current that flows to Boost FET
Iout =	ILED×1.03×M	・・・⑦LED output current
Vout =	(Vf +ΔVf)×N ＋ VLED	・・・⑧DCDC output voltage

Pc[w] : power consumption	Icc[A] : Current of the Maximum circuit	Vcc[V] : power-supply voltage
Ciss1[F] : Boost FET gate capacitance	Ciss2[F] : Buck FET gate capacitance	REG[V] : VREG voltage
Fsw[Hz] : Switching frequency	VLED[V] : LED control voltage	LED[A] : LED output current
N : LED number	M : Parallel number of LED	f[V] : LED forward voltage
△Vf[V] : LED Vf difference	n : Efficiency	

＜Calculation example＞

When assuMing Icc=10 m A, Vcc=12V, Ciss1=65pF, Ciss2=2000pF, VREG=5V, Fsw=2200kHz, VLED=1V, ILED=50mA, N=7steps, M=4 row, Vf=3.5V, ΔVf=0.5V, n=80%

Vout = (3.5V+0.5V)×7 steps＋1V = 29V

Iout = 50mA×1.03×4 row = 0.206A

IL_AVG= (12+29V)/12V×0.206A/0.8 = 0.88A

IFET= 0.88A×29V/ (12V+29V)=0.622A

Pc (4) = 10mA×12V ＋ 65pF×5V×2200kHz×5V ＋ 2000pF×5V×2200kHz×5V ＋ {1.0V×4+0.5V×(4-1)}×50mA = 0.509[W]

● **Power Dissipation of packaging**

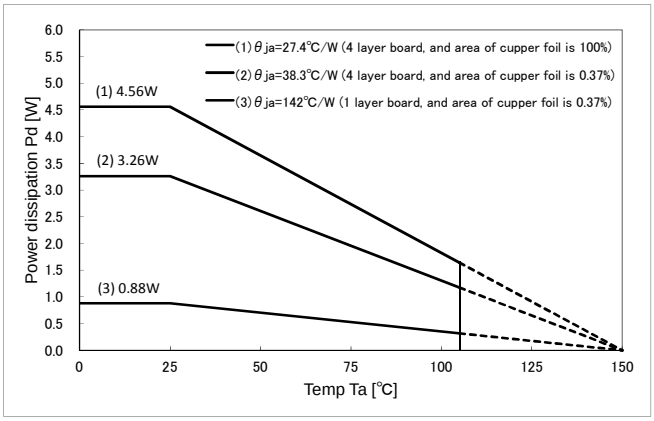


Fig.34 VQFN28SV5050 Power dissipation

Note 1: Power dissipation calculated when mounted on 70mm X 70mm X 1.6mm glass epoxy substrate (1-layer platform/copper thickness 18μm)

Note 2: Power dissipation changes with the copper foil density of the board. This value represents only observed values, not guaranteed values.

● VQFN28SV5050

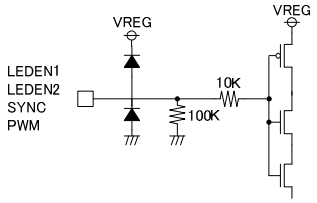
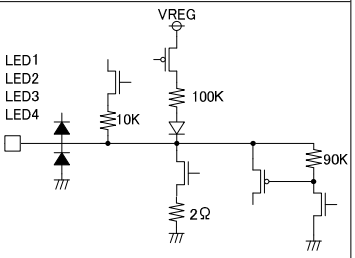
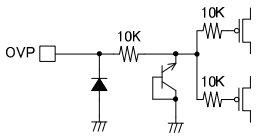
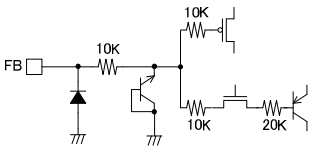
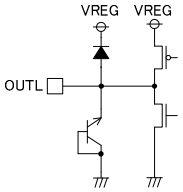
Pd=0.88W (0.176W): Board copper foil area 20.2㎟

Pd=3.26W (0.652W): Board copper foil area 5505㎟

Pd=4.56W (0.912W): Board copper foil area 5505㎟

(Value within parentheses represents power dissipation when Ta=125℃)

● **Input/output Equivalent Circuits** (terminal name follows pin number)

1.LEDEN1,2.LEDEN2,23.SYNC,26.PWM,		3～6. LED1～4
		
7.OVP	8.FB	10.OUTL
		
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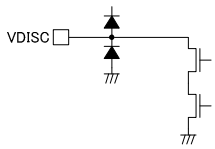	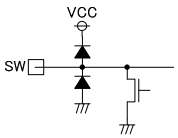	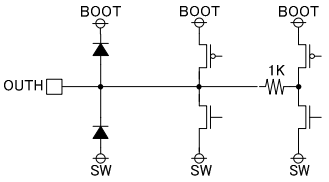
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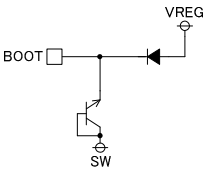	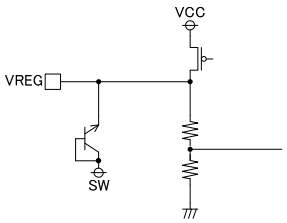	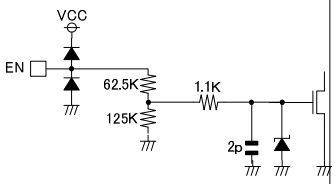
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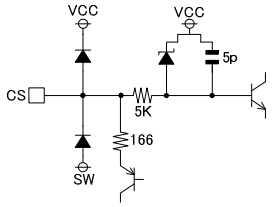
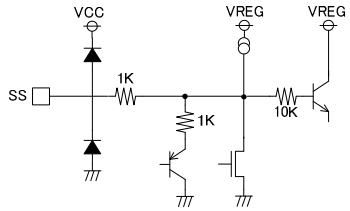
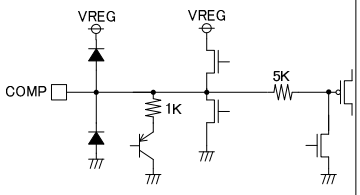
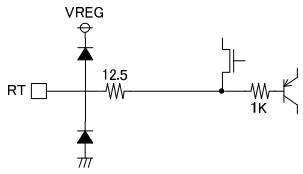
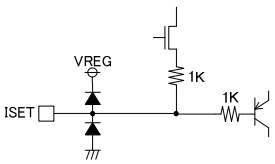
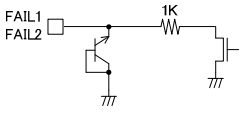
		
22.RT	24.ISET	27.FAIL1,28.FAIL2
		

※All values Typical.

● **Operating Notes**

1) Absolute Maximum ratings

Use of the IC in excess of absolute Maximum ratings (such as the input voltage or operating temperature range) may result in damage to the IC. Assumptions should not be made regarding the state of the IC (e.g., short mode or open mode) when such damage is suffered. If operational values are expected to exceed the Maximum ratings for the device, consider adding protective circuitry (such as fuses) to eliMinate the risk of damaging the IC.

2) Reverse connection of power supply connector

IC might be destroyed because of reverse connection of power supply connector. Please take some measures to put a diode between external power supply and IC power supply terminal as a protection against destroy due to reverse connection.

3) Power supply line

Due to current return generated by back electromotive force of external coil, it is recommended to put a capacitor between power supply and GND as a channel of regenerative current. When deciding capacitor value, please be careful that electrolytic capacitor value decreases at lower temperatures.

Moreover, rush current might flow momentarily by the order of turning on power supply and delay in IC with two or more power supplies. Please pay attention to capacity of power supply coupling, width and drawing of power supply and GND pattern wiring. Please make power supply lines, where large current flows, wide enough to reduce resistance of power supply patterns since resistance of power supply pattern might influence usual operation.

4) GND potential

Ensure that the GND pin is held at the Minimum potential in all operating conditions.

5) Thermal Design

Use a thermal design that allows for a sufficient margin for power dissipation (Pd) under actual operating conditions.

6) Inter-pin shorts and mounting errors

Use caution when orienting and positioning the IC for mounting on printed circuit boards. Improper mounting may result in damage to the IC. Shorts between output pins or between output pins and the power supply and GND pins caused by poor soldering or foreign objects may result in damage to the IC.

7) Operation in strong electromagnetic fields

Exercise caution when using the IC in the presence of strong electromagnetic fields as doing so may cause the IC to malfunction.

8) ASO (Area of Safety Operation)

When using this IC, do not exceed the absolute Maximum ratings and ASO of output Tr.

9) Thermal shutdown circuit (TSD)

This IC also incorporates a built-in TSD circuit for the protection from thermal destruction. The IC should be used within the specified power dissipation range. However, in the event that the IC continues to be operated in excess of its power dissipation limits, the rise in the chip's junction temperature T_j will trigger the TSD circuit, shutting off all output power elements. The circuit automatically resets itself once the junction temperature T_j drops down to normal operating temperatures. The TSD protection will only engage when the IC's absolute Maximum ratings have been exceeded; therefore, application designs should never attempt to purposely make use of the TSD function.

10) Testing on application boards

When testing the IC on an application board, connecting a capacitor directly to a low-impedance pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC’s power supply should always be turned off completely before connecting or removing it from a jig or fixture during the evaluation process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

11) IC input pins and parasitic elements

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. PN junctions are formed at the intersection of these P layers with the N layers of other elements, creating parasitic diodes and/or transistors. For example (refer to the figure below):

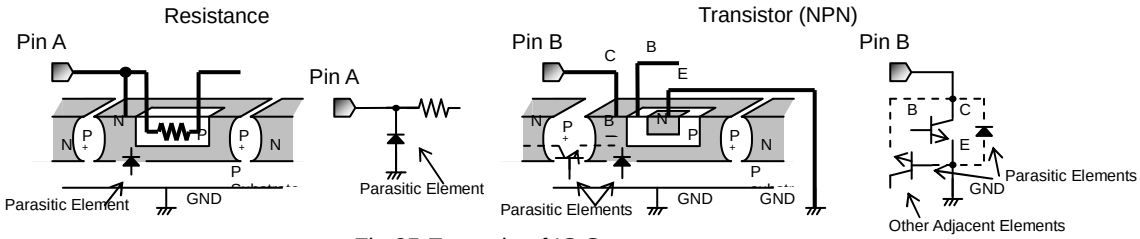


Fig.35 Example of IC Structure

- When GND > Pin A and GND > Pin B, the PN junction operates as a parasitic diode
- When GND > Pin B, the PN junction operates as a parasitic transistor

Parasitic diodes occur inevitably in the structure of the IC, and the operation of these parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Accordingly, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

12) Ground wiring patterns

When using both small-signal and large-current GND traces, the two ground traces should be routed separately but connected to a single ground potential within the application in order to avoid variations in the small-signal ground caused by large currents. Also ensure that the GND traces of external components do not cause variations on GND voltage.

Status of this document

The Japanese version of this document is formal specification. A customer may use this translation version only for a reference to help reading the formal version.

If there are any differences in translation version of this document formal version takes priority

●Ordering Information

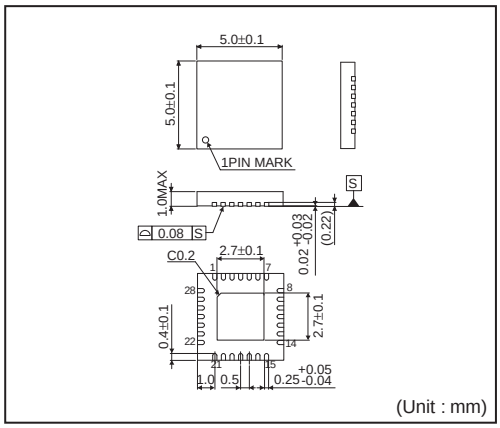
B	D	8	1	A	3	4	M	U	V	-	ME2

Package
MUV:VQFN28SV5050

Packaging
M: high reliability
E2: Embossed carrier tape

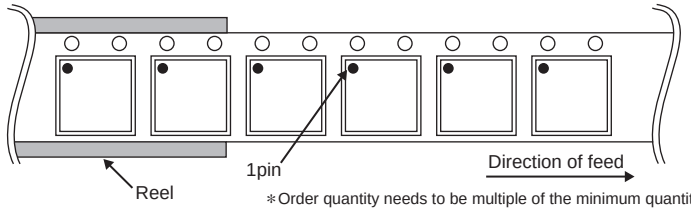
●Physical Dimension Tape and Reel Information

VQFN28SV5050



<Tape and Reel information>

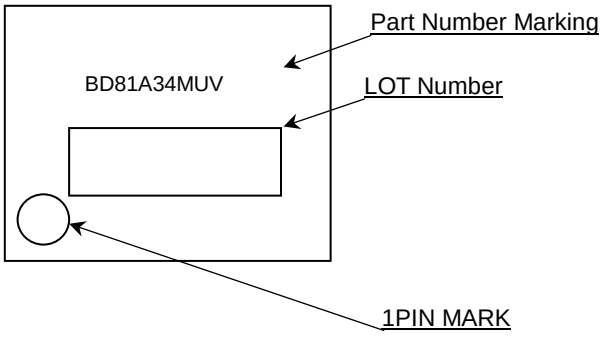
Tape	Embossed carrier tape
Quantity	2500pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



∗Order quantity needs to be multiple of the minimum quantity.

●Marking Diagram

VQFN28SV5050(TOP VIEW)



●**Revision History**

Date	Revision	Changes
13 Feb. 2013	001	New Release