

**AOL1454**  
**N-Channel Enhancement Mode Field Effect Transistor**

**General Description**

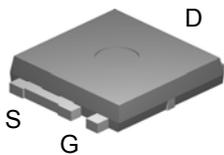
The AOL1454 uses advanced trench technology to provide excellent  $R_{DS(ON)}$ , low gate charge. It is ESD protected. This device is suitable for use as a low side switch in SMPS and general purpose applications. *Standard Product AOL1454 is Pb-free (meets ROHS & Sony 259 specifications).*

**Features**

$V_{DS}$  (V) = 40V  
 $I_D$  = 50A ( $V_{GS}$  = 10V)  
 $R_{DS(ON)}$  < 9m $\Omega$  ( $V_{GS}$  = 10V)  
 $R_{DS(ON)}$  < 13m $\Omega$  ( $V_{GS}$  = 4.5V)

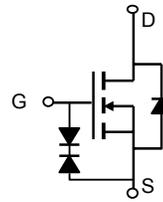
**ESD Protected**  
**UIS Tested**  
**Rg, Ciss, Coss, Crss Tested**

Ultra SO-8™ Top View



**Fits SOIC8 footprint !**

Bottom tab connected to drain


**Absolute Maximum Ratings  $T_A=25^\circ\text{C}$  unless otherwise noted**

Parameter	Symbol	Maximum	Units
Drain-Source Voltage	$V_{DS}$	40	V
Gate-Source Voltage	$V_{GS}$	$\pm 20$	V
Continuous Drain Current <sup>B</sup>	$I_D$	$T_C=25^\circ\text{C}$ <sup>H</sup>	50
		$T_C=100^\circ\text{C}$	48
Pulsed Drain Current <sup>C</sup>	$I_{DM}$	100	A
Continuous Drain Current <sup>A</sup>	$I_{DSM}$	$T_A=25^\circ\text{C}$	17
		$T_A=70^\circ\text{C}$	13
Avalanche Current <sup>C</sup>	$I_{AR}$	30	A
Repetitive avalanche energy $L=0.3\text{mH}$ <sup>C</sup>	$E_{AR}$	135	mJ
Power Dissipation <sup>B</sup>	$P_D$	$T_C=25^\circ\text{C}$	60
		$T_C=100^\circ\text{C}$	30
Power Dissipation <sup>A</sup>	$P_{DSM}$	$T_A=25^\circ\text{C}$	5.0
		$T_A=70^\circ\text{C}$	3.2
Junction and Storage Temperature Range	$T_J, T_{STG}$	-55 to 175	$^\circ\text{C}$

**Thermal Characteristics**

Parameter	Symbol	Typ	Max	Units
Maximum Junction-to-Ambient <sup>A</sup>	$R_{\theta JA}$	$t \leq 10\text{s}$	20	$^\circ\text{C/W}$
Maximum Junction-to-Ambient <sup>A</sup>		Steady-State	50	$^\circ\text{C/W}$
Maximum Junction-to-Case <sup>D</sup>	$R_{\theta JC}$	1.8	2.5	$^\circ\text{C/W}$

**Electrical Characteristics (T<sub>J</sub>=25°C unless otherwise noted)**

Symbol	Parameter	Conditions	Min	Typ	Max	Units
<b>STATIC PARAMETERS</b>						
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	I <sub>D</sub> =250μA, V <sub>GS</sub> =0V	40			V
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> =40V, V <sub>GS</sub> =0V T <sub>J</sub> =55°C			1 5	μA
I <sub>GSS</sub>	Gate-Body leakage current	V <sub>DS</sub> =0V, V <sub>GS</sub> = ±20V			±100	μA
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =250μA	1	2	3	V
I <sub>D(ON)</sub>	On state drain current	V <sub>GS</sub> =10V, V <sub>DS</sub> =5V	100			A
R <sub>DS(ON)</sub>	Static Drain-Source On-Resistance	V <sub>GS</sub> =10V, I <sub>D</sub> =20A T <sub>J</sub> =125°C		7.5 10	9.0	mΩ
		V <sub>GS</sub> =4.5V, I <sub>D</sub> =20A		10.3	13	mΩ
g <sub>FS</sub>	Forward Transconductance	V <sub>DS</sub> =5V, I <sub>D</sub> =20A		47		S
V <sub>SD</sub>	Diode Forward Voltage	I <sub>S</sub> =1A, V <sub>GS</sub> =0V		0.7	1	V
I <sub>S</sub>	Maximum Body-Diode Continuous Current				50	A
<b>DYNAMIC PARAMETERS</b>						
C <sub>iss</sub>	Input Capacitance			1600	1920	pF
C <sub>oss</sub>	Output Capacitance	V <sub>GS</sub> =0V, V <sub>DS</sub> =20V, f=1MHz		320		pF
C <sub>rss</sub>	Reverse Transfer Capacitance			100		pF
R <sub>g</sub>	Gate resistance	V <sub>GS</sub> =0V, V <sub>DS</sub> =0V, f=1MHz		3.4		Ω
<b>SWITCHING PARAMETERS</b>						
Q <sub>g</sub> (10V)	Total Gate Charge			22		nC
Q <sub>g</sub> (4.5V)	Total Gate Charge	V <sub>GS</sub> =10V, V <sub>DS</sub> =20V, I <sub>D</sub> =20A		10.5		nC
Q <sub>gs</sub>	Gate Source Charge			4.2		nC
Q <sub>gd</sub>	Gate Drain Charge			4.8		nC
t <sub>D(on)</sub>	Turn-On Delay Time			6.5		ns
t <sub>r</sub>	Turn-On Rise Time	V <sub>GS</sub> =10V, V <sub>DS</sub> =20V, R <sub>L</sub> =1Ω,		12.5		ns
t <sub>D(off)</sub>	Turn-Off Delay Time	R <sub>GEN</sub> =3Ω		33		ns
t <sub>f</sub>	Turn-Off Fall Time			16		ns
t <sub>rr</sub>	Body Diode Reverse Recovery Time	I <sub>F</sub> =20A, dI/dt=100A/μs		31		ns
Q <sub>rr</sub>	Body Diode Reverse Recovery Charge	I <sub>F</sub> =20A, dI/dt=100A/μs		33		nC

A: The value of R<sub>θJA</sub> is measured with the device in a still air environment with T<sub>A</sub>=25°C. The power dissipation P<sub>D</sub> and current rating I<sub>D</sub> are based on T<sub>J(MAX)</sub>=150°C, using t ≤ 10s junction-to-ambient thermal resistance.

B: The power dissipation PD is based on T<sub>J(MAX)</sub>=175°C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.

C: Repetitive rating, pulse width limited by junction temperature T<sub>J(MAX)</sub>=175°C.

D: The R<sub>θJA</sub> is the sum of the thermal impedance from junction to case R<sub>θJC</sub> and case to ambient.

E: The static characteristics in Figures 1 to 6 are obtained using <300 μs pulses, duty cycle 0.5% max.

F: These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of T<sub>J(MAX)</sub>=175°C. The SOA curve provides a single pulse rating.

G: These tests are performed with the device mounted on 1 in 2 FR-4 board with 2oz. Copper, in a still air environment with T<sub>A</sub>=25°C.

H: The maximum current rating is limited by bond-wires.

Rev0: Oct 2006

THIS PRODUCT HAS BEEN DESIGNED AND QUALIFIED FOR THE CONSUMER MARKET. APPLICATIONS OR USES AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS ARE NOT AUTHORIZED. AOS DOES NOT ASSUME ANY LIABILITY ARISING OUT OF SUCH APPLICATIONS OR USES OF ITS PRODUCTS. AOS RESERVES THE RIGHT TO IMPROVE PRODUCT DESIGN, FUNCTIONS AND RELIABILITY WITHOUT NOTICE.

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

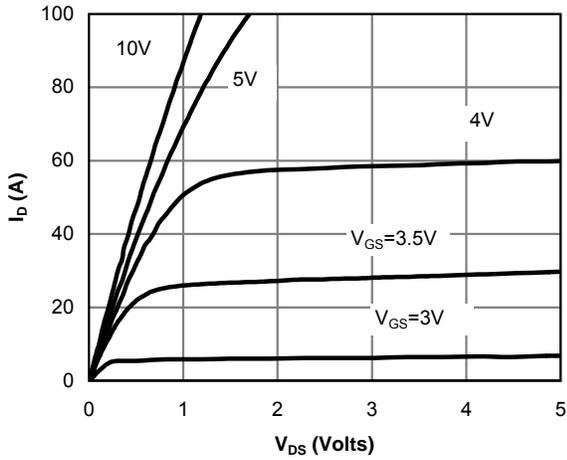


Figure 1: On-Region Characteristics

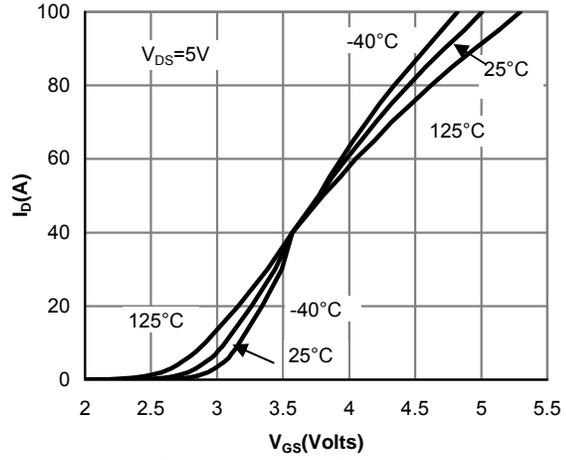


Figure 2: Transfer Characteristics

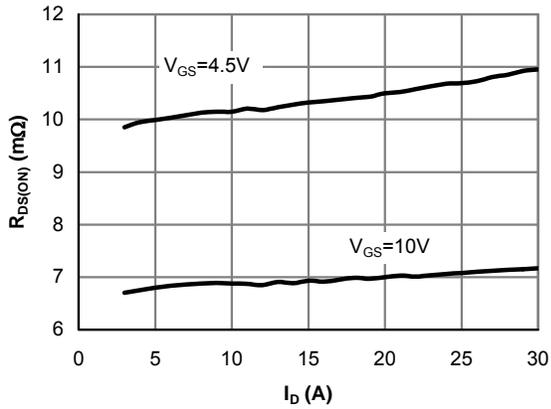


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

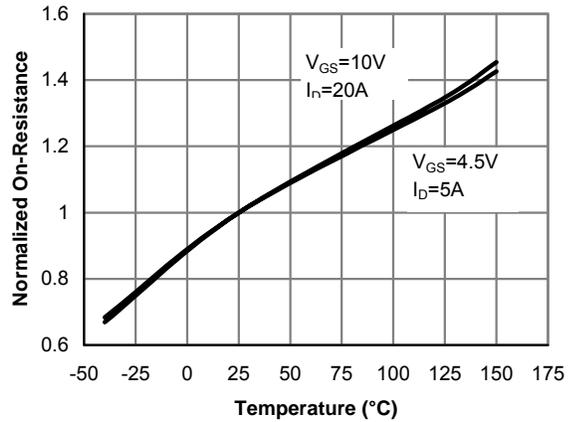


Figure 4: On-Resistance vs. Junction Temperature

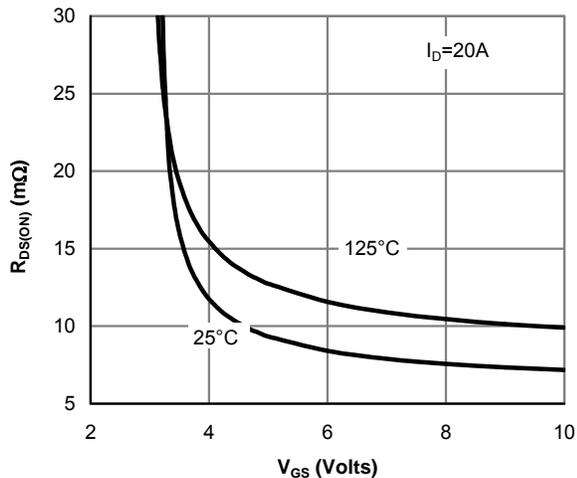


Figure 5: On-Resistance vs. Gate-Source Voltage

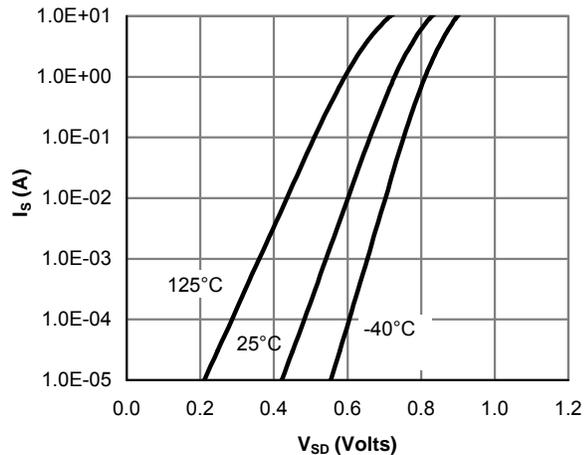


Figure 6: Body-Diode Characteristics

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

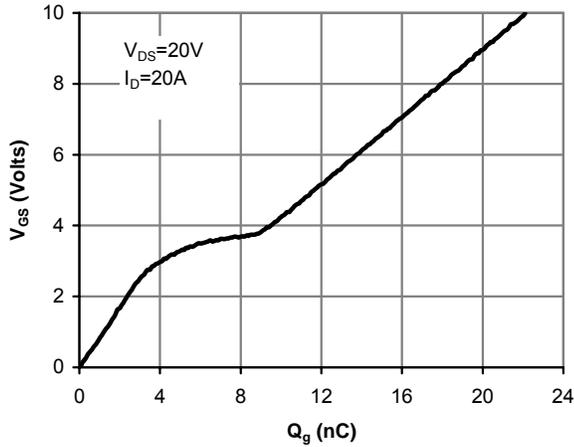


Figure 7: Gate-Charge Characteristics

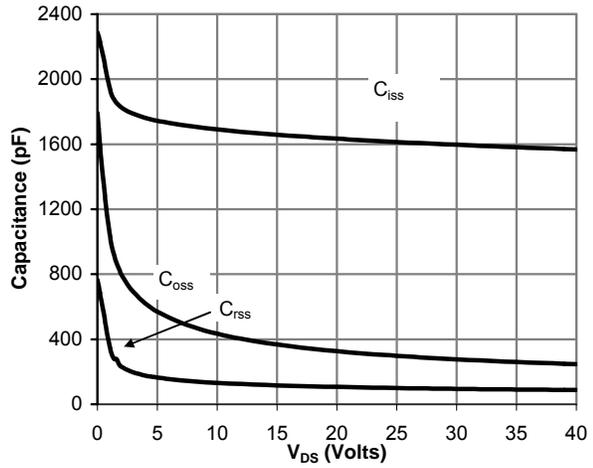


Figure 8: Capacitance Characteristics

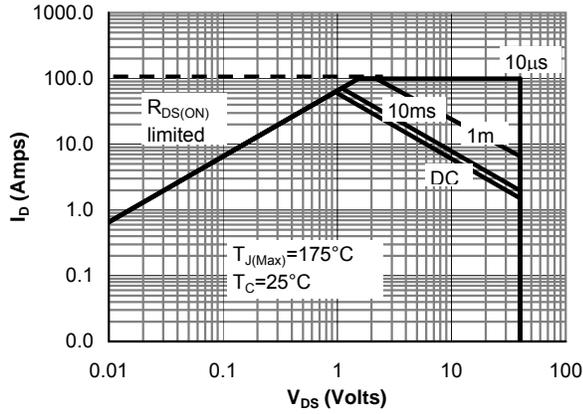


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

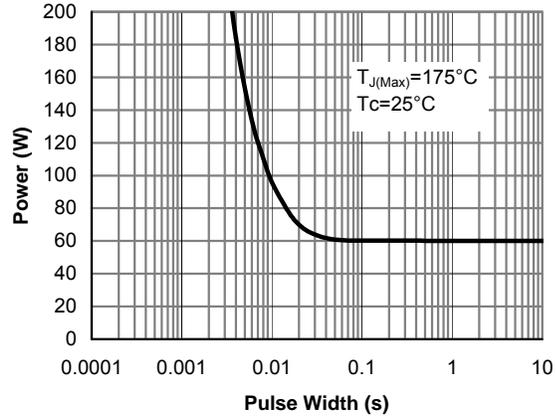


Figure 10: Single Pulse Power Rating Junction-to-Case (Note F)

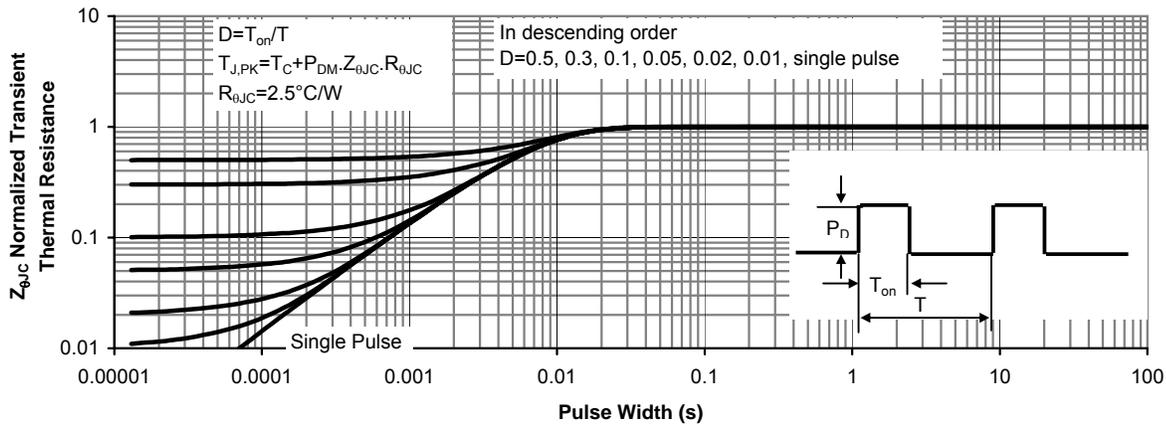


Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

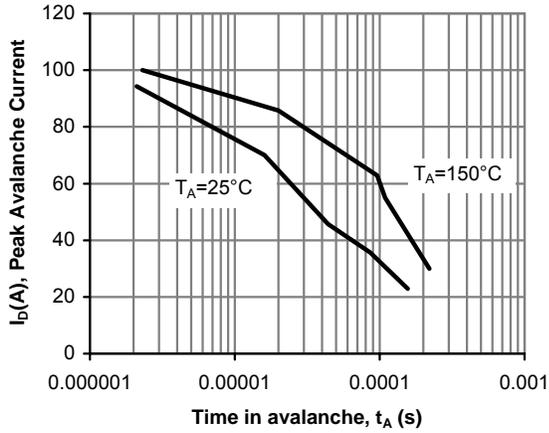


Figure 12: Single Pulse Avalanche capability

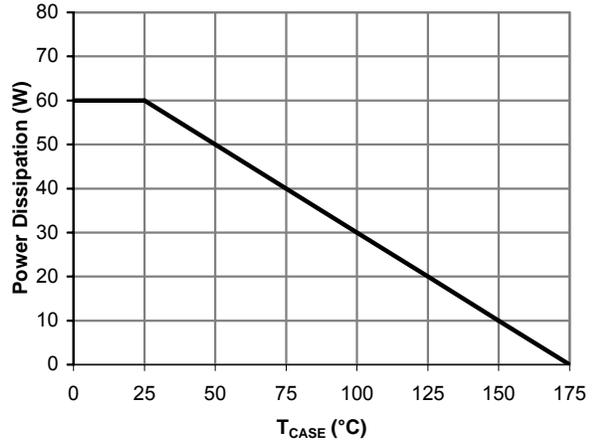


Figure 13: Power De-rating (Note B)

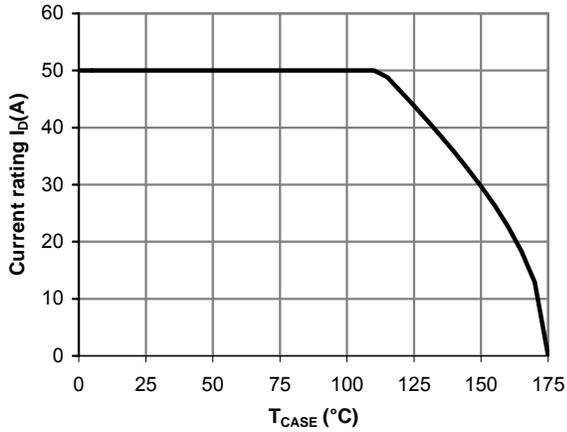


Figure 14: Current De-rating (Note B)

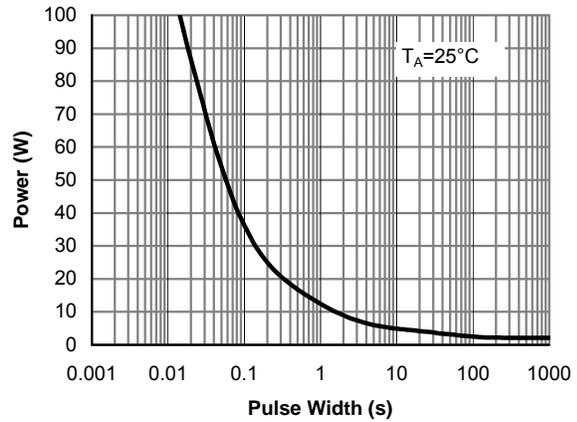


Figure 15: Single Pulse Power Rating Junction-to-Ambient (Note G)

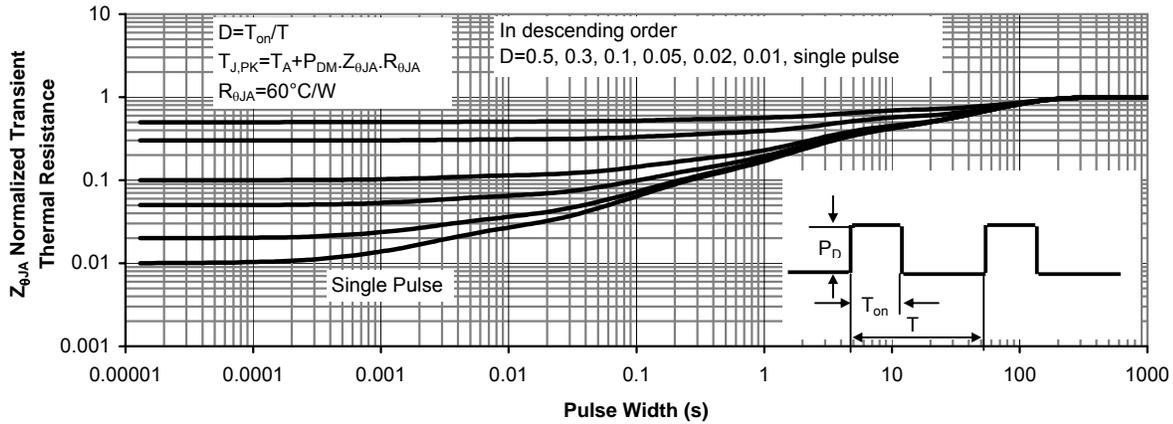


Figure 16: Normalized Maximum Transient Thermal Impedance (Note G)