

- Member of the Texas Instruments Widebus™ Family
- UBT™ Transceiver Combines D-Type Latches and D-Type Flip-Flops for Operation in Transparent, Latched, or Clocked Mode
- Operates From 1.65 V to 3.6 V
- Max t_{pd} of 4.4 ns at 3.3 V
- ± 24 -mA Output Drive at 3.3 V
- Simultaneously Generates and Checks Parity
- Option to Select Generate Parity and Check or Feed-Through Data/Parity in A-to-B or B-to-A Directions
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)

description/ordering information

This 18-bit (dual-octal) noninverting registered transceiver is designed for 1.65-V to 3.6-V V_{CC} operation.

The SN74ALVCH16901 is a dual 9-bit to dual 9-bit parity transceiver with registers. The device can operate as a feed-through transceiver or it can generate/check parity from the two 8-bit data buses in either direction.

The SN74ALVCH16901 features independent clock (CLKAB or CLKBA), latch-enable (LEAB or LEBA), and dual 9-bit clock-enable (CLKENAB or CLKENBA) inputs. It also provides parity-enable (SEL) and parity-select (ODD/EVEN) inputs and separate error-signal (ERRA or ERRB) outputs for checking parity. The direction of data flow is controlled by OEAB and OEBA. When SEL is low, the parity functions are enabled. When SEL is high, the parity functions are disabled, and the device acts as an 18-bit registered transceiver.

ORDERING INFORMATION

T _A	PACKAGE [†]	ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 85°C	TSSOP – DGG	Tape and reel	SN74ALVCH16901DGGR

[†] Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

DGG PACKAGE (TOP VIEW)	
1CLKENAB	1 64 1CLKENBA
LEAB	2 63 LEBA
CLKAB	3 62 CLKBA
1ERRA	4 61 1ERRB
1APAR	5 60 1BPAR
GND	6 59 GND
1A1	7 58 1B1
1A2	8 57 1B2
1A3	9 56 1B3
V _{CC}	10 55 V _{CC}
1A4	11 54 1B4
1A5	12 53 1B5
1A6	13 52 1B6
GND	14 51 GND
1A7	15 50 1B7
1A8	16 49 1B8
2A1	17 48 2B1
2A2	18 47 2B2
GND	19 46 GND
2A3	20 45 2B3
2A4	21 44 2B4
2A5	22 43 2B5
V _{CC}	23 42 V _{CC}
2A6	24 41 2B6
2A7	25 40 2B7
2A8	26 39 2B8
GND	27 38 GND
2APAR	28 37 2BPAR
2ERRA	29 36 2ERRB
OEAB	30 35 OEBA
SEL	31 34 ODD/EVEN
2CLKENAB	32 33 2CLKENBA



description/ordering information (continued)

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The A and B I/Os and APAR and BPAR inputs have bus-hold circuitry. Active bus-hold circuitry holds unused or undriven data inputs at a valid logic state. Use of pullup or pulldown resistors with the bus-hold circuitry is not recommended.

Function Tables

FUNCTION[†]

INPUTS					OUTPUT B
CLKENAB	OEAB	LEAB	CLKAB	A	
X	H	X	X	X	Z
X	L	H	X	L	L
X	L	H	X	H	H
H	L	L	X	X	B_0^{\ddagger}
L	L	L	↑	L	L
L	L	L	↑	H	H
L	L	L	L	X	B_0^{\ddagger}
L	L	L	H	X	$B_0^{\$}$

[†] A-to-B data flow is shown; B-to-A flow is similar, but uses OEBA, LEBA, and CLKENBA.

[‡] Output level before the indicated steady-state input conditions were established

[§] Output level before the indicated steady-state input conditions were established, provided that CLKAB was low before LEAB went low

PARITY ENABLE

INPUTS			OPERATION OR FUNCTION	
SEL	OEBA	OEAB		
L	H	L	Parity is checked on port A and is generated on port B.	
L	L	H	Parity is checked on port B and is generated on port A.	
L	H	H	Parity is checked on port B and port A.	
L	L	L	Parity is generated on port A and B if device is in FF mode.	
H	L	L	Parity functions are disabled; device acts as a standard 18-bit registered transceiver.	Q _A data to B, Q _B data to A Q _B data to A Q _A data to B Isolation
H	L	H		
H	H	L		
H	H	H		

Function Tables (Continued)

PARITY

INPUTS								OUTPUTS			
SEL	OEBA	OEAB	ODD/EVEN	Σ OF INPUTS A1–A8 = H	Σ OF INPUTS B1–B8 = H	APAR	BPAR	APAR	ERRA	BPAR	ERRB
L	H	L	L	0, 2, 4, 6, 8	N/A	L	N/A	N/A	H	L	Z
L	H	L	L	1, 3, 5, 7	N/A	L	N/A	N/A	L	H	Z
L	H	L	L	0, 2, 4, 6, 8	N/A	H	N/A	N/A	L	L	Z
L	H	L	L	1, 3, 5, 7	N/A	H	N/A	N/A	H	H	Z
L	L	H	L	N/A	0, 2, 4, 6, 8	N/A	L	L	Z	N/A	H
L	L	H	L	N/A	1, 3, 5, 7	N/A	L	H	Z	N/A	L
L	L	H	L	N/A	0, 2, 4, 6, 8	N/A	H	L	Z	N/A	L
L	L	H	L	N/A	1, 3, 5, 7	N/A	H	H	Z	N/A	H
L	H	L	H	0, 2, 4, 6, 8	N/A	L	N/A	N/A	L	H	Z
L	H	L	H	1, 3, 5, 7	N/A	L	N/A	N/A	H	L	Z
L	H	L	H	0, 2, 4, 6, 8	N/A	H	N/A	N/A	H	H	Z
L	H	L	H	1, 3, 5, 7	N/A	H	N/A	N/A	L	L	Z
L	L	H	H	N/A	0, 2, 4, 6, 8	N/A	L	H	Z	N/A	L
L	L	H	H	N/A	1, 3, 5, 7	N/A	L	L	L	Z	N/A
L	L	H	H	N/A	0, 2, 4, 6, 8	N/A	H	H	Z	N/A	H
L	L	H	H	N/A	1, 3, 5, 7	N/A	H	L	Z	N/A	L
L	H	H	L	0, 2, 4, 6, 8	0, 2, 4, 6, 8	L	L	Z	H	Z	H
L	H	H	L	1, 3, 5, 7	1, 3, 5, 7	L	L	Z	L	Z	L
L	H	H	L	0, 2, 4, 6, 8	0, 2, 4, 6, 8	H	H	Z	L	Z	L
L	H	H	L	1, 3, 5, 7	1, 3, 5, 7	H	H	Z	H	Z	H
L	H	H	H	0, 2, 4, 6, 8	0, 2, 4, 6, 8	L	L	Z	L	Z	L
L	H	H	H	1, 3, 5, 7	1, 3, 5, 7	L	L	Z	H	Z	H
L	H	H	H	0, 2, 4, 6, 8	0, 2, 4, 6, 8	H	H	Z	H	Z	H
L	H	H	H	1, 3, 5, 7	1, 3, 5, 7	H	H	Z	L	Z	L
L	L	L	L	N/A	N/A	N/A	N/A	PE [†]	Z	PE [†]	Z
L	L	L	H	N/A	N/A	N/A	N/A	PO [‡]	Z	PO [‡]	Z

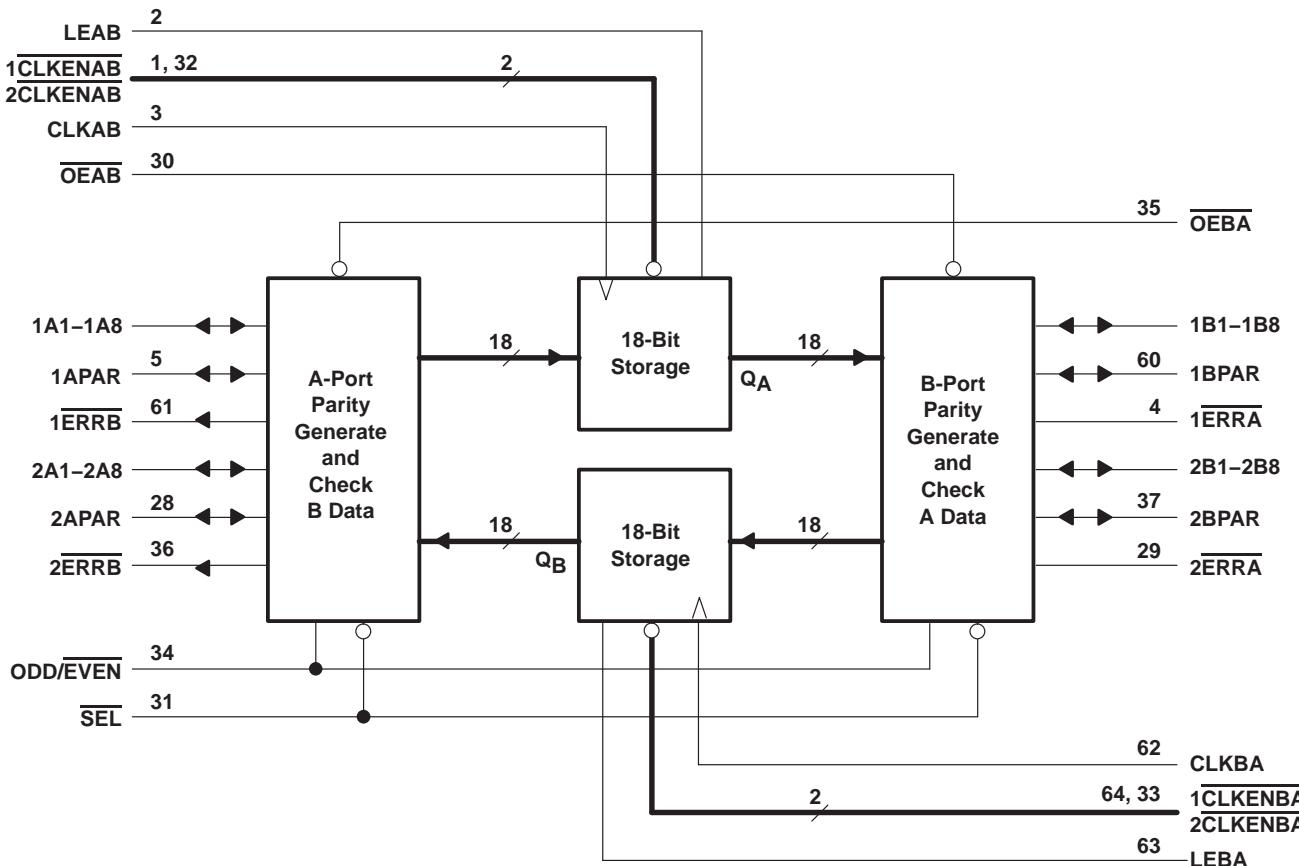
[†] Parity output is set to the level so that the specific bus side is set to even parity.

[‡] Parity output is set to the level so that the specific bus side is set to odd parity.

SN74ALVCH16901
18-BIT UNIVERSAL BUS TRANSCEIVER
WITH PARITY GENERATORS/CHECKERS

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functional block diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	-0.5 V to 4.6 V
Input voltage range, V_I : Except I/O ports (see Note 1)	-0.5 V to 4.6 V
I/O ports (see Notes 1 and 2)	-0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Notes 1 and 2)	-0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$)	-50 mA
Output clamp current, I_{OK} ($V_O < 0$)	-50 mA
Continuous output current, I_O	±50 mA
Continuous current through each V_{CC} or GND	±100 mA
Package thermal impedance, θ_{JA} (see Note 3)	55°C/W
Storage temperature range, T_{stg}	-65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed..
2. This value is limited to 4.6 V maximum.
3. The package thermal impedance is calculated in accordance with JEDEC 51-7.

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recommended operating conditions (see Note 4)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	1.65	3.6	V
V_{IH}	High-level input voltage	$V_{CC} = 1.65\text{ V to }1.95\text{ V}$	$0.65 \times V_{CC}$	V
		$V_{CC} = 2.3\text{ V to }2.7\text{ V}$	1.7	
		$V_{CC} = 2.7\text{ V to }3.6\text{ V}$	2	
V_{IL}	Low-level input voltage	$V_{CC} = 1.65\text{ V to }1.95\text{ V}$	$0.35 \times V_{CC}$	V
		$V_{CC} = 2.3\text{ V to }2.7\text{ V}$	0.7	
		$V_{CC} = 2.7\text{ V to }3.6\text{ V}$	0.8	
V_I	Input voltage	0	V_{CC}	V
V_O	Output voltage	0	V_{CC}	V
I_{OH}	High-level output current	$V_{CC} = 1.65\text{ V}$	-4	mA
		$V_{CC} = 2.3\text{ V}$	-12	
		$V_{CC} = 2.7\text{ V}$	-12	
		$V_{CC} = 3\text{ V}$	-24	
I_{OL}	Low-level output current	$V_{CC} = 1.65\text{ V}$	4	mA
		$V_{CC} = 2.3\text{ V}$	12	
		$V_{CC} = 2.7\text{ V}$	12	
		$V_{CC} = 3\text{ V}$	24	
$\Delta t/\Delta v$	Input transition rise or fall rate		10	ns/V
T_A	Operating free-air temperature	-40	85	°C

NOTE 4: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	MIN	TYP [†]	MAX	UNIT
V _{OH}	I _{OH} = -100 μ A	1.65 V to 3.6 V	V _{CC} – 0.2			V
	I _{OH} = -4 mA	1.65 V		1.2		
	I _{OH} = -6 mA	2.3 V		2		
	I _{OH} = -12 mA	2.3 V		1.7		
		2.7 V		2.2		
		3 V		2.4		
	I _{OH} = -24 mA	3 V		2		
V _{OL}	I _{OL} = 100 μ A	1.65 V to 3.6 V		0.2		V
	I _{OL} = 4 mA	1.65 V		0.45		
	I _{OL} = 6 mA	2.3 V		0.4		
	I _{OL} = 12 mA	2.3 V		0.7		
		2.7 V		0.4		
		3 V		0.55		
I _I	V _I = V _{CC} or GND	3.6 V		\pm 5		μ A
I _{I(hold)}	V _I = 0.58 V	1.65 V		25		μ A
	V _I = 1.07 V	1.65 V		-25		
	V _I = 0.7 V	2.3 V		45		
	V _I = 1.7 V	2.3 V		-45		
	V _I = 0.8 V	3 V		75		
	V _I = 2 V	3 V		-75		
	V _I = 0 to 3.6 V [‡]	3.6 V		\pm 500		
I _{OZ} [§]	V _O = V _{CC} or GND	3.6 V		\pm 10		μ A
I _{CC}	V _I = V _{CC} or GND, I _O = 0	3.6 V		40		μ A
Δ I _{CC}	One input at V _{CC} – 0.6 V, Other inputs at V _{CC} or GND	3 V to 3.6 V		750		μ A
C _i	Control inputs V _I = V _{CC} or GND	3.3 V		3		pF
C _{io}	A or B ports V _O = V _{CC} or GND	3.3 V		7.5		pF
C _o	ERR ports V _O = V _{CC} or GND	3.3 V		6		pF

[†] All typical values are at V_{CC} = 3.3 V, T_A = 25°C.[‡] This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.[§] For I/O ports, the parameter I_{OZ} includes the input leakage current.

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timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

		$V_{CC} = 1.8\text{ V}$		$V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$		$V_{CC} = 2.7\text{ V}$		$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency		†		125		125		125	MHz
t_w	Pulse duration	CLK↑	†	3	3	3	3	ns		
		LE high	†	3	3	3	3			
t_{su}	Setup time	A, APAR or B, BPAR before CLK↑	†	1.9	2	1.7	1.7	ns		
		<u>CLKEN</u> before CLK↑	†	2.1	2.1	1.7	1.7			
		A, APAR or B, BPAR before LE↓	†	1.4	1.3	1.2	1.2			
t_h	Hold time	A, APAR or B, BPAR after CLK↑	†	0.4	0.4	0.5	0.5	ns		
		<u>CLKEN</u> after CLK↑	†	0.5	0.5	0.7	0.7			
		A, APAR or B, BPAR after LE↓	†	0.9	1.1	0.9	0.9			

† This information was not available at the time of publication.

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switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 1.8 V		V _{CC} = 2.5 V ± 0.2 V		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		
			MIN	TYP	MIN	MAX	MIN	MAX	MIN	MAX	
f _{max}			†		125		125		125	MHz	
t _{pd}	A or B	B or A	†		1	5.2		4.8	1	4.4	
		BPAR or APAR	†		2	8.9		7.6	2	6.7	
	APAR or BPAR	BPAR or APAR	†		1	5.7		5.2	1	4.7	
		ERRA or ERRB	†		2	9.7		8.7	2	7.5	
	ODD/EVEN	ERRA or ERRB	†		1.5	8.7		7.9	1.5	6.8	
		BPAR or APAR	†		1.5	8.3		7.6	1.5	6.5	
	SEL	BPAR or APAR	†		1	6.1		5.9	1	5.1	
	CLKAB or CLKBA	A or B	†		1	6.4		5.8	1	5.1	
		BPAR or APAR parity feed through	†		1.5	7.1		6.3	1.5	5.6	
		BPAR or APAR parity generated	†		2.5	10.2		8.7	2	7.7	
		ERRA or ERRB	†		2.5	10.5		8.9	2	7.9	
	LEAB or LEBA	A or B	†		1	6		5.5	1	4.8	
		BPAR or APAR parity feed through	†		1.5	6.7		6	1.5	5.3	
		BPAR or APAR parity generated	†		2.5	9.8		8.3	2	7.4	
		ERRA or ERRB	†		2.5	9.9		8.5	2	7.5	
t _{en}	OEAB or Oeba	B, BPAR or A, APAR	†		1.4	6.3		6.1	1	5.3	ns
t _{dis}	OEAB or Oeba	B, BPAR or A, APAR	†		1.3	6.1		5.2	1.5	4.9	ns
t _{en}	OEAB or Oeba	ERRA or ERRB	†		1.4	6.2		5.5	1	4.9	ns
t _{dis}	OEAB or Oeba	ERRA or ERRB	†		1.3	7.3		6.5	1	5.7	ns
t _{en}	SEL	ERRA or ERRB	†		1.4	6.7		6.5	1	5.5	ns
t _{dis}	SEL	ERRA or ERRB	†		1.3	6.4		5.4	1.5	4.9	ns

† This information was not available at the time of publication.

operating characteristics, T_A = 25°C

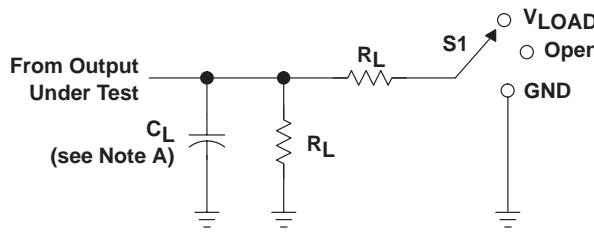
PARAMETER	TEST CONDITIONS	V _{CC} = 1.8 V			V _{CC} = 2.5 V			V _{CC} = 3.3 V		
		TYP	TYP	TYP	TYP	TYP	TYP	TYP	TYP	
C _{pd}	Power dissipation capacitance	Outputs enabled	C _L = 50 pF, f = 10 MHz	†	22		27			pF
		Outputs disabled		†	5		8			

† This information was not available at the time of publication.



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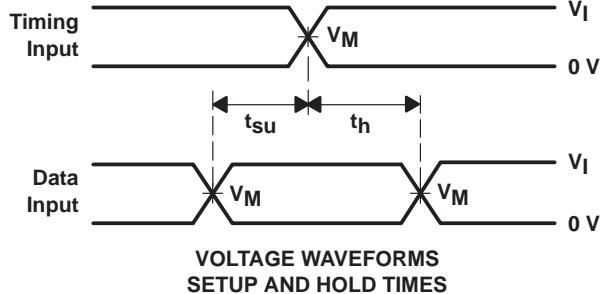
PARAMETER MEASUREMENT INFORMATION



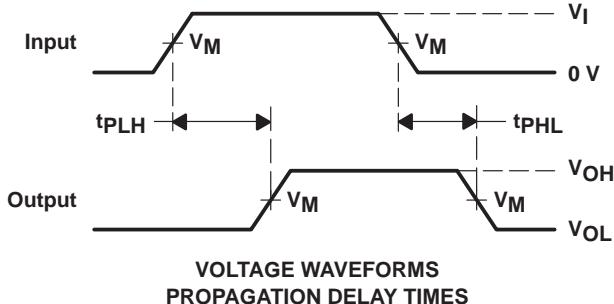
TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	V_{LOAD}
t_{PHZ}/t_{PZH}	GND

LOAD CIRCUIT

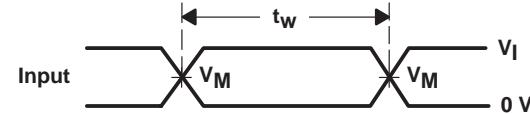
V _{CC}	INPUT		V _M	V _{LOAD}	C _L	R _L	V _Δ
	V _I	t _r /t _f					
1.8 V	V _{CC}	≤2 ns	V _{CC} /2	2 × V _{CC}	30 pF	1 kΩ	0.15 V
2.5 V ± 0.2 V	V _{CC}	≤2 ns	V _{CC} /2	2 × V _{CC}	30 pF	500 Ω	0.15 V
2.7 V	2.7 V	≤2.5 ns	1.5 V	6 V	50 pF	500 Ω	0.3 V
3 V ± 0.3 V	2.7 V	≤2.5 ns	1.5 V	6 V	50 pF	500 Ω	0.3 V



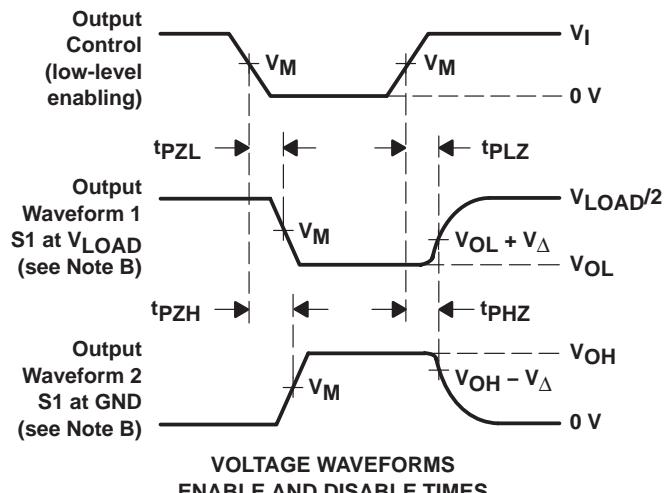
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES:

- A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω.
- D. The outputs are measured one at a time, with one transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
- F. t_{PZL} and t_{PZH} are the same as t_{en}.
- G. t_{PLH} and t_{PHL} are the same as t_{pd}.
- H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
74ALVCH16901DGGRE4	ACTIVE	TSSOP	DGG	64	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74ALVCH16901DGGRG4	ACTIVE	TSSOP	DGG	64	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALVCH16901DGGR	ACTIVE	TSSOP	DGG	64	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBsolete: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

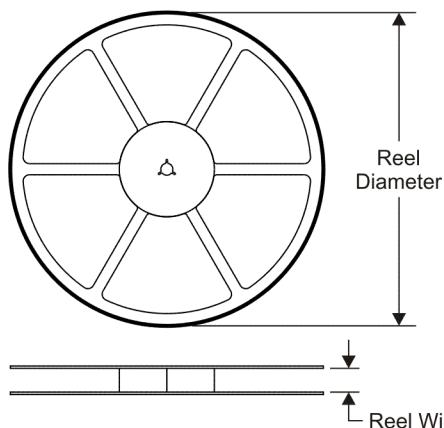
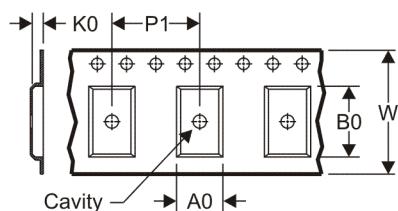
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

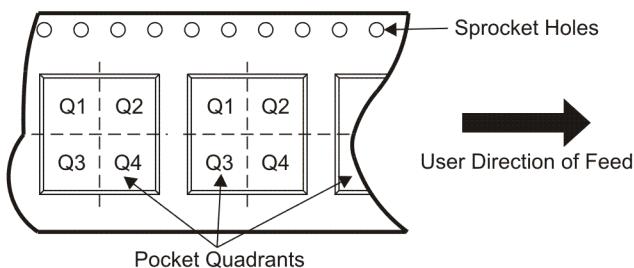
⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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TAPE AND REEL INFORMATION
REEL DIMENSIONS

TAPE DIMENSIONS


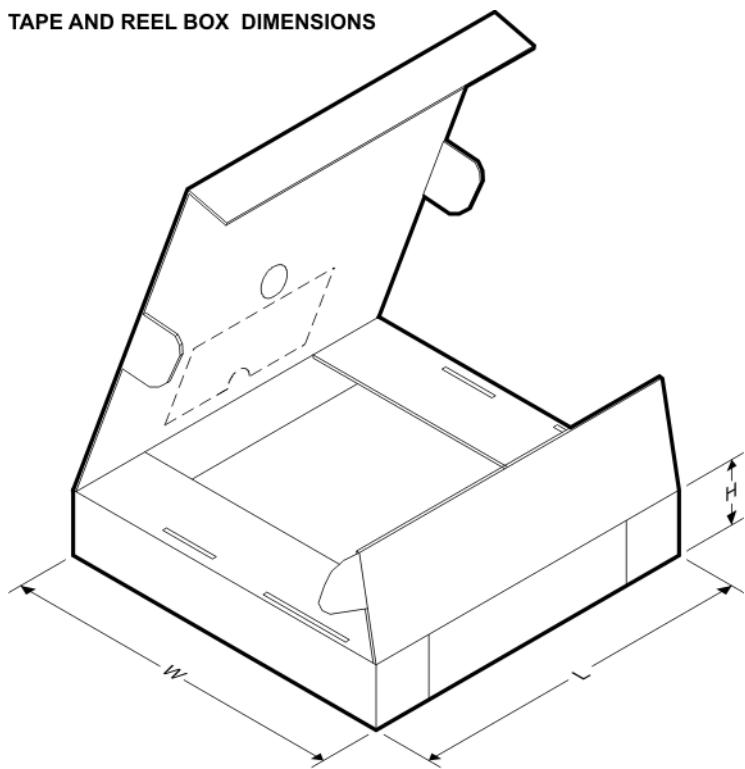
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74ALVCH16901DGGR	TSSOP	DGG	64	2000	330.0	24.4	8.4	17.3	1.7	12.0	24.0	Q1

TAPE AND REEL BOX DIMENSIONS



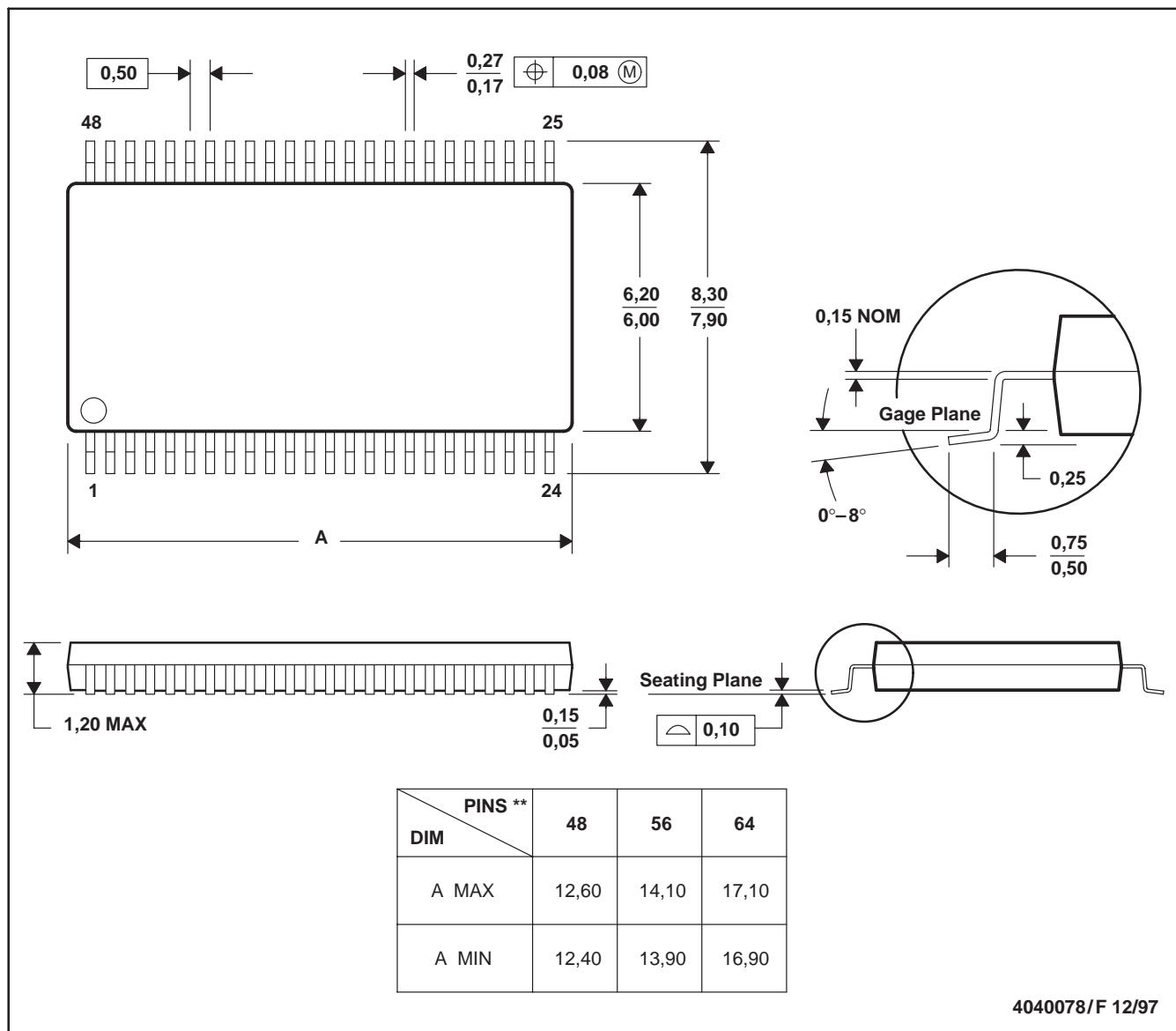
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74ALVCH16901DGGR	TSSOP	DGG	64	2000	346.0	346.0	41.0

DGG (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

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