CA3274

Current Limiting Power Switch with Current Limiter Sense Flag

April 1994

Features

- **Drive-Current Limiting at Output**
- **Current-Sense Buffer and Reference**
- **200mA Driver Current Capability**
- **Logic-Level Control Input**
- **Current Limiting Flag Output**
- **50dB Minimum PSRR**
- **5μs Typical Switch Time**
- **Separate Signal and Power Grounds**

Applications

- **Solenoid Switch Driver**
- **Relay Driver**
- **Lamp Control Switch**
- **Ignition Coil Pre-Driver**
- **Constant Current Driver**
- **Current Limiting Switch**
- **Fault Output Sense Appliance**
- **Power Supply Fault Mode Control**

Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
CA3274E	-40°C to +85°C	8 Lead Plastic DIP

Description

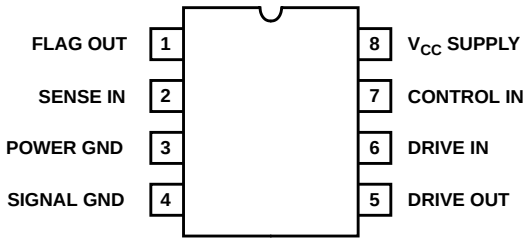
The CA3274 is a controlled current switch and may be used in general purpose switching applications that require specified maximum levels of current. The functional block diagram of the CA3274 is shown and a typical application circuit is shown in Figure 1. An internal emitter follower has 200mA of source drive output capability. The Control Input is a Schmitt trigger buffer amplifier for noise immunity in the environments typical of industrial and automotive control systems.

Current sensing in the emitter circuit of a power-darlington output stage is fed back from a sampling resistor to the sense input of the CA3274 which has a 335mV typical offset. For the example shown in Figure 1, a sampling resistor of 0.056Ω permits 6.0A (0.335/0.056) of current in the emitter of the output driver. When the current limiter is activated, the flag output changes state conditionally. If the control input is the “0” state, the flag output will remain in a “1” state. If the control input is in the “1” state and the sense input is less than the voltage reference level of 335mV, the flag output will remain in the “1” state. If the control input is the “1” state and the sense input is equal to or greater than the 335mV reference level, the flag output goes to the “0” state. The output flag switch may be used to accurately establish dwell timing in automotive applications. When the control input goes to “0”, the flag is reset to “1”. Noise-immunity hold-off is used to prevent pre-triggering of the flag output and is noted as t_D in the timing diagram of Figure 2.

The flag output may be used for diagnostic feedback via the current sense input to detect a fault mode. In this case the sampled drive current is either from the emitter of the CA3274 internal power transistor or an external output amplifier, such as a darlington power transistor or power-FET output stage. The CA3274 has separate power and signal grounds to minimize transient-loop feedback to the input ground and thus prevent false triggering of the output. Optionally, the output from the CA3274 may be taken from the open collector (DRIVE IN) at pin 6. An external resistor at pin 6 may be used to set the level at which Q2 will saturate, providing additional limiting protection for the maximum forward-drive from the CA3274.

Pinout

CA3274 (PDIP)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge; follow proper IC Handling Procedures.

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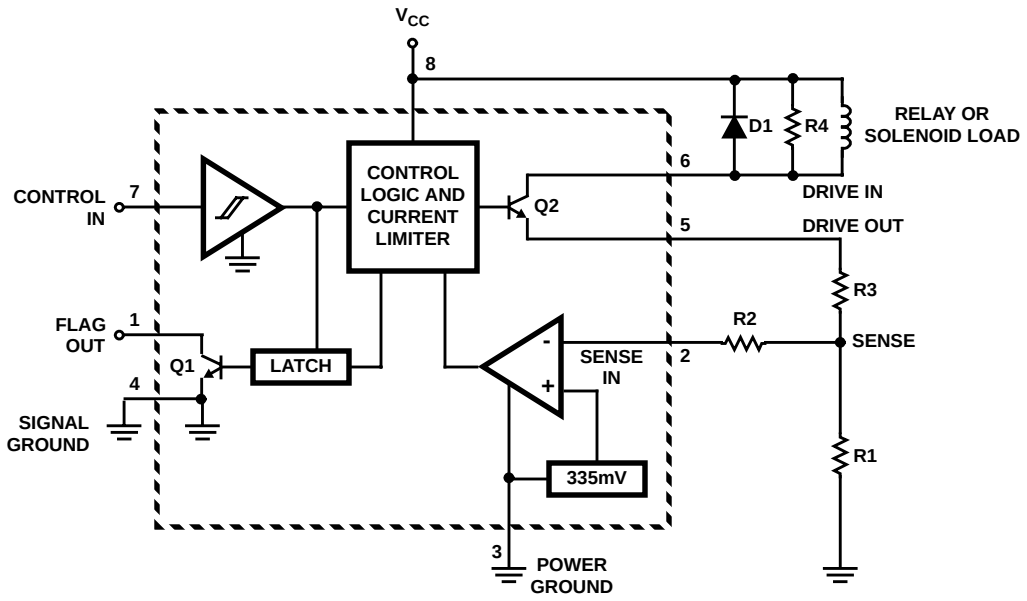
Block Diagram



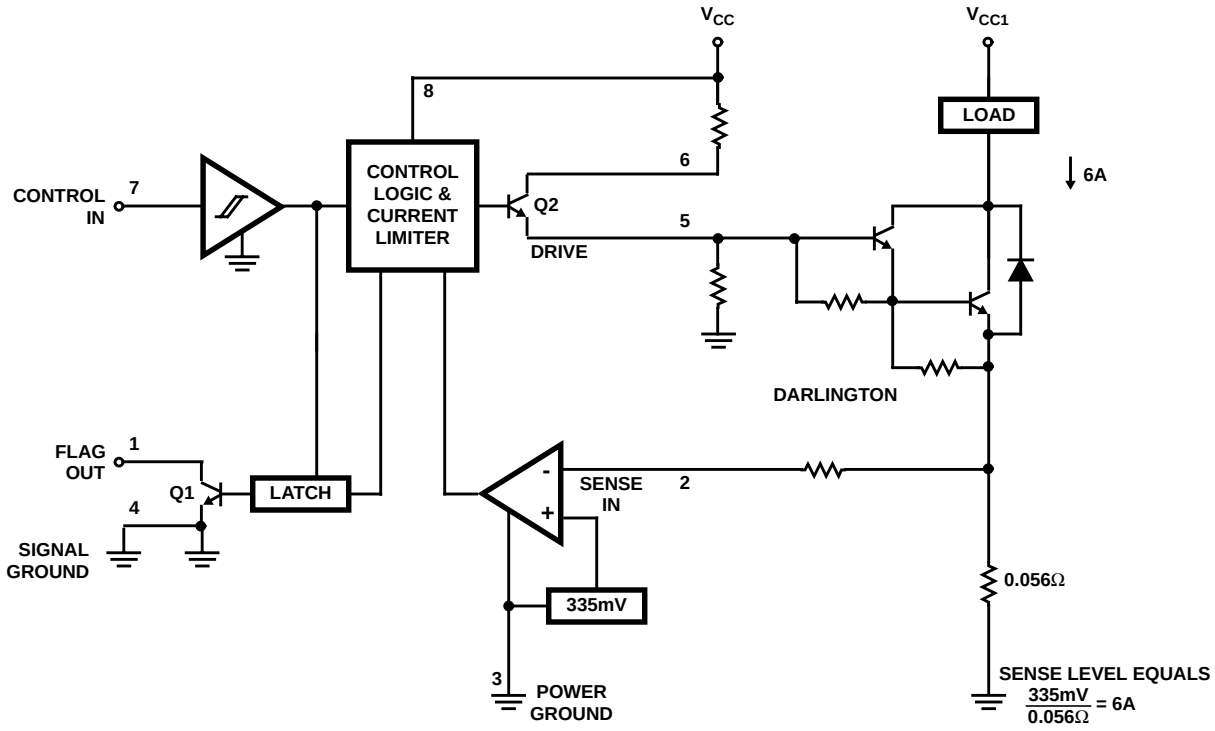


FIGURE 1. TYPICAL APPLICATION AS A POWER SWITCH PRE-DRIVER SWITCH

Absolute Maximum Ratings

Operating Drive Supply, V_{CC} 16V
Maximum Output Current, I_O 200mA
Control, Sense Input. . . . . Gnd - 0.5V, V_{CC} + 0.5V
Signal, Power Differential Ground Voltage. . . . . ±1V

Thermal Information

Thermal Resistance θ_{JA}
Plastic DIP Package 8 Lead . . . . . 130^{o}C/W
Power Dissipation, P_D
Up to 70^{o}C. 630mW
Above 70^{o}C . . . . . Derate linearly at 7.7mW/^{o}C
Operating Temperature Range . . . . . -40^{o}C to +85^{o}C
Storage Temperature Range. . . . . -55^{o}C to +150^{o}C
Lead Temperature (During Soldering)
At distance 1/16in. (1.59mm ± 0.79mm) from
case for 10s Max. . . . . +265^{o}C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

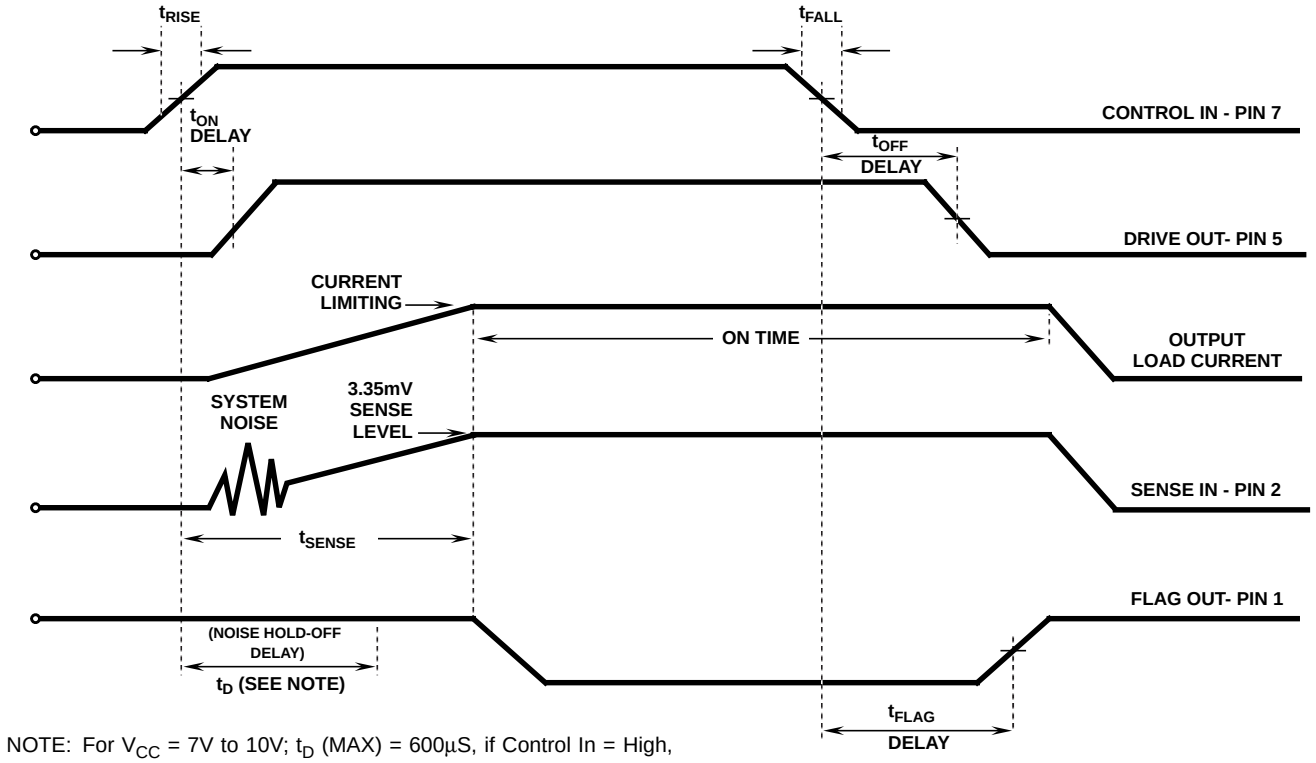
Electrical Specifications

At T_A = -40^{o}C to +85^{o}C, Unless Otherwise Specified

PARAMETERS	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Power Supply Current: S1 = 2	I_{CCH}	Control = High (Output On)	-	-	25	mA
	I_{CCL}	Control = Low (Output Off)	-	-	5	mA
Control Input: S1 = 3	V_{THDH}	Thd. Voltage, High	-	-	3.5	V
	V_{THDL}	Thd. Voltage, Low	0.9	-	-	V
	V_{THDH}-V_{THDL}	Hysteresis	0.4	0.65	2.0	V
	I_{IL}	Leakage, 0.0 to 5.5V	-20	-	+20	µA
Driver In, Out (Pin 6, 5): S1 = 3	V_{SAT}	Output Saturation Voltage, I_{CC1} = 200mA, $V_{CONTROL}$ = High	-	-	0.5	V
	I_{LEAK}	Collector Output Leakage, $V_{CONTROL}$ = Low	-	-	100	µA
Flag Output Low: S1 = 2	V_{FSAT}	V_{SENSE} = High, I_{FLAG} = 3mA	-	-	0.8	V
Flag Output High: S1 = 3	V_{FLEAK}	Output Leakage, V_{CC} = V_{FLAG} = 10V	-	-	10	µA
Prop. Delay: S1 = 1	t_{ON}, t_{OFF}	Control In to Drive Out	-	5	-	µs
	t_{FLAG}	Drive Off to Flag Off	-	10	-	µs
	t_D	Flag Delay from Control In	150	-	600	µs
Sense Input Thd. Level: S1 = 1	V_{SENTHD}		310	335	360	mV
Power Supply Rejection Ratio	PSSR		50	-	-	dB

NOTES:

1. Refer to Figure 3 Test Diagram for electrical test connections.
2. Refer to Figure 2 Timing Diagram for logic switching and prop delay.
3. Unless otherwise specified: V_{CC} = V_{CC1} = V_{CC2} = 7V to 10V;
V_{SENSE} = "Low"; $V_{CONTROL}$ = "Low";
Control in levels are defined as "Low" equals 0.0V and "High" equals 5.0V.



NOTE: For V_{CC} = 7V to 10V; t_D (MAX) = 600µS, if Control In = High, Sense In = High; Pin 1, Flag Out can go low only if $t_{SENSE} \geq t_D$

FIGURE 2. CA3274 TIMING DIAGRAM

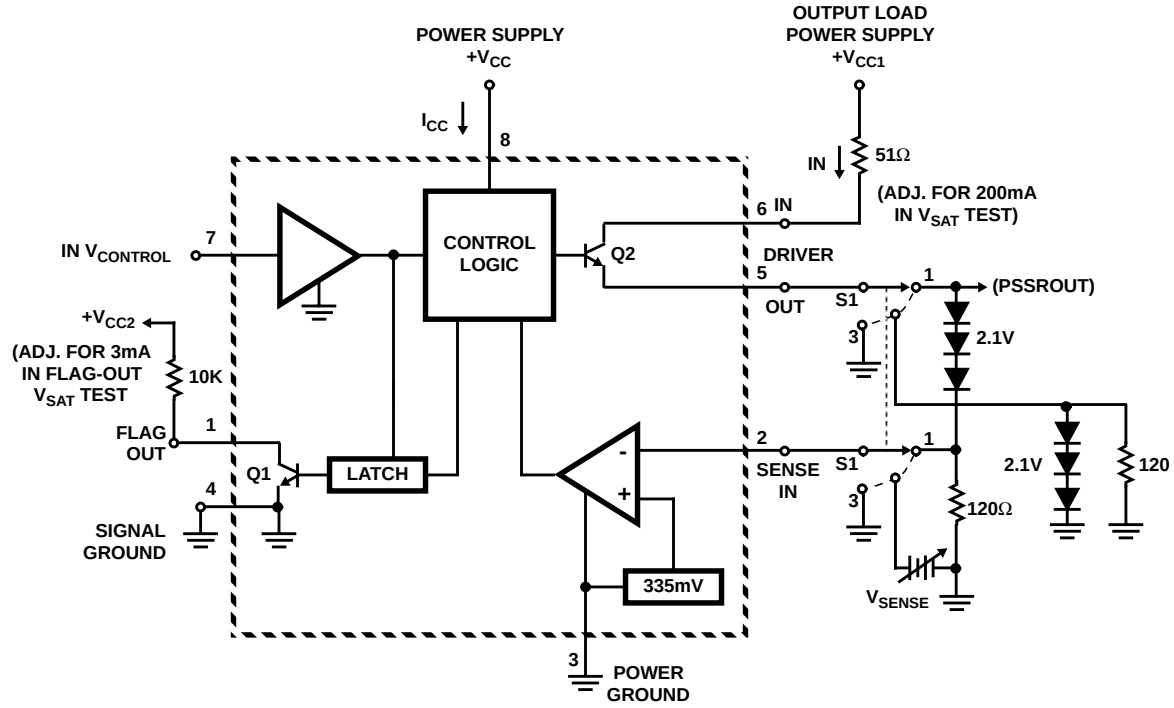


FIGURE 3. CA3274 TEST CIRCUIT

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